Application Report
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Design of a Narrow VDC (NVDC) System Charger Voltage Regulator Using bq24721/30

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ABSTRACT

Narrow VDC architecture is an emerging technique for notebook computer power supply systems with the potential advantages of lower cost and higher efficiency. This application report presents the typical application topologies and the detailed design of a narrow VDC system charger voltage regulator using the bq24721 or bq24730.The measurement results have been demonstrated and are discussed in this report.

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1 Introduction of NVDC Technique

Power-path selection architecture has been adopted in most existing notebook computer battery management circuits. This configuration normally consists of a battery charger and a set of power-path selection switches, as illustrated in Figure 1. When the adapter is on, it is connected to the VDC node directly via the power-path switches Q1 and Q2. The VDC node is the input power from which all other power rails are derived. After the adapter is removed, the battery pack connects to the VDC node through Q3 and powers the DC/DC converters and system loads. Consequently, the VDC voltage varies between the lowest battery voltage and highest adapter voltage, normally about 8.7 V to 19 V.

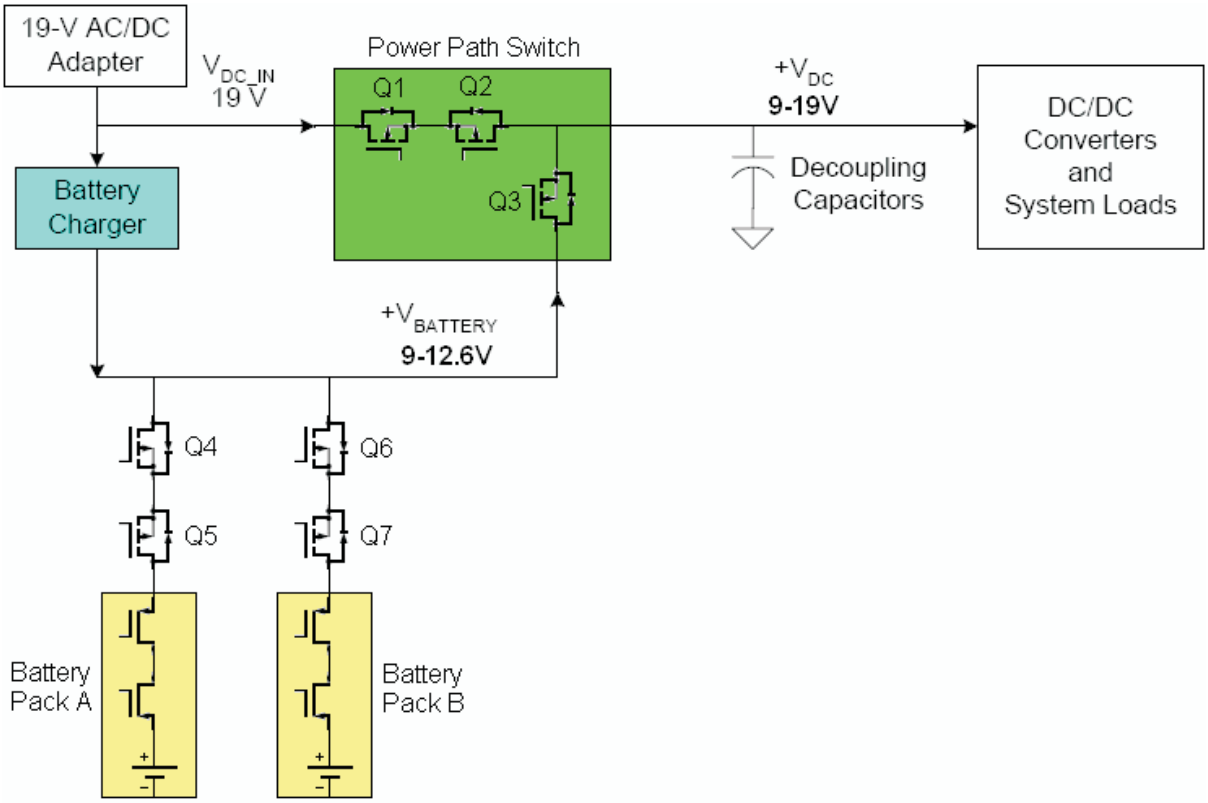

Figure 1. Conventional Power Delivery Path in a Notebook Computer

Narrow VDC (NVDC) is an initiative by Intel™ intended to increase notebook system efficiency by lowering the voltage range of the system load in notebook computers. The objective of the NVDC technique is to reduce power loss by reducing the voltage range of the VDC node. The voltage range reduction is accomplished by replacing the battery charger circuit with a system charger voltage regulator (VR), as shown in Figure 2. The change from battery charger to system charger VR narrows the VDC range. As a result, this enables DC/DC converter optimizations in the system and allows the removal of the power-path switch, saving additional power, board area, and cost. This technique is called the narrow VDC (NVDC) technique.

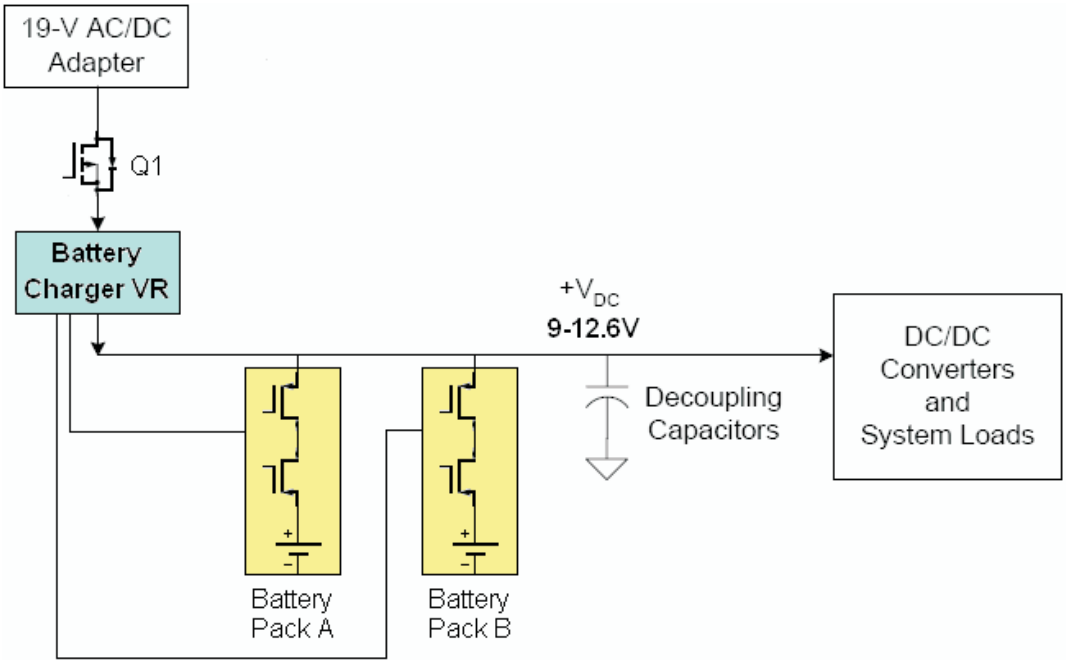

Figure 2. NVDC Power Delivery Path in a Notebook Computer

The major advantages of NVDC configurations are:

1. It is possible to use 20-V power MOSFETs with lower R_{DSON} and lower cost in the downstream DC-DC converters.
2. Due to the narrower line variation range, the DC-DC converter design optimization is easier. This normally leads to higher efficiency and better line transient response.
3. The MOSFET counts on the power path can be reduced, from 5 to 1 for single-pack system and 7 to 1 for dual-pack system.

The potential disadvantages of NVDC configurations are:

1. Lower system voltage leads to a higher bus current which may increase the conduction losses of the copper traces and compromise the power-loss saving by using lower voltage-rating devices.
2. The size, cost, and power dissipation of the charger may be higher because higher current-rating MOSFETs and inductor have to be used.
3. A bad or deeply depleted battery pack clamps the system bus voltage even if the adapter is on. In the path-selection configuration, the system functions as long as the adapter is on, no matter whether the battery voltage is normal or not.

2 NVDC System Architectures Using bq24721/30

The bq24721/30 allows implementation of an NVDC charger. In NVDC, the adapter is not allowed to connect to the system load. Instead, the system load is only connected to the output of the battery charger. This ensures that the system load only detects the minimum-to-maximum voltage of the battery pack. Although this method of connecting the load directly to the battery pack has already been used for various other applications, the system approach to optimize efficiency and cost is making it more popular. In NVDC, the charger is required to process both charge current and system load at the same time; therefore, the power stage needs to be designed accordingly for the increase in total current. The selector FETs are not needed. The converter current is different from the battery sense current; so, two output sense resistors are needed. The SYNN and SYNP current sense pins allow sensing the converter current (for protection) independently of the battery charge current.

The implementations of a NVDC charger VR with a bq24721 device are shown in Figure 3 and Figure 4, which represent 2-sense-resistor version and 3-sense-resistor version, respectively. As shown in Figure 5, the configuration of 3-sense resistor NVDC charger VR using bq24730 is similar to that of the 3-sense-resistor NVDC charger VR using bq24721. If input current sense/limit accuracy is absolutely necessary, then three sense resistors can be used.

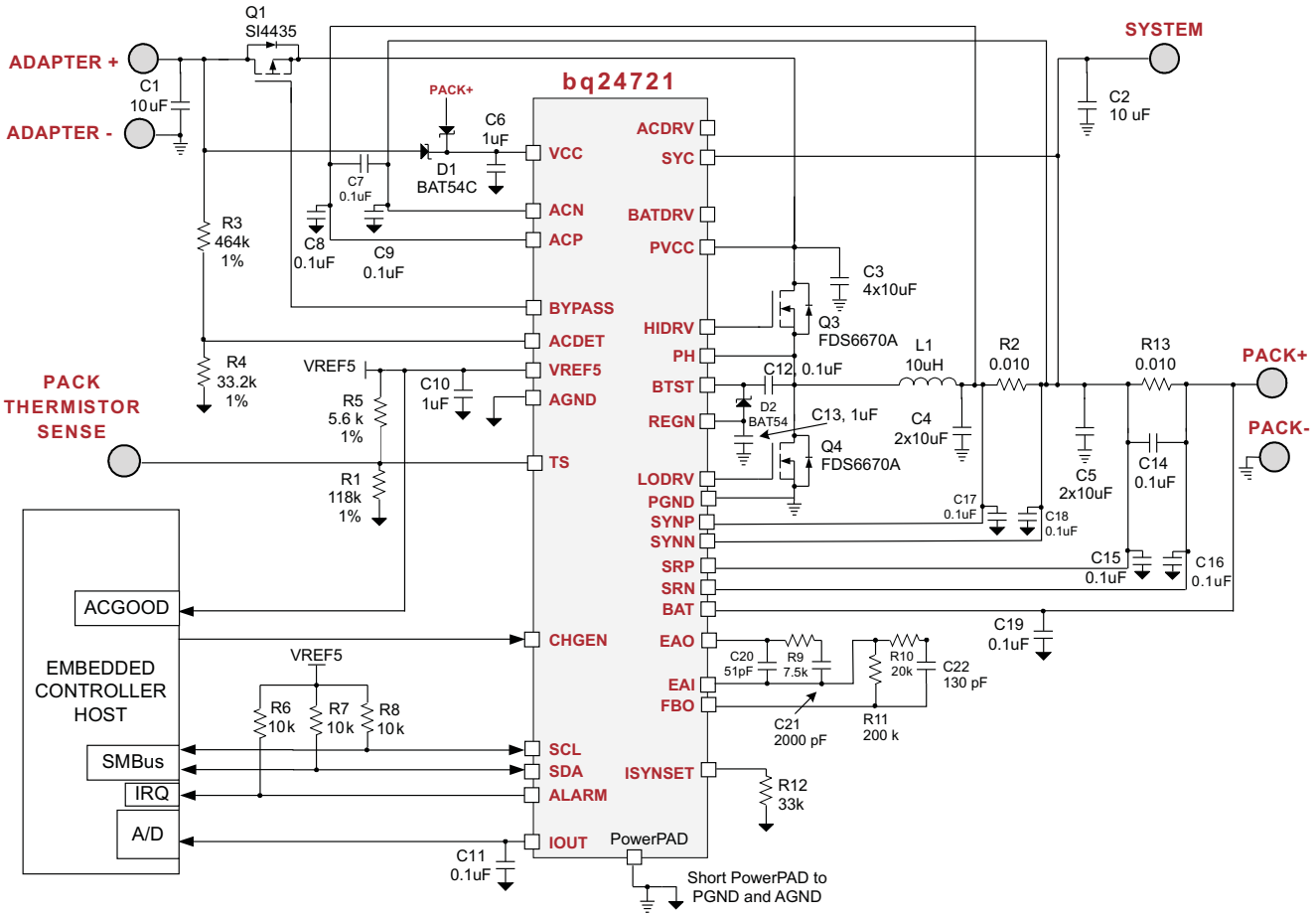

Figure 3. Typical bq24721 NVDC Application (Two Sense Resistors)

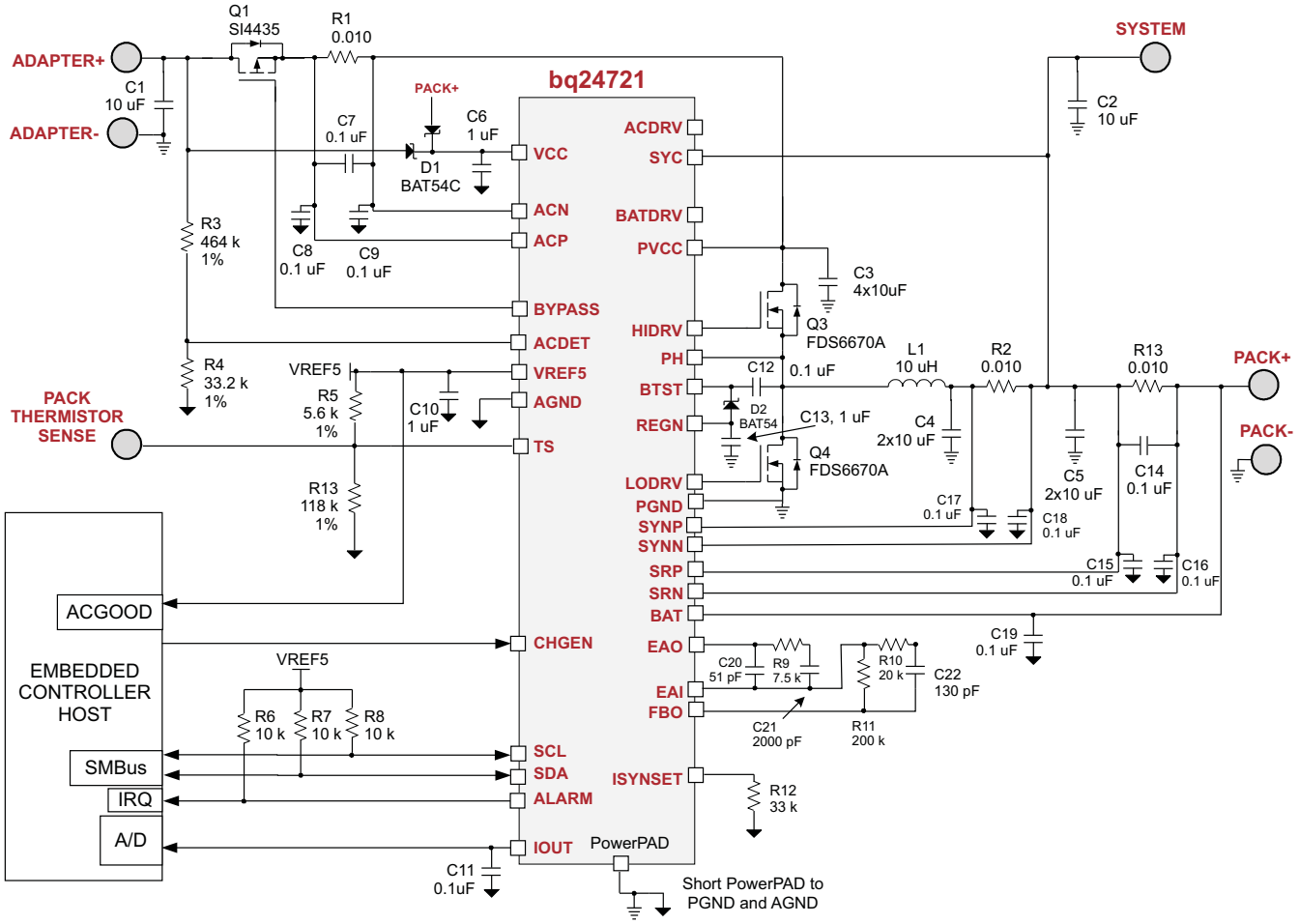

Figure 4. Typical bq24721 NVDC Application (Three Sense Resistors)

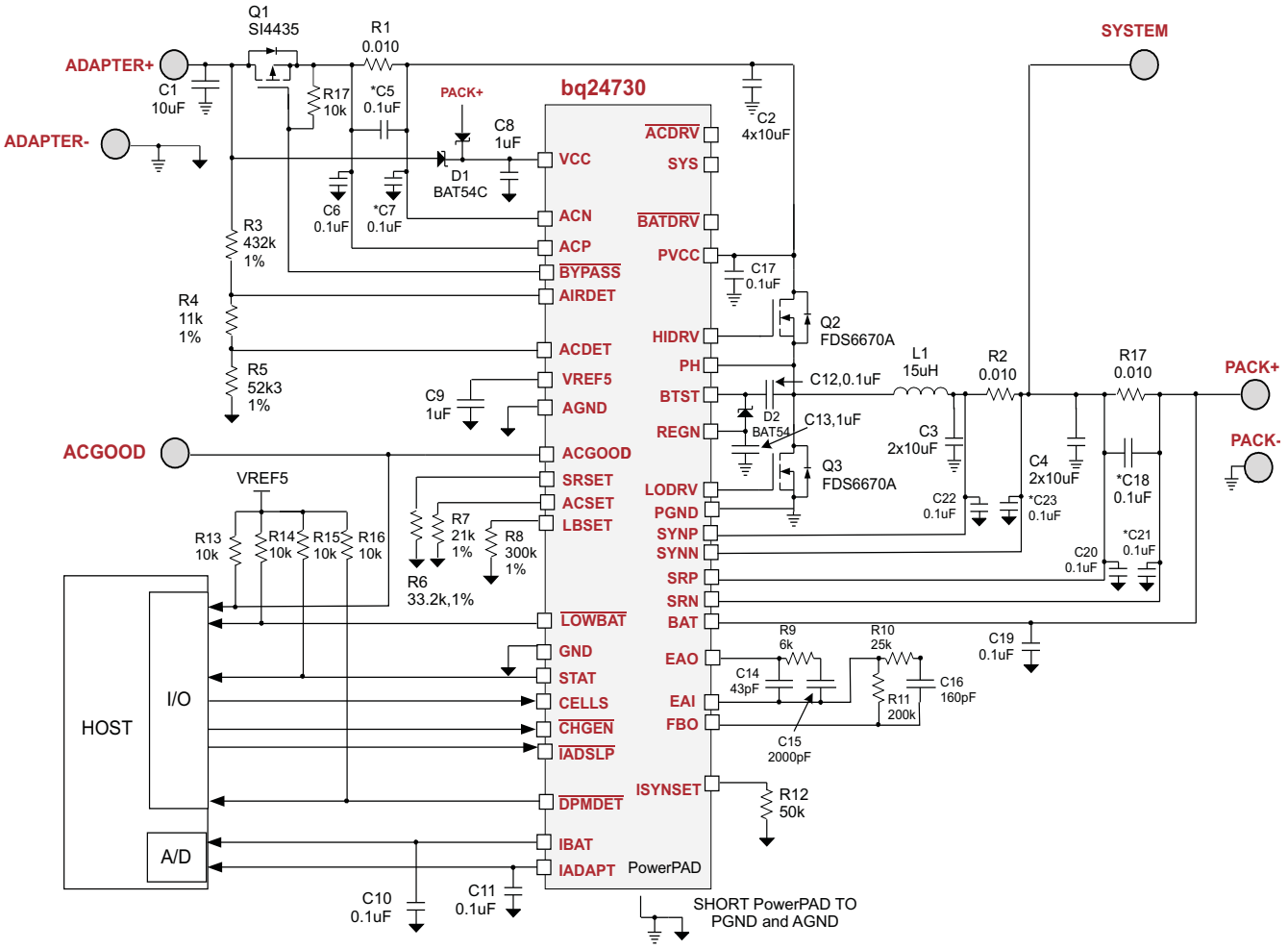

Figure 5. Typical bq24730 NVDC Application (Three Sense Resistors), [VI = 20 V, II(lim) = 4.76 A, I(Charge) = 3 A, V(BAT) = 16.8 V 4-Cells]

Figure 6 shows a method to implement an bq24730-based NVDC charger using only two output sense resistors. The input current is limited, but is not directly sensed. Input current is indirectly regulated by connecting ACP/ACN and SYNN/SYNP pins across the converter protection resistor and adding a resistor from the SRSET pin to the battery positive node in addition to the programming resistor from ACSET to GND. The current variation on R_2 after R_{18} is added as given by:

$$\Delta I_{R2} = -\frac{1000\left(V_{BAT} - 1\right)}{R_{18} \times R_2} \approx -\frac{1000 \times V_{BAT}}{R_{18} \times R_2} \quad (1)$$

which is reversely proportional to V_{BAT}. By selecting the right value for R_{18}, the total input current can be indirectly regulated.

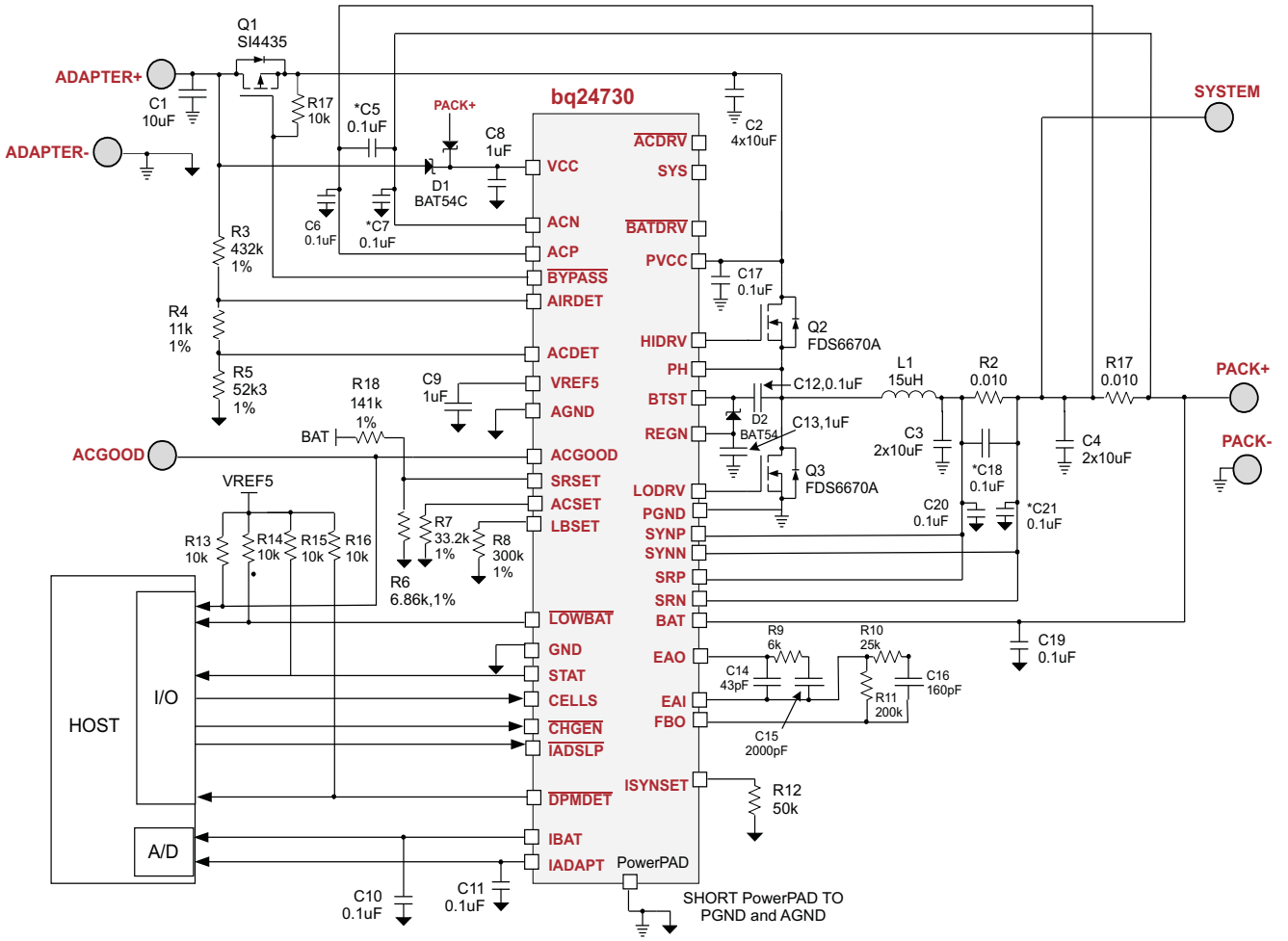

Figure 6. Typical bq24730 NVDC Application (Two Sense Resistors), [VI = 20 V, II(lim) = 4.76 A, I(Charge) = 3 A, V(BAT) = 16.8 V 4-Cells]

3 Design Example

3.1 Specifications

- Adapter voltage: 19 V±3%, 3.4 A
- Battery packs: 3s2p Li-Ion battery, 3600 mAH
- Battery voltage: 4.2 V/Cell (V_{BAT_max} = 12.6 V, V_{BAT_min} = 9 V)
- Fast charge current I_{BAT} = 3 A
- Dynamic power management (DPM) current threshold I_{DPM}: 3.3 A

A typical 3-sense-resistor NVDC charger circuit using bq24730 is used, as shown in Figure 5.

3.2 Determine the Inductor L

Given 35% ripple current, the inductance when $V_{OUT} = V_{BAT\_max}$ during charging:

$$L = \frac{V_{IN} - V_{BAT\_max}}{\Delta I_L} \times \frac{V_{BAT\_max}}{V_{IN}} \times \frac{1}{f_S} = \frac{19 - 12.6}{35\% \times 3} \times \frac{12.6}{19} \times \frac{1}{300 \times 10^3} = 13.5\ \mu H \quad (2)$$

The inductance when $V_{OUT} = V_{BAT\_min}$:

$$L = \frac{V_{IN} - V_{BAT\_min}}{\Delta I_L} \times \frac{V_{BAT\_min}}{V_{IN}} \times \frac{1}{f_S} = \frac{19 - 9}{35\% \times 3} \times \frac{9}{19} \times \frac{1}{300 \times 10^3} = 15.04\ \mu H \quad (3)$$

Select L = 15 µH,

$$\Delta I_{L\_MAX1} = \frac{V_{IN} - V_{BAT\_max}}{L} \times \frac{V_{BAT\_max}}{V_{IN}} \times \frac{1}{f_S} = \frac{19 - 12.6}{15 \times 10^{-6}} \times \frac{12.6}{19} \times \frac{1}{300 \times 10^3} = 0.94\ A \quad (4)$$

$$\Delta I_{L\_MAX2} = \frac{V_{IN} - V_{BAT\_min}}{L} \times \frac{V_{BAT\_min}}{V_{IN}} \times \frac{1}{f_S} = \frac{19 - 9}{15 \times 10^{-6}} \times \frac{9}{19} \times \frac{1}{300 \times 10^3} = 1.05\ A \quad (5)$$

The maximum inductor current is limited by the peak current detection threshold associated with pin SYNP and pin SYNN:

$$I_{Lpk} = 2 \times IBAT = 2 \times 3 = 6\ A \quad (6)$$

Select Coiltronics DR127-150 inductor (15 µH, SMT, 5 A, saturation current 9.66 A, 25 mΩ)

3.3 Determine the Losses on the MOSFETs

The FDS6680A was selected. The FDS6680A is a NMOS, 30-V, 12-mΩ device in an SO-8 package.

The maximum RMS current of the upper switch Q_2 can be estimated by

$$I_{RMS\_Q2} = \sqrt{D_{max}\left(I_{RE\_MAX}^2 + \frac{1}{12}\Delta I_{L\_MAX1}^2\right)} = \sqrt{\frac{12.6}{19}\left(5.13^2 + \frac{1}{12} \times 0.94^2\right)} = 4.18\ A \quad (7)$$

The conduction losses of the upper switch Q_2 are given by

$$P_{COND\_Q2} I_{RMS\_Q2}^2 \times R_{DSON\_Q2} = 4.18^2 \times 12 \times 10^{-3} = 210\ mW \quad (8)$$

The first-order approximation of the upper MOSFET switching losses:

$$P_{swon\_Q2} = I_{R2\_MAX} \times V_{IN\_MIN} \times \frac{Q_{GS} + Q_{GD}}{I_G} \times f_{sw} = 5.13 \times 19 \times \frac{5n + 7n}{1} \times 300k = 351\ mW \quad (9)$$

The gate drive losses of Q_2:

$$P_{DRV\_Q2} = Q_{g\_Q2} \times V_{DRV\_Q2} \times f_S = 18\ n \times 19 \times 300\ k = 103\ mV \quad (10)$$

The maximum RMS current of the lower switch Q_3 can be estimated by

$$I_{RMS\_Q3} = \sqrt{\left(1 - D_{min}\right) I_{RE\_MAX}^2} = \sqrt{\left(1 - \frac{9}{19}\right) \times 6^2} = 4.35\ A \quad (11)$$

The conduction losses of the lower switch Q_3 are given by

$$P_{COND\_Q3} = I_{RMS\_Q3}^2 \times R_{DSON\_Q3} = 4.35^2 \times 12 \times 10^{-3} = 227\ mW \quad (12)$$

The lower MOSFET switching losses:

$$P_{BD\_Q2} = V_{IN\_MAX} \times Q_{RR} \times f_S + 2 \times V_{BD} \times I_{R2\_MAX} \times t_{DT} \times f_S$$
$$= 19 \times 21\ n \times 300\ k + 2 \times 0.8 \times 6 \times 30\ n \times 300\ k\Omega = 206\ mW \quad (13)$$

The gate drive losses of Q_3:

$$P_{DRV\_Q3} = Q_{g\_Q3} \times V_{DRV\_Q3} \times f_S = 103\ mW \quad (14)$$

The total losses on the upper MOSFET Q_2:

$$P_{Q2} = 210\ m + 351\ m + 103\ m = 664\ mW \quad (15)$$

The total losses on the lower MOSFET Q_3:

$$P_{Q3} = 227\ m + 206\ m + 103\ m = 536\ mW \quad (16)$$

3.4 Determine the Sense Resistors

Select the default sense resistor value 10 mΩ for all the sense resistors.

The maximum power dissipation on the input current sense resistor Ra is:

$$P_{R1} = I_{IN\_MAX}^2 R_1 = 3.4^2 \times 0.010 = 0.116 \text{ W} \quad (17)$$

The maximum power dissipation on the charge current sense resistor R_{17} is:

$$P_{R17} = I_{BAT}^2 R_{17} = 3^2 \times 0.010 = 0.09 \text{ W} \quad (18)$$

The maximum power dissipation on the total output current sense resistor R_2 is:

$$P_{R2} = I_{Lpk}^2 R_2 = 6^2 \times 0.010 = 0.36 \text{ W} \quad (19)$$

Select 10 mΩ/ 0.5 W with 1206-size, high-precision sensing resistor for each of these sense resistors.

3.5 Determine the Current and Voltage Setting Resistors

The ISYNSET pin is used to program the charge current threshold at which the charger changes from nonsynchronous operation to synchronous operation. This is important in order to prevent negative inductor current. To program the threshold, a resistor is connected from the ISYNSET pin to AGND. The ISYNSET programming resistor can be calculated by:

$$R_{12} = \frac{1 \times 500}{\Delta I_{L\_MAX} \times R_2} = \frac{1 \times 500}{0.94 \times 0.010} = 53.2 \text{ k}\Omega \quad (20)$$

Select R_{12} = 49.9 kΩ

The input (DPM) current can be programmed through a resistor from the ACSET pin to AGND. The ACSET programming resistor can be calculated by:

$$R_7 = \frac{1 \times 1000}{I_{DPM} \times R_1} = \frac{1 \times 1000}{3.3 \times 0.010} = 30.3 \text{ k}\Omega \quad (21)$$

Select R_7 = 30.9 kΩ

The charge current can be programmed through a resistor from the SRSET pin to AGND. The SRSET programming resistor can be calculated by:

$$R_6 = \frac{1 \times 1000}{I_{BAT} \times R_{17}} = \frac{1 \times 1000}{3 \times 0.010} = 33.3 \text{ k}\Omega \quad (22)$$

Select R_6 = 33.2 kΩ

The battery depleted threshold to be programmed is 3 V/cell. The LBSET programming resistor is calculated as:

$$R_8 = \frac{3}{2 \times 5\ \mu} = 300 \text{ k}\Omega \quad (23)$$

3.6 The Compensator Design

For information about the compensator design, see TI application report SLUA371 .

4 Measurement Results

The efficiency measurement results of a conventional bq24730 charger and path selector with various battery voltages are shown in Figure 7. The efficiency increases with the system current because the DPM regulation kicks in and reduces the charge current. The highest efficiency can be up to 98%.

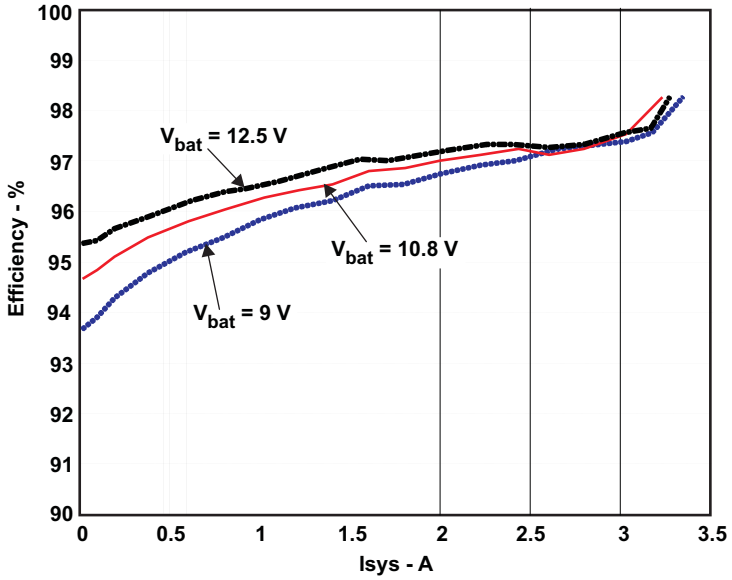

Figure 7. Efficiency Curves of a Regular Application Using bq24730

The efficiency measurement results of a NVDC bq24730 charger VR with various battery voltages are shown in Figure 8. The efficiency curves are relatively flat because the inductor current remains the same over most of the system load range. The highest efficiency can be up to 95.3%, lower than that of the conventional application.

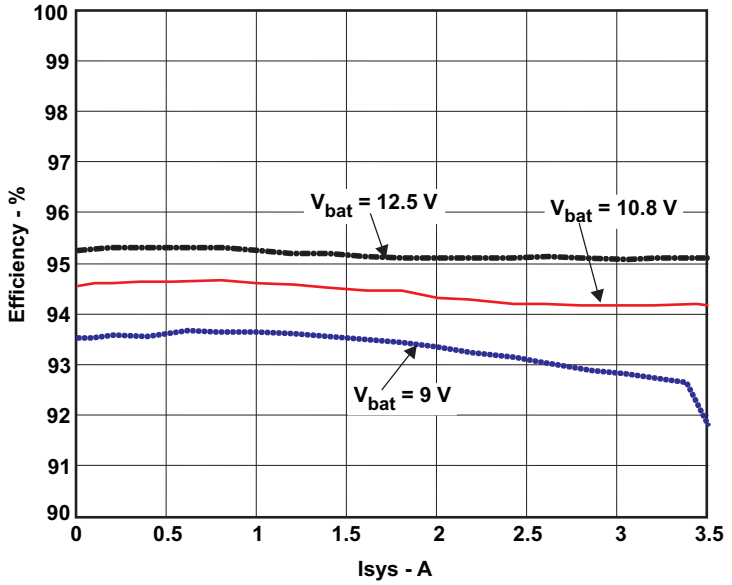

Figure 8. Efficiency Curves of a NVDC Application Using bq24730

The input and battery current responses of the conventional application and NVDC application during system current transients are shown in Figure 9 and Figure 10, respectively. Under the same output power, the input current overshoot of the NVDC charger VR is lower during the DPM transients because the battery helps supply the system load current and reduces the impact to the input.

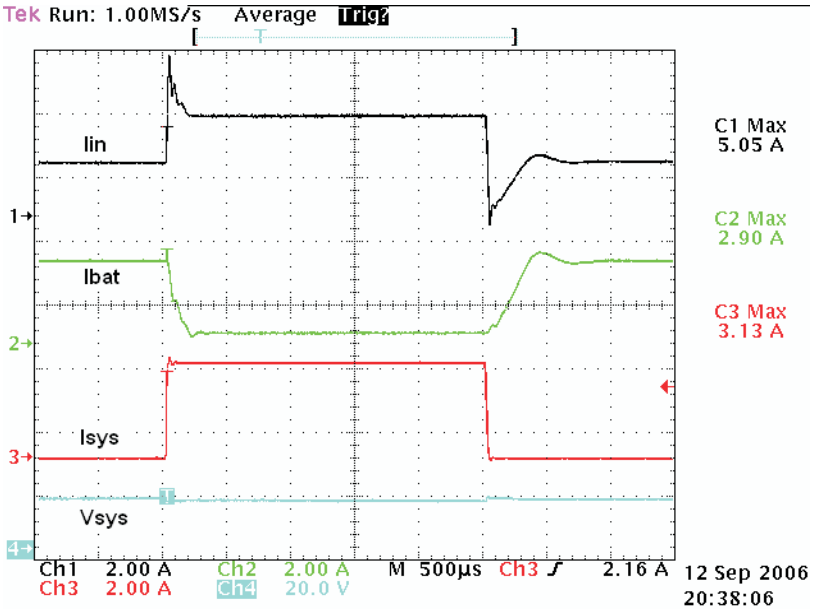

Figure 9. System Load Transient Response – Conventional bq24730 Battery Management Circuit

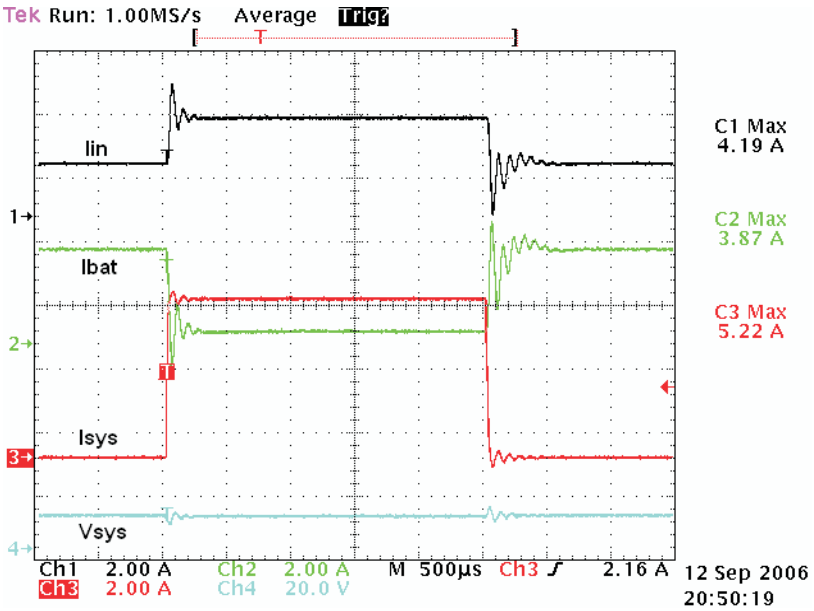

Figure 10. System Load Transient Response - NVDC bq24730 Battery Management Circuit

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