

bq77PL900EVM-001

This evaluation module (EVM) is a complete evaluation system for the bq77PL900, a five- to ten-cell Li-ion battery protection and AFE integrated circuit. The EVM includes one bq77PL900 circuit module, an EV2300 PC interface board, an interface cable, a PC USB cable, and Windows™-based PC software. The circuit module includes one bq77PL900 integrated circuit (IC), sense resistor, power FETs and all other onboard components necessary to protect the cells from overcharge, over discharge, short circuit, and over current discharge in 5 to 10 series cell Li-ion or Li-polymer battery packs. The circuit module connects directly across the cells in a battery. With the EV2300 interface board and software, the user can read the bq77PL900 data registers, program the IC protection limits, and evaluate the overall functionality of the bq77PL900 solution under different operational conditions.

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1 Features

- Complete evaluation system for the bq77PL900 five to ten series cell lithium-ion or lithium-polymer battery protector and analog front end IC in stand-alone mode
- Populated circuit module for quick setup
- PC software and interface board for easy evaluation
- Connections for attaching a the circuit module to a host system

1.1 Kit Contents

- bq77PL900 circuit module
- EV2300 PC interface board
- Connection cable to interface board
- USB cable
- Software CD with the evaluation software
- Set of support documentation

Table 1. Ordering Information

EVM Part Number	Chemistry	Configuration	Capacity
bq77PL900EVM-001	Li-ion	Five to ten cells	Any

2 bq77PL900 Circuit Module and Interfaces

The bq77PL900 circuit module contains the bq77PL900 IC and related circuitry to demonstrate the features of the IC. Two FETs are paired for the high current charge and discharge to reduce resistance in the FETs. A zero volt charge FET and current limit resistor is provided. A thermistor provides temperature sensing for the device. Other components provide support for the IC and connections to the board.

2.1 Circuit Module Connections

Connections are provided for the following interfaces:

- Direct cell connections
- PACK connection
- Evaluation and programming interface (I²C)
- Host monitoring and control
- Regulated power

2.2 Signal Descriptions

Signals available on the EVM are described in this section. For details on the location and connector types, refer to the physical construction section.

Cell connections are described in [Table 2](#). Cell connection sequence is described in [Section 4.2](#).

Table 2. Cell Connections

Reference Designator	Pin Number	Signal	Description
J5	1, 2	BATTERY–	–ve connection of first (bottom) cell, high current connection
J4	3	1N	–ve connection of first (bottom) cell, connected to BATTERY– with R2
	2	1P	+ve connection of first (bottom) cell
	1	2P	+ve connection of second cell
J3	4	3P	+ve connection of third cell
	3	4P	+ve connection of fourth cell
	2	5P	+ve connection of fifth cell
	1	6P	+ve connection of sixth cell
J2	4	7P	+ve connection of seventh cell
	3	8P	+ve connection of eighth cell
	2	9P	+ve connection of ninth cell
	1	10P	+ve connection of tenth cell, connected to BATTERY+ with R1
J1	1, 2	BATTERY+	Most positive cell output, high current connection

Load connections are described in [Table 3](#).

Table 3. PACK Connections

Reference Designator	Pin Number	Signal	Description
J15	1, 2	PACK+	Positive output of evaluation board
J14	1, 2	PACK–	Negative output of evaluation board

Evaluation and programming I2C interface signals are provided on J12 and are described in [Table 4](#).

Table 4. Serial Interface Connections

Reference Designator	Pin Number	Signal	Description
J12	1	GND	Signal reference for the IC
	2	SCLK	Serial interface clock connection
	3	SDATA	Serial interface data connection
	4	EEPROM	EEPROM write enable pin connection

Host monitoring and control signals are described in [Table 5](#).

Table 5. Host Connections

Reference Designator	Pin Number	Signal	Description
J13	1	EEPROM	EEPROM write enable pin connection
	2	SDATA	Serial interface data connection
	3	SCLK	Serial interface clock connection
	4	GND	Signal reference for the IC
	5	XRST	Active low reset from the IC
	6	TS1	Thermistor voltage input to TIN of IC
	7	XALERT	Status register change signal from IC
	8	IOUT	Current monitor output from IC
	9	VOUT	Voltage monitor output from IC
	10	GND	Signal reference for the IC

Regulated power signals are provided for monitoring or connection to a host board. Signals are described in [Table 6](#).

Table 6. Power Output Connections

Reference Designator	Pin Number	Signal	Description
J11	1	GND	Signal reference for the IC
	2	5V	5V output from VREG1
	3	GND	Signal reference for the IC
	4	3.3V	3.3V output from VREG2

3 bq77PL900 Circuit Module Configuration

This section describes how to configure the bq77PL900 circuit module to operate in the desired mode for evaluation, and changes the user may want to make to the board for specific evaluations.

3.1 Cell Count Configuration

Cell count for the bq77PL900 is selected using J6 through J8 to set the level of the CNF pins. Positioning the shunt toward the top of the board (VSEL, connecting pins 2-3) provides a logic high, positioning toward the bottom of the board (GND, connecting pins 1-2) provides a low. [Table 7](#) shows configuration settings for different cell counts.

Table 7. Cell Count Configuration Jumper Position

Cell Count	J8 Position/CNF2	J7 Position /CNF1	J6 Position /CNF0
10	GND/0	GND/0	GND/0
9	GND/0	GND/0	VSEL/1
8	GND/0	VSEL/1	GND/0
7	GND/0	VSEL/1	VSEL/1
6	VSEL/1	GND/0	GND/0
5	VSEL/1	GND/0	VSEL/1

3.2 Logic Level Selection

Selection of the VLOG voltage for the bq77PL900 is provided by J10. The VLOG selection sets the interface voltage for the logic signals on the IC. Selecting the shunt position is described in [Table 8](#). Set VLOG to 5V for EEPROM programming with the EV2300.

Table 8. Logic Level Configuration Jumper Position

Shunt Position	J10 Pins Connected	VLOG Selection
Up	1-2	5V
Down	2-3	3.3V

3.3 Pre-Charge Configuration

The bq77PL900EVM-001 circuit module includes a pre-charge current path. The IC PMS pin is configured by J9. [Table 9](#) shows configuration selections. Refer to the bq77PL900 datasheet for more information. The current path is made up of the pre-charge FET Q5 and resistor R19. The value of R19 on the EVM was selected to meet its power rating with 42V and nominal resistance. The resulting current is low, consider the conditions relevant to your evaluation and replace the resistor with a different value if needed.

Table 9. PMS Pin Selection

Shunt Position	J9 Pins Connected	PMS Selection	Comment
Up	2-3	PACK+	Pre-charge FET not used
Down	1-2	GND	Pre-charge FET used if enabled in EEPROM

3.4 Ground Connection

The IC ground reference on the bq77PL900EVM-001 circuit module is connected to the BATTERY– net near J5 using a zero ohm resistor R39. Due to the voltages which can be induced during high current discharge, ground on the bq77PL900 is recommended on the battery side of the sense resistor. This causes the voltage at the SRP pin to be above ground during discharge. Board resistance will also cause SRB to be above ground during discharge.

The ground connection on the battery side of the sense resistor causes the ground reference of the IC to be modulated from the PACK– terminal by the load current. When connecting to the analog signals, the user should reference the signal ground. For digital signals, the circuitry will need to use the digital ground or accept the modulation of current in the ground reference.

R40 provides an optional grounding position on the battery side of the sense resistor. Although not recommended, R41 provides a grounding option on the pack side of the sense resistor. Be sure to verify that the check voltages at the IC pins are within acceptable datasheet limits during all modes of operation. Note that grounding on the pack side of the sense resistor will not eliminate modulation of the signals due to current, only reduce them by the sense resistor drop. The user should be certain only 1 of R39, R40 or R41 is shorted and that the sense resistor is not bypassed by a connection between PACK– and system ground.

3.5 Cell Monitor Connections

Resistors R1 and R2 are installed by default and allow the high current connections to be used for cell monitoring. If separate connections are desired for cell monitoring, remove the R1 and R2 resistors and make connection from 1N and 10P back to the cells when the equivalent high current connection is made during the cell connection sequence.

3.6 FET Use

The circuit module provides FETs for charge and discharge control. If your evaluation does not require charge FETs, openings are provided in the solder mask near J15 on both the top and bottom side to short the charge FET. An added connection should be large enough to carry the current used in your evaluation. If your evaluation does not require charge or discharge FETs, the BATTERY+ and PACK+ connections should be connected together and to the top of the cell stack to provide power and wake up voltage to the bq77PL900.

3.7 Current Sense Connections

Components R17, R20 and C17 provide a 40 μ s time constant between the sense resistor and current sense terminals. If this delay is objectionable, C17 may need to be reduced or removed for the evaluation.

3.8 Other Circuit Configurations

A reverse clamp diode D12 is provided at the pack outputs to prevent board damage during turn off of inductive loads. This diode will also provide reverse charger protection within the capability of the part. The part used is rated at 3A, be sure this is sufficient for your evaluation. A larger diode may be connected to the pack terminals if needed.

The EVM could be used in a variety of systems. Capacitors C26 to C35 provide some transient protection, by absorbing impulses present from the load. Several capacitors are used rather than one due to the size and the decrease in capacitance at high voltage. If the capacitance is not needed in evaluation, it could be removed. In some applications, the capacitance may not be sufficient for transient suppression. Holes X1 to X6, D9 and RT2 are provided between the pack terminal traces for installation of additional transient suppression components that may be needed for specific system evaluations.

Suppression of transients to the EVM is important both to prevent exceeding the IC voltage ratings, and for proper operation of the system due to the power supply hold up circuit used for the IC on the EVM:

- Diodes D1 and D8 are necessary to prevent rapid loss of supply voltage to the IC during short circuit events, and to prevent negative voltage at the BAT and PACK pins during a reversed charger connection.
- The DSG and CHG gate drive signals from the IC are driven to approximately 12V below the value of the BAT and PACK voltages as seen by the IC. This provides sufficient gate drive to bias the P-Channel FETs fully ON. Under steady-state operating conditions, the voltages at the IC pins will be the same as the voltages at the external terminals.
- Under transient conditions (typically caused by dynamic system loads), the D1/C11 and D8/C24 components will store the peak voltages seen at the external pins. There may be instantaneous differences in the voltages seen at the BAT and PACK pins of the IC relative to the source terminals of the power FETs.
- If these transients are very large, the power FETs may briefly shut off. This happens because the gate drive voltages are referenced to the value of BAT and/or PACK voltage seen at the IC pin, which may be momentarily higher than the actual BAT or PACK voltage in the actual system. The resulting actual V_{gs} differential may not be sufficient to maintain the ON state of the power FETs when the sensed BAT or PACK voltage is higher than the actual BAT or PACK voltage.
- The circuit used for maintaining the supply voltage to the IC may need to be modified in a system that has significant voltage transients to prevent momentary shutoff of the power FETs during these conditions. See [Figure 1](#) for further explanation.
- If your system does not require D1 and D8, these are located on the bottom side of the board and may be shorted. Refer to section 9 for location of these components.

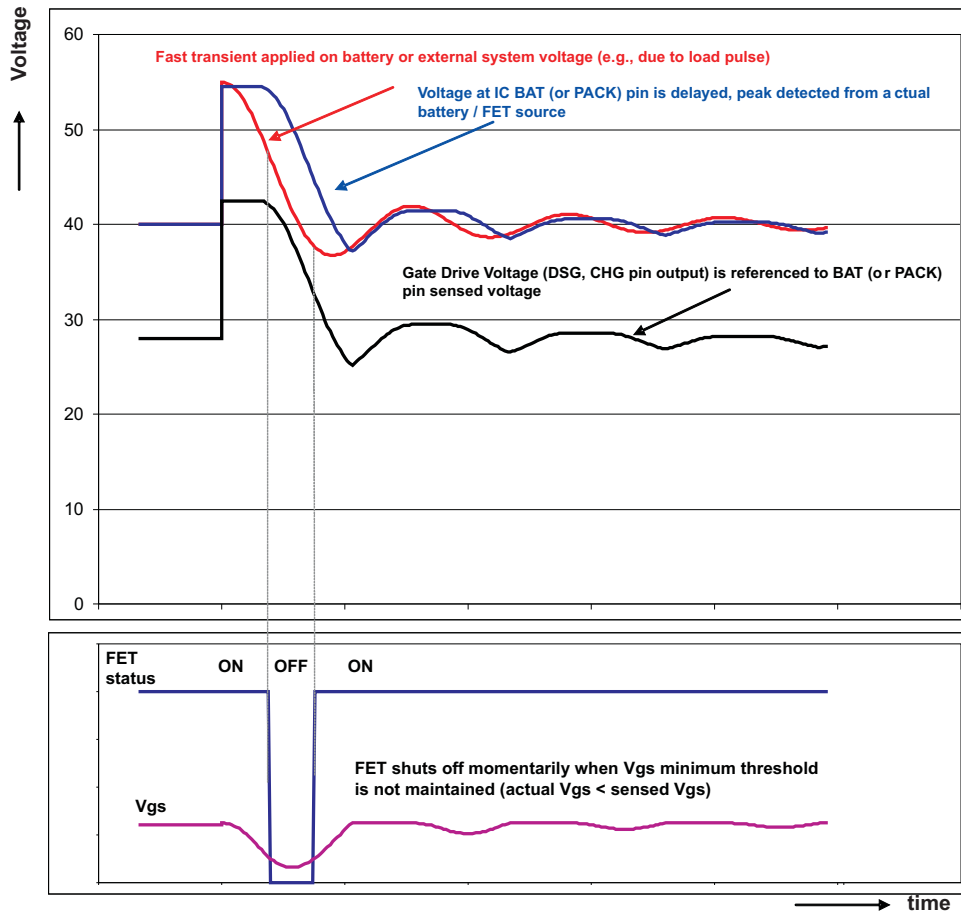


Figure 1. Transient Effect of FET Operation

4 bq77PL900 EVM Hardware Connection and Operation

This section describes the connection of the circuit module and EVM. Simple operation is also described.

4.1 Initial Considerations

Boards are tested after assembly with a basic functional test. This test may not check every connection on the board. Boards should be checked for function in the user's environment before relying on the safety features of the board.

Before connecting the board for operation, configure it for the desired state as described in [Section 3](#).

Be sure to observe the cautions and warnings in this document.

The connection of the EVM will look similar to [Figure 2](#). The manufacturer's rating for the terminal blocks for Pack and Battery connections is 24A nominal per terminal. Parallel connections are provided for high current operation. Note that the EV2300 is not required for basic operation, and it should be connected to the computer and EVM circuit module only after proper installation of software. The software along with the EV2300 allows monitoring of the IC status, setting the programmable safety limits and controlling the device in host mode. Installation of the software and its use are described in a later section.

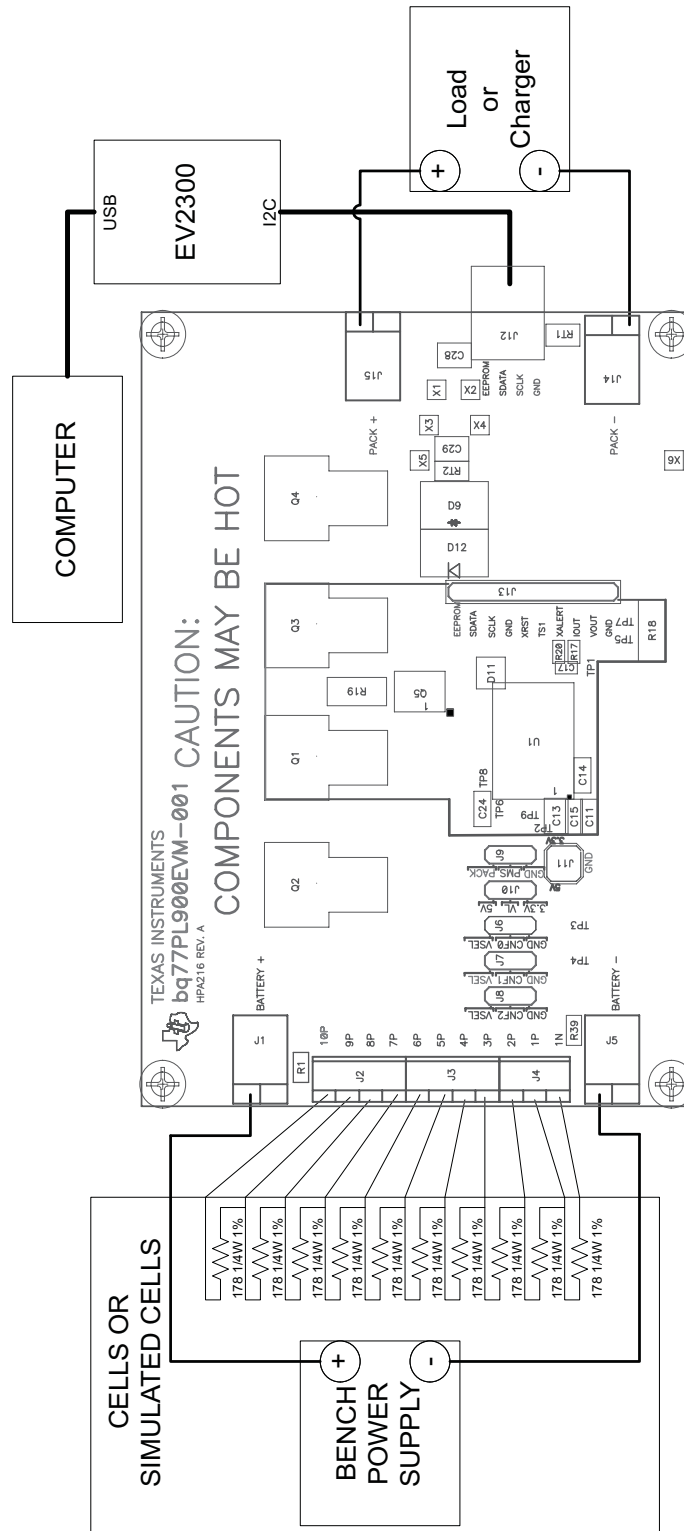


Figure 2. Basic Connections

4.2 Cell Connections

Unused cell inputs should be shorted together. For example, if 8 cells are used, the 10P, 9P and 8P terminals should be connected together.

For initial evaluation, it is suggested power supplies be used for cell simulation to observe the behavior of the device. Resistors can be used for cell voltage simulation to reduce the number of power supplies needed, 180 Ω or similar resistors are suggested. Tolerances can be selected or resistances adjusted to provide desired variations in simulated voltage. Smaller values will work also, the smaller the value, the more current is required from the battery simulator power supply and the smaller the influence on the voltages if cell balancing is operated.

If power supplies or cells are used, inductance in the high current path should be minimized. Inductance in this path can cause inductive transients at the board when the load current is stopped or the bq77PL900 opens the discharge FET with current flow. Use heavy gauge wires for the high current connections; minimize inductances by keeping leads close together.

Cells should be connected in sequence from lowest to highest voltage as described in the following steps:

1. Connect the lowest cell negative terminal to the EVM BATTERY– terminal. Connect it also to the EVM 1N terminal if R2 was removed.
2. Connect the lowest cell positive terminal to the EVM 1P terminal
3. Connect the second lowest cell positive terminal to the 2P terminal
4. Connect the next lowest cell positive terminal to the 3P terminal
5. Continue connecting each higher cell in sequence. When all other connections have been made, connect the most positive cell to the EVM BATTERY+ terminal, then to the 10P terminal if R1 was removed.
6. When removing cells, disconnect in the reverse order.

4.3 Pack Connections

A load or charger is connected to the pack terminals using the terminal blocks provided. It is recommended that the load or charger be connected with the current switched off to prevent arcing or transients during connection of the wires to the terminal blocks.

Although designed for 30A operation, the board may not dissipate enough power to operate without exceeding the ratings. The user should monitor the temperature of the board and components during evaluation and provide cooling air and/or heatsinks as required for operation. The thermal sensor on the board may not respond to protect the FETs from damaging temperatures due to its location and possible thermal gradients on the board.

CAUTION

The bq77PL900 circuit module may be damaged by over temperature. To avoid damage, monitor the temperature during evaluation and provide cooling as needed for your system environment.

WARNING

The bq77PL900 circuit module may become hot during operation due to dissipation of heat. Avoid contact with the board. Follow all applicable safety procedures applicable to your laboratory.

4.4 Thermal Sensor

The thermal protection on the bq77PL900EVM circuit module is set to provide a trip threshold of 60°C with nominal values. Component tolerances and substitute values may alter this trip point. The thermistor in particular will impact the linearity and limit of the temperature sensor. The thermistor could be moved off board for sensing cell temperature, or closer to the FETs or a heatsink or other system component for evaluation. To adjust the value of the trip point, change the value of R22. The linearization resistor R29 will have a lesser effect.

4.5 Basic Operation

The following steps are suggested for basic operation for a board configured for 10 cells with the default safety configuration in EEPROM.

1. Connect cells or cell simulation resistors and a power supply to the battery side of the board. Set the bench supply (if used) to approximately 20V.
2. Connect a disabled load to the pack terminals.
3. Wake up the part by momentarily connecting a charge voltage > 7.5V to the pack terminals. If the load is disconnected, the user can momentarily short the BATTERY+ to PACK+ with a resistor.
4. Monitor the XALERT, 3.3V or 5V outputs to observe the operation of the device as desired.
5. Increase the load to >10A to observe XALERT goes low due to overcurrent or under voltage if the power supply current limits.
6. Remove the load and attach a charger to allow the device to recover.
7. If using a power supply, reduce the voltage of the cells to observe the device shuts off at ~14V.

5 Software Installation

This section describes how to install the software for the bq77PL900EVM-001, and how to connect the PC interface board of the EVM.

5.1 System Requirements

The bq77PL900EVM requires Windows 2000, Windows XP, or Windows Vista. You must have administrative rights on the computer.

5.2 Install The bq77PL900EVM Software

Find the latest software version in the bq77PL900EVM-001 tool folder on <http://focus.ti.com/docs/toolsw/folders/print/bq77PL900evm-001.html> or from power.ti.com. Check periodically for software updates. Use the following steps to install the bq77PL900 Evaluation Software:

1. Copy the archive file to a directory of your choice.
2. Extract the archive containing the installation package into the temporary directory. Be sure to preserve folder names.
3. Driver installation:
Note, if the computer was previously used with the EV2300, driver installation should not be needed.
 - a. Verify the EV2300 is unplugged from the computer.
 - b. In the temporary directory you selected, open the appropriate archive, Driver(USB2300) Installer XP2K-xxx.zip or EV2300VistaDriverInstaller.zip, and extract its contents in a subdirectory/drivers. Choose preserve directory structure option when extracting.
 - c. Run the setup.exe file in the drivers directory. Accept the license terms and answer continue to the warning that drivers are not certified with Microsoft.
 - d. Plug the EV2300 into a USB port.
 - e. Wait until system prompt new hardware found appears. Chose select location manually and use the Browse button to point to subdirectory C:\WINDOWS\TI\USB1.
 - f. Answer continue to the warning that drivers are not certified with Microsoft.
 - g. After installation finishes, another system prompt new hardware found appears. Repeat procedure above, but point to subdirectory C:\WINDOWS\TI\USB2

- h. Answer continue to the warning that drivers are not certified with Microsoft.
 - i. Installation of drivers is now finished.
4. In the temporary folder, double-click on setup.exe and follow the installer instructions to complete the bq77PL900 EVSW installation.

If files from the CD are used:

1. Copy the files from the CD *bq77PL900 EV SW Install* directory into a temporary directory you select.
2. Follow the preceding steps 2–4.

6 Troubleshooting Unexpected Dialog Boxes

Ensure that the files were extracted from the zip file using the Preserve Folder names option.

Ensure that all the files were extracted from the zip file.

The user that is downloading the files must be logged in as the administrator.

The driver is not signed, so the administrator must allow installation of unsigned drivers in the operating system policy.

7 Software Operation

This section describes operation of the software.

Software is started from the sequence Start > All Programs > Texas Instruments > bq77PL900 Evaluation Software.

The software window has 2 sections, a tab section and a status section. The left side of the window displays one of 3 tabs selected by clicking on the tab name and described in the following sections. The right section of the window provides visual indicators of the status register which is polled periodically by the software. The connection status of the I2C is shown above the status section.

7.1 Registers Tab

After the software starts, the registers tab is displayed. The registers tab can be used to read all registers and write selected registers. The scanning check box in the right bottom corner controls continuous scanning of the registers. Register scanning is independent of the status section scanning. When the scanning box is not checked, the values are not automatically read when the tab is selected. Select the "Read All" button to update the register status when scanning is off. Random patterns should not be written to the registers, refer to the data sheet for register bit definitions.



Addr	Name	B7	B6	B5	B4	B3	B2	B1	B0	Hex
0x00	STATUS	CHG	DSG	VGOOD	OVTEMP	UV	OV	OCD	SCD	C0
0x01	OUTPUT_CNTRL	FS	PFALT	RSVD	RSVD	GPOD	CHG	DSG	LTCLR	00 Write
0x02	STATE_CNTRL	IGAIN	VGAIN	RSVD	RSVD	RSVD	RSVD	HOST	SHDN	00 Write
0x03	FNCTN_CNTRL	CBAL10	CBAL9	TOUT	BAT	PACK	IACAL	IAREN	VAREN	00 Write
0x04	CELL_BALANCE	CBAL8	CBAL7	CBAL6	CBAL5	CBAL4	CBAL3	CBAL2	CBAL1	00 Write
0x05	CELL_SEL	RSVD	CAL2	CAL1	CAL0	CELL4	CELL3	CELL2	CELL1	00 Write
0x06	OV_CFG	OWD2	OWD1	OWD0	OVH1	OVH0	OV2	OV1	OV0	00
0x07	UV_LEVEL	SOC_DIS	UVFET_DIS	UVH1	UVH0	UV3	UV2	UV1	UV0	00
0x08	OCV_UV_DELAY	UND3	UND2	UND1	UND0	OCD3	OCD2	OCD1	OCD0	00
0x09	OCDELAY	CBEN	ZVC	SOR	OCDD4	OCDD3	OCDD2	OCDD1	OCDD0	00
0x0A	SCD_CFG	SCDD3	SCDD2	SCDD1	SCDD0	SCD3	SCD2	SCD1	SCD0	00

STATUS

VGOOD

OVTEMP

UV

OV

OCD

SCD

Bit Color Legend: 1 (Green), 0 (Red)

Scan

Read All

Figure 3. Registers Tab Window

7.2 Control Tab

The Control tab is shown in Figure 4. This tab allows the user to adjust control of the features of the part. In stand-alone mode, the features are not applicable and are grayed out. When host mode is selected, the user can make adjustments to demonstrate controls that would be performed by the host in a system implementation. Refer to the data sheet for detailed bit definitions.

The OUTPUT CONTROL section is used primarily to turn on and off FETs and clear errors. The STATE CONTROL section is used to select Host mode, the amplifier gains and shutdown. The FUNCTION CONTROL section contains the Thermistor Power control, but also along with the CELL SEL section allows demonstration of the voltage and current monitor outputs and selections. These would normally be used in a host controlled system to monitor the battery operation and allow calibration of the host measurement system. Refer to the data sheet for more information on the features to support system calibration.

The CELL BALANCE section allows control of individual cell-balancing bits, and should not be randomly written. In host mode the user has control of cell balancing. Cell balancing should be enabled using an algorithm to protect the cell sense IC pins from over voltage induced by the cell balancing function. This is summarized by:

- No adjacent cell balancing
- No every-other-cell balancing.

See the application note *Cell Balancing With the bq77PL900*, [SLUA463](#) for more information on cell balancing.

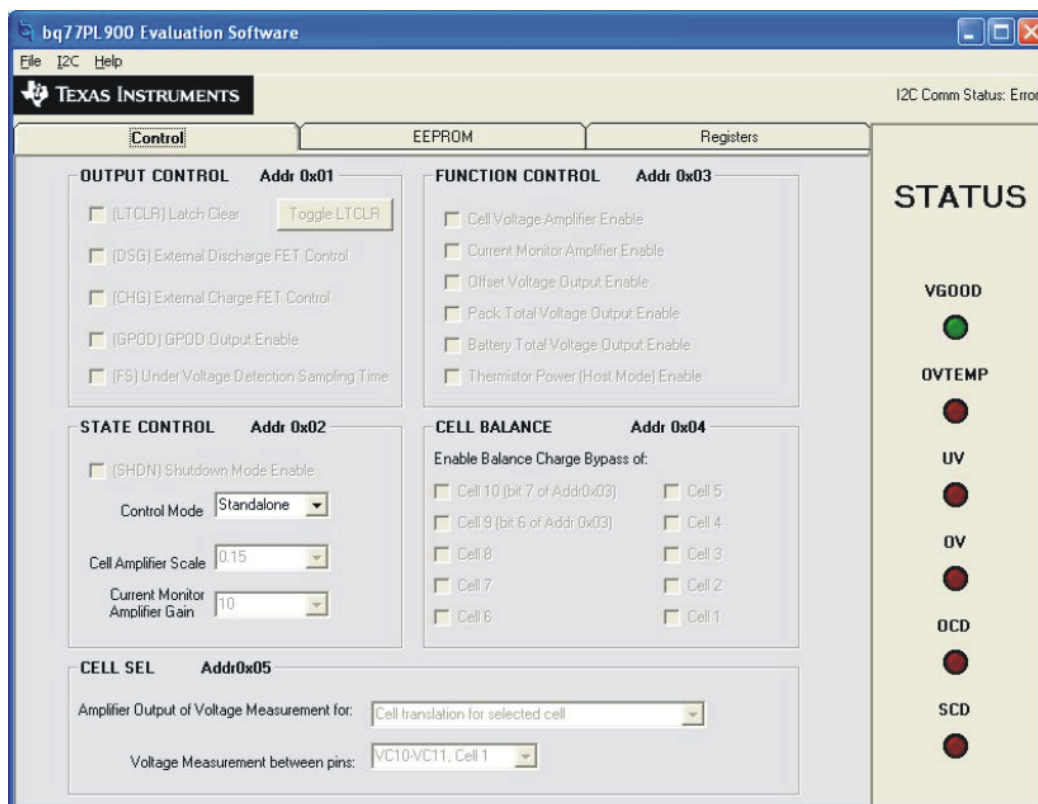


Figure 4. Control Tab Window

7.3 EEPROM Tab

CAUTION

The EV2300 provides 5V for the EEPROM signal when programming. If the board is configured for VLOG = 3.3V during programming, damaging voltages may be imposed on VREG2 and the I2C lines. Disconnect any sensitive host and set VLOG = 5V before programming with the EV2300.

The EEPROM tab is used to change the settings of the protection features of the device. The values are read from the part and the window updated when the tab is selected. Changes can be made using the selection and checkboxes. The Preview button will display the present EEPROM selections in a register format. The preview window must be closed before other operations can take place. Changes will be written to the EEPROM when the Program EEPROM button is selected. Note that the EEPROM can only be written when the voltage to the part is sufficient.

With the EEPROM tab selected, the File menu will have options to save or open EEPROM data. The save option will allow a file to be created from the current settings even if they have not been programmed to the device. The open option will allow a file to be read and replace the values in the window. These values loaded from the file are not written to the EEPROM until the "Program EEPROM" button is selected. Selecting either the Control or Registers tab before programming will cause the settings to be lost. The settings in the device will be read again when the EEPROM tab is selected again. Selections can be made and saved to a file without having a device connected.

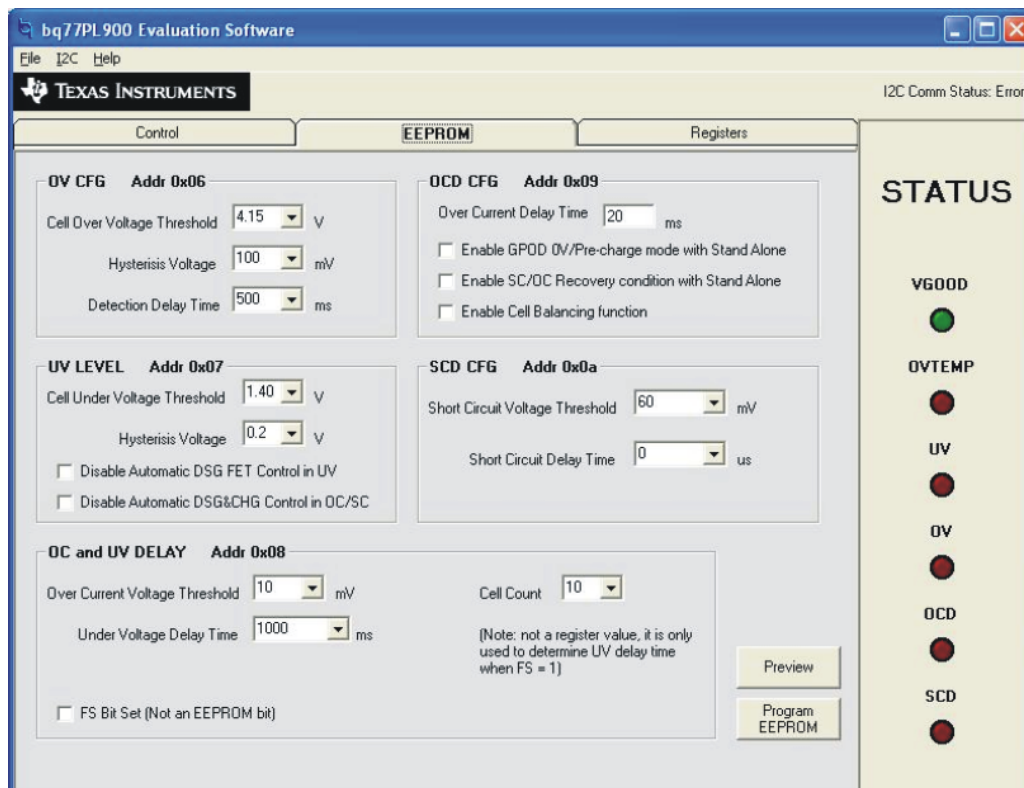


Figure 5. EEPROM Tab Window

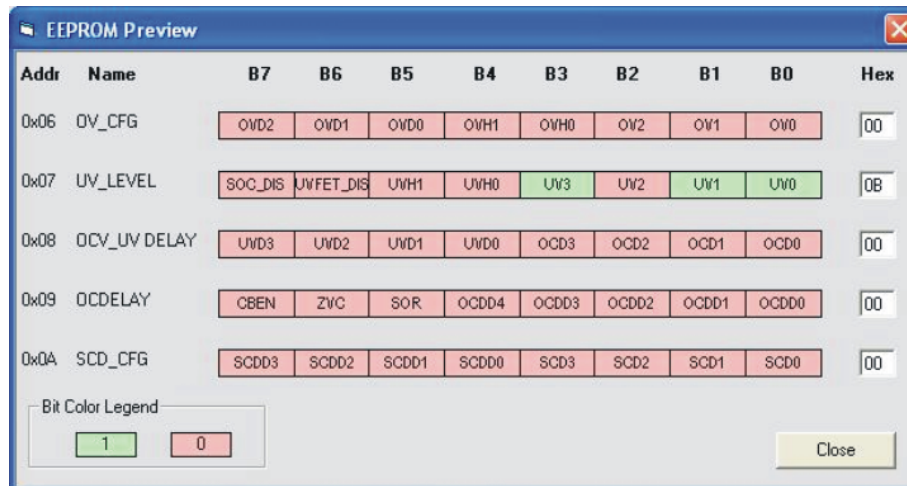


Figure 6. EEPROM Preview Window

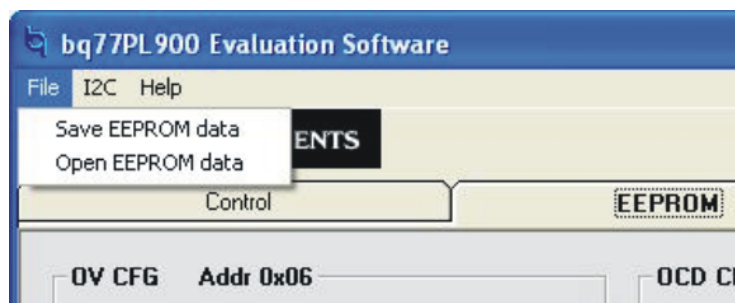


Figure 7. EEPROM File Options

7.4 Basic Operation With Software

The following steps are suggested for basic operation in host mode for a board configured for 10 cells with the default safety configuration in EEPROM.

1. Connect cells or cell simulation resistors and a power supply to the battery side of the board. Set the bench supply (if used) to approximately 20V.
2. Install the software.
3. Connect the EV2300 to the computer with the USB cable.
4. Connect the communication cable from the EV2300 I²C port to the circuit module J12.
5. Start the software.
6. Connect a disabled load to the pack terminals.
7. Wake up the part by momentarily connecting a charge voltage >7.5V to the pack terminals. If the load is disconnected, the user can momentarily short the BATTERY+ to PACK+ with a low value resistor. The device will wake up in standalone mode.
8. Select the control tab in the software window.
9. In the control tab, select 'host' the STATE CONTROL Control Mode box. The features in the window should become clearly visible.
10. Observe using a voltmeter or other method that the pack has no output voltage.
11. In the OUTPUT CONTROL section, select the check boxes for CHG and DSG FETs.
12. Observe using a voltmeter or other method that the pack has an output voltage.
13. Decrease the power supply voltage to approximately 10V. Observe that the UV indicator comes on and the output voltage goes away.

14. Increase the power supply voltage to 20V. Observe that the UV indicator remains on and the output voltage remains off.
15. Click on the Toggle LTCLR button in the OUTPUT CONTROL section. Observe the UV indicator goes out and the output voltage comes on again.

8 Related Documents From Texas Instruments

To obtain a copy of any of the following TI document, call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. When ordering, identify this document by its title and literature number. Updated documents can also be obtained through the TI Web site at www.ti.com

Document	Literature Number
bq77PL900 data sheet	SLUS844
Cell Balancing With the bq77PL900	SLUA463
EV2300 Evaluation Module Interface Board User's Guide	SLUU159A

9 bq77PL900 Circuit Module Physical Construction

This section contains the pcb layout, bill of materials and schematic of the bq77PL900EVM circuit module.

9.1 Board Layout

The bq77PL900EVM circuit module is a 4.5-inch × 3.25-inch 2-layer circuit card assembly. It is designed for easy connection with cell connections on the left side and load connection on the right using standard wires to the terminal blocks. Dual FETs are used to reduce resistance for a design-specified 30A current flow. Wide trace areas are used to reduce voltage drops and provide surface area for heat dissipation without a heatsink. This layout and construction allows easy understanding of the connections for evaluation, but results in a large board. The main solution components are outlined on the silkscreen layer.

See additional information in the configuration and operation sections of this document. [Figure 8](#) to [Figure 13](#) show the board layout.

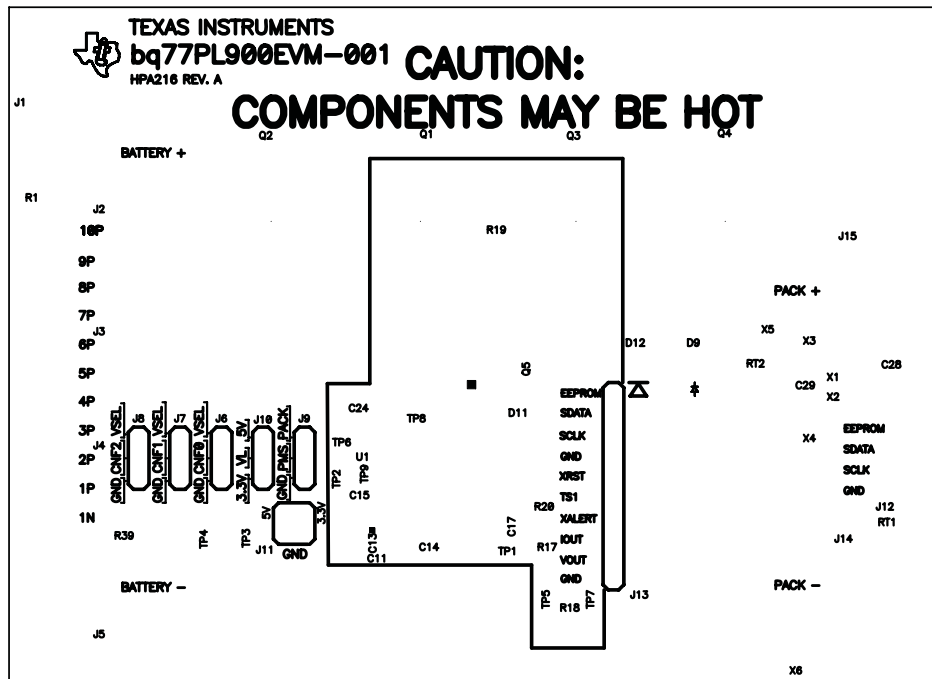


Figure 8. Top Silk Screen

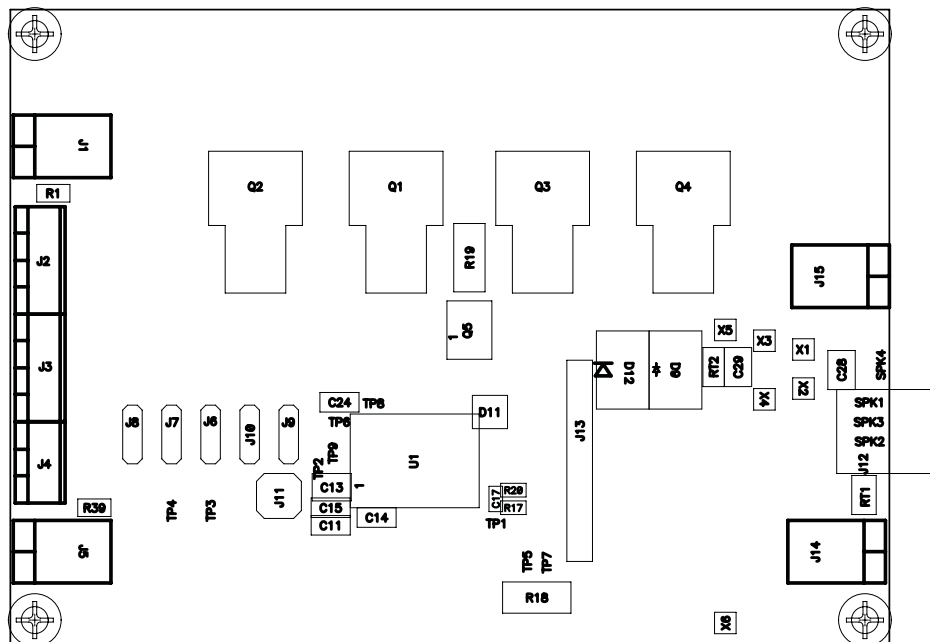


Figure 9. Top Assembly

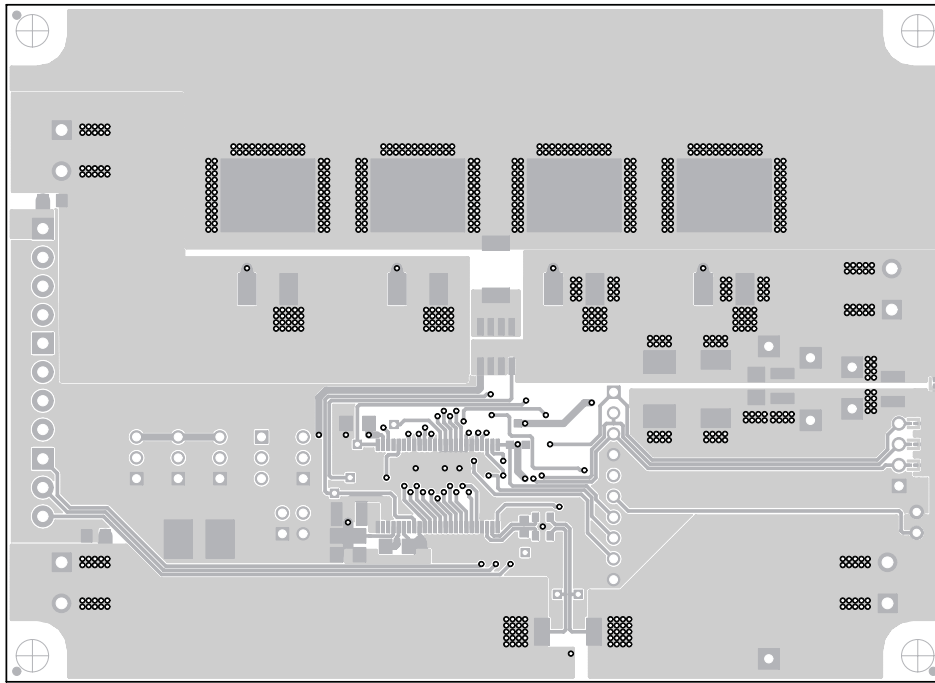


Figure 10. Top Layer

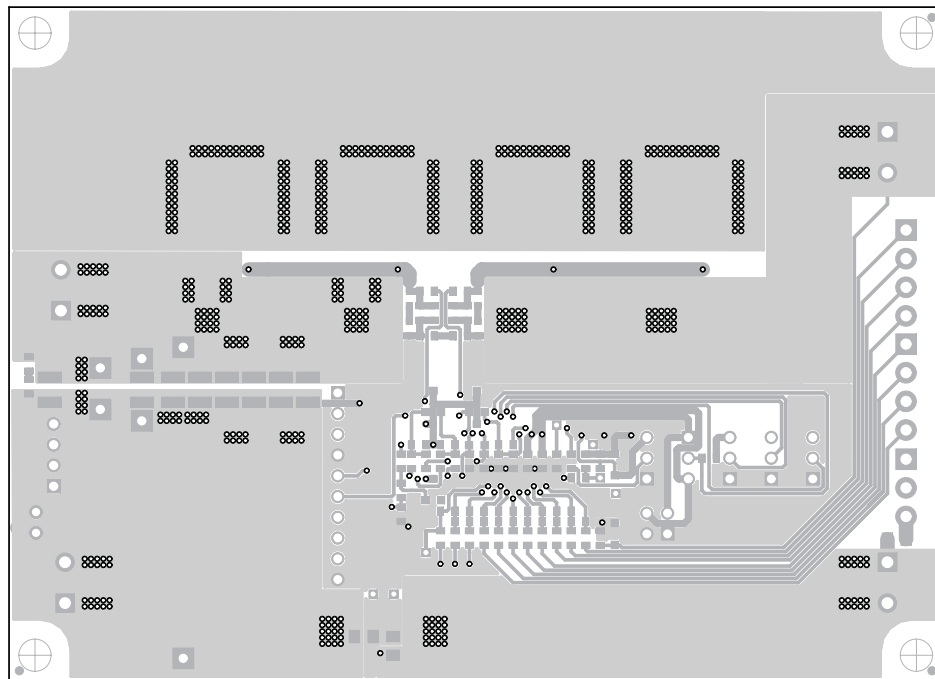


Figure 11. Bottom Layer

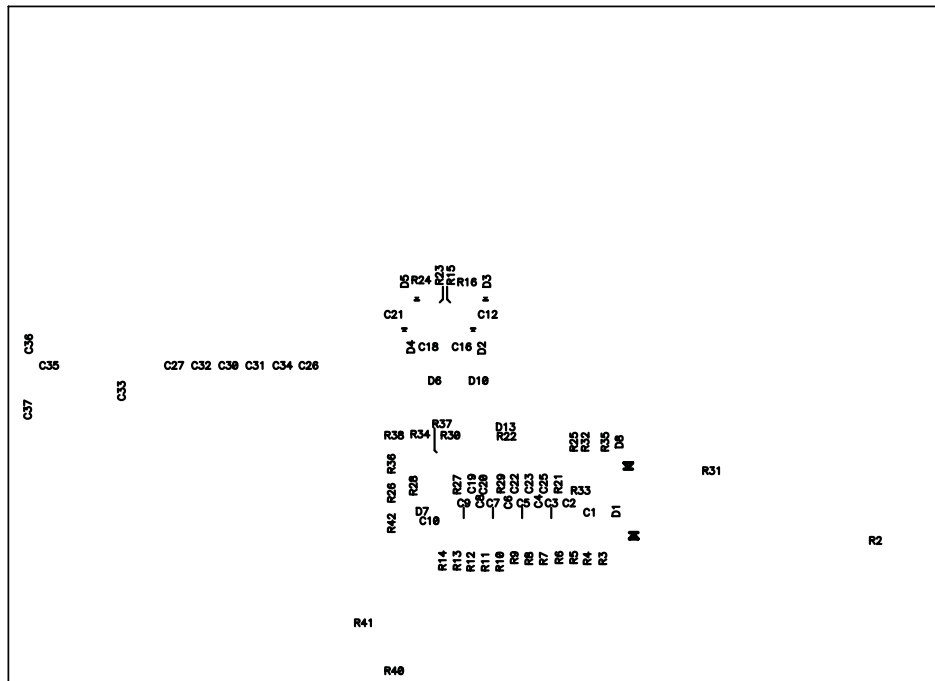


Figure 12. Bottom Silk Screen

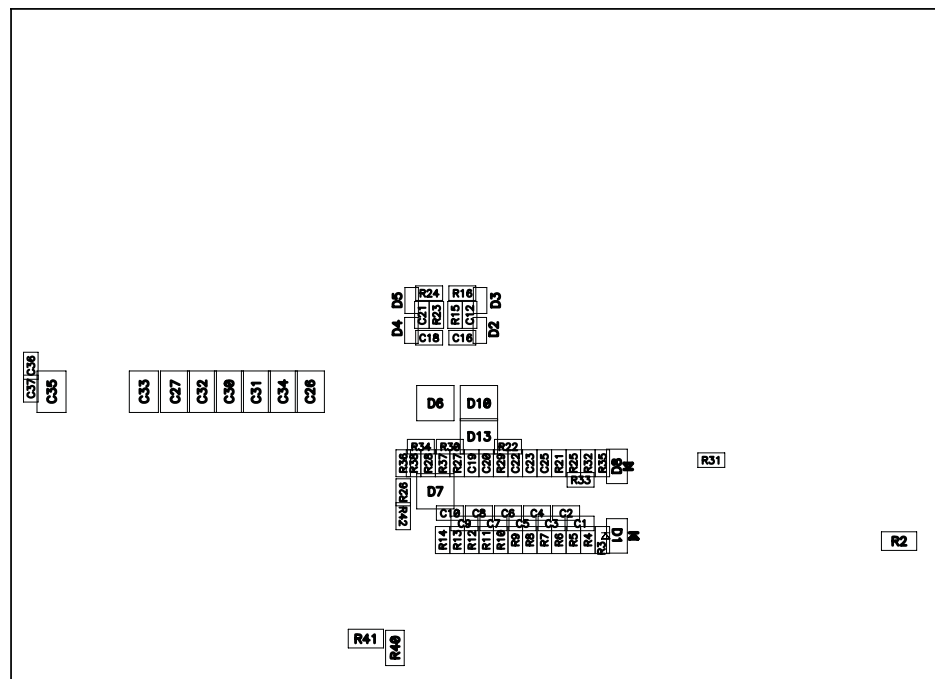


Figure 13. Bottom Assembly

9.2 Bill of Materials

The bill of materials for the circuit module is shown in [Table 10](#). Substitute parts may be used in the manufacturing of the assembly.

Table 10. Bill of Materials

RefDes	Value	Description	Size	Part Number	MFR
C1–C10, C16–C20, C36, C37	0.1 μ F	Capacitor, Ceramic, 50V, X7R, 10%	0603	Std	Std
C11, C24	2.2 μ F	Capacitor, Ceramic, 50V, Y5V, 20%	1206	STD	Std
C12, C21	4.7 nF	Capacitor, Ceramic, 50V, X7R, 20%	0603	Std	Std
C13	4.7 μ F	Capacitor, Ceramic, 50V, Y5V, 20%	1210	Std	Std
C14, C15	1 μ F	Capacitor, Ceramic, 50V, X7R, 10%	1206	Std	Std
C22	10 nF	Capacitor, Ceramic, 16V, X7R, 20%	0603	Std	Std
C23, C25	2.2 μ F	Capacitor, Ceramic, 16V, X7R, 20%	0603	Std	Std
C26–C35	2.2 μ F	Capacitor, Ceramic, 100V, X7R	1210	GRM32ER72A225K	Murata
D1, D8		Diode, Switching, 90V, 225 mA Ifm, High speed	SOD-323	1SS355	Rohm
D10, D11, D13		Diode, TVS Bidirectional , 17 A, 300V	SOT23	SM05T1	ON Semiconductor
D12		Diode, Schottky 3-A 100-V	SMC	MBRS3100T3	On Semi
D2–D5		Diode, Zener, 300mW, 16V	SOD-523	BZX585-C16	Philips
D6, D7		Diode, Dual, Zener, 5.6V, 300mW	SOT23	AZ23C5V6	Vishay-Telefunken
D9		Diode, SMT TVS Unidirectional	DO-214AB	1.5SMCxxx	TSC
J1, J5, J14, J15		Header, Side Entry 2-pin, 5 mm spacing	0.441 \times 0.200 inch	1711026	Phoenix Contact
J11		Header, 2x2-pin, 100 mil spacing (36-pin strip)	0.20 \times 0.20 inch	PTC36DAAN	Sullins
J12		Header, Friction Lock Ass'y, 4-pin Right Angle,	0.400 \times 0.500 inch	22-05-3041	Molex
J13		Header, Male 10-pin, 100mil spacing, (36-pin strip)	0.100 inch \times 10	PTC36SAAN	Sullins
J2, J3		Terminal Block, 4-pin, 6-A, 3.5 mm	0.55 \times 0.25 inch	ED555/4DS	OST
J4		Terminal Block, 3-pin, 6-A, 3.5 mm	0.41 \times 0.25 inch	ED555/3DS	OST
J6–J10		Header, Male 3-pin, 100mil spacing, (36-pin strip)	0.100 inch \times 3	PTC36SAAN	Sullins
Q1–Q4		MOSFET, P-ch, –80V, –110A	DDPAK	SUM110P08-11L	Vishay
Q5		Trans, P-Chan 60V 3A	SO-8	NDS9407	Fairchild
R1, R2, R39	0	Resistor, Chip, 1/10W, 5%	0805	Std	Std
R15, R23, R30, R34	1M Ω	Resistor, Chip, 1/16W, 5%	0603	Std	Std
R16, R21, R24	1K Ω	Resistor, Chip, 1/16W, 5%	0603	Std	Std
R17, R20	200 Ω	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R18	0.001 Ω , 1W \pm 275ppm	Resistor, Chip, 1W, 1%	2512	WSL25121L000FEA	Vishay
R19	1.78k Ω	Resistor, Chip, 1W, 1%	2512	Std	STD
R22	6.98k Ω	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R25, R31, R35	100k Ω	Resistor, Chip, 1/16W, 5%	0603	Std	Std
R26–R28, R36–R38	100 Ω	Resistor, Chip, 1/16W, 5%	0603	Std	Std
R29	61.9k Ω	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R3, R42	10k Ω	Resistor, Chip, 1/16W, 5%	0603	Std	Std
R32	390k Ω	Resistor, Chip, 1/16W, 5%	0603	Std	Std
R33	820k Ω	Resistor, Chip, 1/16W, 5%	0603	Std	Std
R4–R14	510 Ω	Resistor, Chip, 1/16W, 5%	0603	Std	Std
R40, R41		Resistor, Chip, 1/10W, 5%	0805	Std	Std
RT1**	10k Ω	Thermistor, TH, \pm 1%	0.095 \times 0.150 inch	103AT-2	Semitec
RT2		Varistor	1206	VxxMLx1206N	Littelfuse
SPK1–SPK4		Spark Gap, 0.010 inch space	0.050 \times 0.070 inch	Spark Gap	mfg
TP1, TP2, TP5–TP9		Test Point, 0.020 Hole	0.043 inch	STD	STD
TP3, TP4		Test Point, SM, 0.150 \times 0.090	0.185 \times 0.135 inch	5016	Keystone
U1		IC, 5-10 Series Cell L-Ion or L-Polymer Battery Protection and AFE	SSOP-48	BQ77PL900DL	TI
X1– X6		Through Hole, O.040 Dia		STD	STD
—		PCB		HPA216	Any
		Shunt, 100-mil black		929950-00	3m

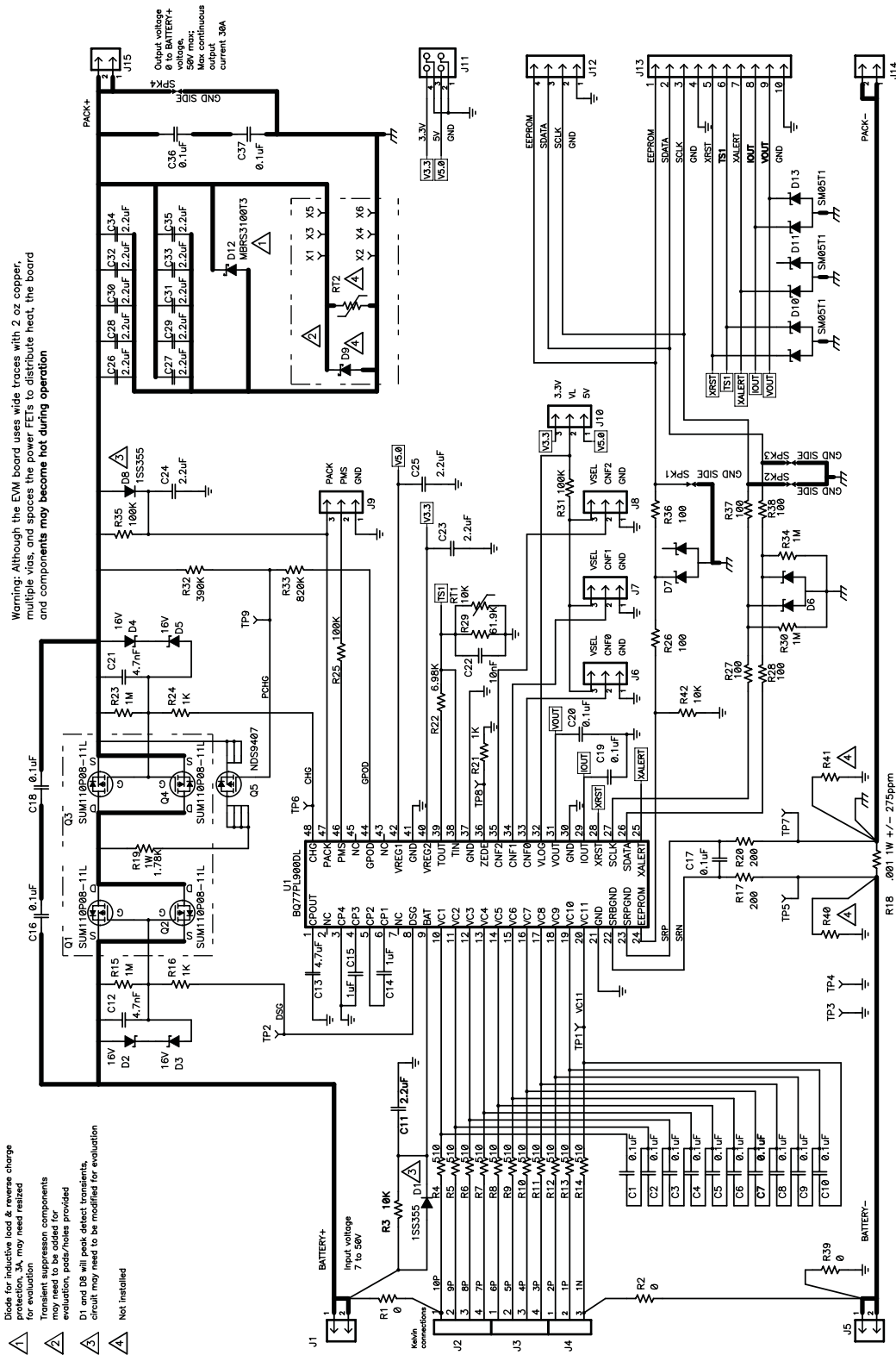


Figure 14. Schematic Diagram

9.3 **bq77PL900 Circuit Module Performance Specification Summary**

This section summarizes the performance specifications of the bq6400 circuit module.

Typical voltage will depend on the number of cells configured. Typical current will depend on the application. Board cooling may be required for continuous operation at or below maximum current.

Table 11. Performance Specification Summary

Specification	Min	Typ	Max	Unit
Input voltage PACK+ to PACK-	7.5	–	50	V
Continuous charge and discharge current	0	–	30	A

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IMPORTANT: TI is providing the enclosed bq77PL900EVM-001 evaluation module under the following conditions:

This evaluation module (EVM) being provided by Texas Instruments (TI) is intended for use for ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY and is not considered by Texas Instruments to be fit for commercial use. As such, this EVM may not be complete in terms of design and/or manufacturing related protective considerations including product safety measures typically found in the end-product incorporating the module. As a prototype, this product does not fall within the scope of the European Union Directive on electromagnetic compatibility and on low voltage and therefore may not meet the technical requirements of the directive. This EVM is not subject to the EU marking requirements.

- **Should this EVM not meet the specifications indicated in the User's Guide the EVM may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY TI AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.**
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- Please read the User's Guide and specifically the section in the User's Guide pertaining to warnings and restrictions prior to handling the product. This section contains important information regarding high temperature and voltages which TI recommends to be read before handling the EVMs. In case of any doubt regarding safety, please contact the TI application engineer.
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Table 12. EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage and the output voltage ranges as specified in the table below.

Input Range, $V_{\text{BATTERY+}}$	0 V to 50 V
Output Range, $V_{\text{PACK+}}$	0 V to 50 V

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60° C. The EVM is designed to operate properly with certain components above 60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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