AN2495
Application note

80 W Very wide input voltage range 3-phase SMPS designed based on L6565 and ESBT STC04IE170HV

Introduction

The purpose of this application note is to explain the design of a 80 W 3-phase auxiliary power supply for Motor Drives and Welding Applications. To have a very good system in terms of both efficiency and cost, the L6565 PWM controller has been selected as well as the STC04IE170HV as the main switch. The combination of these ST parts is to target a highly efficient solution for high DC input voltage, a typical requirement of any three-phase application. The L6565 driver is a variable frequency PWM driver suitable to a design flyback converter working in Quasi-Resonant mode. It boasts some very interesting additional features.

The study on the frequency response, reported in the present document, has been carried out using MATLAB.

All the design choices are thoroughly discussed to allow the user to adapt the project to specific needs. The input voltage can also be extended up to 1000 V DC because there is enough margin to do so. Finally, the experimental results are analyzed to better understand the benefits given by the use of ESBT in this application.

The document is associated with the release of the STEVAL-ISA019V1 (see figure below).

80 W 3-phase SMPS (working prototype)

Contents

List of figures

1 Design specifications and L6565 brief description

Table 1 lists the converter specification data and the main parameters fixed for the demo board.

Table 1. Converter specification data and fixed parameters

Symbol	Description	Values
V_{inmin}	Rectified minimum Input voltage	250
V_{inmax}	Rectified maximum Input voltage	850
V_{out}	Output voltage 1	24 V/3.33 A
V_{aux}	Auxiliary output voltage	15 V/0.1 A
P_{out}	Maximum output Power	80 W
h	Converter efficiency	> 80%
F	Minimum switching frequency	50 kHz
V_{spike}	Max over voltage limited by clamping circuit	200 V

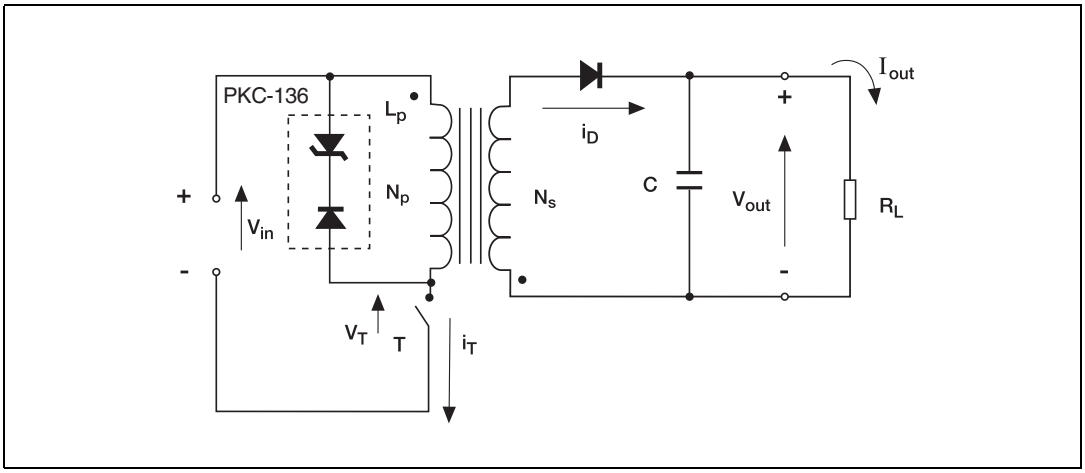
Figure 1 shows a simplified schematic diagram of a fly-back converter.

L6565 has a current mode control and as already stated, is designed to build flyback converters working in quasi-resonant mode and ZVS (zero voltage switching) at turn-on or at least Quasi ZVS that means valley switching during turn-on. This condition allows the designer to reduce as much as possible the power losses at turn-on.

Since the input range is from 250 V up to 850V, the ZVS is obtained only when $V_{in}=V_{inmin}=V_{fl}=250$ V.

L6565 has 8 pin. For the detailed explanation of each pin function please refer to the L6565 datasheet.

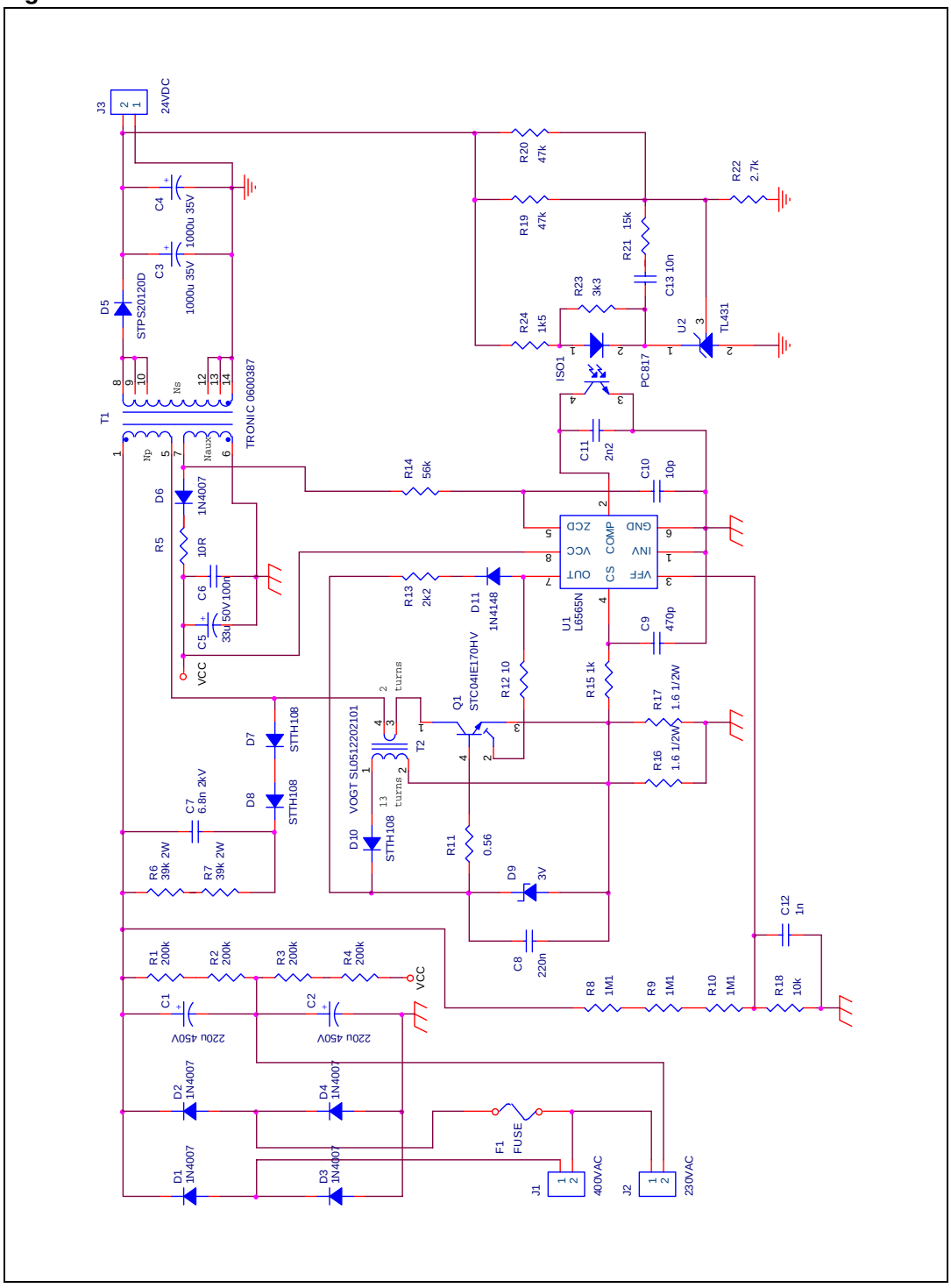
Figure 1. Flyback topology basic diagram



2 Flyback stage design

In *Figure 2* the complete schematic of the 80 W SMPS is shown.

Figure 2. Evaluation board schematic



As commonly known, the voltage stress on the device (power switch) is given by:

Equation 1

$$V_{off} = V_{inmax} - V_{fl} - V_{spike}$$

where V_{fl} = flyback voltage = (V_{out} + $V_{F,\ diode}$)*N_p/N_s and V_{spike} is the maximum over voltage allowed by the clamping network. It has been fixed 200 V. N_p is the number of turns on the primary side while N_s is the number of turns on the main output secondary winding.

Now, taking into account a 200 V margin, the maximum flyback voltage that can be chosen is:

Equation 2

$$V_{fl} = BV - V_{inmax} - V_{spike} - V_{margin} = 1700 - 1000 - 200 - 250 = 250V$$

After calculating the flyback voltage, proceed with the next step in the converter design.

The turn ratio between primary and secondary side is calculated with the following formula:

Equation 3

$$\frac{N_p}{N_s} = \frac{V_{fl}}{V_{out} + V_{F,\ diode}} = \frac{250}{24 + 1} = 10$$

As a first approximation, since the turn-on of the device occurs immediately after the energy stored on the primary side inductance has been totally transferred to the secondary side:

Equation 4

$$V_{dcmin} T_{onmax} = V_{fl} T_{reset}$$

and

Equation 5

$$T_{onmax} + T_{reset} = T_S$$

Where T_{onmax} is the maximum on time, T_{reset} is the time needed to demagnetize the transformer inductance and T_S is the switching time.

Combining the two previous equations T_{onmax} results in:

Equation 6

$$T_{onmax} = \frac{V_{fl} \bullet T_S}{V_{dcmin} + V_{fl}} \cong 10\mu s$$

The next step is to calculate the peak current. According to the converter specification of *Table 1*, output power of 80 W and desired efficiency (at least 80%), by using a formula that does not take into account the losses on the power switch, on the input bridge, and on the rectified network, we have:

Equation 7

$$P_{IN} = 1.25P_{OUT} = \frac{\frac{1}{2} \bullet L_P I_P^{\ 2}}{T_S} = \frac{\frac{1}{2} V_{dcmin}^{\ 2} T_{onmax}^{\ 2}}{L_P T_S}$$

Hence

Equation 8

$$L_P = \frac{V_{dcmin}^{2} T_{onmax}^{2}}{2.5 T_S P_{OUT}} = 1.56mH$$

From here now we can calculate the peak current on primary.

Equation 9

$$I_P = \frac{V_{dcmin} T_{onmax}}{L_P} = 1.6A$$

2.1 Transformer design

2.1.1 Core size

The core size has to be chosen according to the power that must be managed, the primary inductance, and the saturation current as well. An approximate but efficient formula could be used as a starting point. Eventually at the end, the designer may choose a bigger core and repeat the following steps.

Equation 10

$$A_P = 10^3 \left[\frac{L_P I_{rms(primary)}}{\Delta T^{\frac{1}{2}} \bullet K_u \bullet B_{max}} \right]^{1.316} \quad [cm^4]$$

Where:

- ΔT is the maximum temperature variation with respect to the ambient temperature
- K_U is the utilization factor of the window (say the portion of the window used for winding that generally ranges between 0.4 and 0.7)
- B_{max} is the maximum flux in the core.

From *Equation 10*, at the end an ETD34 is the best choice.

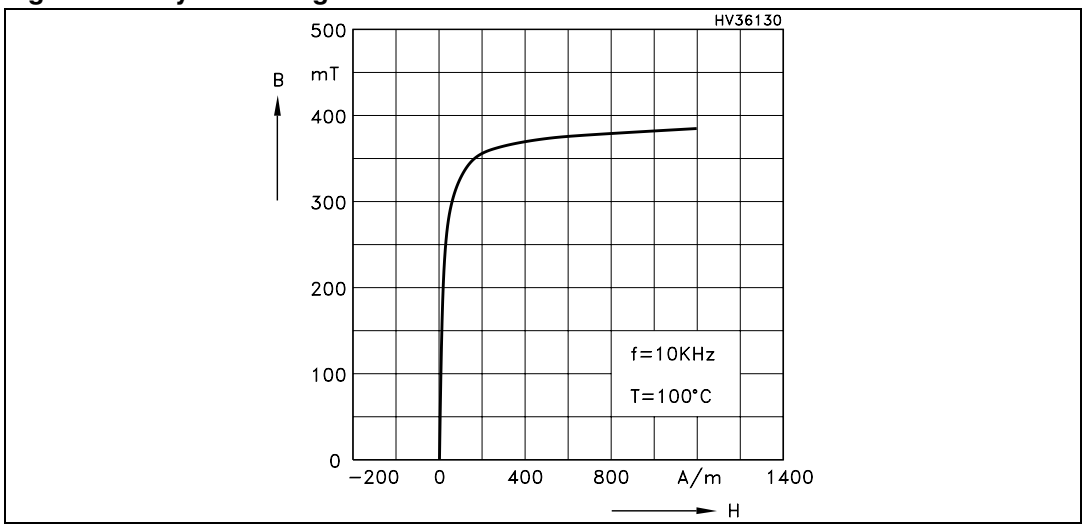
2.1.2 Transformer losses and air gap

From Faraday's law we can define the minimum primary winding turns to avoid saturation of the core. Looking at the saturation curve of the core, we can safely work up to 200 mT:

Equation 11

$$N_{pmin} = \frac{V_{in,\ min} \bullet T_{O(N,\ max)}}{\Delta B \bullet A_e} = \frac{250 \bullet 10\mu}{0.200 \bullet 97\mu} = 117$$

Figure 3. Dynamic magnetization curves



Concerning the gap, from the EPCOS datasheet, we can use the following approximate formula:

Equation 12

$$l_g = \text{gaplenght} = \left(\frac{A_L}{K_1}\right)^{\frac{1}{K_2}}$$

$K_1 = 153$, $K_2 = -0.713$, while A_L has to be calculated.

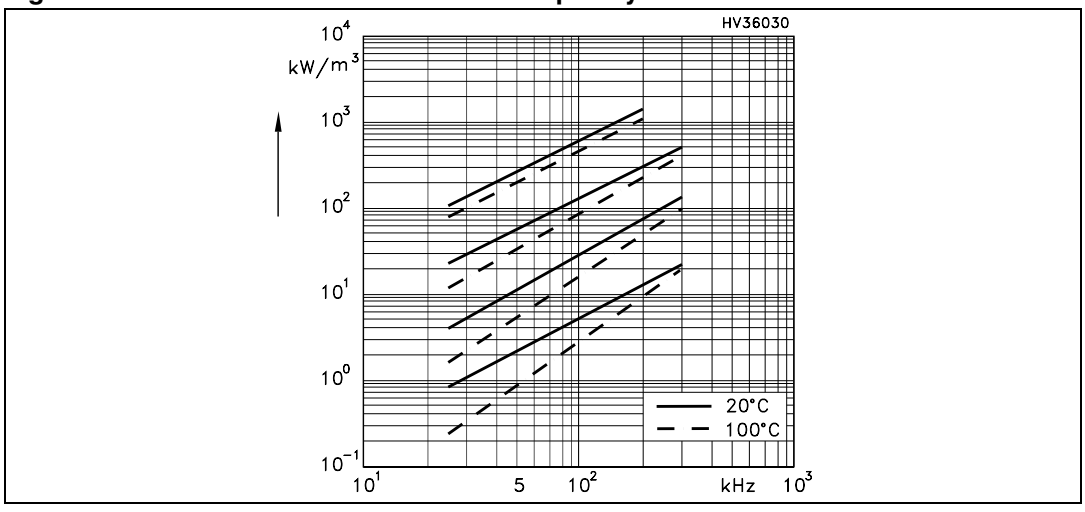
Knowing that $L_p = 1.56mH$ and $N_p = 120$,

Equation 13

$$A_L = \frac{L_P}{N^2_P} = \frac{1.56m}{120^2} = 108nH$$

Hence: $l_g = \text{gaplenght} = \left(\frac{108}{153}\right)^{\frac{1}{-0.713}} = 1.63mm$

Figure 4. Relative core losses versus frequency



From *Figure 4*, operating at 50 kHz with 220 mT flux excursion, the power dissipation density is about 300 mW/cm^3. Once again, referring to the datasheet, the total volume of ETD 34 is 7.63 cm^3, therefore:

Equation 14

$$P_{core} = 0.3 \bullet 7.6 = 2.29W$$

Assuming a 95% efficiency for the transformer, only 4 W can be lost on it, of which about 2.3 is lost on the core while the residual 1.7 W is dissipated on the copper. Achieving this efficiency is detailed in the following *Section 2.1.3: Wire size*.

2.1.3 Wire size

To chose the right wire size we must know the rms current on both the primary and secondary side. Since $I_{peak,\ primary}$ = 1.6 A and $I_{peak,\ secondary}$ = 16 A,

Equation 15

$$I_{rms,\ primary} = 0.65A \quad \text{and} \quad I_{rms,\ secondary} = 6.53A$$

By imposing a 1 W loss on the primary side wire, the maximum series resistance can be calculated as follows:

From the Joule law we can calculate the resistance of both the primary and secondary winding.

Equation 16

$$R_P = \frac{P_{CU,\ pri}}{I_{PRMS}^2} \Rightarrow R_P = 2.36\Omega \qquad R_S = \frac{P_{CU,\ sec}}{I_{SRMS}^2} \Rightarrow R_S = 0.016\Omega$$

From that, knowing the copper resistivity at 100 °C (ρ_{100} = 2.303 10^{-6} Ω cm), and the average wind length L_t (L_t = 5.6 cm), we can easily calculate the wire sections (in cm^2).

Equation 17

$$A_{PCU} = \frac{\rho_{100} N_p L_t}{R_P} = 6.54 \bullet 10^{-4} \qquad [cm^2] \Rightarrow d_p = 0.028[cm]$$

Equation 18

$$A_{SCU} = \frac{\rho_{100} N_S L_t}{R_S} = 0.0096 \qquad [cm^2] \Rightarrow d_s = 0.011[cm]$$

From *Table 2*:

Table 2. Skin effect AC/DC resistance ratios for square - wave currents

		25 kHz			50 kHz			100 kHz			200 kHz		
wire no.	Diameter d, mils	Skin depth S, mils	d/S	R_{ac}/R_{dc}	Skin depth S, mils	d/S	R_{ac}/R_{dc}	Skin depth S, mils	d/S	R_{ac}/R_{dc}	Skin depth S, mils	d/S	R_{ac}/R_{dc}
12	81.6	17.9	4.56	1.45	12.7	6.43	1.55	8.97	9.10	2.55	6.34	12.87	3.50
14	64.7	17.9	3.61	1.30	12.7	5.08	1.54	8.97	7.21	2.00	6.34	10.21	2.90
16	51.3	17.9	2.87	1.10	12.7	4.04	1.25	8.97	5.72	1.70	6.34	8.09	2.30

Table 2. Skin effect AC/DC resistance ratios for square - wave currents (continued)

		25 kHz			50 kHz			100 kHz			200 kHz		
wire no.	Diameter d, mils	Skin depth S, mils	d/S	R_{ac}/R_{dc}	Skin depth S, mils	d/S	R_{ac}/R_{dc}	Skin depth S, mils	d/S	R_{ac}/R_{dc}	Skin depth S, mils	d/S	R_{ac}/R_{dc}
18	40.7	17.9	2.27	1.05	12.7	3.20	1.15	8.97	4.54	1.40	6.34	6.42	1.85
20	32.3	17.9	1.80	1.00	12.7	2.54	1.05	8.97	3.60	1.25	6.34	5.09	1.54
22	25.6	17.9	1.43	1.00	12.7	2.02	1.00	8.97	2.85	1.10	6.34	4.04	1.30
24	20.3	17.9	1.13	1.00	12.7	1.60	1.00	8.97	2.26	1.04	6.34	3.20	1.15
26	16.1	17.9	0.90	1.00	12.7	1.27	1.00	8.97	1.79	1.00	6.34	2.54	1.05
28	12.7	17.9	0.71	1.00	12.7	1.00	1.00	8.97	1.42	1.00	6.34	2.00	1.00
30	10.1	17.9	0.56	1.00	12.7	0.80	1.00	8.97	1.13	1.00	6.34	1.59	1.00
32	8.1	17.9	0.45	1.00	12.7	0.84	1.00	8.97	0.90	1.00	6.34	1.28	1.00
34	6.4	17.9	0.36	1.00	12.7	0.50	1.00	8.97	0.71	1.00	6.34	1.01	1.00

Note: To completely avoid the skin effect, the maximum diameter which is allowed is 20.3 mils which means 0.5 mm.

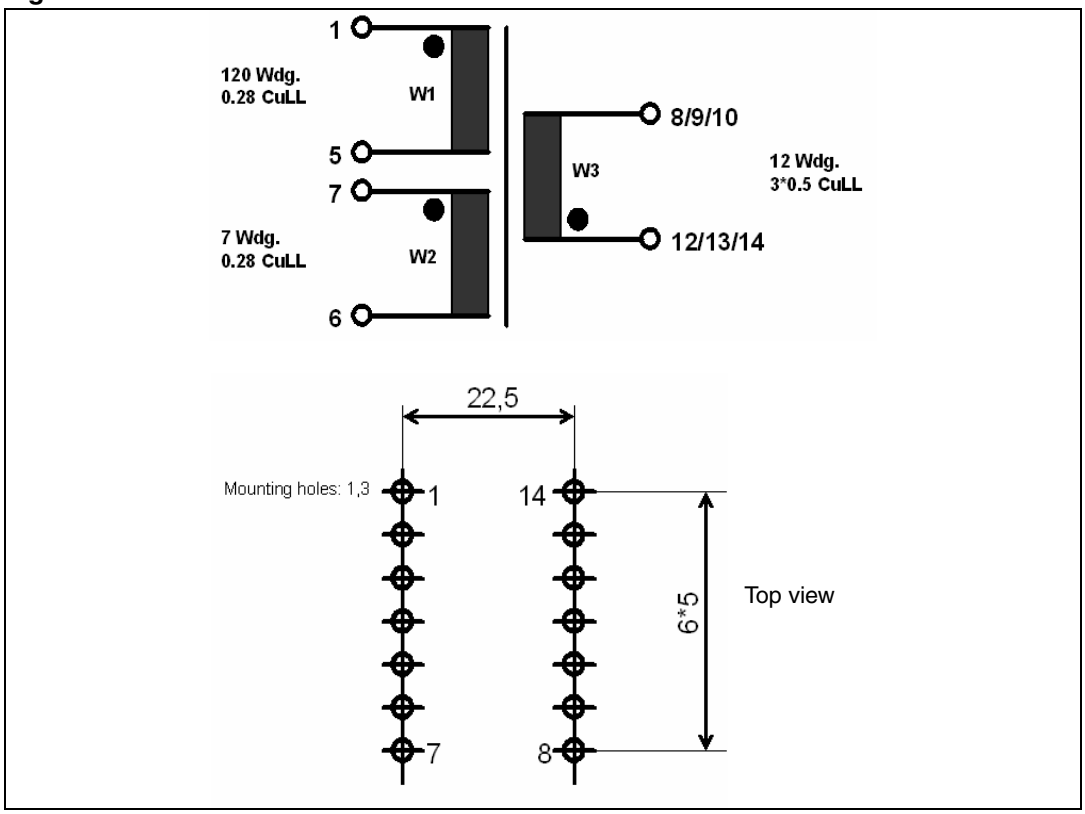
For practical considerations and to better optimize the utilization of the transformer window and at the same time in accordance with *Equation 15* to *Equation 18* and *Table 2*, it can be determined that:

Equation 19

$$d_p = 0.028[cm] \qquad d_s = 0.05[cm] \quad 3 \text{ in parallel}$$

The specifications of the transformer provided by TRONIC according to the above calculations are shown in *Figure 5*.

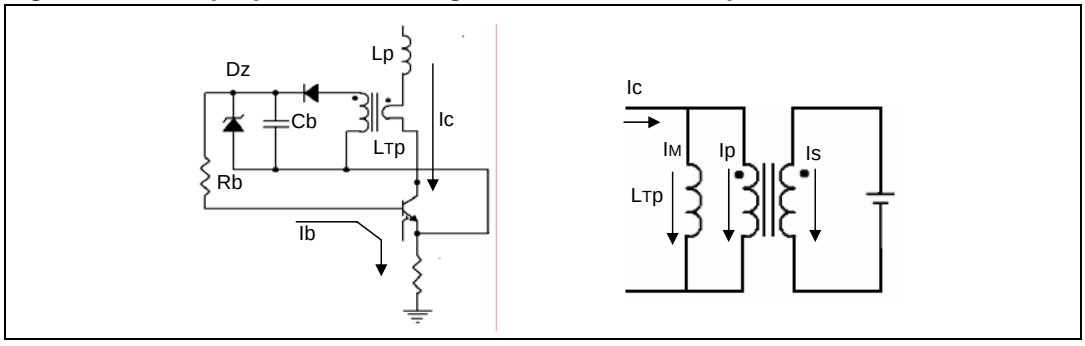
Figure 5. Power transformer Tronic 0600387



3 Base driving circuit design

In practical application, such as SMPS, where the load is variable, the collector current is variable as well. As a consequence it is very important to provide a base current to the device which is related to the collector. In this way it is possible to avoid device over-saturation at low load and to optimize the performance in terms of power dissipation. The best and simplest way to do this is the proportional driving method provided by current transformer, in *Figure 6* At the same time, it is very useful to provide a short pulse to the base to make the turn-on as fast as possible and to reduce the dynamic saturation phenomenon. The pulse is achieved by using the capacitor and the zener in *Figure 6*.

Figure 6. The proportional driving schematic and its equivalent circuit



The I_C/I_B ratio is fixed once the current transformer turn ratio has been chosen. From ESBT STC04DE170 datasheet, and especially looking at the storage time characterization, it is clear that a turn ratio equal to 5 is a good value to ensure the right saturation of ESBT at Ic = 2 A, so that in the current transformer we can fix at first:

Equation 20

$$\frac{N_P}{N_S} = \frac{1}{5}$$

The core magnetic permeability of current transformer has to be as high as possible in order to minimize the magnetization current Im (that is not transferred to the secondary side but only drives the core into saturation). On the contrary, too high permeability core may lead the core into saturation even with a very small magnetization current. To avoid saturation, it is necessary to increase the number of primary turns and the size of the core as well. If a core with a very small magnetic permeability is chosen, it is possible to reduce the number of primary turns and the core size. If the permeability is too small, we may not have current on the secondary side because almost all the collector current becomes magnetization current. As a compromise, a ferrite material with a relative permeability in the range 4500 ÷ 7000 is the best choice.

After selecting the ferrite ring diameter, the minimum primary turns is determined to avoid core saturation from the preliminarily fixed turn ratio N with 0.2. By applying Faraday's law and imposing the maximum flux B_{max} equals to $B_{sat}/2$:

Equation 21

$$V_1 = N_{TP} \bullet \frac{d\varphi}{dt} \cong N_{TP} \bullet A_e \bullet \frac{\Delta B}{\Delta T} \Rightarrow N_{TP} = 2 \bullet \frac{V_1 \bullet T_{onmax}}{A_e \bullet B_{sat}}$$

Where, B_{sat} is the saturation flux of the core which depends on the magnetic permeability.

During the conduction time, the junction base-emitter of ESBT can be seen as a forward biased diode. To complete the secondary side load loop, the voltage drop on both diode D and resistor RB must be added in series with the base of the ESBT. The equivalent secondary side voltage source is given by:

Equation 22

$$V_S = V_{BEon} - V_D - V_{RB} \cong 2.5V$$

Since the magnetization inductance cannot be neglected, only I_P, a fraction of the total collector current, is transferred to the secondary. As a result, the magnetization current has to be first as low as possible. Meanwhile, the value of the magnetization inductance must be taken into account for the proper calculation of transformer primary turns and turns ratio. The magnetization voltage drop, that is, the voltage at the primary of the current transformer, can now be easily calculated:

Equation 23

$$V_1 = V_S \bullet \frac{N_{1T}}{N_{2T}} = 2.5 \bullet \frac{1}{5} = 0.5(V)$$

The magnetization current will be:

Equation 24

$$I_{Mmax} = \frac{V_1 T_{ONmax}}{L_{TP}}$$

The number of primary turns should be increased if I_{Mmax} is relatively high. The core must have window area large enough to hold all primary and secondary windings. Otherwise it is necessary to choose a bigger core size. Once both core material and size are fixed, the turn ratio must be adjusted to get the desiderated I_C/I_B ratio according to *Equation 25* below:

Equation 25

$$N_{eff} = \frac{I_P}{I_B} = \frac{I_{Cmax} - I_{Mmax}}{\frac{I_C}{5}}$$

where I_{Mmax} is the maximum magnetization current.

The insulation between primary and secondary should be considered since the voltage on the primary side during the off time can surpass 1500 V.

The next step is to select the zener diode, the capacitor C_b, and the resistor R_b. The turn-on performance of ESBT is related to the initial base peak current and its duration t_{peak} that is approximately given by *Equation 26*:

Equation 26

$$t_{peak} = 3R_bC_b$$

A suitable value for R_b is 0.56 Ω It can eliminate the ringing on the base current after the peak, and at the same time, it generates negligible power dissipation.

The value t_{peak} can be determined once the minimum on time is set based on the operation frequency. Bear in mind that in practical application, it should never be lower than 200ns. The value of C_b can be counted since the values of t_{peak} and R_b are known.

I_{peak} must be limited in order to avoid an extra saturation of the device. The zener diode D_z controls this and clamps the voltage across the small capacitor C_b. The zener must be chosen according to the following empiric formulas and inside the range of V_{Zmin} and V_{Zmax}:

Equation 27

$$V_{Zmax} = 2(I_{peak}R_b + 1) \qquad V_{Zmin} = 2(I_{peak}R_b)$$

The base peak current is higher with higher clamp voltage (D_z) or smaller capacitance (C_b), which in turn will lead to shorter duration of the peak time.

The higher and longer the base peak current is, the lower the power dissipation during turn-on. The designer must limit the I_b peak both in terms of amplitude and time duration otherwise at low load a very high saturation level may result. If the device is oversaturated, the storage time is too long with higher power dissipation during turn-off. Moreover a long storage time can also lead to output oscillation especially at high input voltage. To overcome the above mentioned problems, it is suggested to set the peak duration to 1/3 the minimum duty cycle.

Following all the formulas mentioned in this section applied to the present job gives:

Equation 28

$$N_{TP} = 2 \bullet \frac{V_1 \bullet T_{onmax}}{A_e \bullet B_{sat}} \approx 2$$

where A_e is the magnetic area considering a ring core with 12.5 mm diameter and the saturation field B_{sat} is 400 mT.

From the first approximated assumption NS should be 10. From bench verification it's very simple to verify that the turn ratio to get the best trade-off between conduction and turn-off losses is 6.

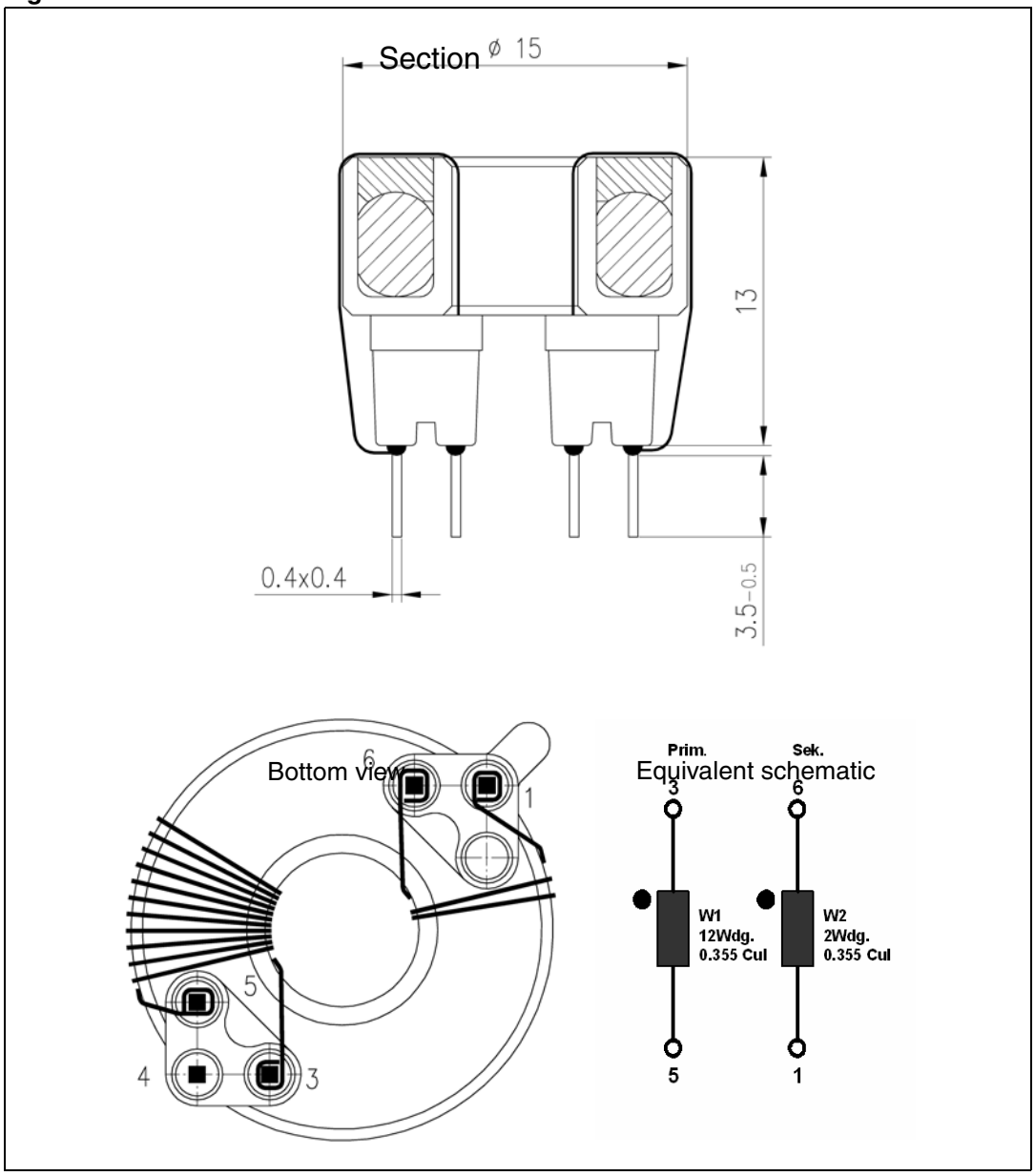
Of course, this verification and final decision has been taken after setting all the other components in the driving network and exactly:

Equation 29

$$t_{peak} = 3R_bC_c = 400ns = C_b = 238nF = C_b = 220nF \text{ (closet commercial value)}$$

Finally the zener has been set to 3 V. *Figure 7* shows current transformer specifications:

Figure 7. Current transformer SL 051 220 21 01



4 Output circuit design

In order to choose the output capacitor, the series resistance of the electrolytic capacitor must be defined.

It is well known that the main cause of the output ripple is the series resistance of the electrolytic capacitor, known as ESR, while the capacitive ripple is absolutely negligible.

Therefore knowing the secondary side peak current is 16 A and imposing a resistive ripple equal to 2% (0.48 V), we have:

Equation 30

$$ESR < \frac{V_{ripple}}{I_{SP}} = \frac{0.48}{16} = 0.03\Omega$$

Using very low ESR output capacitances, from the catalogue we get the relation $ESR*C=32e^{-6}s$ from which:

Equation 31

$$C_{out} > \frac{32 \bullet 10^{-6}}{ESR} = 1066\mu F$$

To have some margin and to have a better thermal spread the final choice is to use two 680 µF capacitors in parallel.

From the Kirchoff voltage law we can calculate the maximum voltage stress on the output diode:

Equation 32

$$V_{off-diode} = V_{out} + \frac{N_S}{N_P} \bullet V_{inmax} = 109V$$

Finally adding a 10% margin, the STPS20120D has been selected.

5 Start-up network design

To allow the circuit to start as soon as the line voltage is applied, it is necessary to pre-charge both C_5 and C_8 capacitances.

A resistor connected to the DC bus directly makes the pre-charge of C_5 electrolytic capacitance. The circuit must start at a minimum DC input voltage of 250 V. The current required by L6565 driver during start-up time determines the (R_1+ R_2+ R_3+ R_4) value. Considering that L6565 driver needs a 0.07 mA maximum start-up current, we obtain:

Equation 33

$$(R_1 + R_2 + R_3 + R_4) < \frac{V_{inmin}}{I_{SU}} = \frac{250V}{0.07mA} \cong 3.6M\Omega$$

Start-up resistance must be lower than 3.6 MΩ in order to reach the best trade-off between power dissipation and time-to-start. As a consequence, before choosing start-up resistor,

we have to determine C_5 capacitance value, which is set according to another requirement. C_5 must be able to supply L6565 driver until the steady state behavior of the converter is established. The time from bench verification is 20 ms maximum. Being minimum hysteresis-voltage (difference between start-up threshold and under-voltage threshold) of L6565 3.7 V, the voltage across C5 has to decrease less than 3.7 V during the start-up period. From L6565 datasheet we know that maximum quiescent current after turn-on is 3.5 mA, then C5 must be chosen such that:

Equation 34

$$\Delta V = \frac{I_Q \bullet \Delta t}{C_5} < 3.7V \Rightarrow C_5 > \frac{3.5mA \bullet 20ms}{3.7V} \cong 19\mu F$$

C_5=33 µF is a good choice in order to guarantee a good margin.

Finally we can set the start-up resistance value in order to reduce time-to-start and contemporarily optimize standby power dissipation. The L6565 has a maximum start-up threshold of 14.5 V, therefore the maximum time-to-start is approximately:

Equation 35

$$\text{Time - to - start} = \frac{C_5 \bullet 14.5V}{\left(\frac{V_{inmin}}{(R_1 + R_2 + R_3 + R_4)}\right) - I_{SU}} \leq 2\,\text{sec} \Rightarrow (R_1 + R_2 + R_3 + R_4) \leq 808k\Omega$$

A good choice is to put in series four 200 kΩ resistances (R_1= R_2= R_3= R_4= 200 kΩ), which dissipate less than 1 W standby power.

The pre-charge of C_8 base capacitance is made connecting it to the OUT pin of L6565 through a diode in series to a 2.2 kΩ resistance.

6 Frequency response and loop compensation

The transfer function in the complex frequency domain of the discontinuous current mode (DCM) flyback converter with L6565 driver is given by:

Equation 36

$$G_1(s) = \frac{V_{out(s)}}{V_{comp(s)}} = \frac{n \bullet R_{out} \bullet (1 - D_{max})}{2 \bullet R_S \bullet (1 + D_{max})} \bullet \frac{(1 + s \bullet C_{out} \bullet ESR)\left(1 - s \bullet \frac{L_p D_{max}}{n^2 R_{out}(1 - D_{max})^2}\right)}{1 + s \bullet \frac{C_{out} R_{out}}{1 + D_{max}}}$$

The parameters and values are listed in *Table 3*.

Table 3. Transfer functions main parameters

Parameter	Description	Value
n	Primary/secondary turn-ratio	10
R_S	Sensing resistor	0.8 Ω
D_{max}	Maximum duty-cycle	0.5

Table 3. Transfer functions main parameters (continued)

Parameter	Description	Value
ESR	Electrolytic series resistance	16 mΩ
$R_{out}=V_{out}/I_{out}$	Output load	7.2 Ω
C_{out}	Output capacitance	2 mF
L_p	Primary inductance	1.56 mH

It is worth noting that the transfer function has one pole and one zero on the left half plane and one more zero on the right half plane. The RHP zero is very difficult, if not impossible, to compensate and therefore must be kept well beyond the closed-loop bandwidth. As a result, the transient response of such system will not be extremely fast.

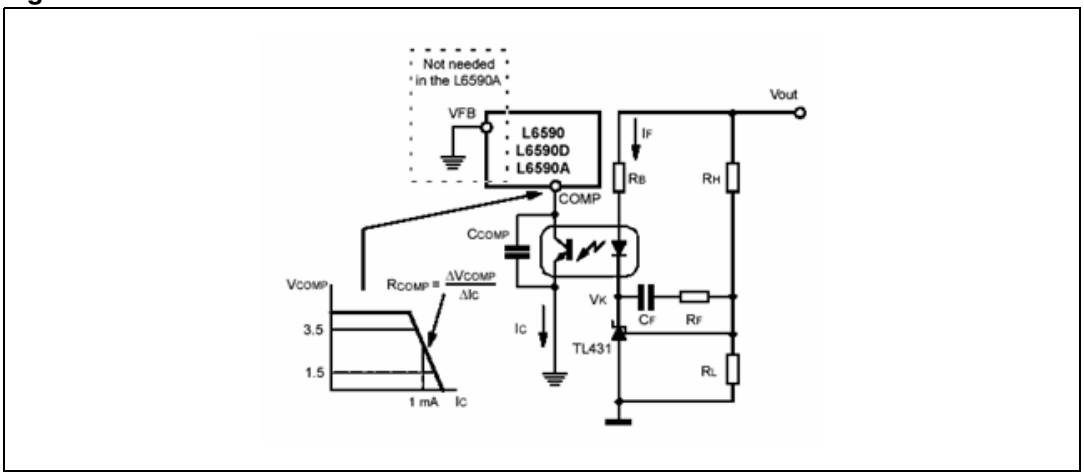
Poles and zeros are given in *Equation 37* and *Equation 38*:

Equation 37

$$f_p = 25Hz; f_{Z1} = 3.5 \bullet 10^5 Hz; f_{Z2} = 5 \bullet 10^3 Hz$$

A good line and load regulation implies a high DC gain, thus the open loop gain should have a pole at the origin. Normally in this case we need a feedback network like the one in *Figure 8*.

Figure 8. Converter feedback network



Its transfer function, which comprises a pole at the origin and a zero-pole pair, is given by:

Equation 38

$$G_2(s) = \frac{v_{comp}(s)}{V_{out}(s)} = \frac{CTR_{max} \bullet R_{COMP}}{R_B R_H C_F} \bullet \frac{1}{s} \bullet \frac{1 + s(R_H + R_F)C_F}{1 + sR_{COMP}C_{comp}}$$

The task of the control loop design is then to determine the transfer function $G_2(s)$ in order to ensure that the resulting closed-loop system is stable and performs well in terms of dynamic response, and line and load regulation. It is well known that the characteristics of the closed-loop system can be inferred from its open loop transfer function properties, that is $G(s) = G_1(s) \cdot G_2(s)$.

Frequency response requirements are summarized below:

1. Optimum dynamic performance requires a large gain bandwidth, that is the open-loop cross-over frequency f_c to be typically chosen equal to $f_{sw}/5$ (f_c = 10 khz).
2. Phase margin φ_m comprised between 45° and 90° is used as a design guideline. This ensures fast transient response with very little ringing. Sometimes this is not enough and so phase shift should be lower than 180° at any frequency below f_c, because a phase shift over 180° would result in a conditionally stable system.
3. Good load and line regulation implies a high DC gain (this requirement is ensured by the feedback network, whose transfer function has a pole at the origin).

First choose a typical value for $R_L = R_{22} = 2.7\ k\Omega$

From the L6565 datasheet we know that $I_{comp} = 5$ mA (source current) and $R_{comp} = 15\ k\Omega$ and can obtain:

Equation 39

$$R_B = R_{24} < \frac{V_{out} - (V_{ref} - V_{diode})}{I_{comp}} = \frac{24V - 3.5V}{5mA} = 4.1k\Omega$$

$R_{24} = 1.5\ k\Omega$ is a good choice. It is good practice to put a 3.3 kΩ resistor ($R_{23} = 3.3\ k\Omega$) in parallel to the photodiode .

The resistive partition has to be set with high precision according to the subsequent formula:

Equation 40

$$R_{high} = R_{22} \bullet \frac{V_{out} - V_{ref}}{V_{ref}} = 23.2k\Omega$$

There is no next closed commercial value so it is a good idea to put two 47 kΩ resistances ($R_{19} = R_{20} = 47\ k\Omega$) in series.

Now C_{11} (C_{comp}), C_{13} (C_F) and R_{21} (R_F) must be set in order to satisfy frequency response requirements.

A good choice is to set the pole of $G_2(s)$ in order to cancel the low frequency zero of $G_1(s)$:

Equation 41

$$\frac{1}{2\pi \bullet R_{comp} \bullet C_{comp}} = 5kHz \Rightarrow C_{11} = C_{comp} \cong 2.12nF$$

The next close commercial value for $C_{11} = 2.2$nF has been chosen.

Similarly C_{13} and R_{21} have been determined by setting the corresponding zero close to the pole of $G_1(s)$ and imposing the open-loop gain to cross the 0 dB axis only once at $f = f_c = 10$ kHz:

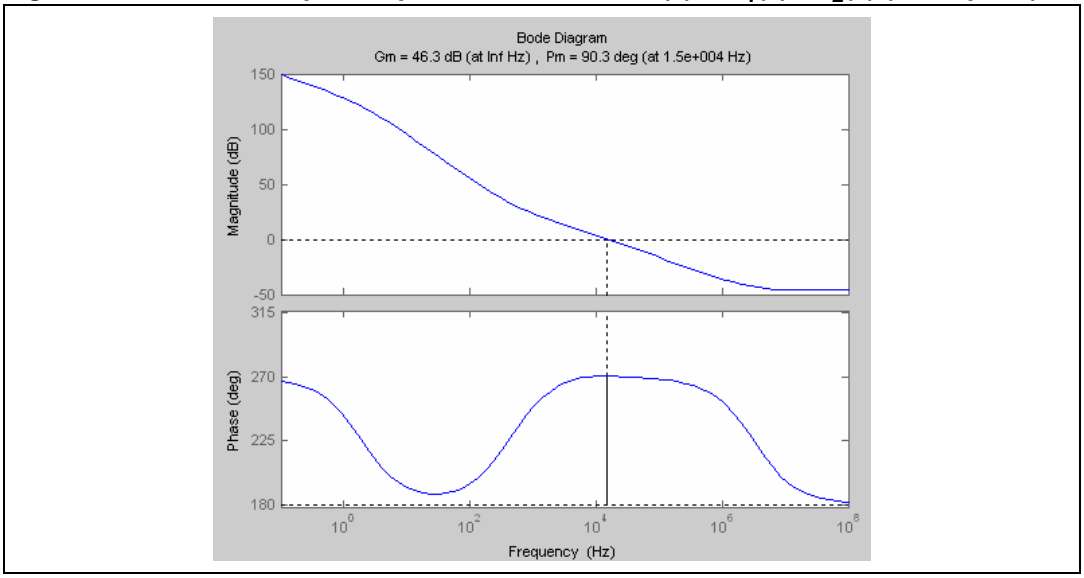
Equation 42

$$\begin{cases} \frac{1}{2\pi \bullet (R_H + R_F) \bullet C_F} = 400Hz \Rightarrow C_{13} = 10nF \\ |G(j\omega)|_{\omega = 2\pi \bullet 10^{-4} rad/sec} = 1 \Rightarrow R_{21} \cong 15k \end{cases}$$

In such a way we ideally get a phase margin of 90 degrees and an adequate closed-loop bandwidth.

Figure 9 shows Bode plots of the stabilized open loop transfer function.

Figure 9. Stabilized open loop transfer function G(s) = $G_1(s) \cdot G_2(s)$ (Bode plots)

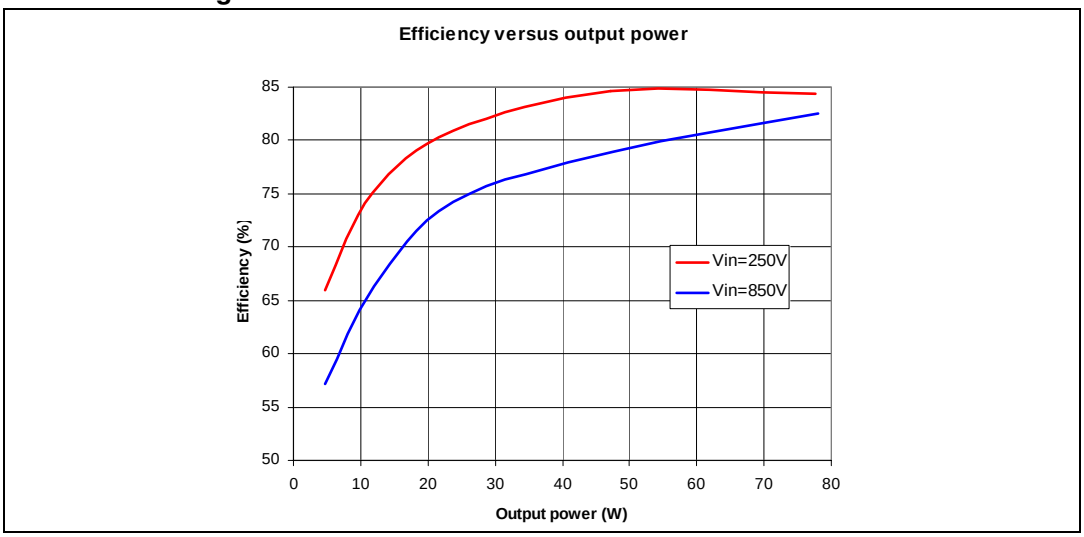


As expected, all requirements have been satisfied by properly choosing the feedback network. Gain bandwidth is quite large, phase margin is around 90°, and system stability margin is improved.

7 Efficiency, waveforms and experimental results

Overall efficiency variation versus output power is illustrated in *Figure 10* for two different values of input voltage.

Figure 10. Overall efficiency versus output power for two different values of input voltage



It is worth noting that with low input voltage (red curve), total efficiency is over 80% at medium and high load working conditions, reaching almost 85%. Efficiency decreases with

input voltage, however it is above 75% at loads higher than 30% even with maximum input voltage.

Theoretical assumptions made so far have been validated with the use of a demo board. A complete description of this board has been carried out and the most meaningful waveforms at any working condition are shown in *Figure 11* through *Figure 16*.

Figure 11, *Figure 12* and *Figure 13* show the prototype steady state behavior, by indicating the gate voltage (blue waveform), the base current (violet waveform) and the collector voltage (sky blue waveform) at maximum load for different input voltages.

Figure 11. Minimum input voltage-maximum load (250 V-80 W) in steady state

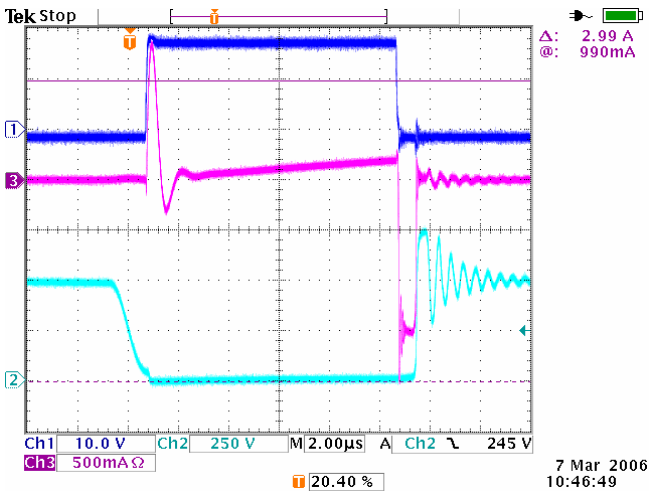


Figure 12. Medium input voltage-maximum load (500 V-80 W) in steady state

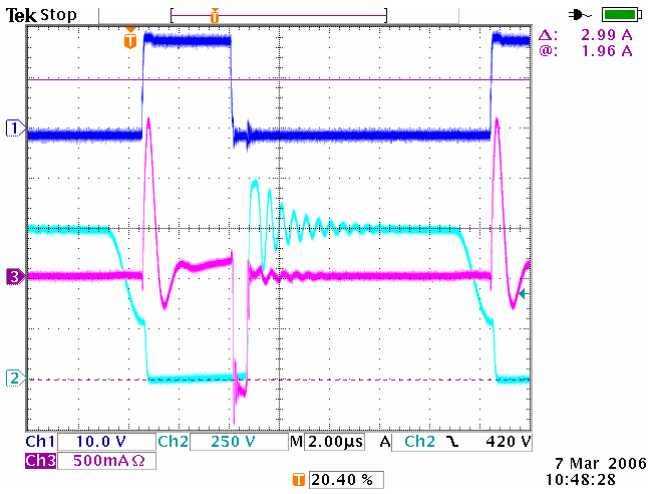
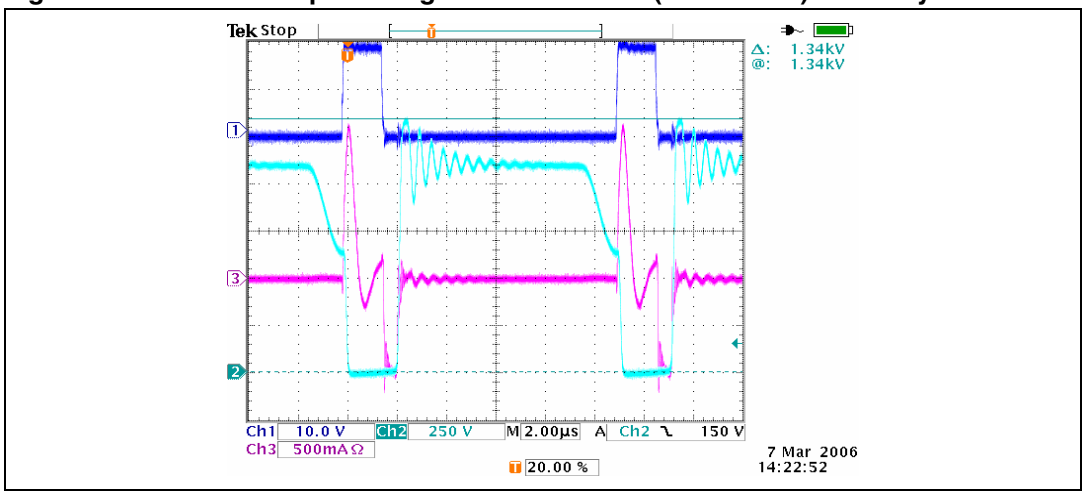


Figure 13. Maximum input voltage-maximum load (850 V-80 W) in steady state



Waveforms in *Figure 14*, *Figure 15*, and *Figure 16* describe the function of the converter at both low and high load conditions with the same input rectified voltage.

Figure 14. Very low load condition (750 V-5 W)

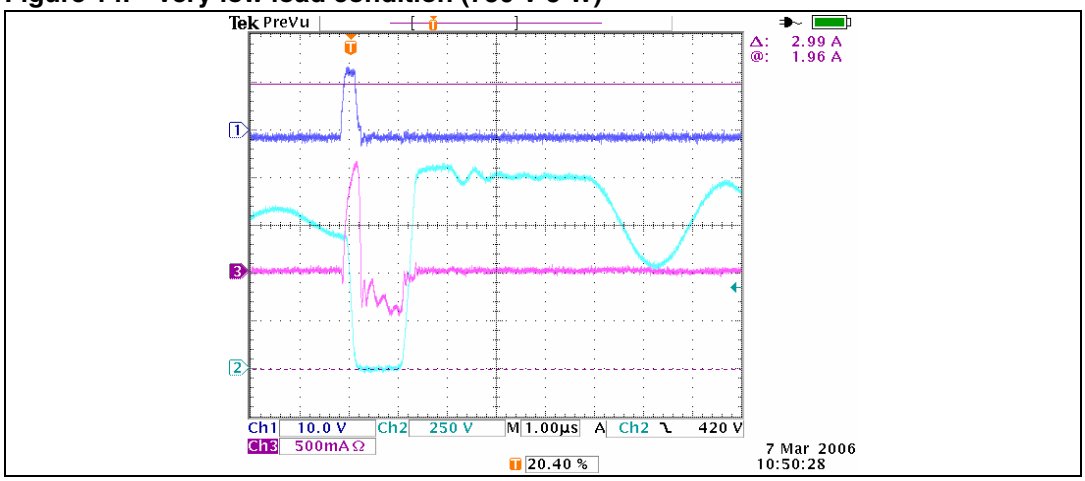


Figure 15. Low load condition (750 V-24 W)

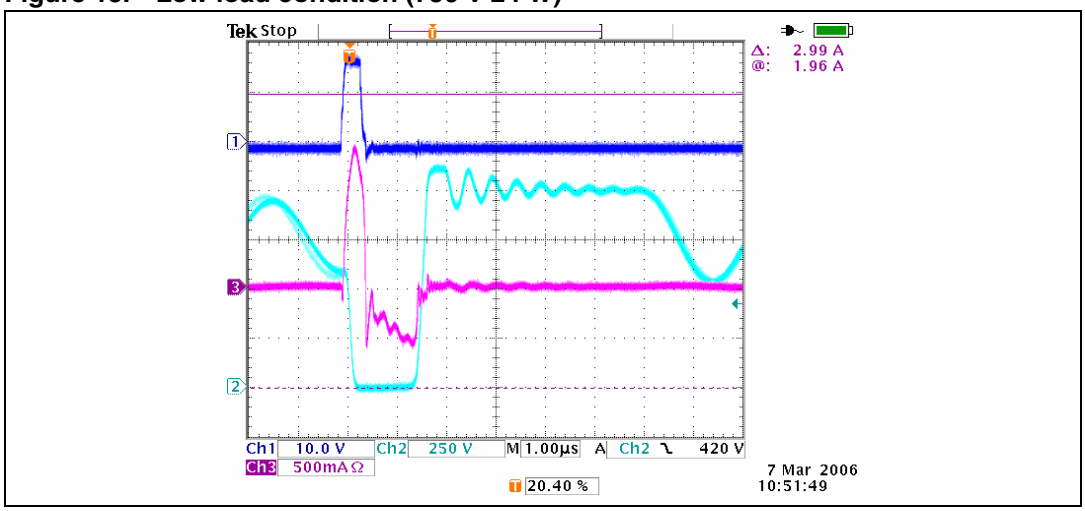
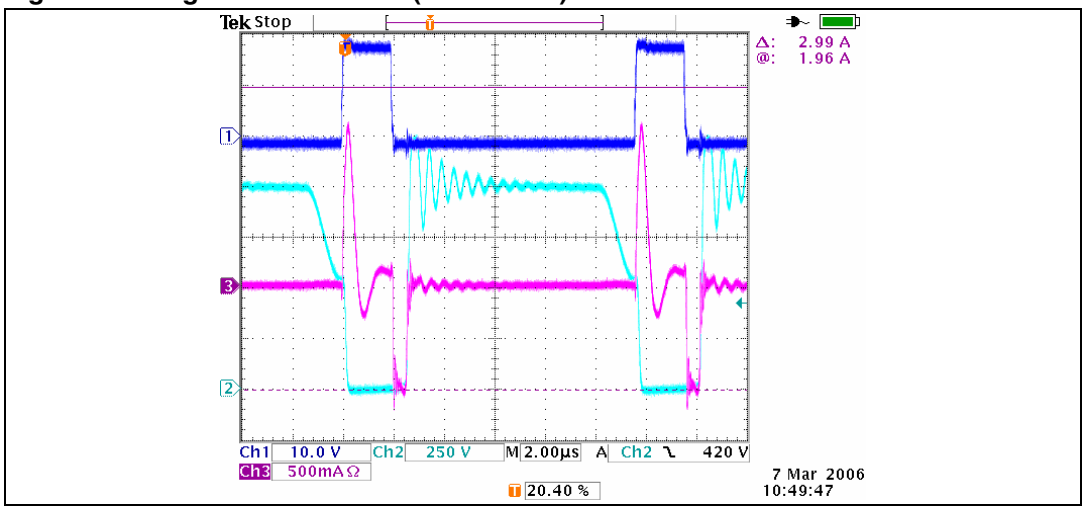
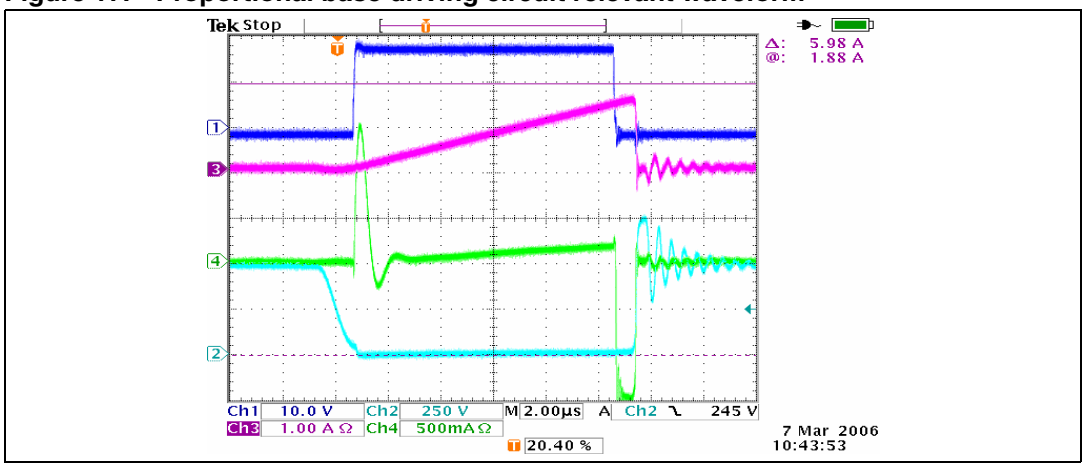


Figure 16. High load condition (750 V-80 W)



The waveform in *Figure 17* illustrates the function of the proportional base driving network. In this graph, collector current is in violet while base current is in sky blue.

Figure 17. Proportional base driving circuit relevant waveform



8 PCB layout and list of material

The printed circuit board is shown in *Figure 18* and *Figure 19*.

Figure 18. PCB layout (top view)

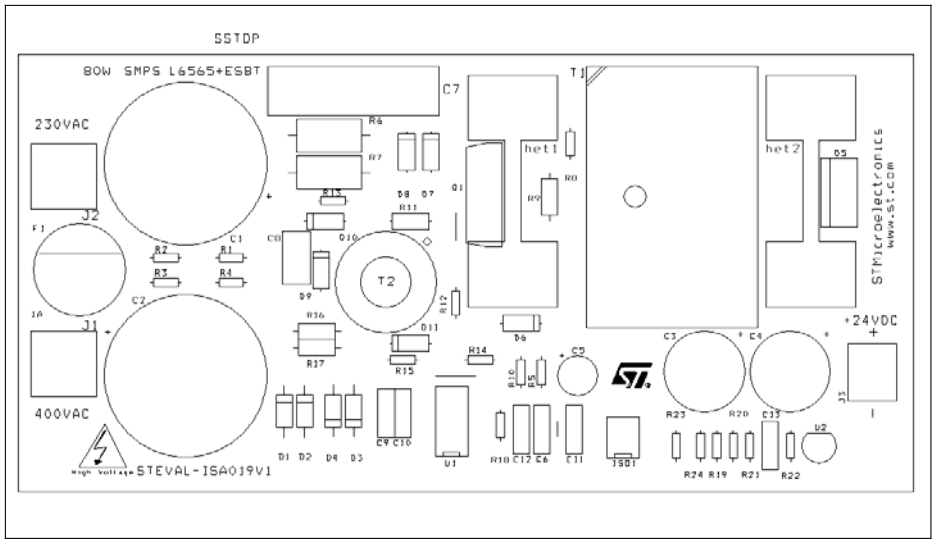
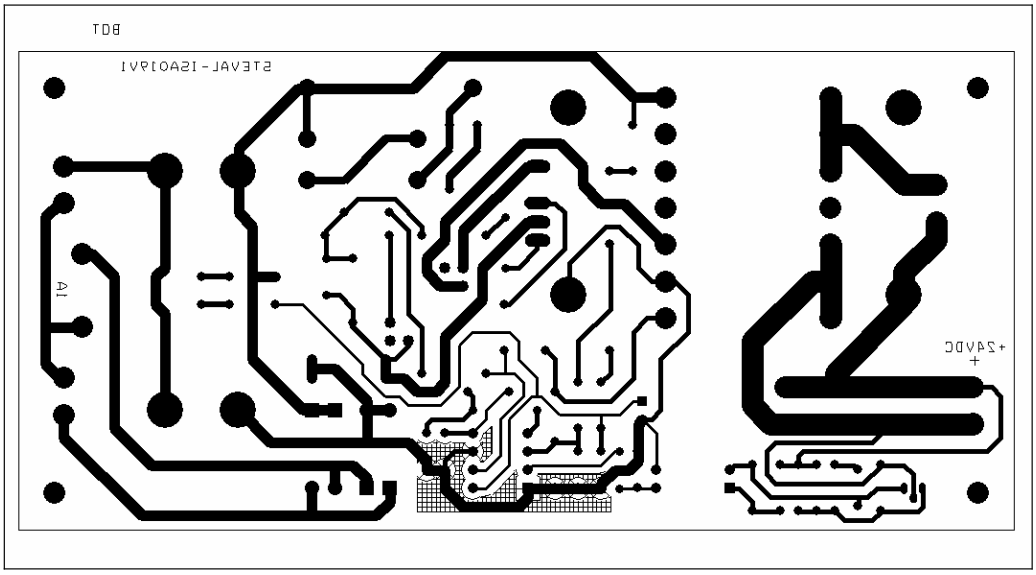


Figure 19. PCB layout (bottom view)



9 Bill of material

The bill of material is listed in *Table 4*.

Table 4. Bill of material

Part	Description
C1,C2	220 µF/450 V
C3,C4	1000 µF/35 V
C5	33 µF/50 V
C6	100 nF
C7	6n8
C8	220 n
C9	470 pF
C10	10 pF
C11	2n2
C12	1 nF
C13	10 n
D1,D2,D3,D4	1N4007
D5	STPS20120D
D6	1N4007
D7,D8,D10	STTH108
D9	3VZener
D11	1N4148
R1, R2, R3, R4	200 k/0.25 W
R5	10 R/0.25 W
R6, R7	39 k/2 W
R8, R9, R10	1M1/0.25 W
R11	0.56 R/1 W
R12	10 R/0.25 W
R13	2k2/0.25 W
R14	56k/0.25W
R15	1k/0.25 W
R16, R17	1 R6/1W
R18	10 k/0.25W
R19, R20	47 k/0.25 W
R21	15 k/0.25 W
R22	2k7/0.25 W

Table 4. Bill of material (continued)

Part	Description
R23	3k3/0.25 W
R24	1k5/0.25 W
Q1	STC04IE170HV
J1, J2	ARK700I/2
J3	ARK500/2
U1	L6565
U2	TL431
ISO1	PC817
F1	FUSE 2 A / 250 V
FUSE HOLDER	HA122100, RM = 10 mm
T1	TRONIC 0600387
T2	VOGT SL0512202101
het1, het2	V7477X

10 References

- STMicroelectronics application note AN1889 "ESBT STC03DE120 IN 3-PHASE AUXILIARY POWER SUPPLY"
- STMicroelectronics application note AN1262 "OFFLINE FLYBACK CONVERTERS DESIGN METHODOLOGY WITH THE L6590 FAMILY"
- STMicroelectronics application note AN2131 "HIGH POWER 3-PHASE AUXILIARY POWER SUPPLY DESIGN BASED ON L5991 AND ESBT STC08DE150"
- STMicroelectronics L6565 datasheet “QUASI-RESONANT SMPS CONTROLLER”
- STMicroelectronics STC04IE170HV datasheet “Emitter switched bipolar transistor ESBT® 1700 V - 4A - 0.17 Ω“
- Abraham I.Pressman, "Switching Power Supply Design", McGraw-Hill, Inc.

11 Revision history

Table 5. Revision history

Date	Revision	Changes
28-Mar-2007	1	First issue
10-Apr-2007	2	*Equation 5* and *Equation 15* modified
20-Jun-2007	3	ESBT part number has been updated