LME49830TB Ultra-High Fidelity High Power Amplifier Reference Design

National Semiconductor
Application Note 1850
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Introduction

The LME49830 EF125WT1 amplifier PCB module showcases National Semiconductor's LME ultra-high fidelity power amplifier input stage ICs (drivers). The LME49830 is a fully complementary bipolar 200V input stage IC with 56mA (typical) of output current that has been optimized for audio applications. With 56mA of current drive, the IC can drive numerous power transistors to achieve high levels of output power.

The LME49830's ultra-low distortion and low-noise, combined with a user adjustable compensation scheme results in a tightly controlled, but highly dynamic listening experience. User adjustable compensation provides for high-frequency distortion minimization and for slew rate and power bandwidth optimization. The IC's high performance level, features and user customization make the driver a highly reliable, unique input stage solution for high power amplifiers.

While the amplifier module provides a convenient way for performance measurement verification, it also can be used to validate the solution's sonic performance in the desired test environment. The solution presented has undergone listening evaluations in a dedicated sound room for verification of sonic performance.

Overview

The LME49830 IC in combination with a properly designed high-current output stage, with adequate thermal management, can provide output power levels in excess of 1kW. *Figure 1* represents a simple schematic of a typical power amplifier utilizing the LME49830. The LME49830 simplifies power amplifier design by providing a highly reliable, consistent performing low distortion input stage. With the addition of an output stage and a simple DC biasing circuit, the end result is a very high fidelity power amplifier. The LME49830 was designed for output stages using MOSFET devices but may be used with other output device types as well. The LME49830 can be used with just about any MOSFET desired as a result of the 16V DC bias range for the output stage.

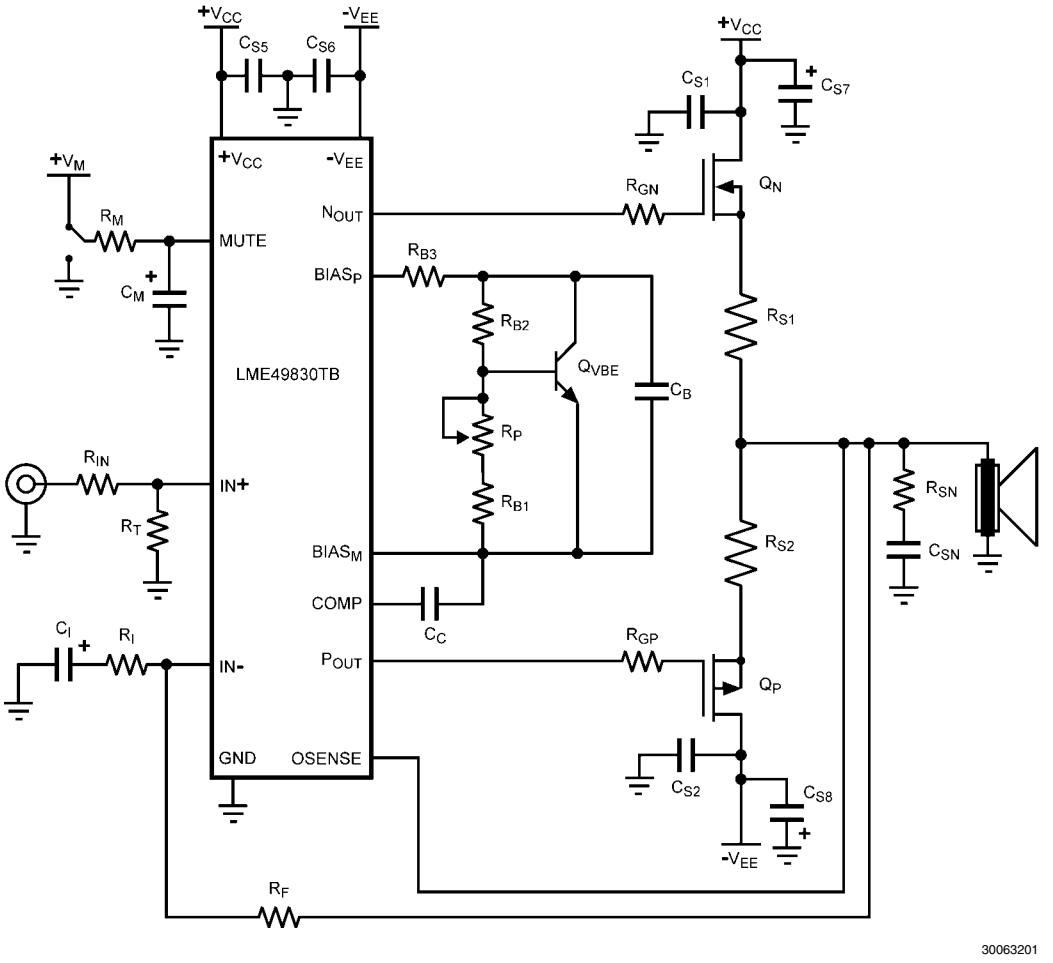


FIGURE 1. Simple Power Amplifier Schematic

With a 200V operating voltage range, an amplifier solution using the LME49830 is mainly limited by the number of output power stage transistors in conjunction with adequate thermal management to keep the power transistors operating within their safe operating area (SOA).

The LME49830 can be configured with a number of different output stage topologies, providing for end-product differentiation and customization. Shown in *Figure 2* is the common source-follower output stage with three transistors paralleled per side.

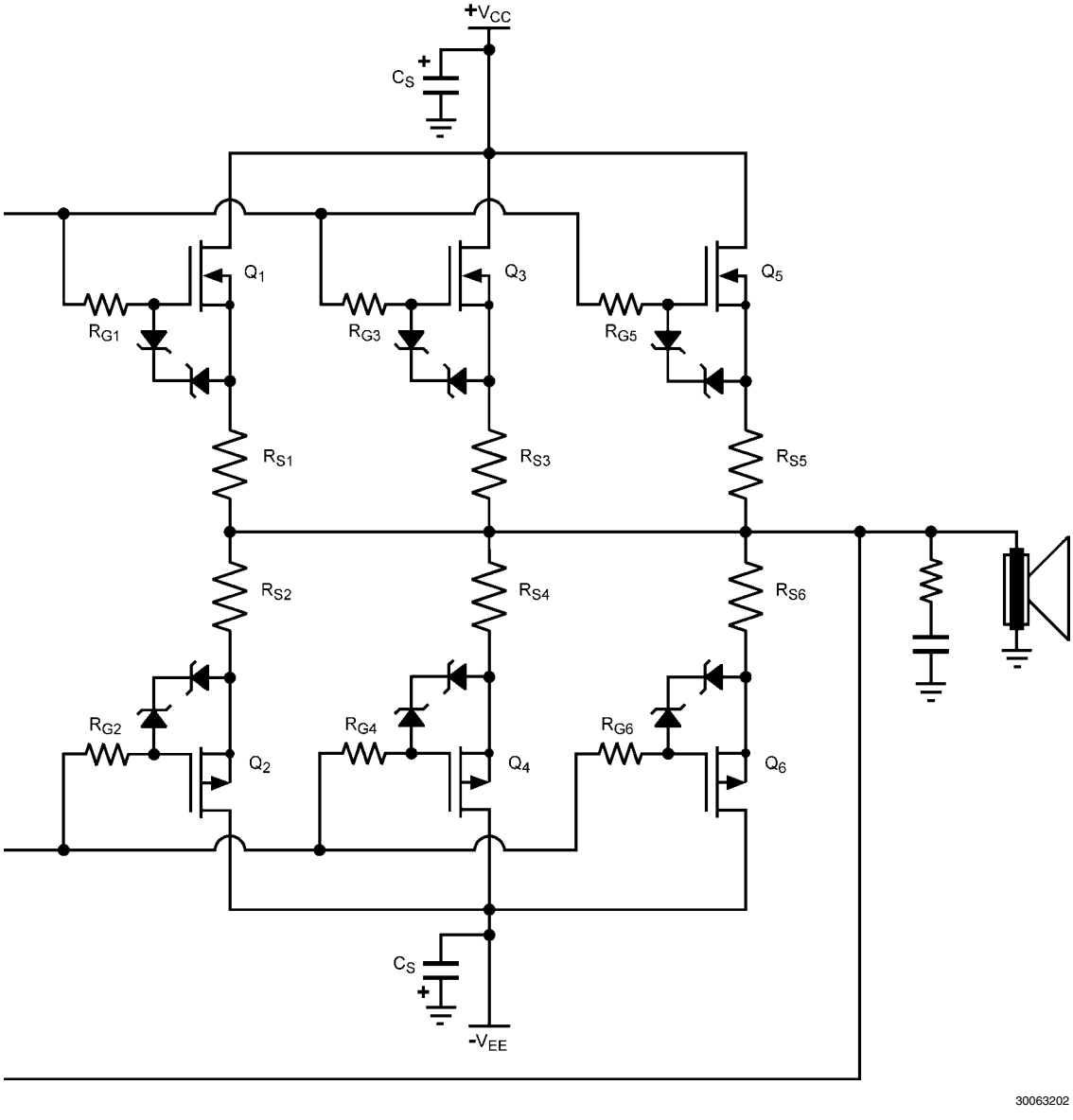


FIGURE 2. Source-Follower Output Stage

Operational Details

The complete amplifier schematic for the EF125WT1 FET PCB is shown in *Figure 3*. Important aspects and explanation of various sections of the circuit will be covered below. The amplifier module is a two device per side MOSFET output stage driven directly from the LME49830. With only two devices per side in the output stage there is no need for an additional current gain stage for higher output stage drive current. The LME49830's drive current of 56mA (typical) provides plenty of drive current for high slew rate and excellent THD. For higher device count output stages, the LME49830's drive current may not be sufficient to meet design target specifications.

The LME49830 amplifier module when running on ±60V power supplies is capable providing the output power levels shown below with a 1kHz signal.

Load	0.1% THD+N	1% THD+N	10% THD+N
4Ω	335W	350W	430W
8Ω	175W	185W	230W

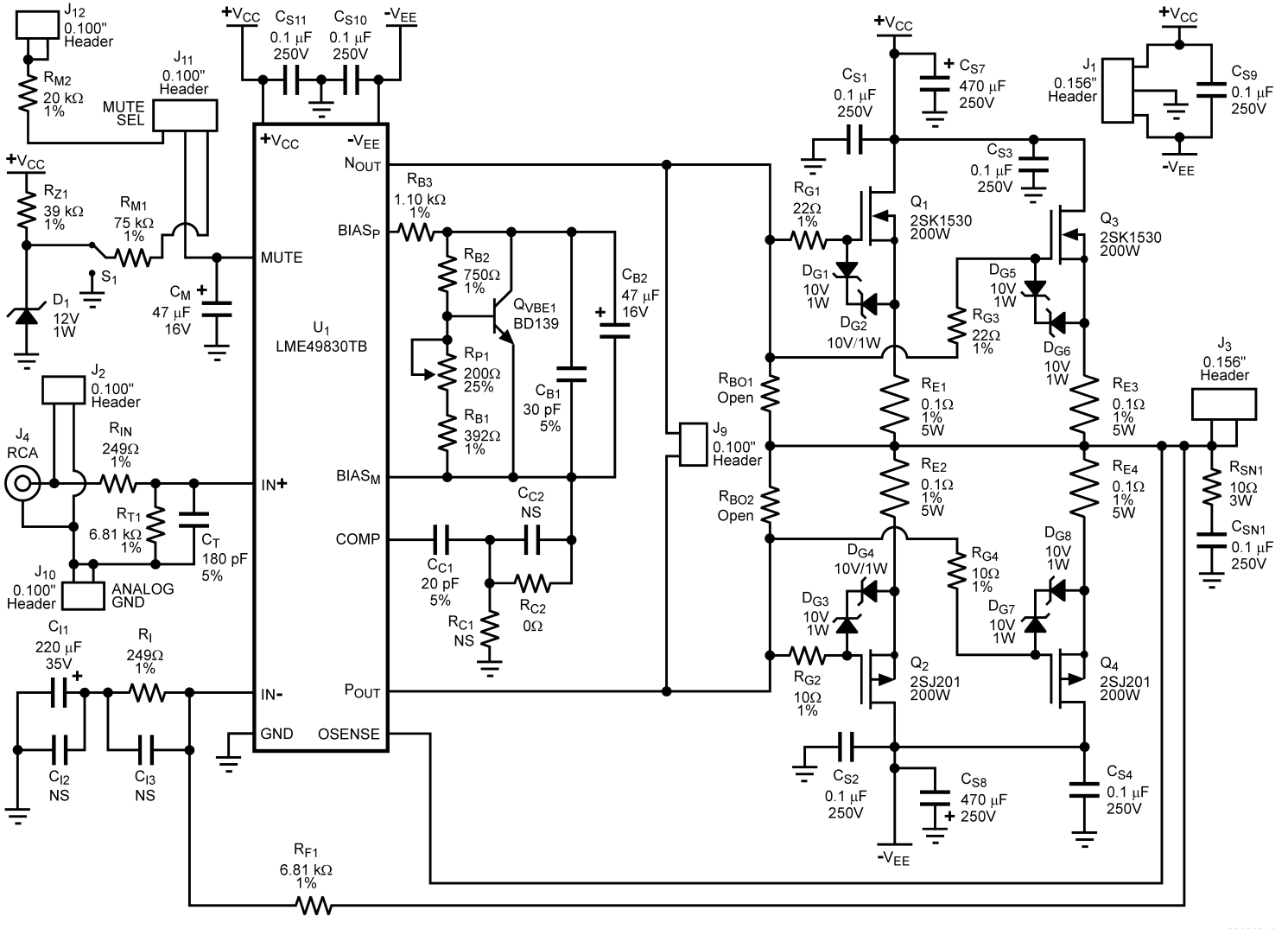


FIGURE 3. LME49830 EF125WT1 FET PCB Amplifier Schematic

It is important to note that the LME49830 EF125WT1 FET PCB amplifier module contains no output stage protection mechanisms. A proper current limit set on the evaluation power supply is the minimum precaution for safety.

The power supply voltage limitation for the EF125WT1 FET module is based on the Toshiba 2SK1530/2SJ201 MOSFET devices, which have a V_{DSS} of 200V as well as the LME49830 which has an absolute maximum supply voltage rating of ±100V (200V). Based on this, it is recommended that the maximum power supply voltage applied to the amplifier module be less than ±80V. To allow for additional safety margin it is recommended that the maximum power supply voltage is ±75V.

While power supply voltages up to ±75V can be applied to the amplifier module, it is recommended that caution be applied when driving a load with an impedance less than 8Ω with continuous sinusoidal signals. Only two output power transistors per side with limited power dissipation capabilities on the provided heat sink does not allow for continuous total output stage power dissipation levels above 140W with only convection cooling. The amplifier module's limiting factor is the output stage power transistor safe operating area (SOA) along with the power dissipation capabilities of the provided heat sink. Continuous operation at both high supply voltages and into loads less than 8Ω, with sinusoidal signals will require additional thermal capacity. Utilizing a high air velocity fan will aid in power dissipation, although this method will still not guarantee SOA violations under high supply voltage and continuous signal driving situations.

It is recommended that the PCB amplifier module be operated with ±60V, driving an 8Ω resistive load with sinusoidal signals for standard performance characterization. When operating above ±60V supply rails or into low impedance loads, care must be taken to keep from exceeding the output power transistor SOA. It is highly recommended to minimize the time that continuous signals are applied to the amplifier under extreme operating conditions. Standard audio performance measurements can be obtained at higher supply voltages with time for the heat sink and devices to cool in between measurements.

The LME49830 EF125WT1 FET PCB amplifier module is intended to be used for performance verification and critical listening evaluations. The PCB module indicates the high level of performance that can be achieved from minimal external components, while still providing significant user design flexibility for end-product differentiation. The PCB module is not intended to be used for long-term temperature and reliability testing or significant high-power analysis due to limited thermal capabilities.

For continual high-power driving analysis, long-term temperature and reliability testing, it is recommended that the amplifier be designed with adequate thermal management for the operating conditions.

OUTPUT STAGE POWER DISSIPATION

The output stage's worst-case maximum power dissipation for purely resistive loads can be determined by the following equation.

$$P_{D(AMP)MAX} = V_{CC}^2/(2\pi^2 R_L) \quad \text{(Watts)}$$

Where V_{CC} is the total supply voltage. For ±75V calculations V_{CC} used in the equation would be 150V.

Table 1 represents the output stage's maximum power dissipation for stated power supply voltages and purely resistive loads.

TABLE 1. Output Stage Maximum Power Dissipation

Output Stage Maximum Power Dissipation		
Load	V_{CC} = ±60V	V_{CC} = ±75V
R_L = 8Ω	91W	142W
R_L = 4Ω	182W	285W

With two power transistors per side on the LME49830 EF125WT1 FET PCB amplifier module, each transistor will dissipate an average of 1/4th of the total output stage power dissipation. It is easy to see that each power transistor would need to dissipate an average of 71W when driving a sinewave continuously into a 4Ω resistive load with a ±75V power supply. Each output device is rated for 150W of power dissipation at a case temperature of 25°C. The power dissipation of each device must be de-rated linearly based on case temperature. At a case temperature of 75°C the power dissipation rating for each device is down to 90W, based on the device datasheets. Instantaneous power dissipation when driving reactive loads will be even greater and may exceed the transistor's safe operating area (SOA).

The heat sink used for the amplifier module is a 4 inch extrusion from Aavid Thermalloy, part number 65605 with a rating of 0.62°C/W. Adding a fan on the heat sink can greatly reduce the thermal resistance depending on the air flow rate of the fan. More information and thermal modeling for the amplifier heat sink can be found on Aavid Thermalloy's website.

Determining the maximum power dissipation while de-rating the output devices base on case temperature with the provided heat sink can be determined by mathematical derivation. The power dissipation of the output devices are de-rated linearly with case temperature. The general formula for a line is y = mx + b. For both output devices, 2SJ201 and 2SK1530, the thermal properties are the same. The power dissipation de-rating graph end points are set by the power dissipation rating at a case temperature (T_C) of 25°C and the maximum channel temperature, which is at 0W power dissipation. These specifications are 150W and 150°C respectively. Two points on the line are know allowing for the solution to the general formula resulting in Equation 1.

$$P_{D(IC)} = -1.2\text{W/°C} * T_C + 180\text{W} \quad \text{(W)} \qquad (1)$$

To determine the case temperature from the device power dissipation the equation is given in Equation 2.

$$T_C = -0.83\text{°C/W} * P_{D(IC)} + 150\text{°C} \quad \text{(°C)} \qquad (2)$$

Inspection of the formula above reveals that the junction-to-case thermal resistance, θ_{JC}, of the device is the absolute value of the slope of the curve in °C/W which is 0.83°C/W.

To determine the maximum device power dissipation while de-rating for increase device case temperature with a given heat sink and ambient temperature a second equation for case temperature can be determined resulting in:

Device Case Temperature (°C) = Heat Sink Temp (°C) + [Device Power Dissipation (W) * Case Thermal Resistance (°C/W)]

$$T_C\ (\text{°C}) = T_{HS}\ (\text{°C}) + [P_{D(IC)}\ (\text{W}) * \theta_{CS}\ (\text{°C/W})]$$

The heat sink temperature is the total power dissipation multiplied by it's thermal resistance plus the ambient temperature:

$$T_{HS}\ (\text{°C}) = [P_{D(TOTAL)}\ (\text{W}) * \theta_{SA}\ (\text{°C/W})] + T_A \quad \text{(°C)}$$

For any number of output devices, $P_{D(TOTAL)}$ = Number of Output Devices * $P_{D(IC)}$ (W). Combining the above gives Equation 3.

$$T_C = (P_{D(TOTAL)} * \theta_{SA}) + T_A + (P_{D(IC)} * \theta_{CS}) \quad \text{(°C)} \qquad (3)$$

Setting Equation 2 equal to equation 3 gives:

$$-0.83°C/W * P_{D(IC)} + 150°C = (P_{D(TOTAL)} * \theta_{SA}) + T_A + (P_{D(IC)} * \theta_{CS})$$

Solving for $P_{D(IC)}$ with four output devices results in Equation 4.

$$P_{D(IC)} = (150°C - T_A) / (4 * \theta_{SA} + \theta_{CS} + \theta_{JC}) \quad (W) \qquad (4)$$

Given:

T_A = 25°C

θ_{CS} = 0.25°C/W, flat, thermal greased surface.

θ_{SA} = 0.62°C/W, rating of provided heat sink.

θ_{JC} = 0.83°C/W = ($T_{J(MAX)}$ - T_A) / ($P_{D(MAX)}$ at T_A).

Results in $P_{D(IC)}$ = 35.1W maximum average power dissipation per device de-rating for case temperature rise with the provided heat sink at an ambient temperature of 25°C. The total average output stage power dissipation is 140.4W. Under these conditions each device's channel temperature will be 150°C, each device case temperature will be 120.9°C, and the heat sink will be 112.1°C.

With some additional substitutions and inspection gives Equation 5 as the very general version of Equation 4.

$$P_{D(IC)} = (T_{J(MAX)} - T_A) / \{\#\text{ of Devices} * \theta_{SA} + \theta_{CS} + [(T_{J(MAX)} - T_A) / (P_{D(MAX)} \text{ at } T_A)]\} \quad (W) \qquad (5)$$

The above calculations are for continuous average power dissipation with sine waves. Music and other program material will have average power dissipation levels lower than a sine wave reducing the heat sink and device temperatures.

LME49830 POWER DISSIPATION

The LME49830 die is contained in a TO-247 package with a junction-to-ambient thermal resistance, θ_{JA}, of 73°C/W and a junction-to-case thermal resistance, θ_{JC}, of 4°C/W. The TO-247 package is an non-isolated package and any attached heat sink will be at the same potential as the negative supply rail.

The LME49830 integrates a complete power amplifier input stage and has an output current drive capability of 56mA. The LME49830 is intended to drive MOSFET transistors in the output stage providing a high-impedance load to the LME49830.

Shown in *Table 2* are maximum power dissipation levels and required minimum heat sink thermal resistances for the stated power supply voltages to keep the LME49830 die temperature below 150°C. The calculations use a 50°C ambient, a LME49830 θ_{JC} of 4°C/W, plus 0.5°C/W additional thermal resistance from case-to-sink (θ_{CS}).

TABLE 2. LME49830 Power Dissipation & Heat Sink Information

LME49830 Power Dissipation & Heat Sink Thermal Resistances		
LME49830	V_{CC} = ±60V	V_{CC} = ±75V
$I_{CCQ(max)}$ = 25mA	3W	3.75W
θ_{SA}	< 28.8°C/W	< 22°C/W

The heat sink used on the EF125WT1 FET amplifier module is from Aavid Thermalloy, part number 530101B00150, with a thermal resistance of 6.3°C/W. As shown in the equation below, even at ±100V rails, the heat sink is sufficient.

$$\theta_{SA} = [(T_{J(MAX)} - T_A) - P_{D(MAX)}(\theta_{JC} - \theta_{CS})] / P_{D(MAX)}$$
$$= [(150°C - 50°C) - 5W(4°C/W + 0.5°C/W)] / 5W$$
$$\leq 15.5°C/W$$

This heat sink used for the LME49830 was selected intentionally for ease of IC mounting, thermal robustness, and mechanical stability. It is recommended that a separate heat sink from the output stage heat sink be used for the LME49830 to maintain a low operating die temperature and minimize thermal interaction.

PCB Connections

INPUT CONNECTIONS

An analog input signal is applied to the LME49830 EF125WT1 FET PCB through either the two pin header, J_2 or through the standard RCA input connector, J_4. For optimum performance a shielded twisted pair cable should be used between the signal source and PCB amplifier module with the shield terminated only at the signal source.

The input is DC coupled, unbalanced and terminated in a 6.8kΩ resistor. The input termination, R_T, and the accompanying gain-setting feedback resistor, R_F, can be changed to a higher value such as 10kΩ or 47kΩ, resulting in a slightly higher THD+N specification due to added resistor thermal noise. R_{IN} and R_I should also be adjusted to maintain the same gain setting. An input high-frequency roll-off filter capacitor limiting high-frequency amplification, C_T, is in parallel with R_T. The combination of these two values set the pole location to 130kHz.

The input sensitivity for this amplifier is 1.37V, resulting in an output power of 175W at 0.1% THD+N into 8Ω running off of ±60V power supply rails.

OUTPUT CONNECTIONS

The output is connected through the two pin header, J_3. The intended impedance for this amplifier is 8Ω or 4Ω, running off of ±60V power supply rails. While the PCB amplifier module is capable of running off of supply rails up to ±100V, the main limitation is the safe operating area of the output stage power transistors. Please refer to the *Operational Details* section for limitations and recommendations.

An RC output snubber network has been provided on the PCB acting as a high-frequency load. A 0.1µF capacitor, C_{SN1} is in series with a 10Ω resistor, R_{SN1}, which has a 3 watt rating at the output. The RC snubber is not needed to provide any snubbing of high-frequency instabilities on the output waveform, generally created in the quasi-saturation region when close to clipping. However, output snubbers are commonly employed to provide a load impedance to the amplifier at high frequencies.

POWER SUPPLY CONNECTIONS

The power supply to the amplifier module is applied to connector J_1. This connector powers both the output stage power transistors and the LME49830. Operating voltages from ±20V to ±100V may be applied to the amplifier module. Please refer to the *Operational Details* section for limitations and precautions when operating at elevated supply voltages.

The power supply cabling to the amplifier PCB should have sufficient current handling capability for the desired amplifier output power. It is recommended that 18 gauge stranded wire

be used to connect the low-impedance power supply to the PCB, keeping connections as short as possible.

GND CONNECTION OPTIMIZATION

Shown in *Figure 4*, is a detailed diagram showing optimum ground connections with two options for the clean signal GND connection. It is important to note that a separate ground connection must be made from the signal generator GND to the power supply star GND, providing a reference between the input and output. Only one option in *Figure 4* should be used for the clean GND. This is because there is no electrical ground connection between the input stage and the output stage power supply bypass capacitors on the PCB amplifier module. This was done intentionally to eliminate any interaction of ground currents between the input and output stages.

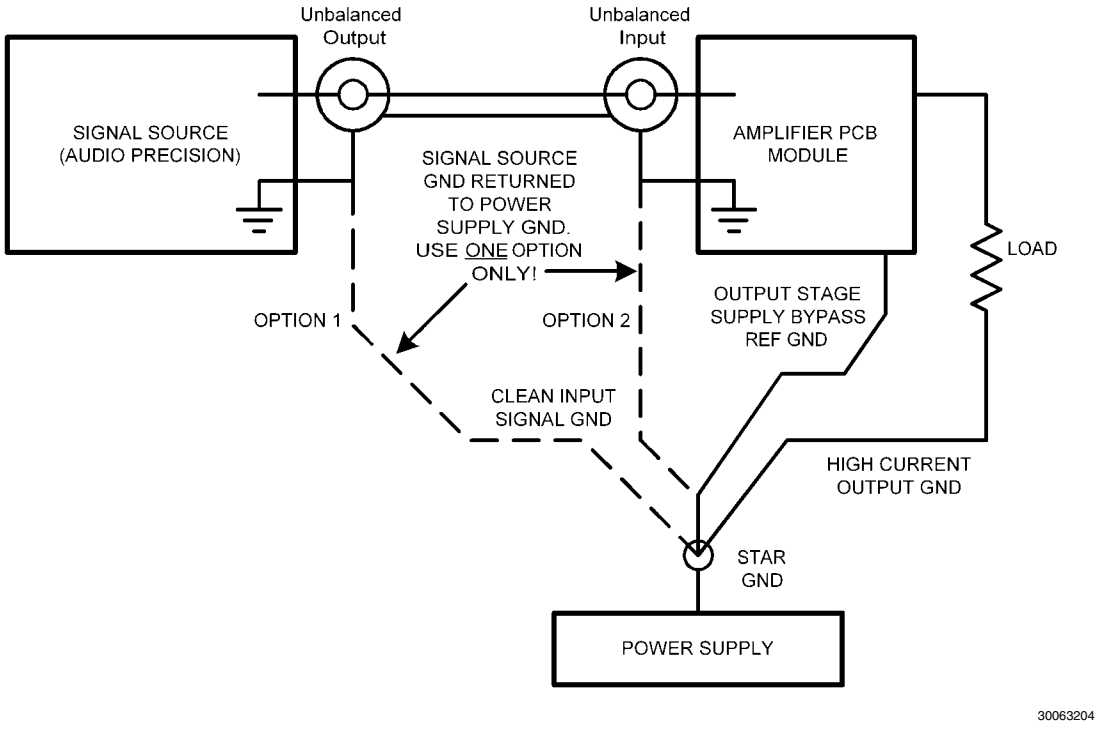


FIGURE 4. Amplifier Module Test Setup GND Connections

If the signal source is not grounded back to the power supply star point, the output will float up, drawing a large amount of current from the positive power supply. Therefore, it is important that the PCB's low-level clean signal ground is referenced back to the star ground from either a connection at the Audio Precision or from analog ground, J_{10} on the PCB, but only one connection typically gives the best THD+N performance.

Also note that there is no output load ground return connection on the PCB. This was also done intentionally to ensure that the high-current output ground return current is tied back at the star ground point.

In order to obtain the lowest level distortion measurements, it is important to make an oscilloscope chassis ground connection to the power supply star ground point while NOT using the scope probe ground clip. Connecting the scope probe ground clip to AGND, while probing the output stage, may significantly increase distortion.

Due to the physical size limitation of providing large valued reservoir capacitors on the PCB, it is expected that the user provide a low-inductance connection to either a low impedance power supply or bulk capacitance.

In order to minimize amplifier distortion in a lab environment, it is recommended to provide high-valued reservoir capacitors between the lab power supply and the PCB amplifier module. It is also recommended to keep connections between the reservoir capacitors and the amplifier module as short as possible. 39,000µF of reservoir capacitance per supply rail was used for bench testing to obtain the performance indicated in this document.

MUTE FUNCTION

A reference voltage is used for the mute circuit in the EF125WT1 FET amplifier module, as shown in *Figure 5*. This reference voltage allows varying power supply voltages to be applied to the LME49830 without continually adjusting the mute resistance. The mute current is set to 160µA using the on-board (+12V) mute voltage. J_{11} and J_{12} allow for an external mute voltage of 2.6V to 5V to be used or the user can adjust the value of the R_{M2} mute resistor for any desired voltage.

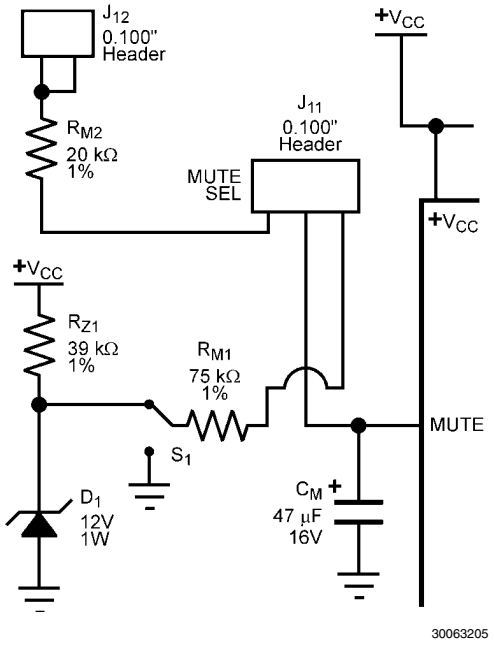


FIGURE 5. Mute Circuit Reference Voltage

Detailed design information for proper mute circuit operation and reference voltage set up can be found in the LME49830 datasheet. Also shown in the datasheet is the excellent level of mute attenuation of -120dB for audio signals. The LME49830 mute function has a smooth turn-on/off transition so that clicks and pops are minimized. Adding a capacitor to the MUTE pin can totally eliminate any clicks and pops that may occur with the trade-off being a delay when changing modes. A 47µF Mute capacitor is supplied on the EF125WT1 FET PCB for a virtually silent mode change with minimal delay.

GAIN AND FREQUENCY RESPONSE

The amplifier module is configured as non-inverting mode. The gain is set by:

$$A_V = 1 + R_{F1} / R_I \quad (V/V)$$

The gain is set to 28.3V/V (29dB) with R_{F1} set to 6.8kΩ and R_I set to 249Ω. The low frequency response is set by the combination of C_{I1} and R_I by the equation:

$$f = 1/(2\pi C_{I1} R_I) \quad (Hz)$$

The low frequency -3dB roll-off point is 2.9Hz. Additionally, there are component footprints for additional capacitors in parallel with C_{I1} (C_{I2}) and R_I (C_{I3}) as shown in *Figure 6*.

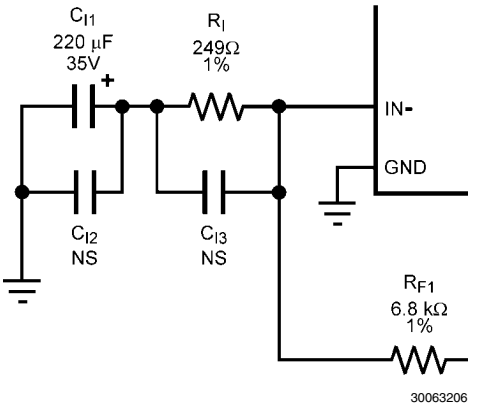


FIGURE 6. Gain And Low Frequency Response

Experimentation with high quality film capacitors in these locations may result in additional sonic improvements. Such investigation is not covered in this document.

Output Stage Biasing

The LME49830 is a robust, consistently high-performing amplifier input stage that eliminates numerous discrete input stage design issues. Intricate inter-stage design dependencies that commonly affect optimum distortion performance are no longer a problem for discrete designers, ensuring that new amplifier designs get to market faster and more reliably.

One of the key benefits of designing with the LME49830 is the ability to select a preferred output stage topology and power devices. This simple, yet flexible input stage solution makes it easy to combine a preferred output topology and achieve ultra high-fidelity performance with an integrated form-factor. System designers can continue to differentiate their power amplifier solutions from their competitors, by utilizing their time-developed output stage intellectual property. The LME49830 also provides an integration factor that increases the number of channels per chassis area, while maintaining an ultra high-fidelity level never before obtained from an integrated circuit.

With the benefits and flexibility that this solution provides, there is a little complexity and some variability in setting the output stage's DC bias voltage. The DC bias voltage, or mode of operation - Class A, B, or A/B, is set by the designer and is partially dependent upon the topology and the output power device selected. Different MOSFET devices have significantly varying threshold voltages. There are other topology configurations but other topologies are beyond the scope of this document.

Besides the DC voltage bias setting, there is a bias circuit difference depending upon whether BJTs or MOSFETs are used as the power delivery device. BJTs are subject to thermal runaway and therefore require a thermally compensated bias circuit. If MOSFETs are selected as the power device, there may not be a need for a thermally compensated bias circuit depending on the specific MOSFET devices.

Shown below in *Table 3* is a list of recommended MOSFETs that have been evaluated with the LME49830. This list of parts was not meant to be an exhaustive list, but rather some of the more common power devices that are currently used in audio power amplifiers. For more information regarding MOSFET driving issues and recommendations, please refer to AN-1645, "LM4702 Driving a MOSFET Output Stage".

TABLE 3. Recommended MOSFET Power Devices

Manufacturer	NFET	PFET
Toshiba	2SK1530	2SJ201
International Rectifier	IRFP240	IRFP9240
Renesas(1)	2SK1058	2SJ162

(1) Renesas devices have a different pin out compared to the Toshiba and IR devices (Source and Drain pins reversed) requiring a different PCB.

The LME49830 has a maximum DC bias voltage of 16V for use with just about any MOSFET device. The high output drive current from the LME49830 makes it ideal for very high power amplifier applications.

V_{BE} MULTIPLIER

The LME49830's $BIAS_P$ and $BIAS_M$ pins are available to create the DC bias of the output stage. Depending on the device characteristics and design goals, a thermally compensated circuit may be needed in order to have stable bias at the desired current across temperature. A non-compensated bias circuit would consist of a resistor or potentiometer and one or two capacitors between the BIAS pins of the LME49830. The EF125WT1 FET PCB uses a thermally compensated V_{BE} multiplier for the bias circuit with the Toshiba 2SK1530/2SJ201 devices in the output stage.

The V_{BE} multiplier's transistor, which needs to be mounted directly next to one of the power transistors on the heat sink, will sense the output device's temperature with some temperature gradient through the common heat sink. With a correctly designed V_{BE} multiplier circuit the bias current of the output stage will remain relatively stable over the device temperature operating range.

The V_{BE} multiplier circuit created by Q_{VBE1} with associated resistors and capacitors is shown in *Figure 7*. The output stage bias can initially be adjusted through potentiometer, R_{P1} in order to optimize for lowest crossover distortion, desired sound quality or mode of operation – Class A, B, or AB.

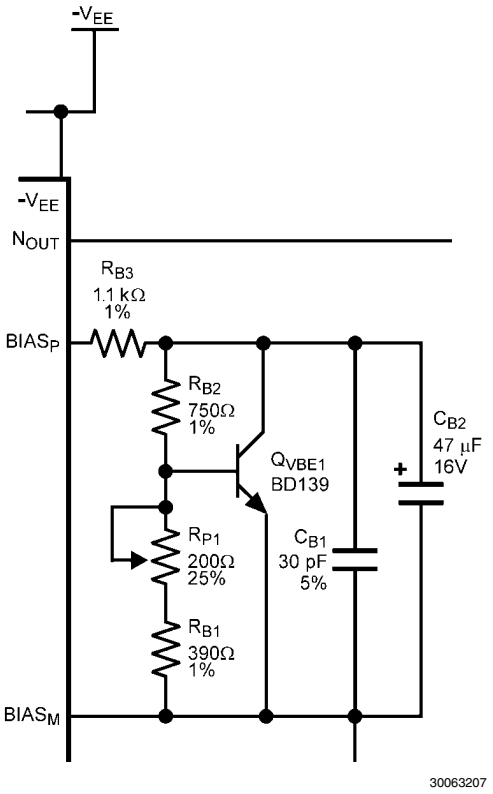


FIGURE 7. Output Stage DC Biasing V_{BE} Multiplier Circuit

The DC bias voltage can be measured by connecting a voltmeter between pins 1 and 2 of J_9. The DC bias voltage is measured from gate-to-gate of the output stage. When R_{P1} is set at its minimum, the total output stage bias current will be approximately 500mA. When set at its maximum, the total output stage bias current will be approximately 175mA. The bias current setting of the EF125WT1 FET module before leaving the factory, and for all performance data, is approximately 225mA. This equates to approximately 112mA per power transistor of power stage quiescent current (~250mA from each supply rail at ±60V). Changing the value of R_{B2} to 620Ω will change the bias range to approximately 115mA to 325mA.

It should be noted that the bias adjustment potentiometer, R_{P1}, is available for your convenience in analyzing the performance effects of output stage bias adjustment. The potentiometer can be replaced in a final design with a simple resistor once the desired DC biasing voltage has been selected.

Please also note that the V_{BE} Multiplier terminals are very sensitive to loading, so when obtaining any performance measurements, be sure that the multi-meter or scope probe has been removed from DC Bias Monitoring header, J_9.

The Q_{VBE1} thermal properties are not an exact match to the MOSFET output device thermal properties. An additional, temperature independent bias resistor, R_{B3}, is used to adjust the bias voltage to more closely match the output devices for stable bias current over temperature. This resistor changes the slope of the bias voltage vs. temperature curve by reducing the effect of the V_{BE} voltage of Q_{VBE1}.

Shown in the equation below is the relationship between the voltage setting resistors and the V_{BE} multiplier's output voltage, V_{CE}.

$$V_{BIAS} = (R_{B3} * 2mA) + V_{BE} [1 + R_{B2} / (R_{B1} + R_{P1})]$$

For a Class AB amplifier design, bias current is chosen such that crossover distortion is minimized while also keeping quiescent power dissipation low. Higher bias current reduces harmonic distortion levels at the cost of increased power dissipation. At some point there is little reduction with increased bias current and resulting power dissipation. A tradeoff in the bias current level must be made between THD performance and power dissipation.

MOSFET output stages typically need higher bias current than BJT output stages for good performance in a Class AB amplifier design. What amount of bias current each solution's output stage will require depends completely on the user's specific tastes and/or target specifications. Shown in *Table 4* are THD+N measurements with a 1kHz signal at 10W into 8Ω load with a 22kHz measurement bandwidth at different total supply current settings. The LM49830 current is approximately 25mA so the output stage bias current is equal to the total supply current minus 25mA.

TABLE 4. Bias Current And Measured THD+N

Supply Current per Supply	1kHz THD+N at 10W/8Ω, 22kHz BW
50mA	0.00364%
100mA	0.00176%
150mA	0.00120%
200mA	0.00089%
250mA	0.00078%
300mA	0.00070%
500mA	0.00067%
1A	0.00067%

Table 4 indicates that the a range of 200mA to 300mA of supply current per power supply produces low magnitude harmonics and manageable power dissipation.

Different bias current levels are shown in the graphs and oscilloscope photos below. For each graph the output power level is 10W into an 8Ω resistive load with 1kHz signal. Each oscilloscope photo shows the input and output signal plus the time domain distortion residual. The measurement equipment is set to notch out the fundamental frequency of the test signal. The fundamental is reduced by more than -110dB relative to 0dB. 0dB is set equal to the voltage for 10W into 8Ω. The graphs show how an insufficient bias current results in THD that is dominated by crossover distortion. Under bias is also indicated by the high level and number of harmonics in the FFT graphs.

THD+N curves over frequency representing the level of crossover distortion associated with varying output stage bias currents are shown in *Figure 8*. The output power level is 10W into an 8Ω load with an 80kHz measurement bandwidth for all plots.

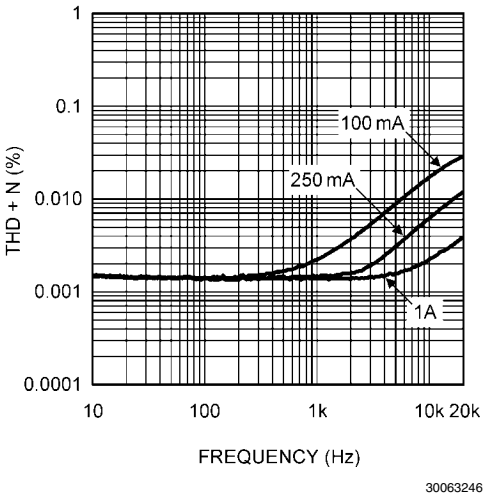


FIGURE 8. THD+N Versus Frequency Versus Bias Current

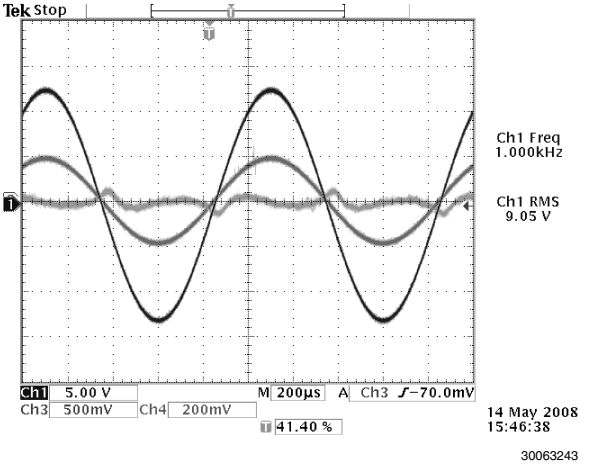


FIGURE 9. 100mA Bias Current Distortion Residual

An under biased output stage is clearly exhibited by sharp, narrow glitches on the distortion residual at the zero crossing point of the output voltage.

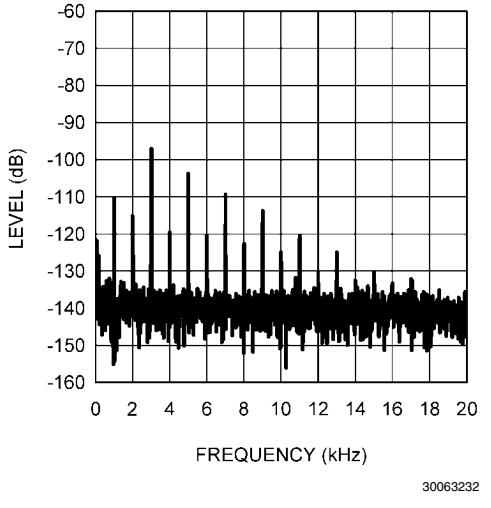


FIGURE 10. 100mA Bias Current Output FFT

The under biased time domain distortion residual is represented above by an FFT that exhibits high odd harmonic distortion over a large number of harmonics. The odd harmonics increase significantly from an optimally biased FFT, while the even order harmonics remain relatively unchanged.

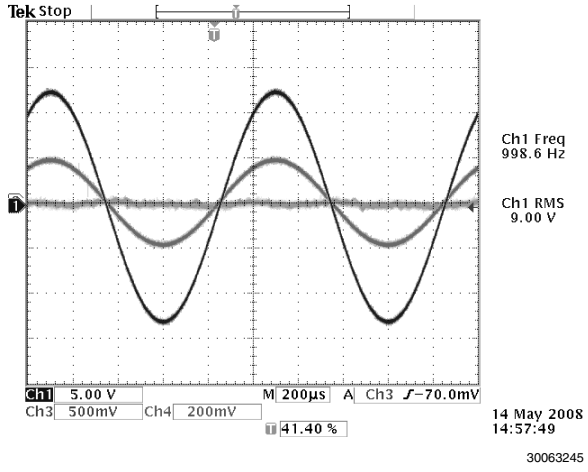


FIGURE 11. 250mA Bias Current Distortion Residual

A correctly biased output stage shows a very flat distortion residual except for the zero crossing point where very small glitches can be observed.

Notice that while the distortion residual at the crossover region is quite small, the overall distortion of the amplifier with this level of residual is 0.00078% THD+N.

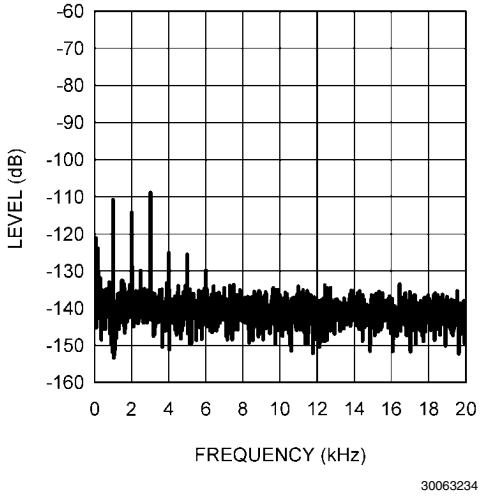


FIGURE 12. 250mA Bias Current Output FFT

A correctly biased time domain distortion residual is represented above by an FFT that exhibits fairly evenly balanced amplitudes of even and odd harmonics as they decrease over frequency. Most of the distortion products are below the fundamental or test signal of 1kHz.

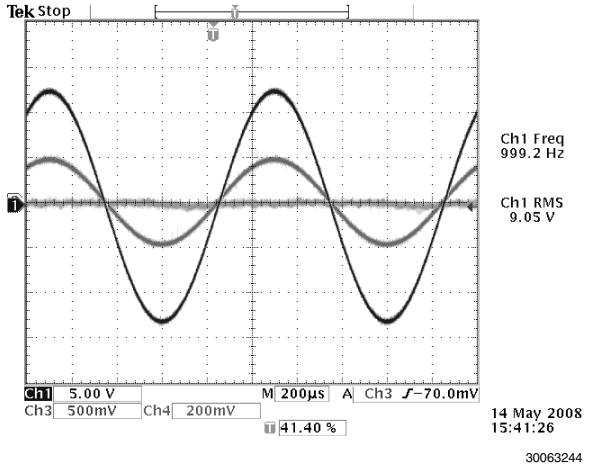


FIGURE 13. 1A Bias Current Distortion Residual

A high bias (Class A) output stage shows no crossover distortion and a very flat time domain distortion residual.

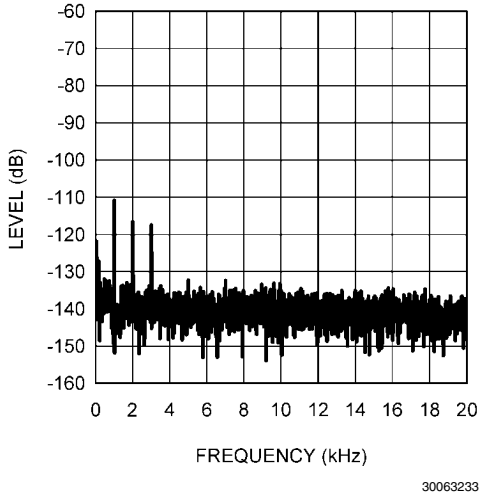


FIGURE 14. 1A Bias Current Output FFT

A class A bias level shows very low harmonics in number and amplitude. The tradeoff is high power dissipation and low efficiency.

BIAS STABILITY

The Total Quiescent Current versus Time graph (*Figure 15*) was created by running the output stage at 40W into an 8Ω resistive load until steady state device case and heat sink temperature are reached. The input signal is turned off (Time = 0) and the bias current recorded over time. It should be noted that the graph units are not linear as indicated. Bias current is measured at 10 second intervals for the first two minutes after the input signal was turned off then at 30 second intervals up to five minutes. One final measurement is taken at 10 minutes. The time steps are one reason for the different slopes on the time curve. There are two plots on the graph, one indicating the quiescent bias at a heat sink temperature of 35°C and the other indicating the bias over time after producing 40W of output power. There are several factors that affect the data such as θ_{JC} of the package and heat sink size which contribute to thermal delay.

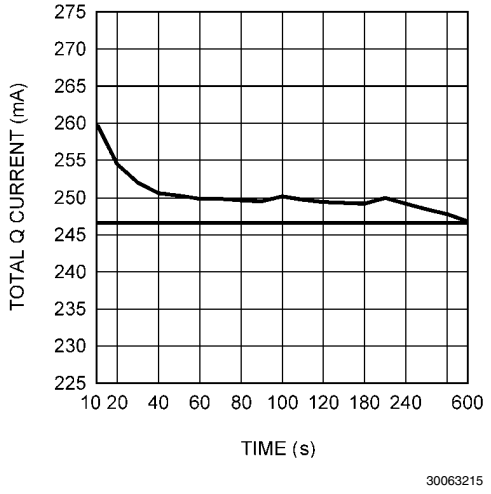


FIGURE 15. Bias Current Vs. Time

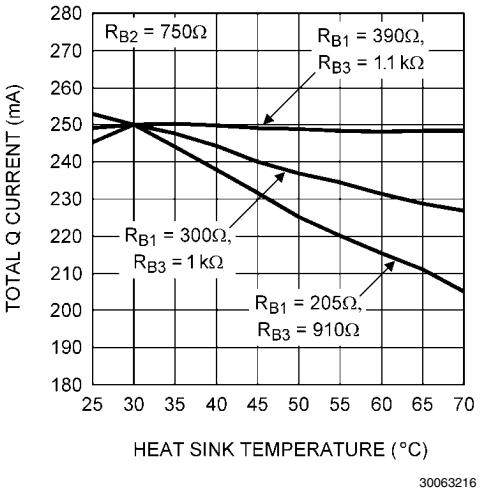


FIGURE 16. Bias Current Vs. Heat Sink Temperature

It is not possible to measure the exact instantaneous channel temperature of discrete devices. There is a temperature gradient from the channel or junction of the output device to the heat sink. An additional temperature gradient exist along the heat sink to the Q_{VBE1} transistor and the thermal resistances of the Q_{VBE1} transistor case. When the output devices are producing power (and dissipating more power than quiescent conditions) the temperature gradient from the channel of the output devices to the junction of the Q_{VBE1} transistor is greater than under quiescent conditions. The thermal resistance is relatively constant but as the power dissipation increases the temperature gradient linearly increases. With the channel temperature higher than the bias voltage setting, the output device current is higher. The current will reduce down to quiescent levels as the channel cools and the temperature gradient from output device channel to Q_{VBE1} junction is equal to quiescent steady state conditions. The graph in *Figure 15* shows the phenomenon as the total current is higher when the input signal is first turned off and then returns down to the steady state bias levels by 10 minutes. It should be noted that within 40 seconds the bias current has returned to within ~4mA of the steady state bias current. With a different heat sink and device mounting placement the response will be different.

Figure 16 shows the bias current as a function of heat sink temperature. The bias current is set when the heat sink reaches 30°C and all the thermal gradients are established at a steady state mode. Using different values for R_{B1} and R_{B3} with R_{B2} set to 750Ω shows how the thermal compensation can be increased (over compensated) for reduced current at higher heat sink temperatures. The data for *Figures 16*, *17* are taken as the heat sink temperature increases under quiescent conditions (no signal) up to 50°C. For the higher heat sink temperatures, the heat sink is heated to 87°C by driving a load then the current recorded as the heat sink cools. Because of the larger temperature gradients when driving a signal the data is collected starting at 70°C when the temperature gradients are near steady state quiescent conditions. To remove differences in bias settings, the bias currents are normalized to 250mA.

Figure 17 shows how the bias current changes as a percent verses heat sink temperature. The percent change uses the bias current at a heat sink temperature of 30°C for a baseline.

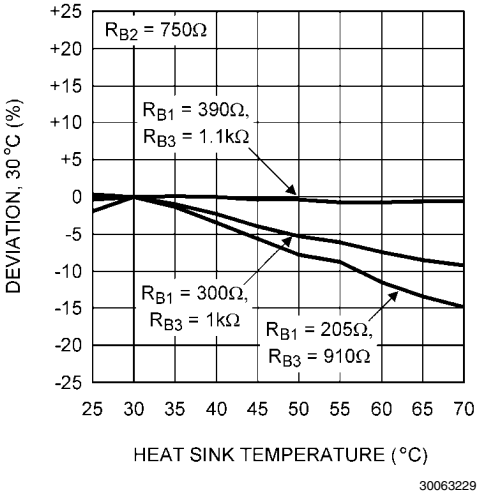


FIGURE 17. Bias Current Change Percent Vs. Heat Sink Temperature

Based on the data above the bias resistors are set to R_{B1} = 392Ω, R_{B2} = 750Ω, and R_{B3} = 1.10kΩ.

BIASING PROCEDURE

Where to set the bias current of the output stage is entirely up to the designer, essentially one of the features of the solution. It is however, important to set up the biasing of the output stage after being warmed up a while,

By allowing the amplifier to first warm up, the distortion is optimized at the temperature that the amplifier will normally be operated. The amplifier will then be operating at its optimum bias point with reduced distortion under normal operating temperature conditions.

Set the DC bias voltage to your preference of distortion level once the amplifier has warmed up to a temperature indicative of normal operation. It is common to evaluate the distortion residual in the time domain and/or the residual's harmonics in the frequency domain when optimizing the DC bias. Additionally, it is common to evaluate the DC bias setting for higher

frequencies where crossover distortion is easily recognized above the measurement unit's noise floor. Frequencies of 3kHz and 5kHz generally allow for significant harmonics to be present even when using a 30kHz measurement-unit low-pass filter.

The goal is to determine the desired potentiometer setting (or eventually a fixed resistance) that will be required for the end-design. This is accomplished by optimizing the distortion residuals from a measurement perspective or by optimizing the desired sound quality from a listening perspective. Removing the amplifier's input signal allows for measurement of the DC bias voltage and the quiescent current running through each leg of power transistors. Simple DC voltage measurement across the source degeneration resistors provides each leg's quiescent current.

Please note that the V_{BE} multiplier terminals are very sensitive to loading, so when obtaining any performance measurements, be sure that the multi-meter or scope probe has been removed from DC Bias Monitoring header, J_9.

Compensation

SINGLE-POLE COMPENSATION

The slew rate specification of an amplifier defines its "speed" by establishing an upper limit of how fast its output can respond to input signal transient changes. The amplifier's slew rate is defined by the equation below.

One of the features of the LME49830 is the ability to set the amplifier's slew rate and power bandwidth through the selection of the external compensation capacitor value. Lowering the value of the compensation capacitor increases the amplifier's slew rate and hence its power bandwidth.

$$\text{Slew Rate} = \Delta V/\Delta t = 2\pi f_{MAX} V_{Opk}$$

The amplifier's power bandwidth is also determined through this equation and can be related to the amplifier's slew rate as shown below.

$$f_{PBW} = \text{Slew Rate}/2\pi V_{Opk}$$

The power bandwidth equation indicates that higher output power amplifiers will require larger slew rates to maintain a constant power bandwidth. Shown in *Table 5* are the required amplifier slew rates for a 100kHz power bandwidth for different output power levels.

TABLE 5. Slew Rates For 100kHz Power Bandwidth

Output Power (W) (R_L = 8Ω)	$V_{O(PEAK)}$ (V)	Slew Rate (µs) (f_{BW} = 100kHz)
125	44.7	28
250	63.2	40
500	89.4	56

The maximum slew rate for an amplifier will be dependent upon the value of the compensation capacitor, in conjunction with the maximum tail current of the input differential transistor pair.

$$\text{Slew Rate} = dV/dt = I_{MAX} / C_{COMP}$$

The LME49830 has a maximum input differential pair tail current of 550µA, so corresponding slew rates for compensation capacitor values are shown in *Table 6*.

TABLE 6. LME49830 Slew Rate vs Compensation Capacitor

Compensation Capacitor, C_{COMP} (pF)	Slew Rate (V/µs)
5	110
10	55
12	46
15	37
18	31
20	27
25	22
30	19
60	9
100	5.5

Since slew rate requirements are different depending upon desired power bandwidth and output power level, we can calculate the needed compensation capacitor for a given design based on the equation below.

$$C_{COMP} = I_{TAIL} / 2\pi f V_{Opk}$$

Shown in *Table 7* are appropriate compensation capacitor values for 100kHz power bandwidths at the stated amplifier output power levels.

TABLE 7. Compensation Capacitor Required Per Reference Design

Reference Design (8Ω)	Compensation Capacitor, C_{COMP} (pF)	Slew Rate (V/µs)	Power Bandwidth (kHz)
125W	20	28	100
250W	12	40	100
450W	10	53	100

Figure 18 represents a 24V/µs slew rate from a 20pF compensation capacitor. This value is a tad shy of the estimated 27V/µs, however, taking into account the tolerances of the compensation capacitor (±5%) and the IC's tail current, a 24V/µs slew rate is a realistic value.

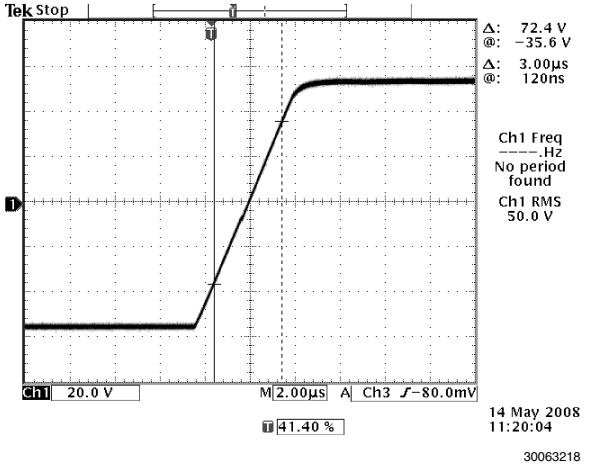


FIGURE 18. Single-Pole Compensation Slew Rate

The power bandwidth for the power amplifier at 150W into 8Ω when using a 20pF compensation capacitor is 10Hz - 90kHz (±0.5dB) and 10Hz - 130kHz (±3dB) as shown in *Figure 19* below. The snubber is removed before taking the graph with the C_T capacitor still in place. The slew rate limitation of 24V/µs dominates the frequency response.

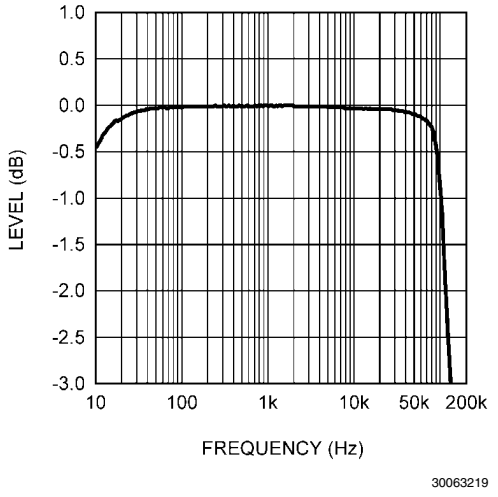


FIGURE 19. Single-Pole Compensation Power Bandwidth vs Frequency

TWO-POLE COMPENSATION

In addition to single-pole compensation, there are component placeholders on the EF125WT1 FET PCB amplifier module for a two-pole compensation scheme as shown in *Figure 20*. The addition of passive components R_{C1} and C_{C2} create a pole at the frequency stated by the equation below.

$$f_{P2} = 1/2\pi C_{C2} R_{C1} = 1/2\pi(62pF)(6.2k\Omega) = 414kHz$$

The two-pole compensation scheme allows for increased loop gain at higher frequencies, resulting in increased slew rate, dynamics and reduced high-frequency distortion. Experimentation with these components will show the benefit of reduced distortion at higher frequencies, but care must be taken to not extend the pole out too far or instabilities may result.

The PCB comes from the factory with R_{C2} (0Ω) installed for a single-pole compensation scheme and must be removed in order for C_{C2} to be effective in the circuit. Mica capacitors from Cornell Dubilier are used for frequency compensation. Typically, the second compensation capacitor is chosen to be between two and 10 times the value of C_{C1}. A value five times C_{C1} is a safe starting point. The resistance value is then selected based on the location of the desired pole. Recommended starting values are 12pF for C_{C2} and 5.1kΩ for R_{C1}.

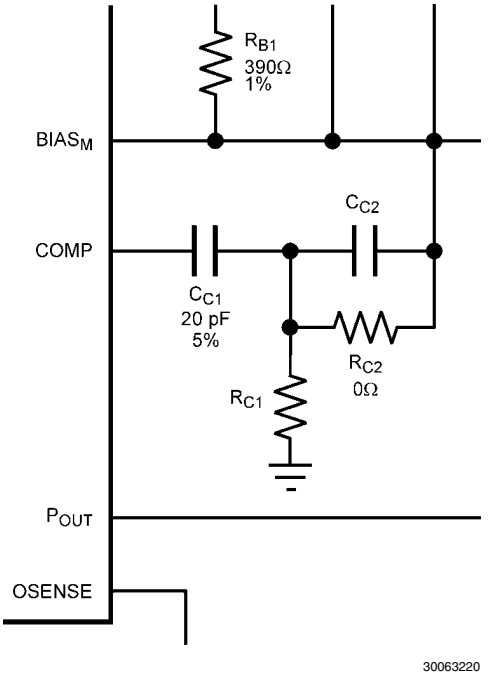


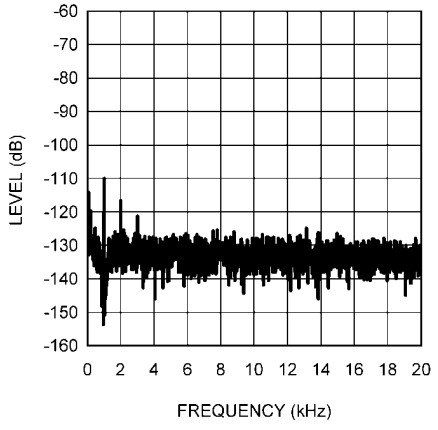
FIGURE 20. Two-Pole Compensation Connections

Not only is there a reduction in higher frequency distortion, there is also a power bandwidth benefit from using 2-pole compensation as a result of increase slew rate.

Performance Graphs (±60V)

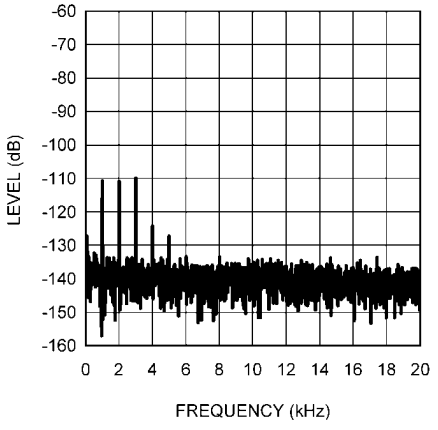
The following pages contain standard audio performance graphs of the amplifier module, running off ±60V power supply rails driving either an 8Ω or 4Ω load. These performance graphs represent the high performance capabilities of the solution.

FFT vs Frequency (Reading)
f = 1kHz, P_{OUT} = 1W, R_L = 8Ω
22kHz BW



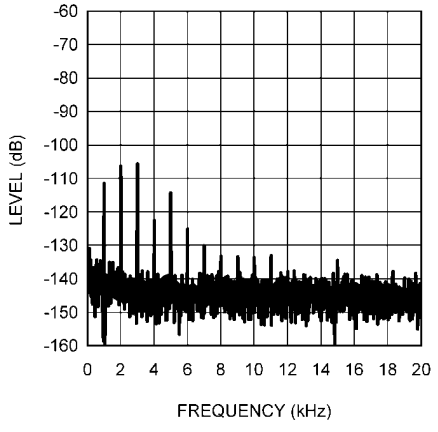
30063239

FFT vs Frequency (Reading)
f = 1kHz, P_{OUT} = 10W, R_L = 8Ω
22kHz BW



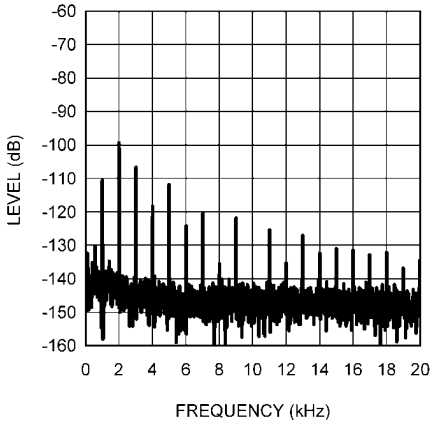
30063236

FFT vs Frequency (Reading)
f = 1kHz, P_{OUT} = 50W, R_L = 8Ω
22kHz BW



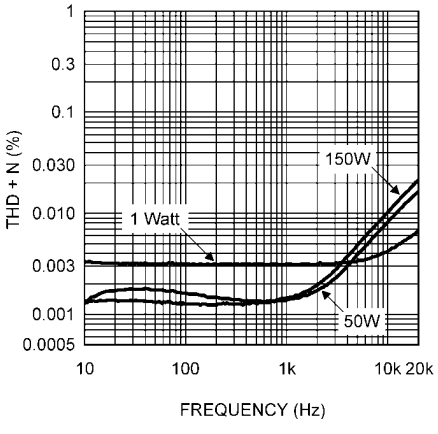
30063242

FFT vs Frequency (Reading)
f = 1kHz, P_{OUT} = 150W, R_L = 8Ω
22kHz BW



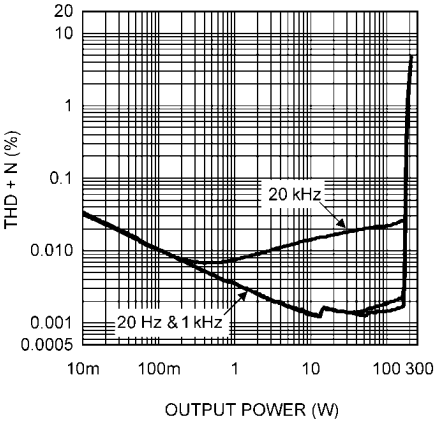
30063237

THD+N vs Frequency
P_{OUT} = 1W, 50W, 150W, R_L = 8Ω
80kHz BW



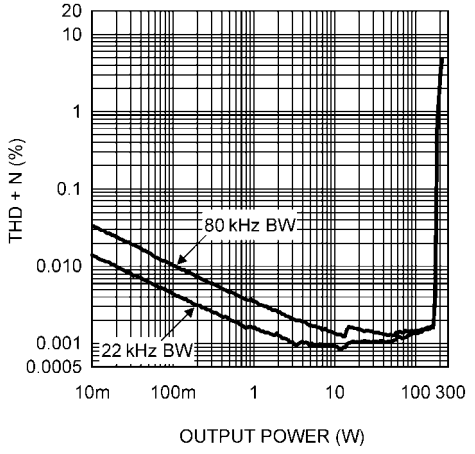
30063248

THD+N vs Output Power
f = 20Hz, 1kHz, 20kHz, R_L = 8Ω
80kHz BW



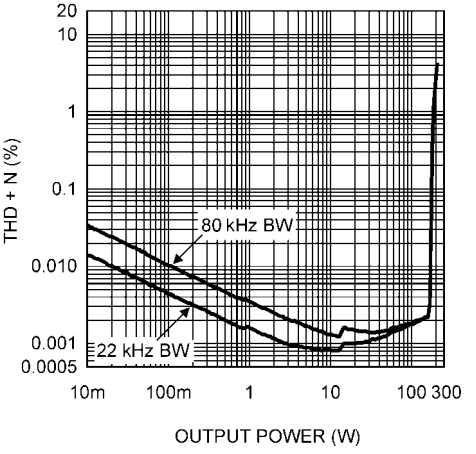
30063252

THD+N vs Output Power
f = 1kHz, R_L = 8Ω
22kHz and 80kHz BW



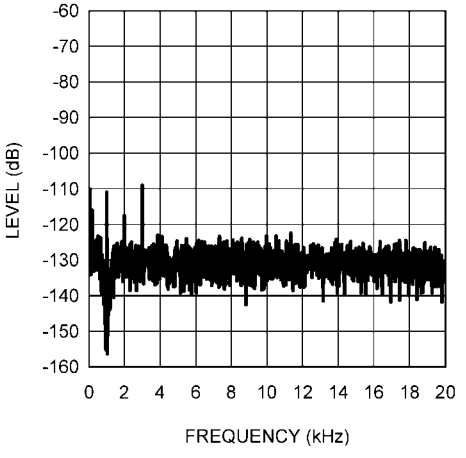
30063250

THD+N vs Output Power
f = 20Hz, R_L = 8Ω
22kHz and 80kHz BW



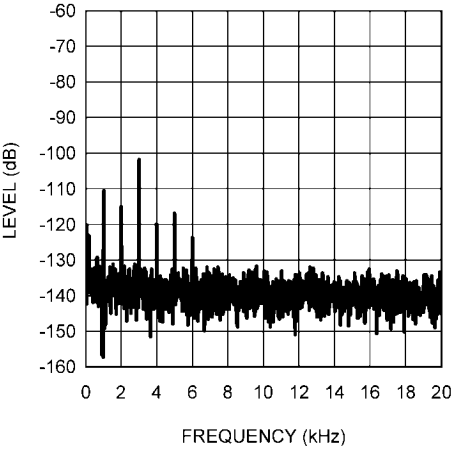
30063254

FFT vs Frequency (Reading)
f = 1kHz, P_{OUT} = 1W, R_L = 4Ω
22kHz BW



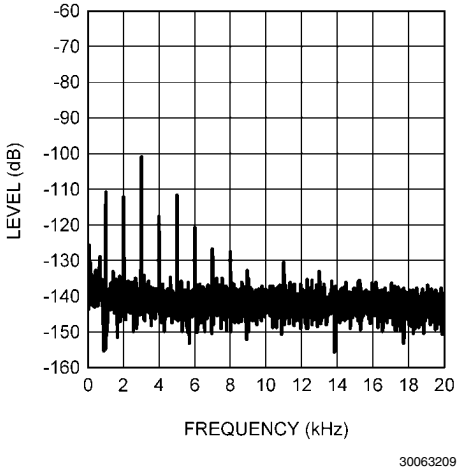
30063238

FFT vs Frequency (Reading)
f = 1kHz, P_{OUT} = 10W, R_L = 4Ω
22kHz BW



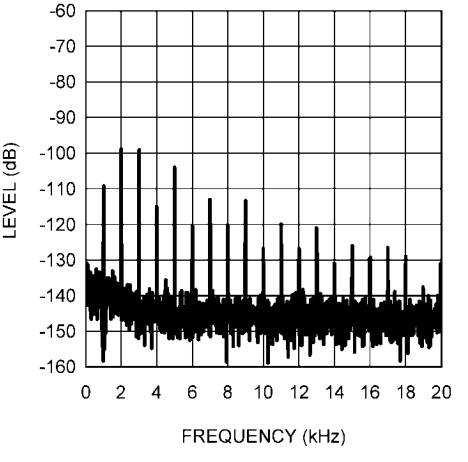
30063235

FFT vs Frequency (Reading)
f = 1kHz, P_{OUT} = 50W, R_L = 4Ω
22kHz BW



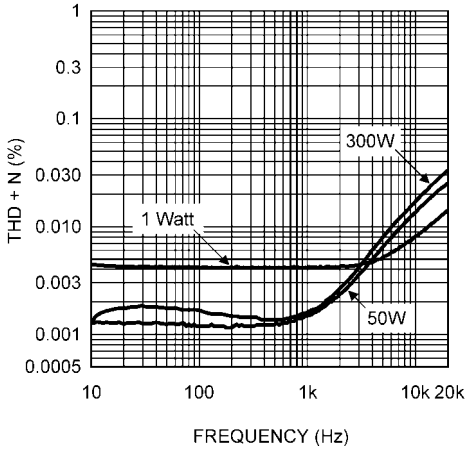
30063209

FFT vs Frequency (Reading)
f = 1kHz, P_{OUT} = 300W, R_L = 4Ω
22kHz BW



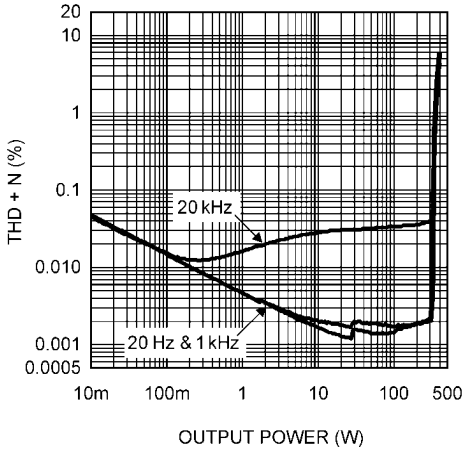
30063240

THD+N vs Frequency
P_{OUT} = 1W, 50W, 300W, R_L = 4Ω
80kHz BW



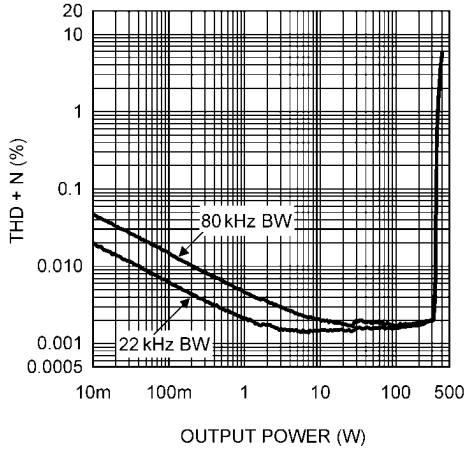
30063247

THD+N vs Output Power
f = 20Hz, 1kHz, 20kHz, R_L = 4Ω
80kHz BW



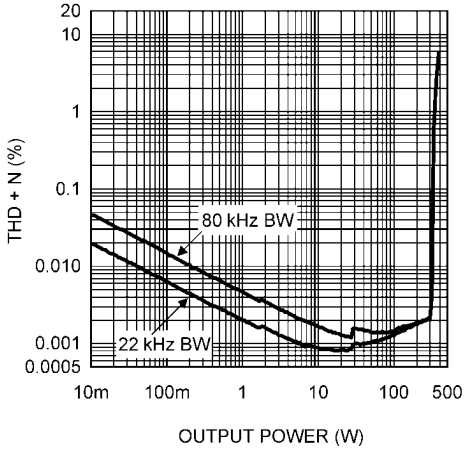
30063251

THD+N vs Output Power
f = 1kHz, R_L = 4Ω
22kHz and 80kHz BW



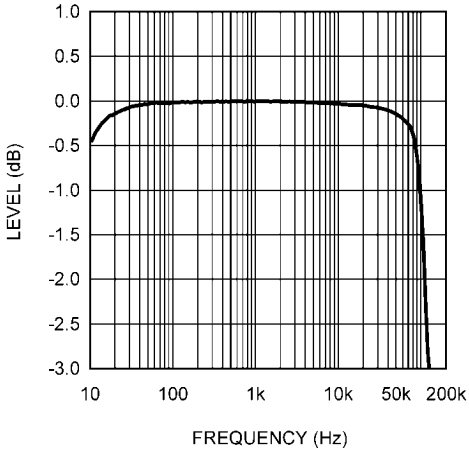
30063249

THD+N vs Output Power
f = 20Hz, R_L = 4Ω
22kHz and 80kHz BW



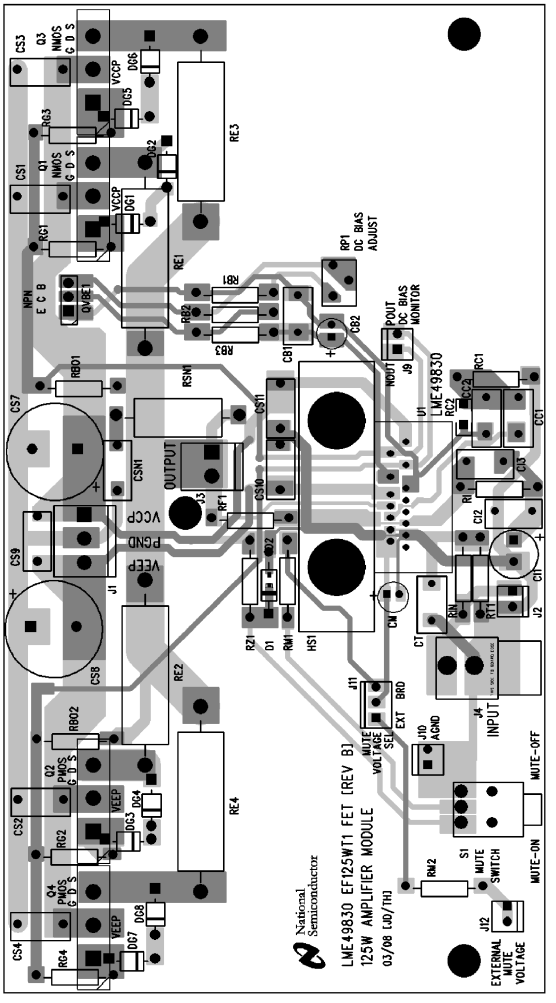
30063253

Frequency Response
P_{OUT} = 300W, R_L = 4Ω



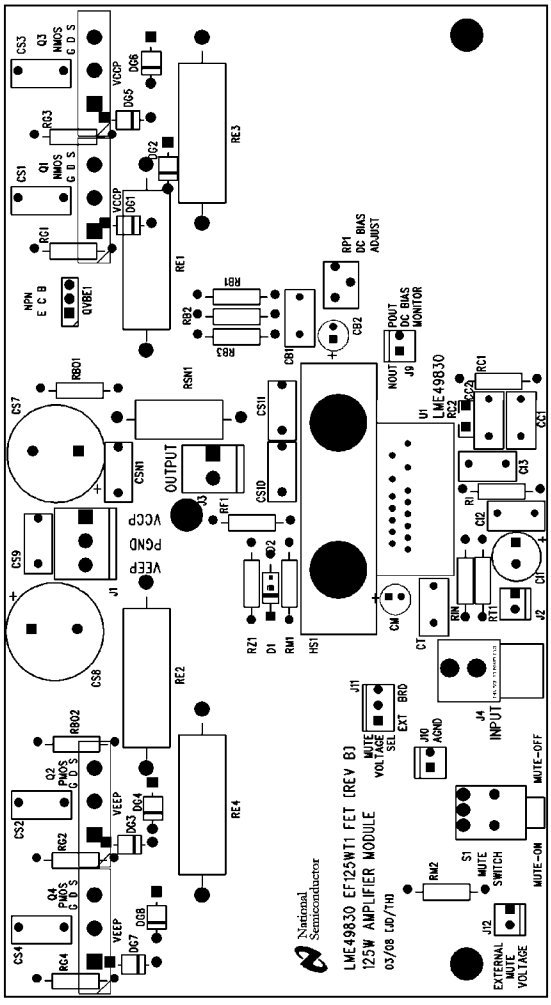
30063231

Board Layer Views



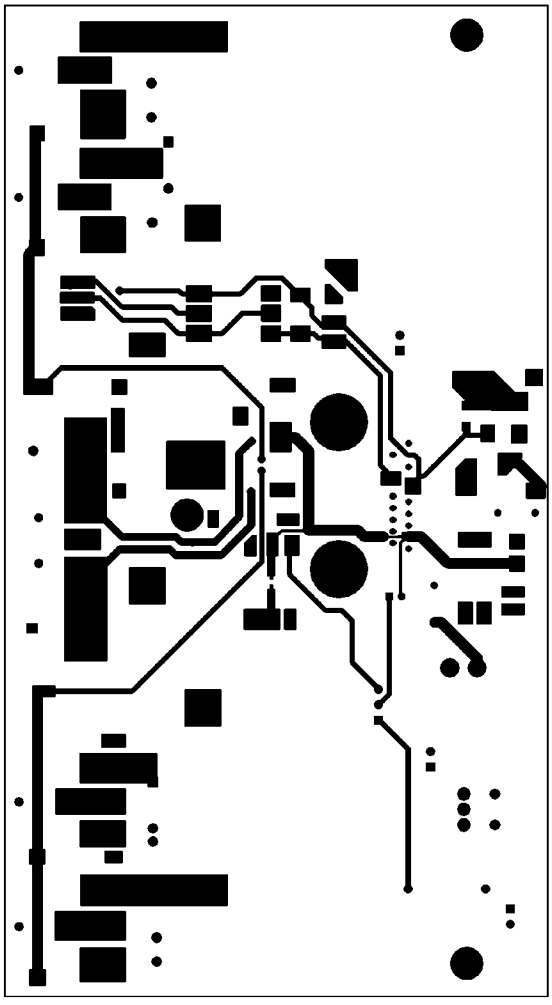
30063226

FIGURE 21. PCB Composite View From Top



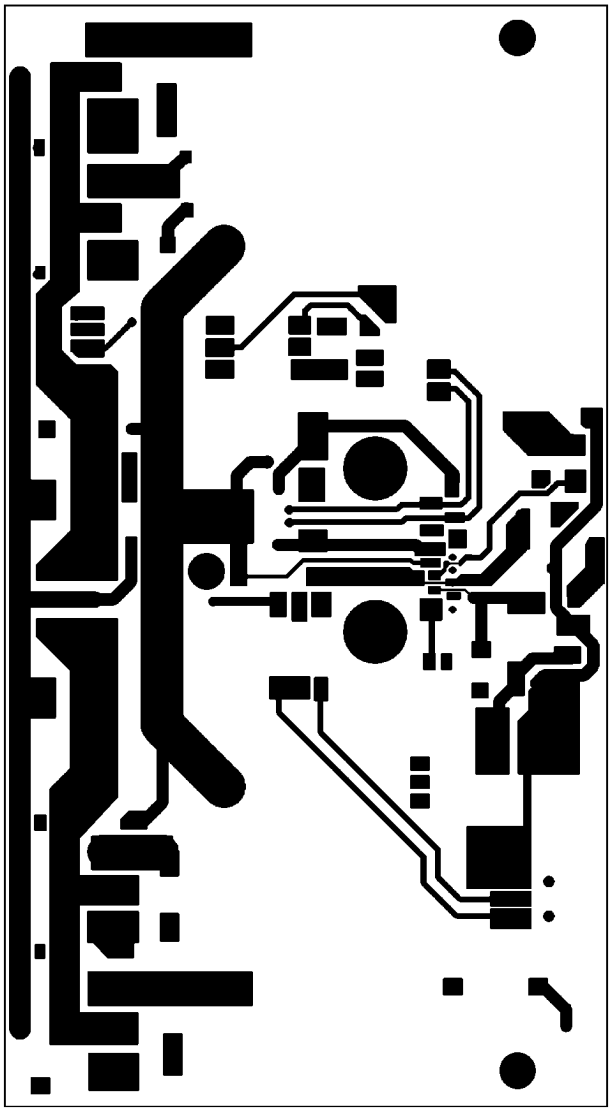
30063227

FIGURE 22. PCB Top Silk Screen View



30063228

FIGURE 23. PCB Top Layer View



30063225

FIGURE 24. PCB Bottom Layer View

Bill of Materials

Reference	Value	Tolerance	Description	Manufacturer	Part Number
CS1, CS2, CS3, CS4, CS10, CS11, CS9, CSN1	0.1µF	10%	250V, metalized polyester film, 7.5mm lead spacing	Panasonic	ECQ-E2104KF
CS7, CS8	470µF	20%	100V, radial electrolytic, 7.5mm lead spacing	Panasonic	EEU-FC2A471
CC1	20pF	5%	500V multilayer mica, 3.6mm lead spacing	CDE Cornell Dubilier	CD15ED200J03
CB1	30pF	5%	500V multilayer mica, 3.6mm lead spacing	CDE Cornell Dubilier	CD15ED300J03
CB2, CM	47µF	20%	16V, radial electrolytic, 2mm lead spacing	Panasonic	EEU-FC1C470
CI1	220µF	20%	35V radial electrolytic, 3.5mm lead spacing	Panasonic	EEU-FC1V221L
CT	180pF	10%	Polyester film, 5mm lead spacing	Panasonic	ECQ-B1H181KF
CC2, CI2, CI3			Not Used		
D1	12V	5%	500mW Zener Diode, DO-35	Fairchild Semiconductor	1N5242BTR
DG1, DG2, DG3, DG4, DG5, DG6, DG7, DG8	10V	5%	1W Zener diode, DO-41	Fairchild Semiconductor	1N4740A
U1	200V		Complementary MOSFET power amplifier input stage	National Semiconductor	LME49830TB
Q_{VBE1}	80V, 1.5A		NPN transistor, TO-126	Fairchild Semiconductor	BD13916STU
Q1, Q3	200V, 12A		N-Channel MOSFET, 150W, TO-3PL (2-21F1B)	Toshiba	2SK1530-YF
Q2, Q4	200V, 12A		P-Channel MOSFET, 150W, TO-3PL(2-21F1B)	Toshiba	2SJ201-YF
RSN1	10Ω	5%	3 Watt metail oxide, axial through hole	Vishay/ BCcomponents	NFR0300001009JAC00
RG1, RG3	22.1Ω	1%	¼ Watt metal film, axial through hole	International Yageo Corp.	MFR-25FBF-22R1
RG2, RG4	10.0Ω	1%	¼ Watt metal film, axial through hole	International Yageo Corp.	MFR-25FBF-10R0
RE1, RE2, RE3, RE4	0.1Ω	1%	5 Watt silicone wirewound, through hole	Vishay/Dale	RS005R1000FS73

Reference	Value	Tolerance	Description	Manufacturer	Part Number
RC2	0Ω	5%	¼ Watt metail film, SMT 1206 (3216)	Panasonic	ERJ-S080R00V
RB1	392Ω	1%	¼ Watt metal film, axial through hole	International Yageo Corp.	MFR-25FBF-392R
RB2	750Ω	1%	¼ Watt metal film, axial through hole	International Yageo Corp.	MFR-25FBF-750R
RB3	1.10kΩ	1%	¼ Watt metal film, axial through hole	International Yageo Corp.	MFR-25FBF-1K10
RP1	200Ω	25%	0.2 Watt single turn potentiometer, through hole	Bourns Inc.	3306W-1-201
RIN, RI	249Ω	1%	¼ Watt metal film, axial through hole	International Yageo Corp.	MFR-25FBF-249R
RT, RF1	6.81kΩ	1%	¼ Watt metal film, axial through hole	International Yageo Corp.	MFR-25FBF-6K81
RM1	75.0kΩ	1%	¼ Watt metal film, axial through hole	International Yageo Corp.	MFR-25FBF-75K0
RM2	20.0kΩ	1%	¼ Watt metal film, axial through hole	International Yageo Corp.	MFR-25FBF-20K0
RZ1	39.2kΩ	1%	¼ Watt metal film, axial through hole	International Yageo Corp.	MFR-25FBF-39K2
RBO1, RBO2, RC1			Not Used		
S1	20V		SPDT On-On right angle, through hole	C & K Components	ET01MD1ABE
J1			3 pin 156mil header, straight, tin plating	Molex/Waldom Electronics Corp.	26-60-4030
J3			2 pin 156mil header, straight, tin plating	Molex/Waldom Electronics Corp.	26-60-4020
J4			RCA phono jack, PCB mount, black	Kobiconn	161-0097-E
J2, J9, J10, J12			2 pin 100mil header, straight, tin plating	Molex/Waldom Electronics Corp.	22-23-2021
J11			3 pin 100mil header, straight, tin plating	Molex/Waldom Electronics Corp.	22-03-2031
	6.3°C/W		LME49830 heat sink	Aavid Thermalloy	530101B00150
	0.62°C/W		Output stage heat sink, 4 inch length	Aavid Thermalloy	65605

Revision History

Rev	Date	Description
1.0	07/01/08	Initial release.
1.01	12/02/08	Text edits.

Notes

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