Effective Edge Selection of BCLK with Great Jitter

IDT82V1074 Application Note AN-380

In MPI mode, the BCLK clock signal of the IDT82V1074 synchronizes the PCM data transfer on the DX1/DX2 and DR1/DR2 lines. The frequency of the BCLK signal varies from 256 kHz to 8.192 MHz in steps of 64 kHz. The IDT82V1074 transmits and receives the PCM data either on the rising edge or on the falling edge of the BCLK signal. Refer to the IDT82V1074 datasheet for further details.

The IDT82V1074 has greater jitter tolerance when it receives the PCM data on the rising edge of the BCLK signal than on the falling edge.

When the IDT82V1074 receives the PCM data on the rising edge, the duty cycle of the BCLK signal should be between 45% and 55%, and the peak-to-peak phase jitter (> 4 kHz) of the BCLK signal should be less than ±20 ns.

When the IDT82V1074 receives the PCM data on the falling edge,

- *for a 6.2 MHz to 8 MHz BCLK signal, its duty cycle should be between 45% and 55%, and its peak-to-peak phase jitter (> 80 kHz) should be less than ±2 ns.*
- *for a 4 MHz to 6.2 MHz BCLK signal, its duty cycle should be between 45% and 55%, and its peak-to-peak phase jitter (> 80 kHz) should be less than ±10 ns.*
- *for a BCLK signal of less than 4 MHz, its duty cycle should be between 45% and 55%, and its peak-to-peak phase jitter (> 4 kHz) should be less than ±20 ns.*