

Fairchild's Process Enhancements Eliminate the CMOS SCR Latch-Up Problem In 74HC Logic

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Enhancements Eliminate the CMOS SCR Latch-Up Problem In 74HC Logic

INTRODUCTION

SCR latch-up is a parasitic phenomena that has existed in circuits fabricated using bulk silicon CMOS technologies. The latch-up mechanism, once triggered, turns on a parasitic SCR internal to CMOS circuits which essentially shorts V_{CC} to ground. This generally destroys the CMOS IC or at the very least causes the system to malfunction. In order to make MM54HC/MM74HC high speed CMOS logic easy to use and reliable it is very important to eliminate latch-up. This has been accomplished through several layout and process enhancements. It is primarily several proprietary innovations in CMOS processing that eliminates the SCR.

First, what is "SCR latch-up?" It is a phenomena common to most monolithic CMOS processes, which involves "turning on" a four layer thyristor structure (P-N-P-N) that appears from V_{CC} to ground. This structure is formed by the parasitic substrate interconnections of various circuit diffusions. It most commonly can be turned on by applying a voltage greater than V_{CC} or less than ground any input or output, which forward biases the input or output protection diodes. *Figure 1* schematically illustrates these diodes found in the MM54HC/MM74HC family. Standard CD4000 and MM54C/MM74C logic also has a very similar structure. These diodes can act as the gate to the parasitic SCR, and if enough current flows the SCR will trigger. A second method of turning on the SCR is to apply a very large supply voltage across the device. This will breakdown internal diodes causing enough current to flow to trigger latch-up. In HC logic the typical V_{CC} breakdown voltage is above 10V so this method is more uncommon. In either case, once the SCR is turned on a large current will flow from V_{CC} to ground, causing the CMOS circuit to malfunction and possibly damage itself.

CMOS SCR problems can be minimized by proper system design techniques or added external protection circuits, but obviously the reduction or elimination of latch-up in the IC itself would ease CMOS system design, increase system reliability and eliminate additional circuitry. For this reason it was important to eliminate this phenomena in Fairchild's high speed CMOS logic family.

Characterization of this proprietary high speed CMOS process for latch up has verified the elimination of this parasitic mechanism. In tests conducted under worst case conditions ($V_{CC}=7V$ and $T_A=125^\circ C$) it has been impossible to latch-up these devices on the inputs or on the outputs.

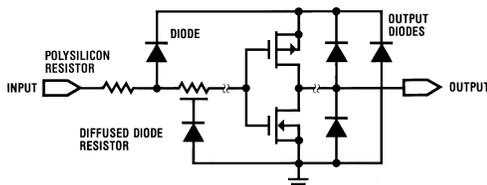


FIGURE 1. Schematic Diagram of Input and Output Protection Structures

In testing for latch-up, caution must be exercised when trying to force large currents into an IC. As with any integrated circuit there are maximum limitations to the current handling capabilities of the internal metalization, and diodes, and thus they can be damaged by excessive currents. This is discussed later in the test section.

To enable the user to understand what latch-up is and how it has been eliminated, it is useful to review the operating of a simple discrete SCR, and then apply this to the CMOS SCR. Since most latch-up problems historically have been caused by extraneous noise and system transients, the AC characteristics of CMOS latch are presented. Also various methods of external and internal protection against latch-up is discussed as well as example test methods for determining the latch up susceptibility of CMOS IC's.

SIMPLE DISCRETE SCR OPERATION

To understand the behavior of the SCR structure parasitic to CMOS IC's, it is first useful to review the basic static operation of the discrete SCR, and then apply it to the CMOS SCR. There are two basic trigger methods for this SCR. One is turning on the SCR by forcing current into its gate, and the second is by placing a large voltage across its anode and cathode. *Figure 2* shows the basic four layer structure biased into its forward blocking state. The SCR action can be more easily understood if this device is modeled as a cross coupled PNP and NPN transistor as shown in *Figure 3*.

In the case of latch-up caused by forward biasing a diode, if current is injected into the base of Q2, this transistor turns on, and a collector current beta times its base current flows into the base of Q1. Q1 in turn amplifies this current by beta and feeds it back into the base of Q2, where the current is again amplified. If the product of the two transistors' Beta becomes greater than one, $B(NPN) \times B(PNP) > 1$, this current multiplication continues until the transistors saturate, and the SCR is triggered. Once the regenerative action occurs a large anode current flows, and the SCR will remain on even after the gate current is removed, if enough anode current flows to sustain latch-up. However, if the transistor current gains are small no self sustaining positive feedback will occur, and when the base current is removed the collector current will stop. In a similar manner the SCR can be triggered by drawing current by forward biasing the base of Q1.

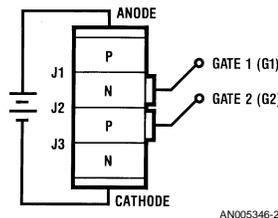


FIGURE 2. Simplified SCR Structure

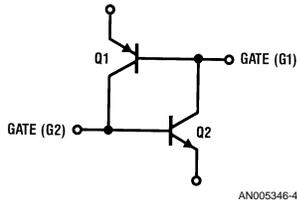
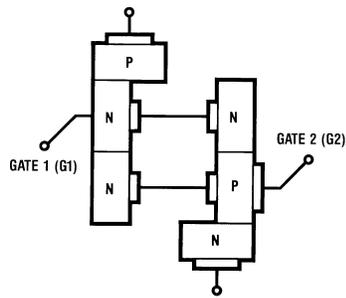


FIGURE 3. Cross-Coupled Transistor Model of SCR

The second case, the SCR may also be triggered without injecting any gate current. In the forward blocking state the small leakage current that is present does not trigger the SCR, but if the voltage is increased to a point where significant leakage currents start conducting, these currents could also trigger the SCR, again forming a low impedance path through the device. The same requirement that the Beta product of the PNP and NPN be greater than one in order for the SCR to trigger applies here as well. This leakage current trigger is characteristic of Schottky diode operation.

THE CMOS SCR: STATIC DC OPERATION

For discussion purposes CMOS SCR latch up characteristics can be divided into two areas. One is the basic operation of the SCR when static DC voltages are applied, and the second is the behavior when transients or pulses are applied.

First looking at the device statically, the parasitic SCR in CMOS integrated circuits is much more complex and its triggering is somewhat different than the simple SCR already discussed. However, the regenerative feedback effect is basically the same. Figure 4 shows a simplified P- well CMOS structure illustrating only the diffusions and the resultant parasitic transistors. The NPN transistor is a vertical device whose emitter is formed by n+ diffusions. The P- well forms the base and the N- substrate forms the collector of the NPN. The PNP transistor is a lateral device. Its emitter is formed by p+ diffusions, its base is the N- substrate, and its collector is the P- well.

Figure 5 illustrates a cross section of a simplified N- well process and its corresponding parasitic bipolar transistors. In this process the NPN is a lateral device and the PNP is vertical. Essentially the description of the P- well SCR is the same as the N- well version except the NPN is a low gain lateral device and the PNP is a high gain vertical transistor. Thus the following discussion for the P- well also applies to the N- well with this exception.

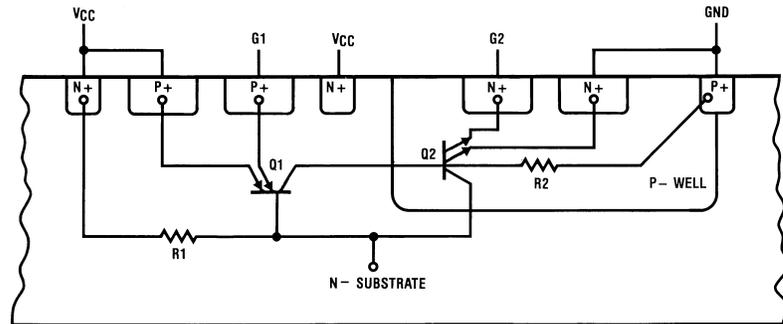


FIGURE 4.

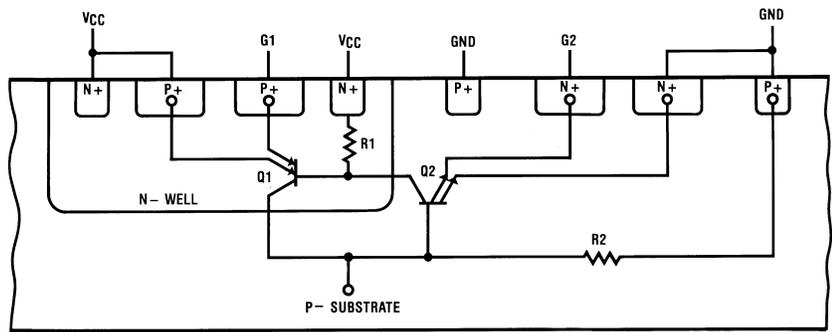


FIGURE 5. Simplified Cross Section of CMOS Processes a) P- well and b) N- well

The transistors for the P- well CMOS process are drawn schematically in Figure 6, so that their cross coupled interconnection is more easily seen. The SCR structure in Figure 6 differs from that of Figure 3 in two ways. First, the transistors of Figure 6 have multiple emitters, due to the many diffusions on a typical die. One emitter of each transistor could function as the trigger input to the SCR. Secondly, R1 and R2 have been added and are due to P- and N- substrate resistances between the base of each transistor and the substrate power supply contacts.

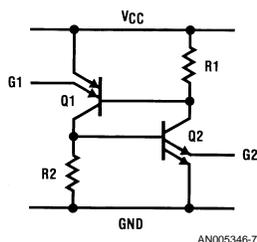


FIGURE 6. Schematic of Simple SCR Model

Like the discrete SCR there are two basic methods of turning the CMOS SCR on. The first method is however slightly different. In the CMOS parasitic SCR current cannot be directly injected into the base of one of its transistors. Instead either node G1 must be raised above V_{CC} enough to turn on Q1, or node G2 must be lowered below ground enough to turn on Q2. If G1 is brought above V_{CC} , current is injected from the emitter of Q1 and is swept to the collector of Q1. The collector of Q1 feeds the base of Q2 and also R2. R2 has the effect of stealing current from the base of Q2, but as current flows through R2 a voltage will appear at the base of Q2. Once this voltage reaches 0.6 volts Q2 will turn on and feed current from its collector back into R1 and into Q1. If 0.6 volts is generated across R1, Q1 then turns on even more.

Again, if the two transistors have enough gain and enough anode current flows to sustain the SCR, it will turn on, and remain on even after G1 is returned to V_{CC} . The actual requirements for latch up are altered by the two resistors, R1 and R2. Since the resistors shunt some current away from the base of both transistors, the resistors essentially reduce the effective gains of the transistors. Thus the transistors must actually have much higher gains in order to achieve an overall SCR loop gain greater than one, and hence enable the SCR to trigger. The actual equations to show quantitatively how the resistors effect the SCR's behavior could be derived, but it is sufficient to notice that as R1 and R2 become smaller the SCR becomes harder to turn on. IC designers utilize this to reduce latch up.

The second method of turning on the SCR mentioned earlier also applies here. If the supply voltage is raised to a large value, and internal substrate diodes start breaking down excessive leakage currents will flow possibly triggering the SCR. The resistors also affect this trigger method as well, since they steal some of the leakage currents from Q1 and Q2, and hence it takes more current to trigger the SCR. In high speed CMOS the process enhancements reduce the transistor betas and hence eliminate latch up by this mechanism as well.

While useful, the SCR model of Figures 5, 6 is very simplified, since in actuality the CMOS SCR is a structure with many transistors interconnected by many resistances. Although still somewhat simplified, Figure 7 attempts to illustrate how the parasitics on a chip connect. It is important to remember that any transistor or diode diffusion can parasitically form part of the SCR. In the figure transistor Q1 and Q2 are single emitter transistors formed by the input protection diodes. Internal P and N channel transistors have no external connection and are represented by Q3 and Q4. Q5 and Q6 represent output transistor diffusions, and the second

emitter corresponds to the output. All of these transistors are connected together by the N- substrate and P- well resistances, which are illustrated by the resistor mesh.

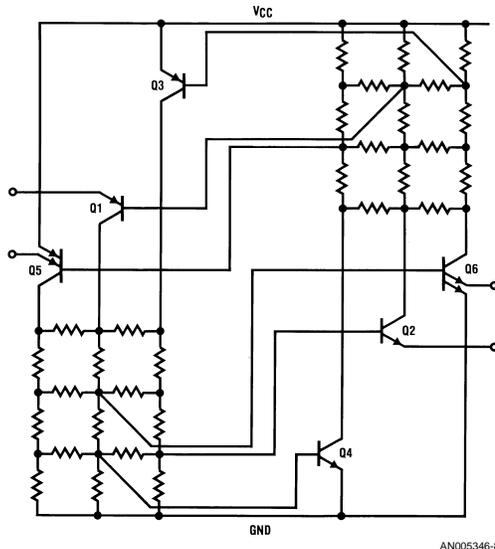


FIGURE 7. Distributed Model of CMOS SCR

If any of the emitters associated with the trigger inputs G1-G4 become forward biased the SCR may be triggered. Also due to the intertwined nature of this structure, part of the SCR may be initially latched up. In this case only a limited amount of current may flow, but this limited latch up may spread and cause other parts to be triggered until eventually the whole chip is involved.

In general the trigger to the SCR has been conceptualized as a current, since ideally the CMOS input looks into the base of the SCR transistors. However this may not be quite true. There may be some resistance in series with each base, due to substrate or input protection resistances. In newer silicon gate CMOS processes, MM54HC/MM74HC for example, a poly-silicon resistor is used for electrostatic protection, and this enables larger voltages to be applied to the circuit pins without causing latchup. This is because the poly resistor actually forms a current limit resistor in series with the diodes. In most applications the designer is more concerned with accidental application of a large voltage, and the use of the poly resistor internally enables good voltage resistance to latch up. CMOS outputs are directly connected to parasitic output diodes since no poly resistor can be placed on an output without degrading output current drive. Thus the output latch up mechanism is usually thought of as a current.

Temperature variations will affect the amount of current required to trigger the SCR. This is readily understandable since temperature effects the bipolar transistor's gain and the resistance of the base-emitter resistors. Generally, as the temperature is increased less current is needed to cause latch-up. This is because as temperature increases the bipolar transistor's base-emitter voltage decreases and the base-emitter resistor value increases. Figure 8 plots trigger current versus temperature for a sensitive CMOS input. This data was taken on a CMOS device without any layout or pro-

cess enhancements to eliminate latch up. Increasing temperature from room to 125°C will reduce the trigger current by about a factor of three. Once the circuit is latched up, heating of the device die caused by SCR currents will actually increase the susceptibility to repeated latch up.

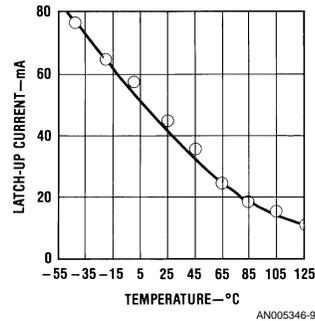


FIGURE 8. Temperature versus SCR Trigger Current for Special CMOS Test Structure

OTHER LATCH UP TRIGGER METHODS

There are some other methods of latching up CMOS circuits, they are not as circuit design related and shall only be briefly mentioned. The first is latch up due to radiation bombardment. In hostile environments energetic atomic particles can bombard a CMOS die freeing carriers in the substrate. These carriers then can cause the SCR to trigger. This can be of concern in high radiation environments which call for some sort of radiation hardened CMOS logic.

Another latch up mechanism is the application of a fast rise or fall spike to the supply inputs of a CMOS device. Even if insufficient current is injected into the circuit the fast voltage change could trigger latch up. This occurs because the voltage change across the part changes the junction depletion capacitances, and this change in capacitance theoretically could cause a current that would trigger the SCR latch. In actual practice this is very difficult to do because the response time of the SCR (discussed shortly) is very poor. This is hardly a problem since power supplies must be adequately decoupled anyway.

A third latch up cause which is completely internal to the IC itself and is out of the control of the system designer is internally triggered latch up. Any internal switching node connects to a diode diffusion, and as these diffusions switch the junction depletion capacitance associated with these nodes changes causing a current to be generated. This current could trigger the SCR. The poor frequency response of the SCR tends to make this difficult, but as chip geometries are shrunk packing densities will increase and the gain of the lateral PNP transistor increase. This may increase the latch up susceptibility. It is up to the IC designer to ensure that this doesn't happen, and care in the layout and circuit design of 54HC/74HC logic has ensured that this will be avoided.

THE CMOS SCR: TRANSIENT BEHAVIOR

With the introduction of fast CMOS logic the transient nature of the CMOS SCR phenomena becomes more important because signal line ringing and power supply transients are more prevalent in these systems. Older metal gate CMOS (CD4000 & 74HC) circuits have slow rise and fall times

which do not cause a large amount of line ringing. Power supply spiking is also somewhat less, again due to slow switching times associated with these circuits.

The previous discussion assumed that the trigger to the CMOS SCR was essentially static and was a fixed current. Under these conditions a certain value current will cause the SCR to trigger, but if the trigger is a short pulse the peak value of the pulse current that will trigger the SCR can be much larger than the static DC trigger current. This is due to the poor frequency characteristics of the SCR.

For short noise pulses, $<5 \mu\text{s}$, the peak current required to latch up a device is dependent on the duty cycle of the pulses. At these speeds it is the average current that causes latch-up. For example, if a 1 MHz 50% duty cycle over-voltage pulse train is applied to a device that latched with 20 mA DC current, then typically the peak current required will be about 40 mA. For a 25% duty cycle the peak current would be 80 mA. An example of this is shown in Figure 9 which plots latch up current against over-voltage pulse width at 1 MHz.

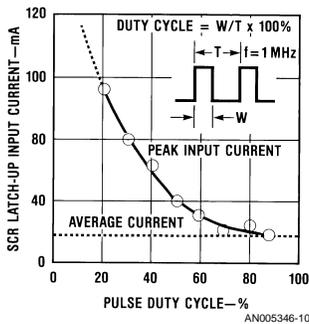


FIGURE 9. Trigger Current of SCR of Input Overvoltage Pulses at High Repetition Rate on Special Test Unit

If the pulse widths become long, many microseconds, the latch up current will approach the DC value even for low duty cycles. This is shown in Figure 10 which plots peak trigger current vs pulse width for the same test device used in Figure 9. The repetition rate in this case is a slow 2.5 kHz (period=400 μs). These long pulse widths approach the trigger time of the SCR, and thus pulses lasting several microseconds are long enough to appear as DC voltages to the SCR. This indirectly indicates the trigger speed of the SCR to be on the order of ten to fifteen microseconds. This is however dependent on the way the IC was designed and the processing used.

In normal high speed systems noise spikes will typically be only a few nanoseconds in duration, and the average duty cycle will be small. So even a device that is not designed to be latch up resistant, will probably not latch up even with significant line ringing on its inputs or outputs (Then again . . .). However, in some systems where inductive or other loads are used transients of several microseconds can be easily generated. For example, some possible applications are automotive and relay drivers. In other CMOS logic fami-

lies spikes of this nature are much more likely to cause the SCR to trigger, but here again MM54HC/MM74HC high speed CMOS is immune.

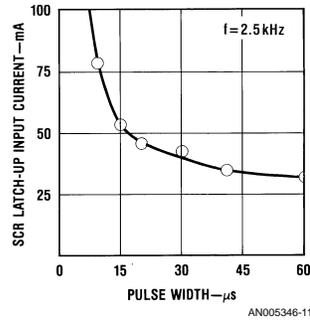


FIGURE 10. Trigger Current of Pulse on Special Test Unit SCR for Single Transient Overvoltage

PREVENTING SCR LATCH UP: USER SYSTEM DESIGN SOLUTIONS

SCR latch-up can be prevented either on the system level or on the IC level. Since Fairchild's MM54HC/MM74HC series will not latch up, this eliminates the need for the system designer to worry about preventing latch up at the system level. This not only eases the design, but negates the need to add external diodes and resistors to protect the CMOS circuit, and hence additional cost. (Note however that even though the devices don't latch up, diode currents should be limited to their Absolute Maximum Ratings listed in the Data Sheets).

If one is using a CMOS device that may latch up, older CD4000 CMOS or another vendors HC for example, and its input or output voltages may forward bias the input or output diodes then some external circuitry may need to be added to eliminate possible SCR triggering. As with the previous discussions of latch-up preventing SCR latch-up falls into two categories: the static case, and the transient condition. Each is related but has some unique solutions.

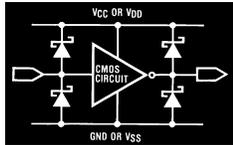
In the static condition to ensure SCR latch up does not occur, the simplest solution is to design CMOS systems so that their input/output diodes don't become forward biased. To ease this requirement some special circuits that have some of their input protection diodes removed are provided, and this enables input voltages to exceed the supply range. These devices are MM54HC4049/50, CD4049/50, and MM54C901/2/3/4.

If standard logic is used and input voltages will exceed the supply range, an external network should be added that protects the device by either clamping the input voltage or by limiting the currents which flow through the internal diodes. Figure 11 illustrates various input and output diode clamping circuits that shunt the diode currents when excessive input voltages are applied. Usually either an additional input or output diode is required, rarely both, and if the voltages only exceed one supply then only one diode is necessary. If an external silicon diode is used the current shunt is only par-

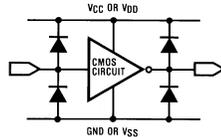
tially effective since this diode is in parallel with the internal silicon protection diode, and both diodes clamp to about 0.7V.

A second method, limiting input current, is very effective in preventing latch-up, and several designs are shown in *Figure 12*. The simplest approach is a series input resistor. It is recommended that this resistor should be as large as possible without causing excessive speed degradation yet en-

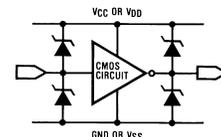
sure the input current is limited to a safe value. If speed is critical, it is better to use a combination diode-resistor network as shown in *Figure 12*. These input networks effectively limit input currents while using lower input resistors. The series resistor may not be an ideal solution for protecting outputs because it will reduce the effective drive of the output. In most cases this is only a problem when the output must drive a lot of current or must switch large capacitances quickly.



Schottky Diodes

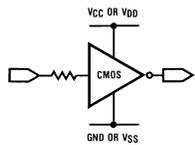


Germanium Diodes

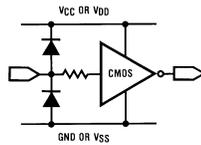


Zener Diodes

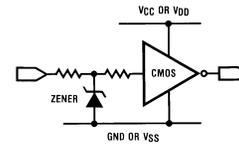
FIGURE 11. External Input and Output Protection Diodes Circuits for Eliminating SCR Latch-up



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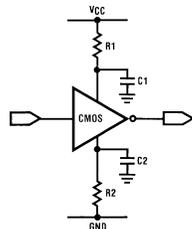
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FIGURE 12. Input Resistor and Resistor-Diode Protection Circuits for Eliminating Latch-up

A third approach is instead of placing resistors in series with the inputs to place them in series with the power supply lines as shown in *Figure 13*. The resistors must be bypassed by capacitors so that momentary switching currents don't produce large voltage transients across R1 and R2. These resistors can limit input currents but primarily they should be chosen to ensure that the supply current that can flow is less than the holding current of the SCR. Thus even though the input current can cause latch up it cannot be sustained and the IC will not be damaged.



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FIGURE 13. Supply Resistor-Capacitor Circuits for Eliminating Latch-up

This last solution has the advantage of fewer added components, but also has some disadvantages. This method may not prevent latch up unless the resistors are fairly large, but this will greatly degrade the output current drive and switching characteristics of the device. Secondly, this circuit protects the IC from damage but if diodes currents are applied

causing large supply currents, the circuits will logically malfunction where as with other schemes logic malfunction can be prevented as well.

PREVENTING LATCH UP: IC DESIGN SOLUTIONS

The previous latch up solutions involve adding extra components and hence extra cost and board space. One can imagine that in a microprocessor bus system if for some reason the designer had to protect each output of several CMOS devices that are driving a 16-bit address bus that up to 32 diodes and possibly 16 resistors may need to be added. Thus for the system designer the preferable solution is to use logic that won't latch up.

Most methods previously employed to eliminate latch up are either not effective, increase the die size significantly, and/or degrade MOS transistor performance. The process enhancements employed on 54HC/74HC logic circumvent these problems. Primarily it is effective without degrading MOS performance.

When designing CMOS integrated circuits, there are many ways that the SCR action of these circuits can be reduced. One of the several methods of eliminating the SCR is to reduce the effective gain of at least one of the transistors, thus eliminating the regenerative feedback. This can be accomplished either by modifying the process and/or by inserting other parasitic structures to shunt the transistor action. Also the substrate resistances modeled as R1 and R2 in *Figures 4, 6* can be reduced. As these resistances approach zero more and more current is required to develop enough voltage across them to turn on the transistors.

As mentioned, the current gains of the NPN and PNP parasitic transistors directly affect the current required to trigger the latch. Thus some layout and process enhancements can be implemented to reduce the NPN and PNP Betas. In a P-well process the gain of the vertical NPN is determined by the specific CMOS process, and is dependent on junction depths and doping concentrations. These parameters also control the performance of the N-MOS transistors as well and so process modification must be done without degrading CMOS performance. To reduce the gain of the vertical PNP the doping levels of the P-well can be increased. This will decrease minority carrier lifetimes. It will also reduce the substrate resistance lowering the NPN base-emitter resistance. However this will increase parasitic junction capacitances, and may affect NMOS threshold voltages and carrier mobility. The depth of the well may be increased as well. This

will reduce layout density due to increased lateral diffusion, and increase processing time as it will take longer to drive the well deeper into the substrate.

The lateral PNP's gain is determined by the spacing of input and output diode diffusions to active circuitry and minority carrier life times in the N- substrate. The carrier life times are a function of process doping levels as well, and care must be exercised to ensure no MOS transistor performance degradation. Again the doping levels of the substrate can be increased, but this will increase parasitic junction capacitances, and may alter the PMOS threshold characteristics. The spacing between input/output diodes and other diffusions can be increased. This will increase the PNP's base width, lowering its beta. This may be done only a limited amount without significantly impacting die size and cost.

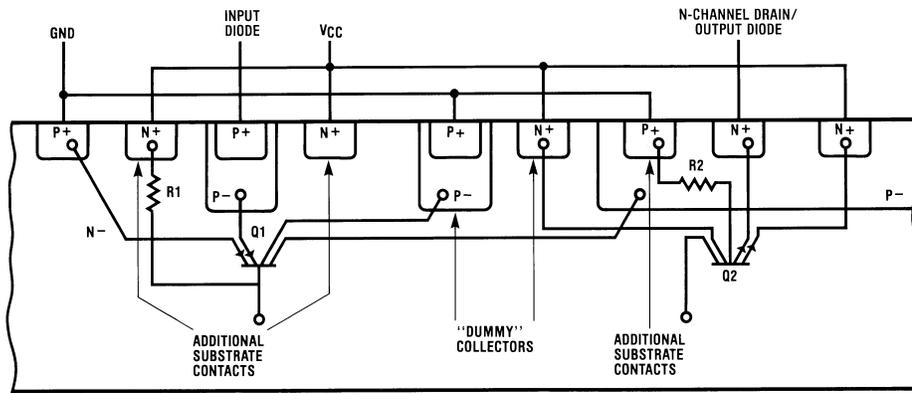


FIGURE 14. Simplified CMOS Cross Section Showing Added Latch-up Reduction Structures

Another method for enhancing the latch-up immunity of MM54HC/MM74HC is to short out the SCR by creating additional parasitic transistors and reducing the effective substrate resistances. These techniques employ the use of ring structures (termed guard rings) to surround inputs and outputs with diffusions that are shorted to V_{CC} or ground. These diffusions act to lower the substrate resistances, making it harder to turn on the bipolar transistors. They also act

“dummy” collectors that shunt transistor action by collecting charges directly to either V_{CC} or ground, rather than through active circuitry. Figure 14 shows a cross section of how this might look and Figure 15 schematically illustrates how these techniques ideally modify the SCR structure.

Ideally, in Figure 15 if the inputs are forward biased any transistor action is immediately shunted to V_{CC} or ground

through the “dummy” collectors. Any current not collected will flow through the resistors, which are now much lower in value and will not allow the opposite transistor to turn on.

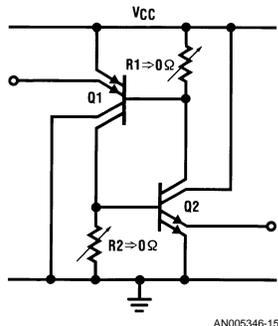


FIGURE 15. Schematic Representation of SCR with Improvements to Reduce Turn On.

Unfortunately in order to reduce latch up these techniques add quite significantly to the die size, and still may not be completely effective.

The ineffectiveness of the ringing structures at completely eliminating latch up is for one because the collectors are only surface devices and carriers can be injected very deep into the N- substrate. Thus they can very easily go under the fairly small “dummy” collectors and be collected by the relatively large active P- well. A possible solution might be to make the collector diffusions much deeper. This suffers from the same drawbacks as making the well deeper, as well as requiring additional mask steps increasing process complexity. Secondly, the base emitter resistances can be reduced only so much, but again only the surface resistances are reduced. Some transistor action can occur under the P- well and deep in the N- bulk where these surface shorts are only partially effective.

The above discussion described modifications to a P- well process. For an N- well process the descriptions are the same except that instead of a P- well an N- well is used resulting in a vertical PNP instead of an NPN and a lateral NPN instead of a PNP.

These methods are employed in 54HC/74HC CMOS logic, but in addition processing enhancements were made that effectively eliminate the PNP transistor. The primary enhancement is a modification to the doping profile of the N- substrate (P- well process). This lowers the conductivity of the substrate material while maintaining a lightly dope surface concentration. This allows optimum performance NMOS and PMOS transistors while dramatically reducing the gain of the PNP and its base-emitter resistance. The gain of the PNP is reduced because the minority carrier lifetimes are reduced. This modification also increases the effectiveness of the “dummy” collectors by maintaining carriers closer to the surface. This then eliminates the SCR latch up mechanism.

TESTING SCR LATCH-UP

There are several methods and test circuits that can be employed to test for latch-up. The one primarily used to characterize the 54HC/74HC logic family is shown in *Figure 16*. This circuit utilizes several supplies and various meters to ei-

ther force current into the V_{CC} diodes or force current out of the ground diodes. By controlling the input supply a current is forced into or out of an input or output of the test device. As the input supply voltage is increased the current into the diode increases. Internal transistor action may cause some supply current to flow, but this should not be considered latch up. When latch-up occurs the power supply current will jump, and if the input supply is reduced to zero the power supply current should remain. The input trigger current is the input current seen just prior to the supply current jumping.

Testing latch-up is a destructive test, but in order to test 54HC/74HC devices without causing immediate damage, test limits for the amount of input or output currents and supply voltages should be observed. Even though immediate damage is avoided, SCR latch-up test is a destructive test and the IC performance may be degraded when testing to these limits. Therefore parts tested to these limits should not be used for design or production purposes. In the case of Fairchild’s high speed CMOS logic the definition of “latch-up proof” requires the following test limits when using the standard DC power supply test as is shown in *Figure 16*.

1. Inputs: When testing latch-up on CMOS inputs the current into these inputs should be limited to less than 70 mA. Application of currents greater than this may damage the input protection poly resistor or input metalization, and prevent further testing of the IC.
2. Outputs: When testing outputs there is a limit to the metalization’s current capacity. Output test currents should be limited to 200 mA. This limitation is due again to metalization short term current capabilities, similar to inputs. Application of currents greater than this may blow out the output.
3. Supply: The power supply voltage is recommended to be 7.0V which is at the absolute maximum limit specified in 54HC/74HC and is the worst case voltage for testing latch-up. If a device latches up it will short out the power supply and self destruct. (Another Vendors HC may latch-up for example.) It is recommended that to prevent immediate destruction of other vendors parts that the power supply be current limited to less than 300 mA.

In almost all instances at high temperature, if it is going to occur, latch-up will occur at current values between 0–50 mA. There are a few special considerations when trying to measure worst case latch-up current. Measuring input latch-up current is straight forward, just force the inputs above or below the power supply, but to measure an output it must first be set to a high level when forcing it above V_{CC} , or to a low level when forcing it below ground. When measuring 3-State outputs, the outputs should be disabled, and when measuring analog switches they should be either left open or turned off.

To measure the transient behavior of the test device or to reduce IC heating effects a pulse generator can be used in place of the input supply and an oscilloscope with a current probe should then replace the current meter. Care should be exercised to avoid ground loops in the test hardware as this may short out the supplies.

Although there are several methods of testing latch-up, this method is very simple and easy to understand. It also yields

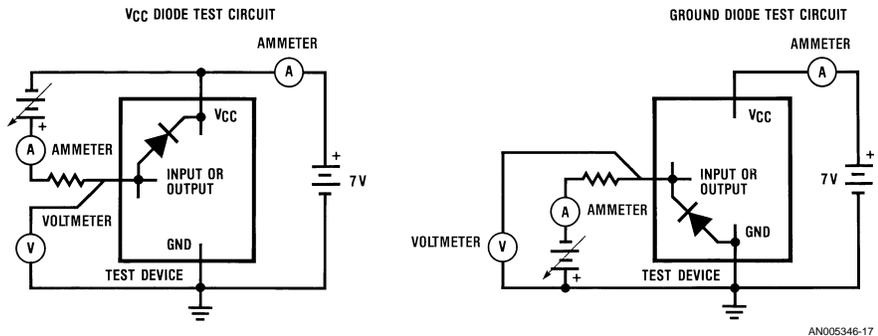
conservative data since manually controlling the supplies is a slow process which causes localized heating on the chip prior to latch-up, and lowers the latch-up current.

CONCLUSION

SCR latch-up in CMOS circuits is a phenomena which when understood can be effectively controlled both from the integrated circuit and system level. Fairchild's proprietary CMOS

process and layout considerations have eliminated CMOS latch-up in the MM54HC/MM74HC family. This will increase the ease of use and design of this family by negating the need for extra SCR protection circuitry as well as very favorable impact system integrity and reliability.

Testing SCR Latch-Up of HCMOS



T_A = 125°C

AN005346-17

FIGURE 16. Bench Test Setup for Measuring Latch-up

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