Fairchild Electronic Device Models

General Information
Fairchild supports both SPICE and IBIS model formats for all interface products. All IBIS (Input Output Buffer Information Specification) models that are currently available are listed on our website (www.fairchildsemi.com/models/) and can be directly downloaded. SPICE models can be obtained via email or by signed NDA (Non-Disclosure Agreement), if required. It is our intent to continually update our website with new models and additional information. If a model, or information on a particular model is not available please inquire to our customer support staff (ensignalab@fairchildsemi.com).

IBIS Models
IBIS is a fast and accurate behavioral method of modeling input/output buffers based on V/I curve data derived from measurement or from SPICE model simulation. It uses a standardized software parsable format in the form of an ASCII file to create the behavioral information needed to model the analog characteristics of digital devices. Fairchild currently offers IBIS Version 3.2 compatible models for most interface products. Below is a brief description about IBIS models and what one may expect from simulation using them.

Characteristics of IBIS models:
1. Follows the IBIS Version 3.2 Specification
2. Represents the DC voltage and current characteristics of a devices' input and output (I/O) structures; Multiple-Pin Models
3. Allows the user to perform transmission line and signal integrity analysis
4. Includes package information on all signal, control, power and ground pins
5. Are created from empirical bench data or SPICE simulation results

Characteristics IBIS models DO NOT provide:
1. Details about the device design, layout, or process information
2. Represent the logic functionality of a device
3. Represent AC characteristics such as propagation delays

No NDA is required for distribution of IBIS models to our customers.

IBIS Models: Creation and Verification
Fairchild IBIS models are created in two ways:
1. Via HSPICE model conversion
   This is done primarily for new designs. It is intended to give the user a pre-silicon model of the device
2. Using empirical bench measurement techniques
   A state of the art automated DC and AC bench is used to collect I-V and V-t data for IBIS model creation

We primarily use the SPICE translation method of creation for IBIS models. A SPICE model correlated to bench measurement is translated via simulation into a valid IBIS model. This translation is done using the ApsimIBIS toolkit® to create accurate IBIS Version 3.2 compatible models, by automated construction from SPICE netlists. The empirical bench measurement technique is generally only used for older products. Fairchild IBIS models are put through extensive verification and correlation procedures to ensure reliable and accurate models. First, the IBIS file syntax is verified using IBIS check software. The model is then used in a variety of simulations using signal integrity analysis tools to ensure correlation to measured data (i.e. rise and fall times over given test loads).

SPICE Models
General Information
SPICE models represent transistor level and process information of integrated circuits. They come as input, output, or I/O sub-circuits (SPICE I/O) or as full circuit (single-slice or full die) models.

Full circuit SPICE models contain the FULL design of the integrated circuit (one path or the full die). However, due to the complexity of most full-circuit models, simulation times can become extensive. In the interest of faster run times and for signal integrity analysis SPICE I/O models are provided. This is the preferred format supported by Fairchild. These models include transistor level sub-circuits of the input, output, or I/O of the IC. I/O models are useful in simulations, such as signal integrity of a critical network since the functionality and timing information of the device is not necessary.

We are committed to providing SPICE models representative of all our new products. We will, in most cases, provide SPICE I/O models for any new product upon request (with signed NDA, if applicable). Full-circuit models are available by special request.
With increasing system performance requirements, many designers are now using behavioral level SPICE modeling to evaluate device and interconnect signal integrity as part of their PCB designs. SPICE models of digital devices are used in many cases for signal integrity simulations (i.e., to modify PCB layout and optimize bus termination schemes). In this case the main interest of the user is to evaluate the I/O characteristics of the device including dynamic and static drive strength, I/O capacitance, edge rate and the impact of ESD or other input structures on clamping signal noise. SPICE I/O models are created for these types of simulations. These models are not recommended for timing or functional simulations.

Below is a brief description about Fairchild SPICE I/O models and what one may expect from simulation with them.

**Characteristics of SPICE I/O Models:**
1. Are HSPICE compatible
2. Represent the DC Voltage and current (V/I) characteristics of a devices’ input and output (I/O) structures; “Single-Path” models
3. Provide some non-proprietary details of the device design and process information
4. Include ESD circuitry
5. Accurately represent the slope characteristics (\(\Delta V/\Delta t\)) of a device output
6. Have capability to model Undershoot, Overshoot and Ground Bounce
7. Are useful in transmission line and signal integrity analysis
8. Have the capability to represent fast, typical, and slow processes
9. Include package information (package model file available for additional package options)

**Characteristics SPICE I/O Models DO NOT provide:**
1. The logical functionality of a device
2. AC characteristics of a device such as propagation delay

In most cases an NDA is not required for distribution of SPICE I/O models to our customers.

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**Contacts**
We welcome any feedback or suggestions on how we can better service our customers modeling needs. For further technical information, refer to the datasheet or contact a Fairchild Technical Response Group representative.

Questions and comments can be sent via e-mail to the EnSigna Lab at:  
ensignalab@fairchildsemi.com  
or visit our web site at  
www.fairchildsemi.com/models

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.