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The Road to 200 Ampere VRM

Alan Elbanhawy, Fairchild Semiconductor

Abstract

Over the past few years DC-DC converters for the PC market have experienced a major push for higher currents at lower voltages and much tighter DC and transient specifications. By all indications, the core voltage is pushing steadily toward 1 Volt at a current in the neighborhood of 200 Amps for servers and high-end applications. This clearly puts enormous pressures on the power supply engineers to design more efficient and cost competitive converters that can meet these requirements while not overloading a cooling system that has to grow to accommodate the same high demands placed on the converter. We were very intrigued by this challenge and decided to explore the possibility of designing such a DC-DC converter today using today's components and observing all the recent advancements in the understanding of the different loss mechanisms in a high frequency, high current switch mode power supply applications. We were able to design a voltage regulator module, VRM that can deliver 1 volt at 200 Amperes. This paper describes this VRM in some details.

Introduction

The goal of our work was to design a VRM that can deliver 1 Volt at 200 amperes and explore in as much details as possible all the challenging aspect of the design and explore ways to overcome them. The most important question we were faced with was which switching devices and in which packages we can use in this design also, how many phases to be used in order to maximize the converter's efficiency while maintaining a low cost bill of materials.

The Design

The maximum current per phase in multiphase synchronous buck converters for the PC core voltage in the late spring of 2003 was hovering around 25–30 Amps per phase. We decided to push the envelop a little bit and go with 40 Amps per phase for two main reasons the first, is to explore the possibility of using such high switched current and examine it's effect on ringing at the switch node as well as the ground plane. The second, from the cost point of view the larger current per phase means lower total number of phases, less number of inductors, MOSFET and gate drivers. This will push the cost down and will result in more efficient PCB space utilization.

MOSFET Package Selection

The package source parasitic inductance plays a major role in determining the fall time of the current in MOSFETs and consequently influences the dynamic losses. Reference [1] and [2] go into details of the mechanics of this effect.

MOSFET package parasitic resistance adds to the silicon RDS(on) and invariably results in higher apparent RDS(on) = RDS(on) Silicon + parasitic resistance. This means that for the optimum utilization of the silicon, we should use the package with the smallest parasitic resistance to minimize the power loss.

It can be shown that the drain inductance leads to ringing specially at high current switching at fast rise and fall times leading to inductor losses and larger EMI may also result from that ringing.

Gate inductance has a complex relationship with the source inductance in affecting the performance of the switching MOSFET and as a rule the smaller the gate inductance the better the performance.

Table 1 shows the results of finite element analysis done on several packages and depicts the different parasitic inductances and resistance of two power BGA packages as they compare to a standard SO8 package. It is worthwhile noting that the parasitic resistance 5x5.5mm BGA is much smaller than that of SO8 and the source inductance is also much smaller than SO8.

Table 1

Package	Parasitic Resistance	Lss	Ldd	Lgg
SO8	2290μΩ	690pH	318pH	1800pH
BGA, 5x5.5	58μΩ	6pH	30pH	40pH
BGA, 2x2.5	209μΩ	10.5pH	54pH	32pH

This led us to conclude that the BGA package is superior to other traditional packages like SO8 and DPAK.

PCB Design

The choice of the PCB design approach was governed by the following consideration:

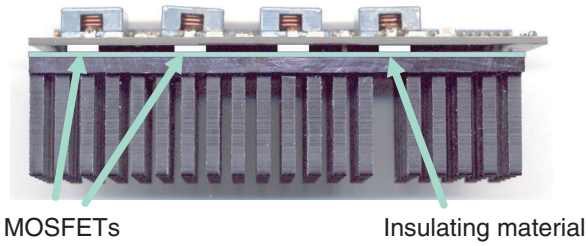

Figure 1. VRM profile showing how the heatsink is mounted on the PCB

- VRM Board size of 4" x 1.2", the smallest practical size.
- The number of layers had to accommodate several factors like the lowest possible PCB parasitic resistance and inductance to minimize PCB losses and inductive ringing. We settled on 8 layers to facilitate sharing the high DC and switched currents between multiple layers and have multiple ground planes. Figure 3 below depicts the ringing measured at the switching node between the HS and LS MOSFETs. Notice the extremely small amplitude of ringing waveform which is attributed to the good PCB layout approach and the BGA package extremely low parasitic inductances
- We chose 2 ounce copper on all layers which allows us to minimize the PCB resistance while using standard copper weight and avoid incurring high cost for special PCB materials if we were to go with 3 or 4 ounce copper
- One of the main points of consideration was the use of several types of vias to facilitate current sharing among different layers without compromise. Figure 2 shows the extensive use of vias right under the BGA package
- Double sided component mounting allows us to mount all the MOSFETs on one side for ease of heat sinking while the rest of the components were placed on the component side

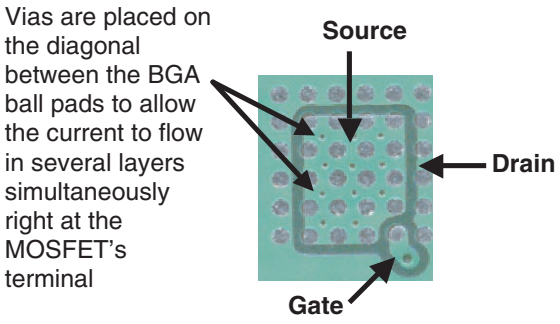

Figure 2. Placement of tented vias under the MOSFET

Heatsink Selection and Mounting:

The selection of the heat sink was done in cooperation with the supplier where a special profile was designed specifically for this application. The design was based on an airflow rate of 400 FPM to limit the PCB temperature to no more than 105°C to be measured at the base of the inductor. The base of the inductor was chosen because preliminary testing showed that the MOSFET drain temperature is about 5–10°C above that of this point allowing us to get an idea about the temperature of both the MOSFET junction and the PCB at the hottest point. Though infrared camera equipment was available to us for use, we decided not to use them but rather use thermocouples for temperature measurements since the heatsink covers all the MOSFETs completely.

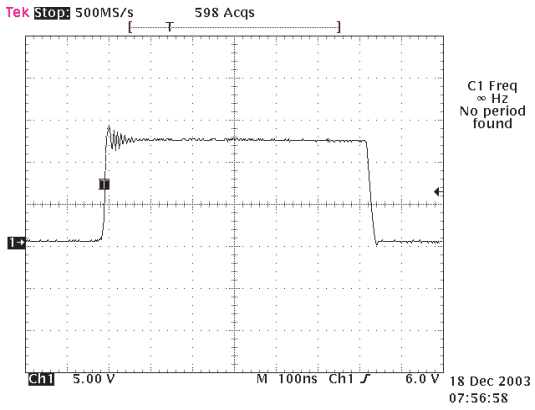

Figure 3. Switch node waveform showing very low ringing

Figure 1 above depicts a profile of one of two VRM modules that constitute the 200 Amps VRM solution. As can be seen, all the BGA MOSFETs are mounted on one side then covered by an insulating material and then the heatsink is applied. Screws were used to fasten the heatsink to the PCB. The insulating material used is of the flexible variety allowing full coverage of the surface of the MOSFET when the right amount of pressure is applied to the fastening screws.

We cannot talk about the heat sink design and selection without talking about airflow. The preliminary exploratory work that we have done clearly indicated the need for airflow to be able to make this design work. This is because the thermal resistance of the heatsink is greatly influenced by airflow where more is needed for the right thermal resistance given that the actual heatsink size is only 4"L x 1.1"W x 1"H. Our experience shows that for the given VRM fitted with a given heatsink, a 400 FPM airflow will more than double the maximum current delivered compared to still air. This means that a small investment in the cooling system may allow for up to 50% savings in the size and cost of the DC-DC converter solution over that designed for still air.

MOSFET Selection

The pivotal point for a successful 40 amp per phase design is the selection of the right MOSFET for the application. This involves having a selection criteria for each of the high side and low side MOSFETs.

Table 2

MOSFET	RDS(on) @ 10V Typ.	RDS(on) @ 4.5V Typ.	Gate Charge Typ.	Gate Thresh-old Typ.
FDZ7064S x One, HS	6.0 mΩ	7.0 mΩ	Qgd=6nC	1.4 V
FDZ5047N x Two, LS	2.3 mΩ	3.2 mΩ	Qg=52nC	1.3 V

High Side (HS) MOSFET

Figure 4 depicts the dynamic, conduction and total power losses as a function of the HS MOSFET On-resistance, RDS(on) for a given figure of merit FOM at a phase current of 40 Amps and a switching frequency of 300 KHz. Historically the HS MOSFET has been selected based primarily on it's switching performance alone with the RDS(on) being only a secondary effect. This clearly is not the case when we are dealing with high current per phase say in excess of 30 Amps. This is because at such higher currents, the conduction losses start to be greater than the dynamic losses and have to be equally considered in the selection to achieve the desired low losses and the high efficiency expected from these VRMs.

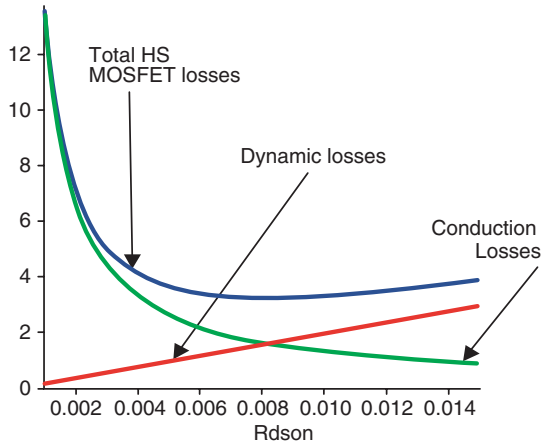

Figure 4. Conduction, dynamic and total power loss as a function of RDS(on) of the HS MOSFET

Close examination of the graph reveals that the optimum value for RDS(on) is around 8mΩ. This will result in the lowest power dissipation. FDZ7064S was chosen for this design.

Low Side (LS) MOSFET

The LS MOSFET selection requires different criterion for optimum performance. For starters the dynamic losses are much smaller than those for the HS MOSFET especially around 200–300KHz. Other performance parameters are considered as follows:

- RDS(on) should be as low as possible governed by cost and whether the gate driver can adequately switch it. Some gate drivers are not capable of driving high values of Cgs capacitors >5nF
- The body diode reverse recovery charge Qrr, should be small enough to add as little losses as possible
- The ratio of gate to drain capacitor to the gate to source capacitor $\frac{Cgd}{Cgs + Cgd}$ should ideally be ≤ Vcc to guarantee no shoot through.

The LS MOSFET selected is FDZ5047N.

$$\frac{Cgd}{Cgs + Cgd} \times Vcc \leq Vgth$$

Table 2 shows some of the important specifications for both the HS and LS MOSFETs selected.

Gate Driver Selection

One of the biggest challenges that we faced in the design of this VRM was that for the selection of the gate driver. We ran several preliminary tests on three different drivers placed on the very same board to evaluate the overall performance of the DC-DC converter. Fig. 5 below depicts the efficiency measured on a single board with three different gate drivers.

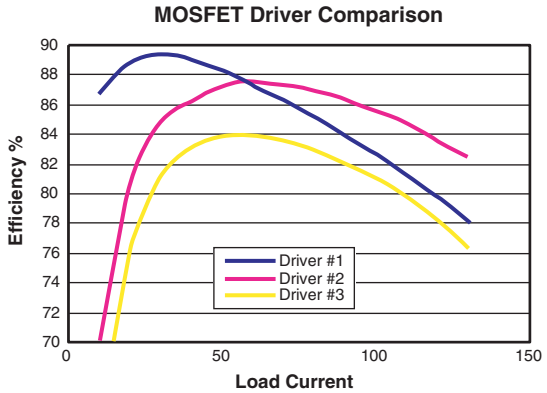

Figure 5. Power efficiency for different gate drivers

It is worthwhile to discuss the selection in more details since it is abundantly clear from the graph that for a given set of MOSFETs, PCB layout and power train components, the final performance of the board in the form of the power converter's efficiency may vary greatly. On the surface, this may be an unexpected result but closer examination leads to the following:

- The driver output voltage affects the MOSFET On-resistance, RDS(on). Higher gate drive voltage means lower RDS(on)

- Higher output driver voltage means higher capacitive losses $Cgs \times Vg^2 \times fsw$
- The rise and fall times of the gate driver in presence of the MOSFET input capacitance affects the dynamic losses. The faster the rise and fall times the lower the dynamic losses
- The actual rise and fall times when driving a MOSFET is ultimately determined by the driver's source resistance and maximum source and sink currents around the gate threshold. Sink current in particular is important for fast switching off of the large LS MOSFET to avoid any shoot through possibilities

The decision was made to go with driver # 2 in Figure 4. This allows for the highest efficiency i.e. the lowest power dissipation at the highest current. This is critical since all the power dissipation in the form of heat has to be removed from the box by the cooling system. Though the performance at very low current is not the best, the CPU is quite unlikely to be operating at these currents anyway.

Efficiency Measurements

The best way to evaluate the performance of this VRM is to measure the overall power efficiency and compare it to currently available VRMs though operating at a much lower currents. The efficiency was measured under the following conditions:

- The VRM board in still air and without the use of a heatsink
- The VRM was measured in 400 FPM air flow and no heatsink
- The VRM was measured in 400 FPM air flow and heatsink

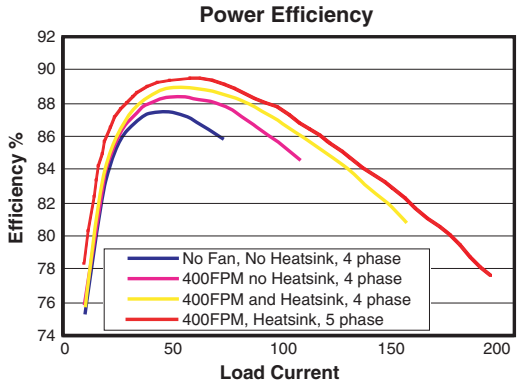

Figure 6. VRM efficiency measurements for 4 and 5 phases

Figure 6 above shows the results of the efficiency measurements. The temperature of the PCB measured at inductor close to the HS MOSFET was not allowed to go higher than 110°C. This is the reason that the 4-phase board could only deliver the full 160 Amps when fitted with the heatsink and placed in a 400 FPM airflow chamber.

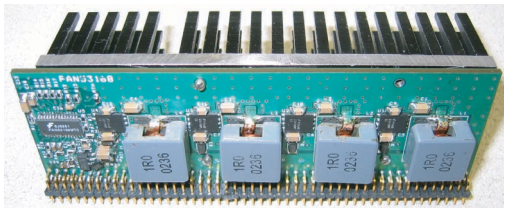

Figure 7. Four phase 160 Amp VRM.

Figure 7 depicts the 4-phase VRM complete and fitted with the heatsink used in the measurements.

Figure 8. Design versatility single, double, four and five phase modules based on the same design

Figure 8 depicts several experimental boards that constitute the background of this paper. On the top a 5 phase 200 Amp module complete with the PWM controller followed on the second row by a 4 phase 160 Amp module and on the third row a 2 phase 80 Amps module flanked by two single phase 40 Amp modules. One can clearly see the flexibility of this approach where a large variety of implementations may be evaluated covering a very wide scope of applications ranging from 40 Amp to 200 Amp or more. The single 40 Amp module offers a very unique approach to solve the problem of transmission of power from the VRM to the CPU. Using a number of these modules allows the motherboard designer the flexibility to place them as close as possible to the CPU while maintaining the freedom of random placement that require very small board space for each i.e. the designer does not need to provide in one area the entire footprint of the 5 phase VRM but rather one module at a time allowing for more efficient space utilization and much shorter transmission path for the current. In Figure 9 towards the center of the board you can observe the set of four power connectors that form a square of about 1.1" x 1.1" that can provide for 4 of these single phase modules and allows the designer to place the PWM controller and its associated components in the center of this square.

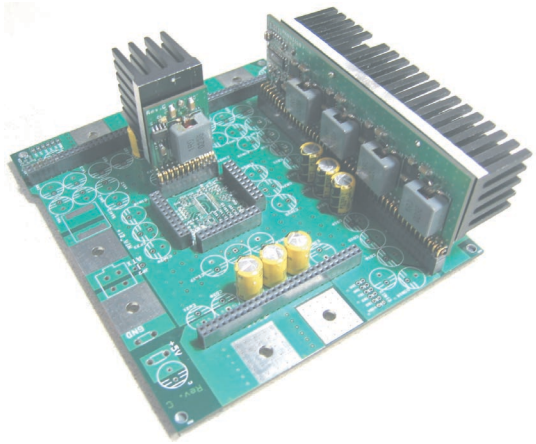

Figure 9. Complete 200 Amp implementation. One 160 Amp 4 phase VRM plus one phase 40 Amp Module

Lessons Learned

- The use of the appropriate MOSFET package is mandatory for a successful design. BGA offered excellent electrical and thermal performance which makes it the right choice for this VRM design.
- The use of airflow to cool down the module is mandatory if we chose to design 30–40 Amps per phase. Figure 6 above shows clearly that 400 FPM air flow without heatsink allows the maximum safe current to go from 75 Amp in still air to 110 Amp while maintaining the maximum PCB temperature to be no more than 110°C, an increase of 47%.
- The PCB should be designed with 6-8 layers at 2 OZ copper each to insure low parasitic resistance.
- Vias play a major role in distributing the switched current right at the MOSFET to several layers which act as parallel conductors reducing both the parasitic resistance and inductance which leads to higher efficiency and lower losses.

Conclusions:

- The industry's current per phase have been hovering around 25-30 Amps. The solution offered here allows for the design of VRMs with up to 40 Amp/phase using one HS and two LS MOSFETs.
- VRMs have been traditionally done on one PCB limiting the flexibility of placement of the power source to the load. We are offering a very flexible multi-sized modules where the designer has the choice of placing different size modules in the best position to minimize power losses and maximize transient response and load line.
- This solution offers one of the largest current density/ phase for the PC market while maintaining safe PCB temperature. The current density is about 50 Amp/inch^2.
- We discussed layout techniques for control and minimization of parasitic resistance and inductance control and excellent dynamic performance.
- Adequate air flow is mandatory for optimum design and performance.

References

[1] Alan Elbanhawy, *Fairchild Semiconductor,* "Effect of Parasitic Inductance on switching performance" *in Proc. PCIM Europe 2003, pp. 251–255*

[2] Alan Elbanhawy, *Fairchild Semiconductor,* "Effect of Parasitic inductance on switching performance of Synchronous Buck Converter" in *Proc. Intel Technology Symposium 2003*

[3] Alan Elbanhawy, *Fairchild Semiconductor,* "Mathematical Treatment for HS MOSFET Turn Off" in *Proc. PEDS 2003*

[4] Alan Elbanhawy, "A quantum Leap in Semiconductor packaging" in Proc. *PCIM China, pp. 60–64*