AND8081/D

Flip Chip CSP Packages

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APPLICATION NOTE

Introduction to Chip Scale Packaging

This application note provides guidelines for the use of Chip Scale Packages related to mounting devices to a PCB. Included is information on PCB layout for Systems Engineers, and manufacturing processes for Manufacturing Process Engineers.

Package Overview

Flip Chip CSP "Package" Overview

Chip Scale packages offered by ON Semiconductor represent the smallest footprint size since the package is the same size as the die. ON Semiconductor offers two types of CSPs, or bumped die – Flip Chip CSP and Standard Bump. This application note covers only the Flip Chip CSPs with larger bumps.

Flip Chip CSP bumped die are created by attaching 300 μm solder spheres to the I/O pads of the active side of the wafer. The I/O layout can either be peripheral or array. No redistribution layer is used.

The 63/37 SnPb solder bumps allow compatibility of the package connections with standard surface mount technology pick and place and reflow processes and standard flip chip mounting systems. The larger solder bumps of the Flip Chip CSP requires no underfill to increase reliability performance.

Devices designed with the smaller standard bumps generally have a peripheral pad layout and a tighter spacing than that of the Flip Chip CSPs. Underfill is recommended to increase board level solder joint reliability.

Package Construction and Process Description

The Flip Chip CSP is a wafer level processing technique. Upon completion of standard wafer processing, a polymeric BCB passivation layer is applied to the wafer, leaving the bonding pads exposed. A sputtered thin film underbump Al/NiV/Cu metallization (UBM) is applied to the device bonding bonds to provide an interface between the die pad metallization and the solder bump. Solder spheres are placed on each exposed pad and reflowed to create an interconnection system ready for board assembly.

Once the bumps are reflowed, wafers are electrically tested, laser marked, sawn into individual die, and packed in tape and reel, bumps down. A typical Flip Chip CSP is represented in Figure 1. Total device thickness will vary, depending on customer requirements.

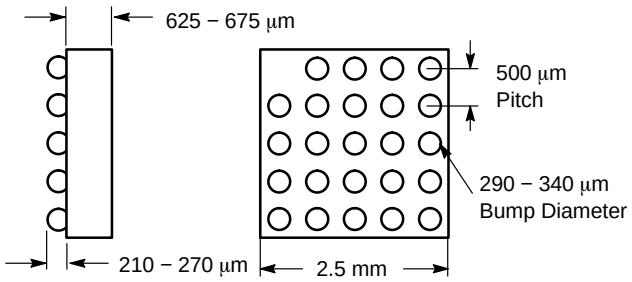

Figure 1. Daisy Chain Flip Chip CSP

Printed Circuit Board Design

Recommended PCB Layout

Two types of land patterns are commonly used for surface mount packages – non−solder mask defined (NSMD) and solder mask defined (SMD), Figure 2. With SMD configured pads, the solder mask covers the outside perimeter of the circular contact pads, thus limiting the solder attach to just the top surface of the exposed pads. With NSMD configured pads, there is a gap between the solder mask and the circular contact pad. NSMD pads are preferred due to better control of the copper etch process as compared with the solder mask etch process in the SMD pad definition. The solder bumps will attach to the NSMD pad wall as well as the pad surface, which provides additional mechanical strength and solder joint fatigue life. SMD pad definition introduces increased levels of stress near the solder mask overlap region which results in solder joint fatigue cracking in extreme temperature cycling conditions. The smaller NSMD pads also provide more room for escape routing on the PCB since they can be smaller in diameter than SMD pads.

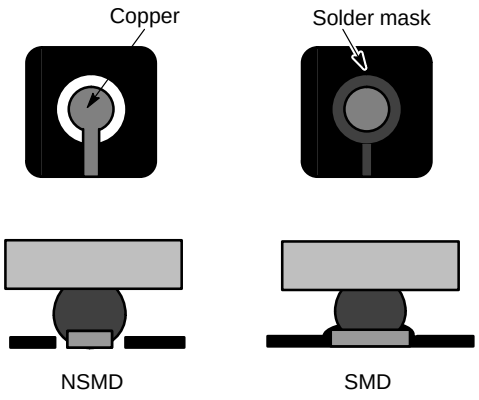

Figure 2. NSMD vs. SMD

A copper layer thickness of less than 1 oz (30 μm) is recommended to maintain a maximum stand−off height and consequently maximum solder joint fatigue life.

Micro−via pads should be NSMD to ensure adequate wetting area of the copper pad.

A summary of recommended design parameters is found in Table 1.

Table 1. PCB Assembly Recommendations

Parameter	500 μm Pitch 300 μm Solder Ball
PCB Pad Size	250 μm $^{+25}_{-0}$
Pad Shape	Round
Pad Type	NSMD
Solder Mask Opening	350 μm ±25
Solder Stencil Thickness	125 μm
Stencil Aperture	250 x 250 μm sq.
Solder Flux Ratio	50/50
Solder Paste Type	No Clean Type 3 or Finer
Trace Finish	OSP Cu
Trace Width	150 μm Max

PCB I/O Contacts Surface Finish Characteristics

Organic solderability preservative (OSP) pad finish is recommended for optimum solder joint reliability. Electroless nickel−immersion gold finish with gold thickness ranging from 0.05 – 0.127 μm may also be used, although solder joint integrity may suffer due to the presence of brittle gold/tin intermetallics. Hot Air Solder Leveled finish (HASL) is not recommended because the process does not give consistent solder volumes on each pad.

Solder Assembly Recommendations

SMT Process Flow

Surface mount assembly operations include printing solder paste onto the PCB.

Solder Paste Characteristics

Type 3 (25 – 45 μm powder), Type 4 (20 – 38 μm powder) or Type 5 (15 – 25 μm powder) ANSI/J−STD−005 compliant solder paste is suggested. No−clean solder paste is recommended. RMA or water soluble (OA) solder paste flux may also be used. Metal load range is from 85 – 90 wt%. Solder flux ratio should be 50/50 by volume.

Solder Stencil and Printing

Stainless steel, brass, or nickel plated stencils with laser cut or metal additive apertures are recommended. Five degree tapered walls are suggested for laser cut stencils to facilitate the release of the paste when the screen is removed from the PCB. Stencil thickness of 0.125 mm with openings approximately the same size as the substrate bond pads are recommended. It is highly recommended that the solder paste height, uniformity, registration and proper placement during the squeegee printing are monitored.

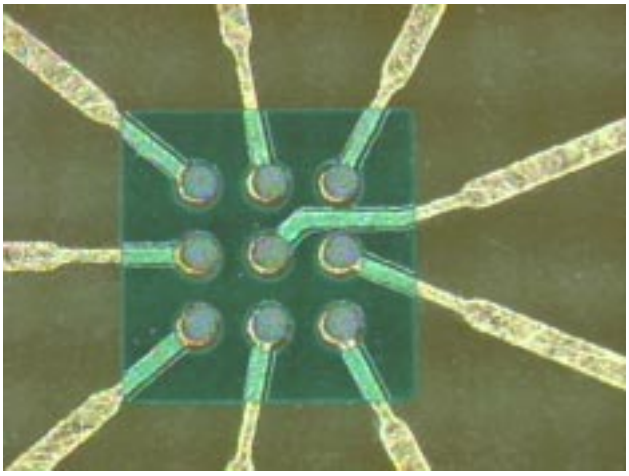

Figure 3. Printed Solder Paste on PCB

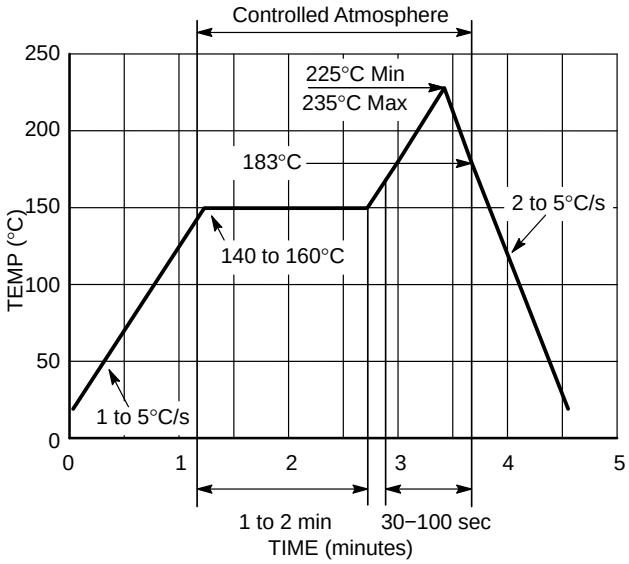

Figure 4. Typical Reflow Profile for Eutectic SnPb Solder

Package Placement

Standard pick and place machines can be used for placing CSPs. Such placement equipment falls into two categories: a vision system to locate the package silhouette commonly known as a chip shooter, or a fine pitch vision system to locate individual bumps. It is preferable to use vision systems employing solder sphere recognition for improved placement accuracy, however throughput is reduced. Little or no force should be exerted on the Flip Chip CSP during placement.

Solder Paste Reflow and Cleaning

When cleaning a No−clean or RMA flux residue, semi−aqueous solvents, saponified water, alcohols and other CFC−free alternatives may be used to sufficiently remove all residue. If cleaning a water soluble flux residue, spray and immersion should be sufficient to remove all ionic contamination and residue.

IR Reflow Profile

A standard surface mount reflow process can be used once the part and solder paste or flux are placed on the PCB. An example of a standard reflow profile is shown in Figure 4. The exact recommended reflow profile is determined by the manufacturer of the paste since the chemistry and viscosity of the flux matrix will vary. These variations will require small changes in the profile in order to achieve an optimized process.

In general, for low temperature eutectic SnPb solder, the temperature of the part should be raised less than or equal to 5°C/sec during the initial stages of the reflow profile. The soak zone then occurs when the part is approximately 150°C and should last 30 to 120 seconds. The temperature is then raised and will be above the liquidus of the solder for 30 to 100 seconds depending on the mass of the board. The peak temperature of the profile should be between 225 and 235°C for 10 seconds or less.

Solder Joint Inspection

The inspection of solder joints is commonly performed with an x−ray inspection system. The x−ray system is used to locate open contacts, shorts between pads, solder voids, and extraneous solder. A cross section of a typical flip chip solder joint is found below in Figure 5.

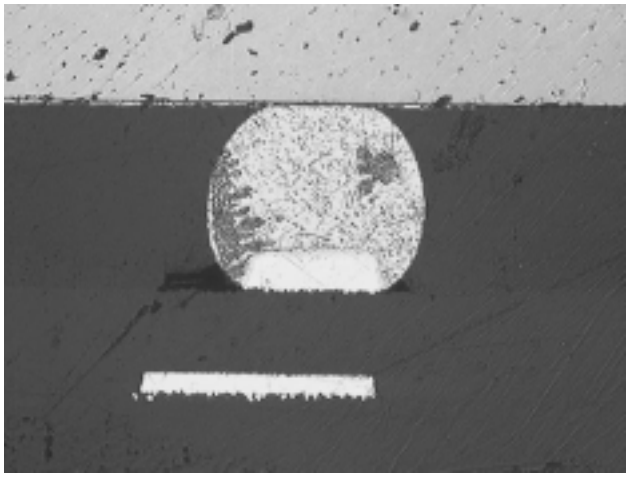

Figure 5. Cross Section of Solder Bump

Underfill

Underfill is not needed for Flip Chip CSP Devices constructed with the larger 300 μm solder spheres. Solder joint reliability tests have shown parts to pass temperature cycling tests without the need for further encapsulation. These devices can, however, withstand the dispense of an underfill as long as the process temperature does not exceed 175°C for up to 5 minutes.

Rework Process

Very similar to that of the rework process for BGAs, the key steps in rework of bumped die product are as follows:

1. CSP removal uses localized heating which duplicates the original reflow profile used for assembly.
2. The reject CSP can be removed once the temperature exceeds the liquidus temperature of the solder.
3. The pads need to be thoroughly cleaned prior to applying flux.
4. A new part is picked up using a vacuum needle pick−up tip and placed onto the board.
5. The replacement part is reflowed to the board using the same convection nozzle and preheat from the bottom, and the original reflow profile.

ON Semiconductor CSP Reliability Test Data

Board Level CSP Package Reliability

ON Semiconductor performed solder joint fatigue testing on Flip Chip CSP test structures per IPC−SM−785 Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments. The test vehicles used were 2.5 x 2.5 mm or 1.5 x 1.5 mm daisy chain die with either a 5 x 5 matrix or a 3 x 3 matrix of solder bumps, respectively, spaced at a pitch of 0.5 mm. These devices were assembled with Type 5 eutectic, SnPb solder paste to .032” thick 4−layer high temperature FR4 test boards, which were designed with 250 μm OSP Cu NSMD pads. Boards were temperature cycled from –40 to 125°C (1 cycle/hr, 15 min ramp, 15 min dwell) and continuously monitored for changes in resistance. The temperature cycling profile is found in Figure 6 below. Table 2 summarizes the daisy chain CSP solder joint reliability test results.

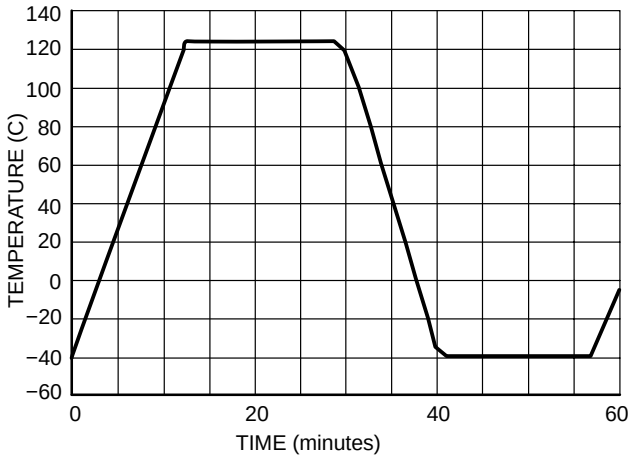

Figure 6. Temperature Cycling Profile for Solder Joint Fatigue Testing

Table 2. ON Semiconductor Flip Chip CSP Solder Joint Reliability Test Results

Flip Chip CSP	Test Condition	Test Board	1210 Cycles	1457 Cycles	1464 Cycles	1643 Cycles
24 bump, 0.32 mm bump diameter	−40 to 125°C, 1 cycle/hr, 15 min ramp, 15 min dwell	OSP Cu pads/flux	0/32	0/32	1/32	3/32
9 bump, 0.32 mm bump diameter	−40 to 125°C, 1 cycle/hr, 15 min ramp, 15 min dwell	NiAu pads/flux	0/32	1/32	1/32	2/32

The test results show that the 1.5 x 1.5 mm CSP devices can pass 1456 temperature cycles, and the 2.5 x 2.5 mm CSP devices can pass 1463 cycles without failure.

Figure 7 is a Weibull plot of the solder joint fatigue data for each of the daisy chain devices.

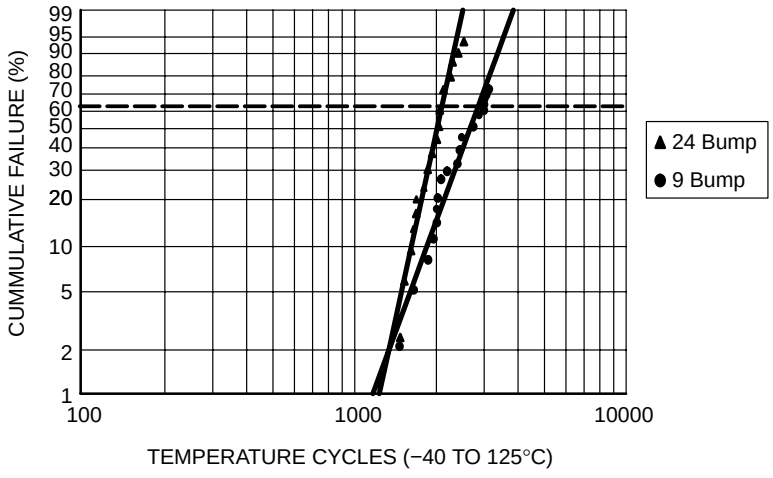

Figure 7. Weibull Plot

Tape and Reel Specifications and Labeling Description

All Flip Chip CSPs are shipped in tape and reel (T & R). CSP T & R requirements are based on the industrial standard EIA−481. The T & R construction is given in Figure 8 below.

Specified tape width: 8 mm

Tape sprocket hole pitch: 4.0 ± 0.1 mm

Compliant to industrial standard EIA−481

The SMD pick and place machines should pick up the component from the point which is located in the center of two adjacent sprocket holes in the feeding direction. This must be taken into account when designing the location of the component in the T & R pocket.

Tape Material:	Small parts other than 0402 (1005 in metric) in 8 mm wide tape: paper (i.e. punched) or embossed (i.e. blister)
Reel Size:	Standard reel diameter is 7 inches (178 mm) for all 8 mm tape.
Reel Material:	Plastic
Device Orientation:	Pin 1 toward sprocket holes.

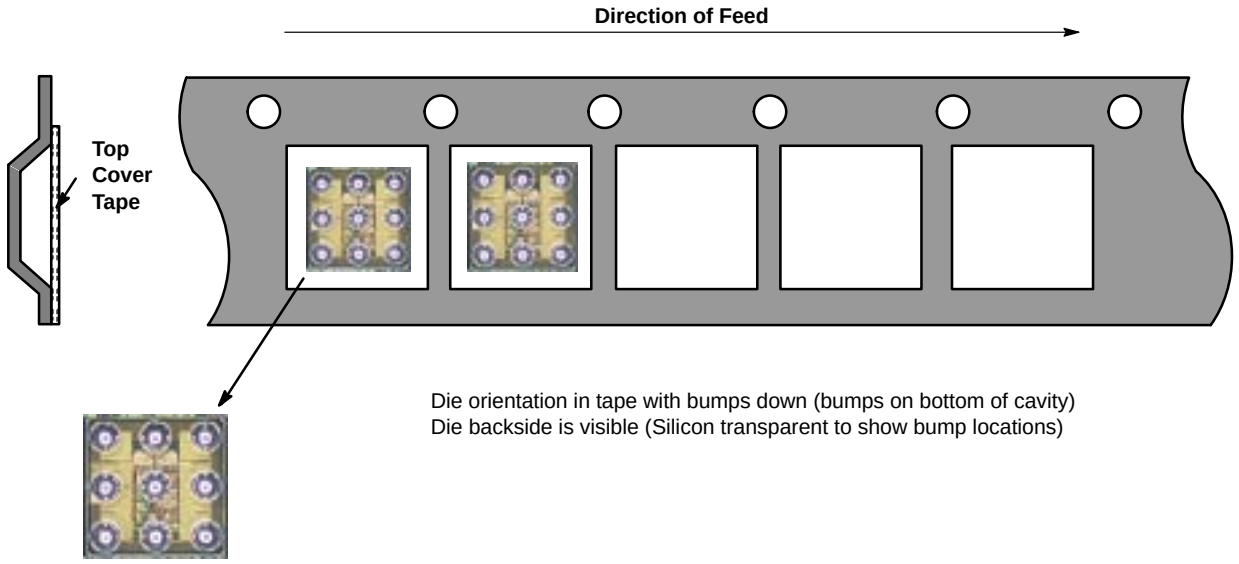

Figure 8. Number of Components per Reel = 3000

The cavity is designed to provide sufficient clearance surrounding the component so that:

1. The part does not protrude beyond either surface of the carrier tape.
2. The part can be removed from the cavity in a vertical direction without mechanical restriction after the top cover tape has been removed.
3. Rotation of the part is limited to 20 degrees maximum.
4. Lateral movement of the part is restricted to 0.05 mm maximum.

Tape with or without parts shall pass around radium R without damage.

Barcode labeling (if required) shall be on the side of the reel opposite the sprocket holes.

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
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