Thyristor Theory and Design Considerations

Handbook

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ON Semiconductor™

ABOUT THYRISTORS

Thyristors can take many forms, but they have certain things in common. All of them are solid state switches which act as open circuits capable of withstanding the rated voltage until triggered. When they are triggered, thyristors become low–impedance current paths and remain in that condition until the current either stops or drops below a minimum value called the holding level. Once a thyristor has been triggered, the trigger current can be removed without turning off the device.

Silicon controlled rectifiers (SCRs) and triacs are both members of the thyristor family. SCRs are unidirectional devices where triacs are bidirectional. An SCR is designed to switch load current in one direction, while a triac is designed to conduct load current in either direction.

Structurally, all thyristors consist of several alternating layers of opposite P and N silicon, with the exact structure varying with the particular kind of device. The load is applied across the multiple junctions and the trigger current is injected at one of them. The trigger current allows the load current to flow through the device, setting up a regenerative action which keeps the current flowing even after the trigger is removed.

These characteristics make thyristors extremely useful in control applications. Compared to a mechanical switch, a thyristor has a very long service life and very fast turn on and turn off times. Because of their fast reaction times, regenerative action and low resistance once triggered, thyristors are useful as power controllers and transient overvoltage protectors, as well as simply turning devices on and off. Thyristors are used in motor controls, incandescent lights, home appliances, cameras, office equipment, programmable logic controls, ground fault interrupters, dimmer switches, power tools, telecommunication equipment, power supplies, timers,

capacitor discharge ignitors, engine ignition systems, and many other kinds of equipment.

Although thyristors of all sorts are generally rugged, there are several points to keep in mind when designing circuits using them. One of the most important is to respect the devices' rated limits on rate of change of voltage and current (dv/dt and di/dt). If these are exceeded, the thyristor may be damaged or destroyed. On the other hand, it is important to provide a trigger pulse large enough and fast enough to turn the gate on quickly and completely. Usually the gate trigger current should be at least 50 percent greater than the maximum rated gate trigger current. Thyristors may be driven in many different ways, including directly from transistors or logic families, power control integrated circuits, by optoisolated triac drivers, programmable unijunction transistors (PUTs) and SIDACs. These and other design considerations are covered in this manual.

Of interest too, is a new line of Thyristor Surge Suppressors in the surface mount SMB package covering surge currents of 50, 80 and 100 amps, with breakover voltages from 77 to 400 volts. NP Series Thyristor Surge Protector Devices (TSPD) protect telecommunication circuits such as central office, access, and customer premises equipment from overvoltage conditions. These are bidirectional devices so they are able to have functionality of 2 devices in one package, saving valuable space on board layout. These devices will act as a crowbar when overvoltage occurs and will divert the energy away from circuit or device that is being protected. Use of the NP Series in equipment will help meet various regulatory requirements including: GR–1089–CORE, IEC 61000–4–5, ITU K.20/21/45, IEC 60950, TIA–968–A, FCC Part 68, EN 60950, UL 1950. See ON Semiconductor application note AND8022/D for additional information.
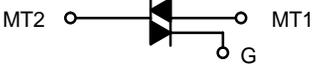
CHAPTER 1
Theory and Applications

Sections 1 thru 9

SECTION 1
SYMBOLS AND TERMINOLOGY

SYMBOLS

The following are the most commonly used schematic symbols for Thyristors:

Name of Device	Symbol
Silicon Controlled Rectifier (SCR)	A o——▶◀— o K, G
Triac	MT2 o——◀▶— o MT1, G
Thyristor Surge Protective Devices & Sidac	MT1 o——N— o MT2
Programmable Unijunction Transistor (PUT)	A o——(▶)— o K, G

THYRISTOR TERMINOLOGY (The following terms are used in SCR and TRIAC specifications.)

Symbol	Terminology	Definition
di/dt	CRITICAL RATE OF RISE OF ON–STATE CURRENT	The maximum rate of change of current the device will withstand after switching from an off–state to an on–state when using recommended gate drive. In other words, the maximum value of the rate of rise of on–state current which a Triac or SCR can withstand without damage.
(di/dt)c	RATE OF CHANGE OF COMMUTATING CURRENT (Triacs)	Is the ability of a Triac to turn off itself when it is driving an inductive load and a resultant commutating dv/dt condition associated with the nature of the load.
dv/dt	CRITICAL RATE OF RISE OF OFF–STATE VOLTAGE	Also, commonly called static dv/dt. It is the minimum value of the rate of rise of forward voltage which will cause switching from the off–state to the on–state with gate open.
I_{DRM}	PEAK REPETITIVE BLOCKING CURRENT	The maximum value of current which will flow at V_{DRM} and specified temperature when the SCR or Triac is in the off–state. Frequently referred to as leakage current in the forward off–state blocking mode.
I_{GM}	FORWARD PEAK GATE CURRENT (SCR) PEAK GATE CURRENT (Triac)	The maximum peak gate current which may be safely applied to the device to cause conduction.
I_{GT}	GATE TRIGGER CURRENT	The maximum value of gate current required to switch the device from the off–state to the on–state under specified conditions. The designer should consider the maximum gate trigger current as the minimum trigger current value that must be applied to the device in order to assure its proper triggering.
I_H	HOLDING CURRENT	The minimum current that must be flowing (MT1 & MT2; cathode and anode) to keep the device in a regenerative on–state condition. Below this holding current value the device will return to a blocking state, off condition.
I_L	LATCHING CURRENT	The minimum current that must be applied through the main terminals of a Triac (or cathode and anode of an SCR) in order to turn from the off–state to the on–state while its I_{GT} is being correctly applied.
I_{RRM}	PEAK REPETITIVE REVERSE BLOCKING CURRENT	The maximum value of current which will flow at V_{RRM} and specified temperature when the SCR or Triac is in the reverse mode, off–state. Frequently referred to as leakage current in the reverse off–state blocking mode.
$I_{T(AV)}$	AVERAGE ON–STATE CURRENT (SCR)	The maximum average on–state current the device may safely conduct under stated conditions without incurring damage.

THYRISTOR TERMINOLOGY (The following terms are used in SCR and TRIAC specifications.)

Symbol	Terminology	Definition
I_{TM}	PEAK REPETITIVE ON−STATE CURRENT (SCR) (also called PEAK DISCHARGE CURRENT)	Peak discharge current capability of a thyristor useful when connected to discharge peak current usually from a capacitor. This is a rarely specified parameter. (See MCR68 and MCR69 data sheets, for examples where it is specified.)
$I_{T(RMS)}$	ON−STATE RMS CURRENT	The maximum value of on−state rms current that can be applied to the device through the two main terminals of a Triac (or cathode and anode if an SCR) on a continuous basis.
I_{TSM}	PEAK NON−REPETITIVE SURGE CURRENT	The maximum allowable non−repetitive surge current the device will withstand at a specified pulse width, usually specified at 60 Hz.
I^2t	CIRCUIT FUSING CONSIDERATIONS (Current squared time)	The maximum forward non−repetitive overcurrent capability that the device is able to handle without damage. Usually specified for one−half cycle of 60 Hz operation.
$P_{G(AV)}$	FORWARD AVERAGE GATE POWER (SCR) AVERAGE GATE POWER (Triac)	The maximum allowable value of gate power, averaged over a full cycle, that may be dissipated between the gate and cathode terminal (SCR), or main terminal 1 if a Triac.
P_{GM}	FORWARD PEAK GATE POWER (SCR) PEAK GATE POWER (Triac)	The maximum instantaneous value of gate power dissipation between gate and cathode terminal for an SCR or between gate and a main terminal MT1 for a Triac, for a short pulse duration.
$R_{\theta CA}$	THERMAL RESISTANCE, CASE−TO−AMBIENT	The thermal resistance (steady−state) from the device case to the ambient.
$R_{\theta JA}$	THERMAL RESISTANCE, JUNCTION−TO−AMBIENT	The thermal resistance (steady−state) from the semiconductor junction(s) to the ambient.
$R_{\theta JC}$	THERMAL RESISTANCE, JUNCTION−TO−CASE	The thermal resistance (steady−state) from the semiconductor junction(s) to a stated location on the case.
$R_{\theta JM}$	THERMAL RESISTANCE, JUNCTION−TO−MOUNTING SURFACE	The thermal resistance (steady−state) from the semiconductor junction(s) to a stated location on the mounting surface.
T_A	AMBIENT TEMPERATURE	The air temperature measured below a device in an environment of substantially uniform temperature, cooled only by natural air currents and not materially affected by radiant and reflective surfaces.
T_C	CASE TEMPERATURE	The temperature of the device case under specified conditions.

THYRISTOR TERMINOLOGY (The following terms are used in SCR and TRIAC specifications.)

Symbol	Terminology	Definition
t_{gt}	TURN−ON TIME (SCR) (Also called Gate Controlled Turn−on Time)	The time interval between a specified point at the beginning of the gate pulse and the instant when the device voltage has dropped to a specified low value during the switching of an SCR from the off state to the on state by a gate pulse.
T_J	OPERATING JUNCTION TEMPERATURE	The junction temperature of the device at the die level as a result of ambient and load conditions. In other words, the junction temperature must be operated within this range to prevent permanent damage.
t_q	TURN−OFF TIME (SCR)	The time interval between the instant when the SCR current has decreased to zero after external switching of the SCR voltage circuit and the instant when the thyristor is capable of supporting a specified wave form without turning on.
T_{stg}	STORAGE TEMPERATURE	The minimum and maximum temperature at which the device may be stored without harm with no electrical connections.
V_{DRM}	PEAK REPETITIVE OFF−STATE FORWARD VOLTAGE	The maximum allowed value of repetitive forward voltage which may be applied and not switch the SCR or Triac on or do damage to the thyristor.
V_{GD}	GATE NON−TRIGGER VOLTAGE	At the maximum rated operational temperature, and at a specified main terminal off−state voltage applied, this parameter specifies the maximum DC voltage that can be applied to the gate and still not switch the device from off−state to and on−state.
V_{GM}	FORWARD PEAK GATE VOLTAGE (SCR) PEAK GATE VOLTAGE (Triac)	The maximum peak value of voltage allowed between the gate and cathode terminals with these terminals forward biased for an SCR. For a Triac, a bias condition between the gate and main terminal MT1.
V_{GT}	GATE TRIGGER VOLTAGE	The gate dc voltage required to produce the gate trigger current.
$V_{(Iso)}$	RMS ISOLATION VOLTAGE	The dielectric withstanding voltage capability of a thyristor between the active portion of the device and the heat sink. Relative humidity is a specified condition.
V_{RGM}	PEAK REVERSE GATE BLOCKING VOLTAGE (SCR)	The maximum allowable peak reverse voltage applied to the gate on an SCR. Measured at a specified I_{GR} which is the reverse gate current.
V_{RRM}	PEAK REPETITIVE REVERSE OFF−STATE VOLTAGE	The maximum allowed value of repetitive reverse voltage which may be applied and not switch the SCR or Triac on or do damage to the thyristor.

THYRISTOR TERMINOLOGY (The following terms are used in SCR and TRIAC specifications.)

Symbol	Terminology	Definition
V_{TM}	PEAK FORWARD ON−STATE VOLTAGE (SCR) PEAK ON−STATE VOLTAGE (Triac)	The maximum voltage drop across the main terminals at stated conditions when the devices are in the on−state (i.e., when the thyristor is in conduction). To prevent heating of the junction, the V_{TM} is measured at a short pulse width and low duty cycle.
$Z_{\theta JA(t)}$	TRANSIENT THERMAL IMPEDANCE, JUNCTION−TO−AMBIENT	The transient thermal impedance from the semiconductor junction(s) to the ambient.
$Z_{\theta JC(t)}$	TRANSIENT THERMAL IMPEDANCE, JUNCTION−TO−CASE	The transient thermal impedance from the semiconductor junction(s) to a stated location on the case.

Thyristor Surge Protector Devices (TSPD) and Sidac Terminology*

Symbol	Terminology	Definition
I_{BO}	BREAKOVER CURRENT	The breakover current I_{BO} is the corresponding parameter defining the V_{BO} condition, that is, where breakdown is occurring.
I_{D1}, I_{D2}	OFF−STATE CURRENT (TSPD)	The maximum value of current which will flow at specific voltages (V_{D1} and V_{D2}) when the TSPD is clearly in the off−state. Frequently referred to as leakage current.
I_{pps}	PULSE SURGE SHORT CIRCUIT CURRENT NON−REPETITIVE (TSPD)	The maximum pulse surge capability of the TSPD (non−repetitive) under double exponential decay waveform conditions.
P_{pk}	INSTANTANEOUS PEAK POWER DISSIPATION (TSPD)	Defines the instantaneous peak power dissipation when the TSPD (thyristor surge suppressor devices) are subjected to specified surge current conditions.
R_s	SWITCHING RESISTANCE (Sidac)	The effective switching resistance usually under a sinusoidal, 60 Hz condition.
V_{BO}	BREAKOVER VOLTAGE	It is the peak voltage point where the device switches to an on−state condition.
$V_{(BR)}$	BREAKDOWN VOLTAGE (TSPD)	V_{BR} is the voltage where breakdown occurs. Usually given as a typical value for reference to the Design Engineer.
V_{DM}	OFF−STATE VOLTAGE (TSPD)	The maximum off−state voltage prior to the TSPD going into a characteristic similar to an avalanche mode. When a transient or line signal exceeds the V_{DM}, the device begins to avalanche, then immediately begins to conduct.
V_T	ON−STATE VOLTAGE (TSPD)	The maximum voltage drop across the terminals at stated conditions when the TSPD devices are in the on−state (i.e., conduction). To prevent overheating, V_T is measured at a short pulse width and a low duty cycle.

* All of the definitions on this page are for ones that were not already previously defined under Triac and SCR terminology.

SECTION 2
THEORY OF THYRISTOR OPERATION

Edited and Updated

To successfully apply thyristors, an understanding of their characteristics, ratings, and limitations is imperative. In this chapter, significant thyristor characteristics, the basis of their ratings, and their relationship to circuit design are discussed.

Several different kinds of thyristors are shown in Table 2.1. Silicon Controlled Rectifiers (SCRs) are the most widely used as power control elements; triacs are quite popular in lower current (under 40 A) ac power applications. Diacs, SUSs and SBSs are most commonly used as gate trigger devices for the power control elements.

Table 2.1. Thyristor Types

*JEDEC Titles	Popular Names, Types
Reverse Blocking Diode Thyristor	† Four Layer Diode, Silicon Unilateral Switch (SUS)
Reverse Blocking Triode Thyristor	Silicon Controlled Rectifier (SCR)
Reverse Conducting Diode Thyristor	† Reverse Conducting Four Layer Diode
Reverse Conducting Triode Thyristor	Reverse Conducting SCR
Bidirectional Triode Thyristor	Triac

* JEDEC is an acronym for the Joint Electron Device Engineering Councils, an industry standardization activity co−sponsored by the Electronic Industries Association (EIA) and the National Electrical Manufacturers Association (NEMA).

† Not generally available.

Before considering thyristor characteristics in detail, a brief review of their operation based upon the common two−transistor analogy of an SCR is in order.

BASIC BEHAVIOR

The bistable action of thyristors is readily explained by analysis of the structure of an SCR. This analysis is essentially the same for any operating quadrant of triac because a triac may be considered as two parallel SCRs oriented in opposite directions. Figure 2.1(a) shows the schematic symbol for an SCR, and Figure 2.1(b) shows the P−N−P−N structure the symbol represents. In the two−transistor model for the SCR shown in Figure 2.1(c), the interconnections of the two transistors are such that regenerative action occurs. Observe that if current is injected into any leg of the model, the gain of the transistors (if sufficiently high) causes this current to be amplified in another leg. In order for regeneration to occur, it is necessary for the sum of the common base current gains (α) of the two transistors to exceed unity. Therefore, because the junction leakage currents are relatively small and current gain is designed to be low at the leakage current level, the PNPN device remains off unless external current is applied. When sufficient trigger current is applied (to the gate, for example, in the case of an SCR) to raise the loop gain to unity, regeneration occurs and the on−state principal current is limited primarily by external circuit impedance. If the initiating trigger current is removed, the thyristor remains in the on state, providing the current level is high enough to meet the unity gain criteria. This critical current is called latching current.

In order to turn off a thyristor, some change in current must occur to reduce the loop gain below unity. From the model, it appears that shorting the gate to cathode would accomplish this. However in an actual SCR structure, the gate area is only a fraction of the cathode area and very little current is diverted by the short. In practice, the principal current must be reduced below a certain level, called holding current, before gain falls below unity and turn−off may commence.

In fabricating practical SCRs and Triacs, a "shorted emitter" design is generally used in which, schematically, a resistor is added from gate to cathode or gate to MT1. Because current is diverted from the N−base through the resistor, the gate trigger current, latching current and holding current all increase. One of the principal reasons for the shunt resistance is to improve dynamic performance at high temperatures. Without the shunt, leakage current on most high current thyristors could initiate turn−on at high temperatures.

Sensitive gate thyristors employ a high resistance shunt or none at all; consequently, their characteristics can be altered dramatically by use of an external resistance. An external resistance has a minor effect on most shorted emitter designs.
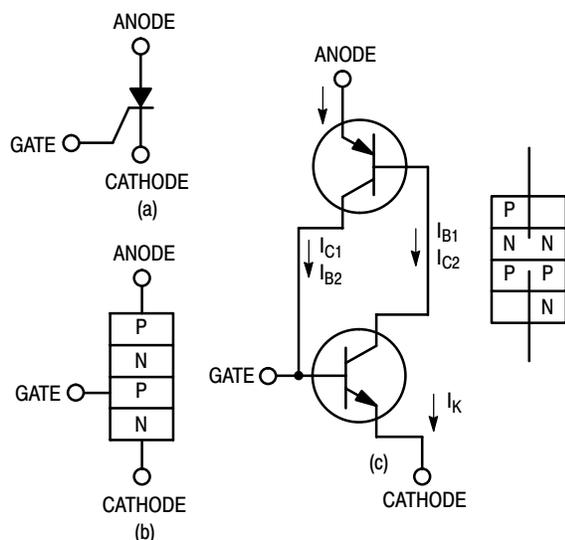
Figure 2.1. Two−transistor analogy of an SCR: (a) schematic symbol of SCR; (b) P−N−P−N structure represented by schematic symbol; (c) two−transistor model of SCR.

Junction temperature is the primary variable affecting thyristor characteristics. Increased temperatures make the thyristor easier to turn on and keep on. Consequently, circuit conditions which determine turn−on must be designed to operate at the lowest anticipated junction temperatures, while circuit conditions which are to turn off the thyristor or prevent false triggering must be designed to operate at the maximum junction temperature.

Thyristor specifications are usually written with case temperatures specified and with electrical conditions such that the power dissipation is low enough that the junction temperature essentially equals the case temperature. It is incumbent upon the user to properly account for changes in characteristics caused by the circuit operating conditions different from the test conditions.

TRIGGERING CHARACTERISTICS

Turn−on of a thyristor requires injection of current to raise the loop gain to unity. The current can take the form of current applied to the gate, an anode current resulting

from leakage, or avalanche breakdown of a blocking junction. As a result, the breakover voltage of a thyristor can be varied or controlled by injection of a current at the gate terminal. Figure 2.2 shows the interaction of gate current and voltage for an SCR.
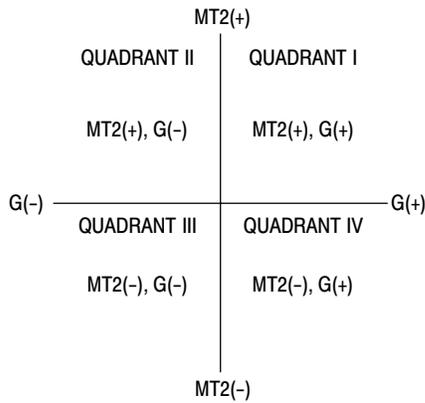
When the gate current I_g is zero, the applied voltage must reach the breakover voltage of the SCR before switching occurs. As the value of gate current is increased, however, the ability of a thyristor to support applied voltage is reduced and there is a certain value of gate current at which the behavior of the thyristor closely resembles that of a rectifier. Because thyristor turn−on, as a result of exceeding the breakover voltage, can produce high instantaneous power dissipation non−uniformly distributed over the die area during the switching transition, extreme temperatures resulting in die failure may occur unless the magnitude and rate of rise of principal current (di/dt) is restricted to tolerable levels. For normal operation, therefore, SCRs and triacs are operated at applied voltages lower than the breakover voltage, and are made to switch to the on state by gate signals high enough to assure complete turn−on independent of the applied voltage. On the other hand, diacs and other thyristor trigger devices are designed to be triggered by anode breakover. Nevertheless they also have di/dt and peak current limits which must be adhered to.
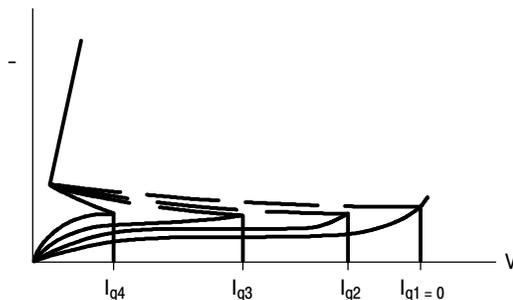
Figure 2.2. Thyristor Characteristics Illustrating Breakover as a Function of Gate Current

A triac works the same general way for both positive and negative voltage. However since a triac can be switched on by either polarity of the gate signal regardless of the voltage polarity across the main terminals, the situation is somewhat more complex than for an SCR.

The various combinations of gate and main terminal polarities are shown in Figure 2.3. The relative sensitivity depends on the physical structure of a particular triac, but as a rule, sensitivity is highest in quadrant I and quadrant IV is generally considerably less sensitive than the others.

MT2(+)

QUADRANT II	QUADRANT I
MT2(+), G(−)	MT2(+), G(+)

G(−) ——————————————— G(+)

QUADRANT III	QUADRANT IV
MT2(−), G(−)	MT2(−), G(+)

MT2(−)

Figure 2.3. Quadrant Definitions for a Triac

Gate sensitivity of a triac as a function of temperature is shown in Figure 2.4.
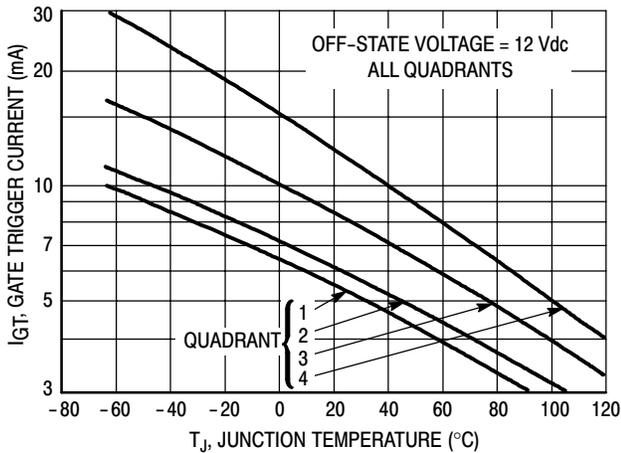
Figure 2.4. Typical Triac Triggering Sensitivity in the Four Trigger Quadrants

Since both the junction leakage currents and the current gain of the "transistor" elements increase with temperature, the magnitude of the required gate trigger current decreases as temperature increases. The gate — which can be regarded as a diode — exhibits a decreasing voltage drop as temperature increases. Thus it is important that the gate trigger circuit be designed to deliver sufficient current to the gate at the lowest anticipated temperature.

It is also advisable to observe the maximum gate current, as well as peak and average power dissipation ratings. Also in the negative direction, the maximum gate ratings should be observed. Both positive and negative gate limits are often given on the data sheets and they may indicate that protective devices such as voltage clamps and current limiters may be required in some applications. It is generally inadvisable to dissipate power in the reverse direction.

Although the criteria for turn−on have been described in terms of current, it is more basic to consider the thyristor as being charge controlled. Accordingly, as the duration of the trigger pulse is reduced, its amplitude must be correspondingly increased. Figure 2.5 shows typical behavior at various pulse widths and temperatures.

The gate pulse width required to trigger a thyristor also depends upon the time required for the anode current to reach the latching value. It may be necessary to maintain a gate signal throughout the conduction period in applications where the load is highly inductive or where the anode current may swing below the holding value within the conduction period.

When triggering an SCR with a dc current, excess leakage in the reverse direction normally occurs if the trigger signal is maintained during the reverse blocking phase of the anode voltage. This happens because the SCR operates like a remote base transistor having a gain which is generally about 0.5. When high gate drive currents are used, substantial dissipation could occur in the SCR or a significant current could flow in the load; therefore, some means usually must be provided to remove the gate signal during the reverse blocking phase.
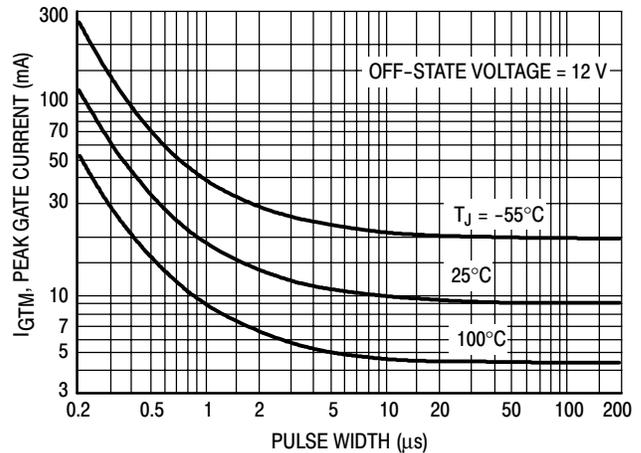
Figure 2.5. Typical Behavior of Gate Trigger Current as Pulse Width and Temperature Are Varied

LATCH AND HOLD CHARACTERISTICS

In order for the thyristor to remain in the on state when the trigger signal is removed, it is necessary to have sufficient principal current flowing to raise the loop gain to unity. The principal current level required is the latching current, I_L. Although triacs show some dependency on the gate current in quadrant II, the latching current is primarily affected by the temperature on shorted emitter structures.

In order to allow turn off, the principal current must be reduced below the level of the latching current. The current level where turn off occurs is called the holding current, I_H. Like the latching current, the holding current is affected by temperature and also depends on the gate impedance.

Reverse voltage on the gate of an SCR markedly increases the latch and hold levels. Forward bias on thyristor gates may significantly lower the values shown in the data sheets since those values are normally given with the gate open. Failure to take this into account can cause latch or hold problems when thyristors are being driven from transistors whose saturation voltages are a few tenths of a volt.

Thyristors made with shorted emitter gates are obviously not as sensitive to the gate circuit conditions as devices which have no built−in shunt.

SWITCHING CHARACTERISTICS

When triacs or SCRs are triggered by a gate signal, the turn−on time consists of two stages: a delay time, t_d, and a rise time, t_r, as shown in Figure 2.6. The total gate controlled turn−on time, t_{gt}, is usually defined as the time interval between the 50 percent point of the leading edge of the gate trigger voltage and 90 percent point of the principal current. The rise time t_r is the time interval required for the principal current to rise from 10 to 90 percent of its maximum value. A resistive load is usually specified.
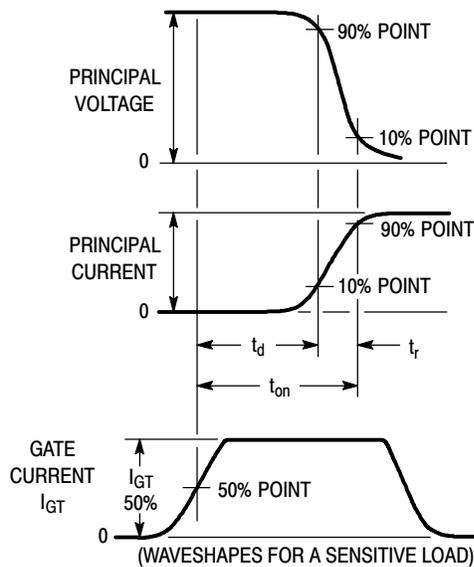
Figure 2.6. Waveshapes Illustrating Thyristor Turn−On Time For A Resistive Load

Delay time decreases slightly as the peak off−state voltage increases. It is primarily related to the magnitude of the gate−trigger current and shows a relationship which is roughly inversely proportional.

The rise time is influenced primarily by the off−state voltage, as high voltage causes an increase in regenerative gain. Of major importance in the rise time interval is the relationship between principal voltage and current flow through the thyristor di/dt. During this time the dynamic voltage drop is high and the current density due to the possible rapid rate of change can produce localized hot spots in the die. This may permanently degrade the blocking characteristics. Therefore, it is important that power dissipation during turn−on be restricted to safe levels.

Turn−off time is a property associated only with SCRs and other unidirectional devices. (In triacs of bidirectional devices a reverse voltage cannot be used to provide circuit−commutated turn−off voltage because a reverse voltage applied to one half of the structure would be a forward−bias voltage to the other half.) For turn−off times in SCRs, the recovery period consists of two stages, a reverse recovery time and a gate or forward blocking recovery time, as shown in Figure 2.7.

When the forward current of an SCR is reduced to zero at the end of a conduction period, application of reverse voltage between the anode and cathode terminals causes reverse current flow in the SCR. The current persists until the time that the reverse current decreases to the leakage level. Reverse recovery time (t_{rr}) is usually measured from the point where the principal current changes polarity to a specified point on the reverse current waveform as indicated in Figure 2.7. During this period the anode and cathode junctions are being swept free of charge so that they may support reverse voltage. A second recovery period, called the gate recovery time, t_{gr}, must elapse for the charge stored in the forward−blocking junction to recombine so that forward−blocking voltage can be reapplied and successfully blocked by the SCR. The gate recovery time of an SCR is usually much longer than the reverse recovery time. The total time from the instant reverse recovery current begins to flow to the start of the forward−blocking voltage is referred to as circuit−commutated turn−off time t_q.

Turn−off time depends upon a number of circuit conditions including on−state current prior to turn−off, rate of change of current during the forward−to−reverse transition, reverse−blocking voltage, rate of change of reapplied forward voltage, the gate bias, and junction temperature. Increasing junction temperature and on−state current both increase turn−off time and have a more

significant effect than any of the other factors. Negative gate bias will decrease the turn−off time.
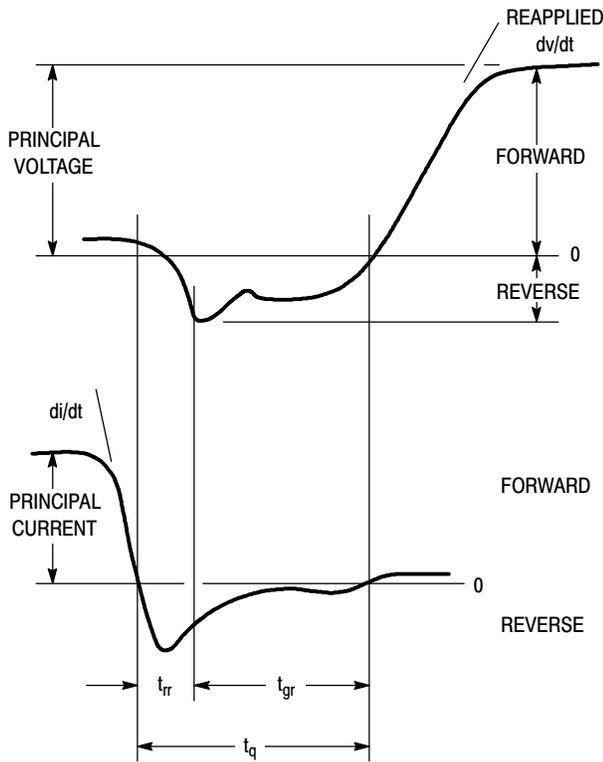
Figure 2.7. Waveshapes Illustrating Thyristor Turn−Off Time

For applications in which an SCR is used to control ac power, during the entire negative half of the sine wave a reverse voltage is applied. Turn off is easily accomplished for most devices at frequencies up to a few kilohertz. For applications in which the SCR is used to control the output of a full−wave rectifier bridge, however, there is no reverse voltage available for turn−off, and complete turn−off can be accomplished only if the bridge output is reduced close to zero such that the principal current is reduced to a value lower than the device holding current for a sufficiently long time. Turn−off problems may occur even at a frequency of 60 Hz particularly if an inductive load is being controlled.

In triacs, rapid application of a reverse polarity voltage does not cause turn−off because the main blocking junctions are common to both halves of the device. When the first triac structure (SCR−1) is in the conducting state, a quantity of charge accumulates in the N−type region as a result of the principal current flow. As the principal current crosses the zero reference point, a reverse current is established as a result of the charge remaining in the N−type region, which is common to both halves of the device. Consequently, the reverse recovery current

becomes a forward current to the second half of the triac. The current resulting from stored charge causes the second half of the triac to go into the conducting state in the absence of a gate signal. Once current conduction has been established by application of a gate signal, therefore, complete loss in power control can occur as a result of interaction within the N−type base region of the triac unless sufficient time elapses or the rate of application of the reverse polarity voltage is slow enough to allow nearly all the charge to recombine in the common N−type region. Therefore, triacs are generally limited to low−frequency −60 Hz applications. Turn−off or commutation of triacs is more severe with inductive loads than with resistive loads because of the phase lag between voltage and current associated with inductive loads. Figure 2.8 shows the waveforms for an inductive load with lagging current power factor. At the time the current reaches zero crossover (Point A), the half of the triac in conduction begins to commutate when the principal current falls below the holding current. At the instant the conducting half of the triac turns off, an applied voltage opposite the current polarity is applied across the triac terminals (Point B). Because this voltage is a forward bias to the second half of the triac, the suddenly reapplied voltage in conjunction with the remaining stored charge in the high−voltage junction reduces the over−all device capability to support voltage. The result is a loss of power control to the load, and the device remains in the conducting state in absence of a gate signal. The measure of triac turn−off ability is the rate of rise of the opposite polarity voltage it can handle without remaining on. It is called commutating dv/dt (dv/dt[c]). Circuit conditions and temperature affect dv/dt(c) in a manner similar to the way t_q is affected in an SCR.

It is imperative that some means be provided to restrict the rate of rise of reapplied voltage to a value which will permit triac turn−off under the conditions of inductive load. A commonly accepted method for keeping the commutating dv/dt within tolerable levels is to use an RC snubber network in parallel with the main terminals of the triac. Because the rate of rise of applied voltage at the triac terminals is a function of the load impedance and the RC snubber network, the circuit can be evaluated under worst−case conditions of operating case temperature and maximum principal current. The values of resistance and capacitance in the snubber area then adjusted so that the rate of rise of commutating dv/dt stress is within the specified minimum limit under any of the conditions mentioned above. The value of snubber resistance should be high enough to limit the snubber capacitance discharge currents during turn−on and dampen the LC oscillation during commutation. The combination of snubber values having highest resistance and lowest capacitance that provides satisfactory operation is generally preferred.
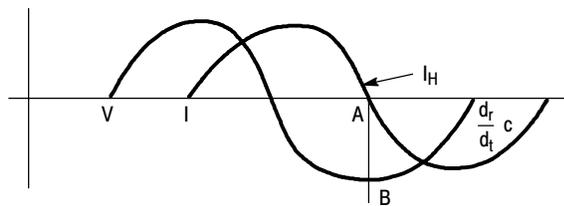
Figure 2.8. Inductive Load Waveforms

FALSE TRIGGERING

Circuit conditions can cause thyristors to turn on in the absence of the trigger signal. False triggering may result from:

1) A high rate of rise of anode voltage, (the dv/dt effect).

2) Transient voltages causing anode breakover.

3) Spurious gate signals.

Static dv/dt effect: When a source voltage is suddenly applied to a thyristor which is in the off state, it may switch from the off state to the conducting state. If the thyristor is controlling alternating voltage, false turn-on resulting from a transient imposed voltage is limited to no more than one-half cycle of the applied voltage because turn-off occurs during the zero current crossing. However, if the principal voltage is dc voltage, the transient may cause switching to the on state and turn-off could then be achieved only by a circuit interruption.

The switching from the off state caused by a rapid rate of rise of anode voltage is the result of the internal capacitance of the thyristor. A voltage wavefront impressed across the terminals of a thyristor causes a capacitance-charging current to flow through the device which is a function of the rate of rise of applied off-state voltage ($i = C$ dv/dt). If the rate of rise of voltage exceeds a critical value, the capacitance charging current exceeds the gate triggering current and causes device turn-on. Operation at elevated junction temperatures reduces the thyristor ability to support a steep rising voltage dv/dt because of increased sensitivity.

dv/dt ability can be improved quite markedly in sensitive gate devices and to some extent in shorted emitter designs by a resistance from gate to cathode (or MT1) however reverse bias voltage is even more effective in an SCR. More commonly, a snubber network is used to keep the dv/dt within the limits of the thyristor when the gate is open.

TRANSIENT VOLTAGES: — Voltage transients which occur in electrical systems as a result of disturbance on the ac line caused by various sources such as energizing transformers, load switching, solenoid closure, contractors and the like may generate voltages which are above the ratings of thyristors. Thyristors, in general, switch from the off state to the on state whenever the breakover voltage of the device is exceeded, and energy is then transferred to the load. However, unless a thyristor is specified for use in a breakover mode, care should be exercised to ensure that breakover does not occur, as some devices may incur surface damage with a resultant degradation of blocking characteristics. It is good practice when thyristors are exposed to a heavy transient environment to provide some form of transient suppression.

For applications in which low-energy, long-duration transients may be encountered, it is advisable to use thyristors that have voltage ratings greater than the highest voltage transient expected in the system. The use of voltage clipping cells (MOV or Zener) is also an effective method to hold transient below thyristor ratings. The use of an RC "snubber" circuit is effective in reducing the effects of the high-energy short-duration transients more frequently encountered. The snubber is commonly required to prevent the static dv/dt limits from being exceeded, and often may be satisfactory in limiting the amplitude of the voltage transients as well.

For all applications, the dv/dt limits may not be exceeded. This is the minimum value of the rate of rise off-state voltage applied immediately to the MT1–MT2 terminals after the principal current of the opposing polarity has decreased to zero.

SPURIOUS GATE SIGNALS: In noisy electrical environments, it is possible for enough energy to cause gate triggering to be coupled into the gate wiring by stray capacitance or electromagnetic induction. It is therefore advisable to keep the gate lead short and have the common return directly to the cathode or MT1. In extreme cases, shielded wire may be required. Another aid commonly used is to connect a capacitance on the order of 0.01 to 0.1 µF across the gate and cathode terminals. This has the added advantage of increasing the thyristor dv/dt capability, since it forms a capacitance divider with the anode to gate capacitance. The gate capacitor also reduces the rate of application of gate trigger current which may cause di/dt failures if a high inrush load is present.

THYRISTOR RATINGS

To insure long life and proper operation, it is important that operating conditions be restrained from exceeding thyristor ratings. The most important and fundamental ratings are temperature and voltage which are interrelated to some extent. The voltage ratings are applicable only up to the maximum temperature ratings of a particular part number. The temperature rating may be chosen by the manufacturer to insure satisfactory voltage ratings, switching speeds, or dv/dt ability.

OPERATING CURRENT RATINGS

Current ratings are not independently established as a rule. The values are chosen such that at a practical case temperature the power dissipation will not cause the junction temperature rating to be exceeded.

Various manufacturers may chose different criteria to establish ratings. At ON Semiconductors, use is made of the thermal response of the semiconductor and worst case values of on−state voltage and thermal resistance, to guarantee the junction temperature is at or below its rated value. Values shown on data sheets consequently differ somewhat from those computed from the standard formula:

$$T_C(max) \quad = T \text{ (rated)} - R_{\theta JC} \times P_{D(AV)}$$

where

T_C (max)	= Maximum allowable case temperature
T (rated)	= Rated junction temperature or maximum rated case temperature with zero principal current and rated ac blocking voltage applied.
$R_{\theta JC}$	= Junction to case thermal resistance
$P_{D(AV)}$	= Average power dissipation

The above formula is generally suitable for estimating case temperature in situations not covered by data sheet information. Worst case values should be used for thermal resistance and power dissipation.

OVERLOAD CURRENT RATINGS

Overload current ratings may be divided into two types: non−repetitive and repetitive.

Non−repetitive overloads are those which are not a part of the normal application of the device. Examples of such overloads are faults in the equipment in which the devices are used and accidental shorting of the load. Non−repetitive overload ratings permit the device to exceed its maximum operating junction temperature for short periods of time because this overload rating applies following any rated load condition. In the case of a reverse blocking thyristor or SCR, the device must block rated voltage in the reverse direction during the current overload. However, no type of thyristor is required to block off−stage voltage at any time during or immediately following the overload. Thus, in the case of a triac, the device need not block in either direction during or immediately following the overload. Usually only approximately one hundred such current overloads are permitted over the life of the device. These non−repetitive overload ratings just described may be divided into two types: multicycle (which include single cycle) and subcycle. For an SCR, the multicycle overload current rating, or surge current rating as it is commonly called, is generally presented as a curve giving the maximum peak values of half sine wave on−state current as a function of overload duration measured in number of cycles for a 60 Hz frequency.

For a triac, the current waveform used in the rating is a full sine wave. Multicycle surge curves are used to select proper circuit breakers and series line impedances to prevent damage to the thyristor in the event of an equipment fault.

The subcycle overload or subcycle surge rating curve is so called because the time duration of the rating is usually from about one to eight milliseconds which is less than the time of one cycle of a 60 Hz power source. Overload peak current is often given in curve form as a function of overload duration. This rating also applies following any rated load condition and neither off−state nor reverse blocking capability is required on the part of the thyristor immediately following the overload current. The subcycle surge current rating may be used to select the proper current−limiting fuse for protection of the thyristor in the event of an equipment fault. Since this use of the rating is so common, manufacturers simply publish the i^2t rating in place of the subcycle current overload curve because fuses are commonly rated in terms of i^2t. The i^2t rating can be approximated from the single cycle surge rating (I_{TSM}) by using:

$$i^2t = I^2{}_{TSM} \times t/2$$

where the time t is the time base of the overload, i.e., 8.33 ms for a 60 Hz frequency.

Repetitive overloads are those which are an intended part of the application such as a motor drive application. Since this type of overload may occur a large number of times during the life of the thyristor, its rated maximum operating junction temperature must not be exceeded during the overload if long thyristor life is required. Since this type of overload may have a complex current waveform and duty−cycle, a current rating analysis involving the use of the transient thermal impedance characteristics is often the only practical approach. In this type of analysis, the thyristor junction−to−case transient thermal impedance characteristic is added to the user's heat dissipator transient thermal impedance characteristic. Then by the superposition of power waveforms in conjunction with the composite thermal impedance curve, the overload current rating can be obtained. The exact calculation procedure is found in the power semiconductor literature.

THEORY OF SCR POWER CONTROL

The most common form of SCR power control is phase control. In this mode of operation, the SCR is held in an off condition for a portion of the positive half cycle and then is triggered into an on condition at a time in the half cycle determined by the control circuitry (in which the circuit current is limited only by the load — the entire line voltage except for a nominal one volt drop across the SCR is applied to the load).

One SCR alone can control only one half cycle of the waveform. For full wave ac control, two SCRs are connected in inverse parallel (the anode of each connected to the cathode of the other, see Figure 2.9a). For full wave dc control, two methods are possible. Two SCRs may be used in a bridge rectifier (see Figure 2.9b) or one SCR may be placed in series with a diode bridge (see Figure 2.9c).

Figure 2.10 shows the voltage waveform along with some common terms used in describing SCR operation. Delay angle is the time, measured in electrical degrees, during which the SCR is blocking the line voltage. The period during which the SCR is on is called the conduction angle.

It is important to note that the SCR is a voltage controlling device. The load and power source determine the circuit current.

Now we arrive at a problem. Different loads respond to different characteristics of the ac waveform. Some loads are sensitive to peak voltage, some to average voltage and some to rms voltage. Figures 2.11(b) and 2.12(b) show the various characteristic voltages plotted against the conduction angle for half wave and full wave circuits. These voltages have been normalized to the rms of the applied voltage. To determine the actual peak, average or rms voltage for any conduction angle, we simply multiply the normalized voltage by the rms value of the applied line voltage. (These normalized curves also apply to current in a resistive circuit.) Since the greatest majority of circuits are either 115 or 230 volt power, the curves have been redrawn for these voltages in Figures 2.11(a) and 2.12(a).

A relative power curve has been added to Figure 2.12 for constant impedance loads such as heaters. (Incandescent lamps and motors do not follow this curve precisely since their relative impedance changes with applied voltage.) To use the curves, we find the full wave rated power of the load, then multiply by the fraction associated with the phase angle in question. For example, a 180° conduction angle in a half wave circuit provides 0.5 x full wave full−conduction power.

An interesting point is illustrated by the power curves. A conduction angle of 30° provides only three per cent of full power in a full wave circuit, and a conduction angle of 150° provides 97 per cent of full power. Thus, the control circuit can provide 94 per cent of full power control with a pulse phase variation of only 120°. Thus, it becomes pointless in many cases to try to obtain conduction angles less than 30° or greater than 150°.

CONTROL CHARACTERISTICS

The simplest and most common control circuit for phase control is a relaxation oscillator. This circuit is shown diagrammatically as it would be used with an SCR in Figure 2.13. The capacitor is charged through the resistor from a voltage or current source until the breakover voltage of the trigger device is reached. At that time, the trigger device changes to its on state, and the capacitor is discharged through the gate of the SCR. Turn−on of the SCR is thus accomplished with a short, high current pulse. Commonly used trigger devices are programmable unijunction transistors, silicon bilateral switches, SIDACs, optically coupled thyristors, and power control integrated circuits. Phase control can be obtained by varying the RC time constant of a charging circuit so that trigger device turn−on occurs at varying phase angles within the controlled half cycle.

If the relaxation oscillator is to be operated from a pure dc source, the capacitor voltage−time characteristic is shown in Figure 2.14. This shows the capacitor voltage as it rises all the way to the supply voltage through several time constants. Figure 2.14(b) shows the charge characteristic in the first time constant greatly expanded. It is this portion of the capacitor charge characteristic which is most often used in SCR and Triac control circuits.

Generally, a design starting point is selection of a capacitance value which will reliably trigger the thyristor when the capacitor is discharged. Gate characteristics and ratings, trigger device properties, and the load impedance play a part in the selection. Since not all of the important parameters for this selection are completely specified, experimental determination is often the best method.

Low−current loads and strongly inductive circuits sometimes cause triggering difficulty because the gate current pulse goes away before the principal thyristor current achieves the latching value. A series gate resistor can be used to introduce a RC discharge time constant in the gate circuit and lengthen trigger pulse duration allowing more time for the main terminal current to rise to the latching value. Small thyristors will require a series gate resistance to avoid exceeding the gate ratings. The discharge time constant of a snubber, if used, can also aid latching. The duration of these capacitor discharge duration currents can be estimated by

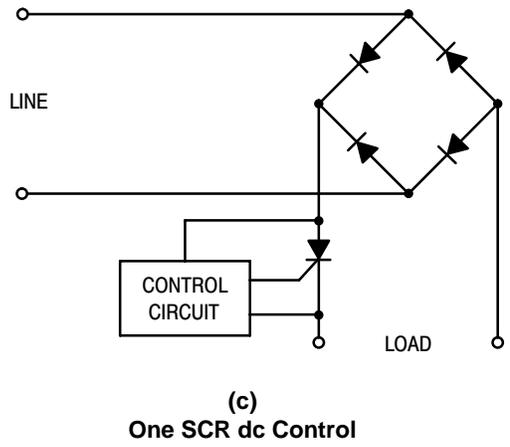$t_{w10} = 2.3$ RC where t_{w10} = time for current to decay to 10% of the peak.
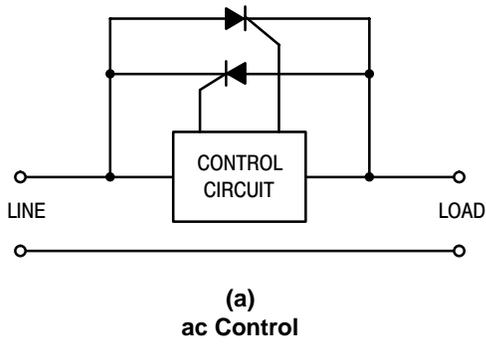
(a)
ac Control

(c)
One SCR dc Control

**Figure 2.9. SCR Connections For Various Methods
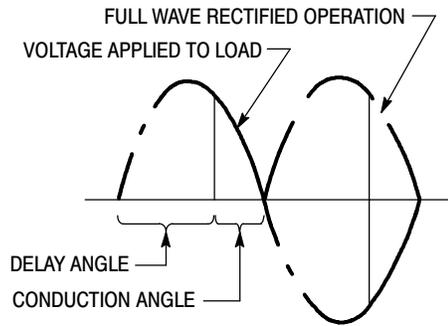Of Phase Control**
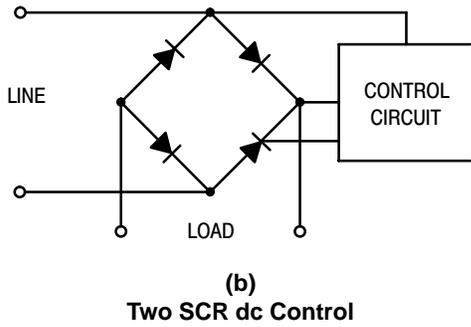

(b)
Two SCR dc Control
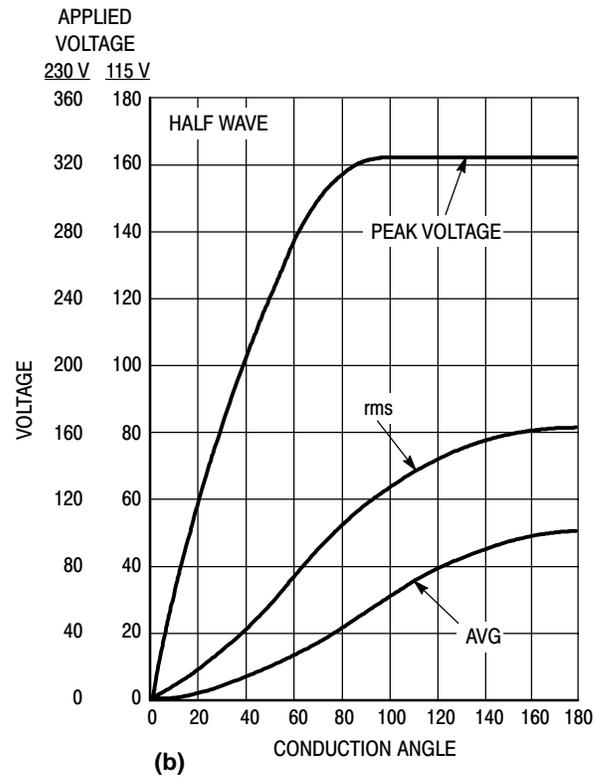

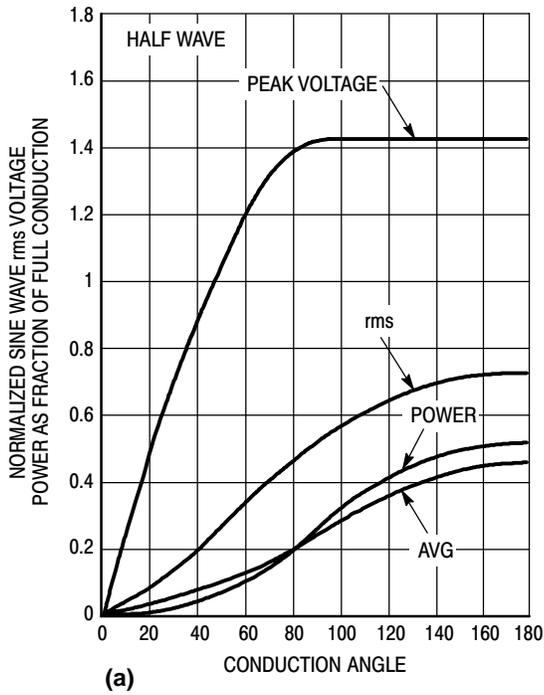**Figure 2.10. Sine Wave Showing Principles
Of Phase Control**

Figure 2.11. Half−Wave Characteristics Of Thyristor Power Control
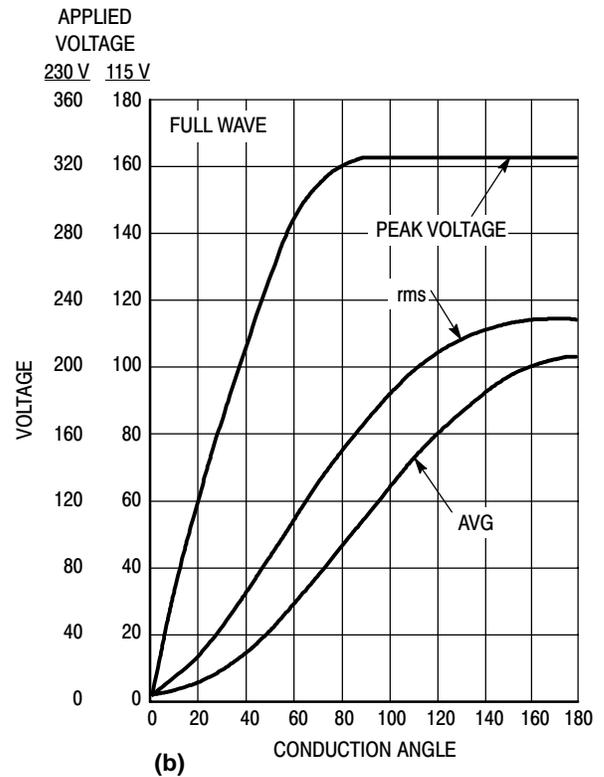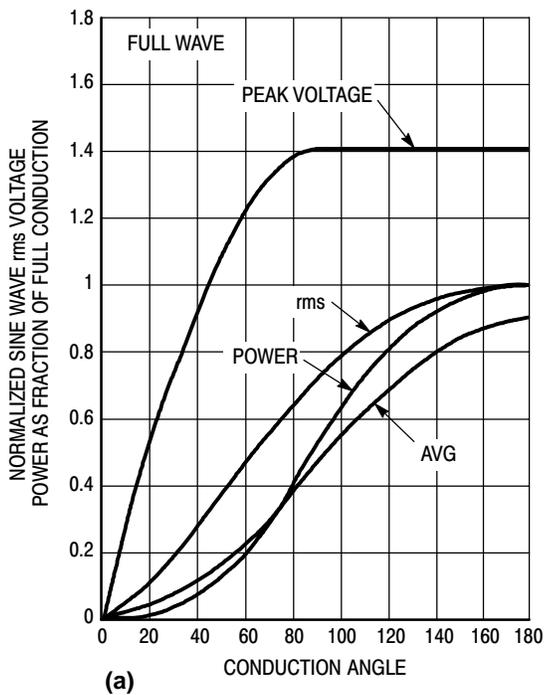

Figure 2.12. Full−Wave Characteristics Of Thyristor Power Control

In many of the recently proposed circuits for low cost operation, the timing capacitor of the relaxation oscillator is charged through a rectifier and resistor using the ac power line as a source. Calculations of charging time with this circuit become exceedingly difficult, although they are still necessary for circuit design. The curves of Figure 2.14 simplify the design immensely. These curves show the voltage–time characteristic of the capacitor charged from one half cycle of a sine wave. Voltage is normalized to the rms value of the sine wave for convenience of use. The parameter of the curves is a new term, the ratio of the RC time constant to the period of one half cycle, and is denoted by the Greek letter τ. It may most easily be calculated from the equation

$$\tau = 2RCf. \quad \text{Where:} \quad \begin{array}{l} R = \text{resistance in Ohms} \\ C = \text{capacitance in Farads} \\ f = \text{frequency in Hertz.} \end{array}$$
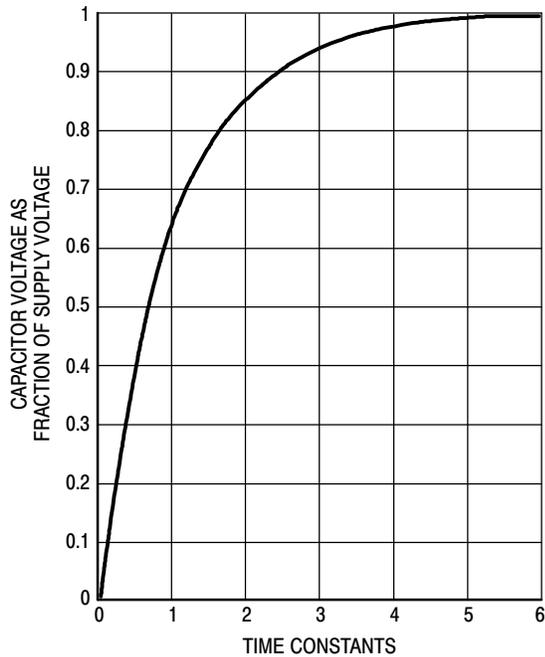

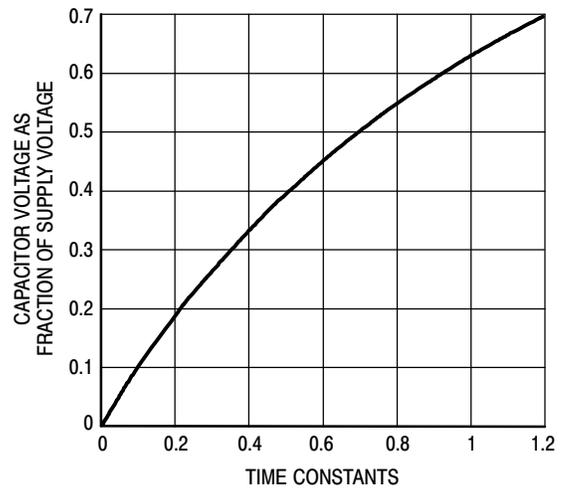**Figure 2.13(a). Capacitor Charging From dc Source**

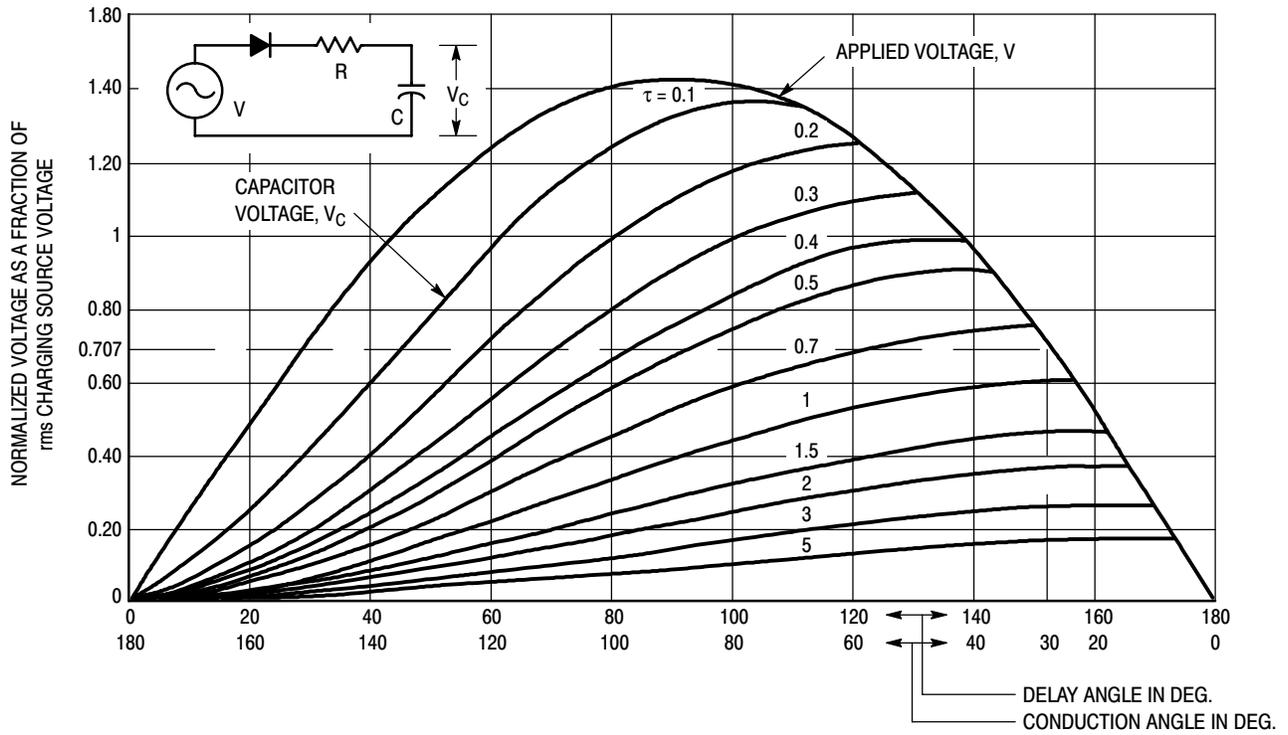**Figure 2.13(b). Expanded Scale**
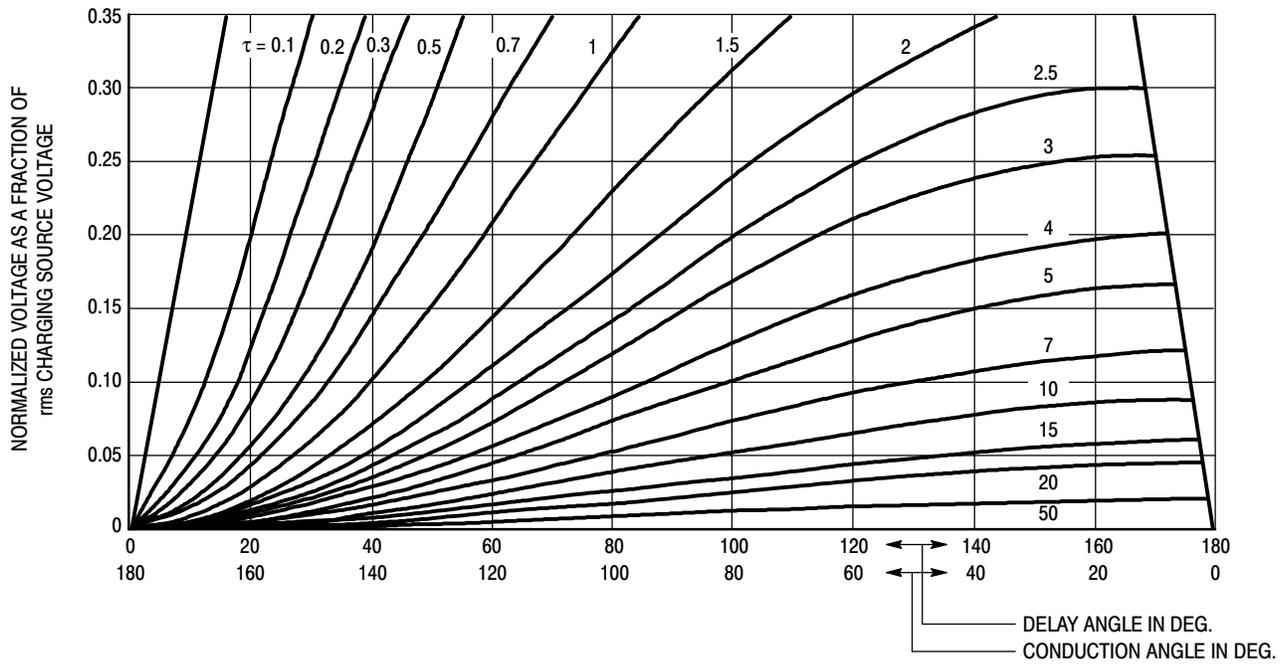
Figure 2.14(a). Capacitor Voltage When Charged

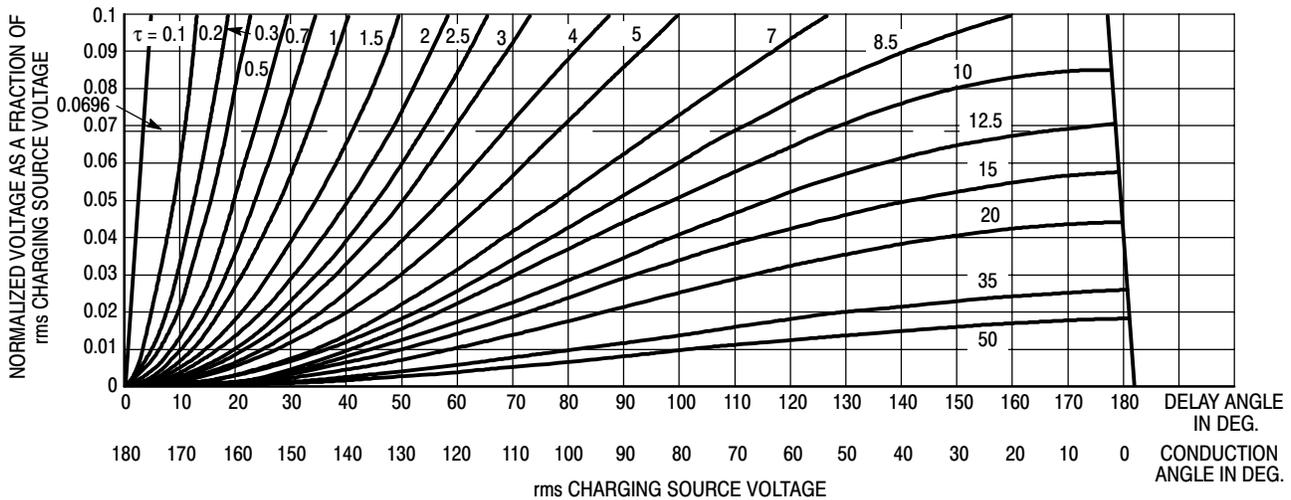Figure 2.14(b). Expansion of Figure 2.15(a).

Figure 2.14(c). Expansion of Figure 2.14(b)

To use the curves when starting the capacitor charge from zero each half cycle, a line is drawn horizontally across the curves at the relative voltage level of the trigger breakdown compared to the rms sine wave voltage. The τ is determined for maximum and minimum conduction angles and the limits of R may be found from the equation for τ.

An example will again clarify the picture. Consider the same problem as the previous example, except that the capacitor charging source is the 115 Vac, 60 Hz power line.

The ratio of the trigger diode breakover voltage to the RMS charging voltage is then

$$8/115 = 69.6 \times 10^{-3}.$$

A line drawn at 0.0696 on the ordinate of Figure 2.14(c) shows that for a conduction angle of 30°, τ = 12, and for a conduction angle of 150°, τ = 0.8. Therefore, since R = τ/(2CF)

$$R_{max} = \frac{12}{2(1.0 \times 10^{-6})60} \ 100 \text{ k ohms,}$$

$$R_{min} = \frac{0.8}{2(1 \times 10^{-6})60} \ 6667 \text{ ohms.}$$

These values would require a potentiometer of 100 k in series with a 6.2 k minimum fixed resistance.

The timing resistor must be capable of supplying the highest switching current allowed by the SBS specification at the switching voltage.

When the conduction angle is less than 90°, triggering takes place along the back of the power line sine wave and maximum firing current thru the SBS is at the start of SBS breakdown. If this current does not equal or exceed "ls" the SBS will fail to trigger and phase control will be lost. This

can be prevented by selecting a lower value resistor and larger capacitor. The available current can be determined from Figure 2.14(a). The vertical line drawn from the conduction angle of 30° intersects the applied voltage curve at 0.707. The instantaneous current at breakover is then

$$I = (0.707 \times 115^{-8})/110 \text{ k} = 733 \text{ μA.}$$

When the conduction angle is greater than 90°, triggering takes place before the peak of the sine wave. If the current thru the SBS does not exceed the switching current at the moment of breakover, triggering may still take place but not at the predicted time because of the additional delay for the rising line voltage to drive the SBS current up to the switching level. Usually long conduction angles are associated with low value timing resistors making this problem less likely. The SBS current at the moment of breakover can be determined by the same method described for the trailing edge.

It is advisable to use a shunt gate–cathode resistor across sensitive gate SCR's to provide a path for leakage currents and to insure that firing of the SCR causes turn–on of the trigger device and discharge of the gate circuit capacitor.

TRIAC THEORY

The triac is a three–terminal ac semiconductor switch which is triggered into conduction when a low–energy signal is applied to its gate. Unlike the silicon controlled rectifier or SCR, the triac will conduct current in either direction when turned on. The triac also differs from the SCR in that either a positive or negative gate signal will trigger the triac into conduction. The triac may be thought of as two complementary SCRs in parallel.

The triac offers the circuit designer an economical and versatile means of accurately controlling ac power. It has several advantages over conventional mechanical switches. Since the triac has a positive "on" and a zero current "off" characteristic, it does not suffer from the contact bounce or arcing inherent in mechanical switches. The switching action of the triac is very fast compared to conventional relays, giving more accurate control. A triac can be triggered by dc, ac, rectified ac or pulses. Because of the low energy required for triggering a triac, the control circuit can use any of many low–cost solid–state devices such as transistors, bilateral switches, sensitive–gate SCRs and triacs, optically coupled drivers and integrated circuits.

CHARACTERISTICS OF THE TRIAC

Figure 2.15(a) shows the triac symbol and its relationship to a typical package. Since the triac is a bilateral device, the terms "anode" and "cathode" used for unilateral devices have no meaning. Therefore, the terminals are simply designated by MT1, MT2, and G, where MT1 and MT2 are the current–carrying terminals, and G, is the gate terminal used for triggering the triac. To avoid confusion, it has become standard practice to specify all currents and voltages using MT1 as the reference point.

The basic structure of a triac is shown in Figure 2.15(b). This drawing shows why the symbol adopted for the triac consists of two complementary SCRs with a common gate. The triac is a five–layer device with the region between MT1 and MT2 being P–N–P–N switch (SCR) in parallel with a N–P–N–P switch (complementary SCR). Also, the structure gives some insight into the triac's ability to be triggered with either a positive or negative gate signal. The region between MT1 and G consists of two complementary diodes. A positive or negative gate signal will forward–bias one of these diodes causing the same transistor action found in the SCR. This action breaks down the blocking junction regardless of the polarity of MT1. Current flow between MT2 and MT1 then causes the device to provide gate current internally. It will remain on until this current flow is interrupted.

The voltage–current characteristic of the triac is shown in Figure 2.16 where, as previously stated, MT1 is used as the reference point. The first quadrant, Q–I, is the region where MT2 is positive with respect to MT1 and quadrant III is the opposite case. Several of the terms used in characterizing the triac are shown on the figure. V_{DRM} is the breakover voltage of the device and is the highest voltage the triac may be allowed to block in either direction. If this voltage is exceeded, even transiently, the triac may go into conduction without a gate signal. Although the triac is not damaged by this action if the current is limited, this situation should be avoided because control of the triac is lost. A triac for a particular application should have V_{DRM} at least as high as the peak of the ac waveform to be applied so reliable control can be maintained. The holding current (I_H) is the minimum value of current necessary to maintain conduction. When the current goes below I_H, the triac ceases to conduct and reverse to the blocking state. I_{DRM} is the leakage current of the triac with V_{DRM} applied from MT2 to MT1 and is several orders of magnitude smaller than the current rating of the device. The figure shows the characteristic of the triac without a gate signal applied but it should be noted that the triac can be triggered into the on state at any value of voltage up to V_{DRM} by the application of a gate signal. This important characteristic makes the triac very useful.

Since the triac will conduct in either direction and can be triggered with either a positive or negative gate signal there are four possible triggering modes (Figure 2.3):

Quadrant I; MT2(+), G(+), positive voltage and positive gate current. Quadrant II; MT2(+), G(−), positive voltage and negative gate current. Quadrant III; MT2(−), G(−), negative voltage and negative gate current. Quadrant IV; MT2(−), G(+), negative voltage and positive gate current.

Present triacs are most sensitive in quadrants I and III, slightly less so in quadrant II, and much less sensitive in quadrant IV. Therefore it is not recommended to use quadrant IV unless special circumstances dictate it.

An important fact to remember is that since a triac can conduct current in both directions, it has only a brief interval during which the sine wave current is passing through zero to recover and revert to its blocking state. For this reason, reliable operation of present triacs is limited to 60 Hz line frequency and lower frequencies.

For inductive loads, the phase–shift between the current and voltage means that at the time the current falls below I_H and the triac ceases to conduct, there exists a certain voltage which must appear across the triac. If this voltage appears too rapidly, the triac will resume conduction and control is lost. In order to achieve control with certain inductive loads, the rate of rise in voltage (dv/dt) must be limited by a series RC network across the triac. The capacitor will then limit the dv/dt across the triac. The resistor is necessary to limit the surge of current from the capacitor when the triac fires, and to damp the ringing of the capacitance with the load inductance.
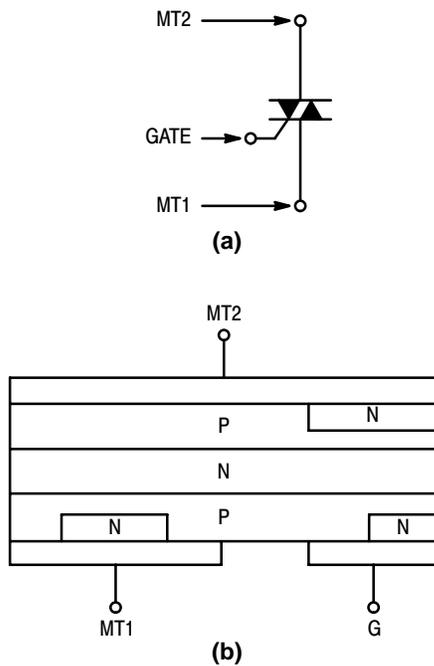
(a)

(b)

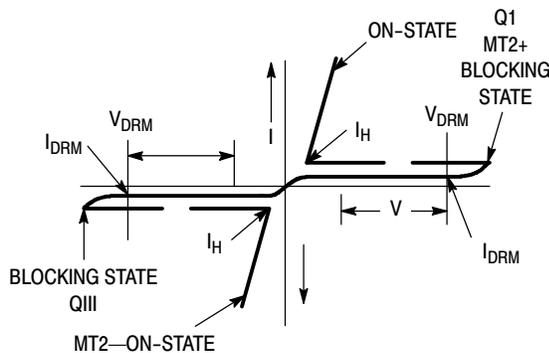**Figure 2.15. Triac Structure and Symbol**

Figure 2.16. Triac Voltage–Current Characteristic

METHODS OF CONTROL

AC SWITCH

A useful application of triac is as a direct replacement for an ac mechanical relay. In this application, the triac furnishes on–off control and the power–regulating ability of the triac is not utilized. The control circuitry for this application is usually very simple, consisting of a source for the gate signal and some type of small current switch, either mechanical or electrical. The gate signal can be obtained from a separate source or directly from the line voltage at terminal MT2 of the triac.

PHASE CONTROL

An effective and widely–used method of controlling the average power to a load through the triac is by phase control. Phase control is a method of utilizing the triac to apply the ac supply to the load for a controlled fraction of each cycle. In this mode of operation, the triac is held in an off or open condition for a portion of each positive and negative cycle, and then is triggered into an on condition at a time in the half cycle determined by the control circuitry. In the on condition, the circuit current is limited only by the load — i.e., the entire line voltage (less the forward drop of the triac) is applied to the load.

Figure 2.17 shows the voltage waveform along with some common terms used in describing triac operation. Delay angle is the angle, measured in electrical degrees, during which the triac is blocking the line voltage. The period during which the triac is on is called the conduction angle.

It is important to note that the triac is either off (blocking voltage) or fully on (conducting). When it is in the on condition, the circuit current is determined only by the load and the power source.

As one might expect, in spite of its usefulness, phase control is not without disadvantages. The main disadvantage of using phase control in triac applications is the generation of electro–magnetic interference (EMI). Each time the triac is fired the load current rises from zero to the load–limited current value in a very short time. The resulting di/dt generates a wide spectrum of noise which may interfere with the operation of nearby electronic equipment unless proper filtering is used.

ZERO POINT SWITCHING

In addition to filtering, EMI can be minimized by zero–point switching, which is often preferable. Zero–point switching is a technique whereby the control element (in this case the triac) is gated on at the instant the sine wave voltage goes through zero. This reduces, or eliminates, turn–on transients and the EMI. Power to the load is controlled by providing bursts of complete sine waves to the load as shown in Figure 2.18. Modulation can be on a random basis with an on–off control, or a proportioning basis with the proper type of proportional control.

In order for zero–point switching to be effective, it must indeed be *zero point* switching. If a triac is turned on with as little as 10 volts across it into a load of a few–hundred watts, sufficient EMI will result to nullify the advantages of adopting zero–point switching in the first place.

BASIC TRIAC AC SWITCHES

Figure 2.19 shows methods of using the triac as an on–off switch. These circuits are useful in applications where simplicity and reliability are important. As previously stated, there is no arcing with the triac, which can be very important in some applications. The circuits are for resistive loads as shown and require the addition of a dv/dt network across the triac for inductive loads.

Figure 2.19(a) shows low−voltage control of the triac. When switch S1 is closed, gate current is supplied to the triac from the 10 volt battery. In order to reduce surge current failures during turn on (t_{on}), this current should be 5 to 10 times the maximum gate current (I_{GT}) required to trigger the triac.

The triac turns on and remains on until S1 is opened. This circuit switches at zero current except for initial turn on. S1 can be a very−low−current switch because it carries only the triac gate current.

Figure 2.19(b) shows a triac switch with the same characteristics as the circuit in Figure 2.19(a) except the need for a battery has been eliminated. The gate signal is obtained from the voltage at MT2 of the triac prior to turn on.

The circuit shown in Figure 2.19(c) is a modification of Figure 2.19(b). When switch S1 is in position one, the triac receives no gate current and is non−conducting. With S1 in position two, circuit operation is the same as that for Figure 2.19(b). In position three, the triac receives gate current only on positive half cycles. Therefore, the triac conducts only on positive half cycles and the power to the load is half wave.

Figure 2.19(d) shows ac control of the triac. The pulse can be transformer coupled to isolate power and control circuits. Peak current should be 10 times $I_{GT(max)}$ and the RC time constant should be 5 times $t_{on(max)}$. A high frequency pulse (1 to 5 kHz) is often used to obtain zero point switching.
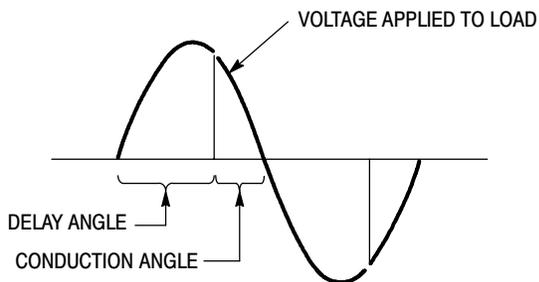

Figure 2.17. Sine Wave Showing Principles of Phase Control

ZERO POINT SWITCHING TECHNIQUES

Zero−point switches are highly desirable in many applications because they do not generate electro−magnetic interference (EMI). A zero−point switch controls sine−wave power in such a way that either complete cycles or half cycles of the power supply voltage are applied to the load as shown in Figure 2.20. This type of switching is primarily used to control power to resistive loads such as heaters. It can also be used for controlling the speed of motors if the duty cycle is modulated by having short bursts of power applied to the load and the load characteristic is primarily inertial rather than frictional. Modulation can be on a random basis with an on−off control, or on a proportioning basis with the proper type of proportioning control.

In order for zero−point switching to be effective, it must be true zero−point switching. If an SCR is turned on with an anode voltage as low as 10 volts and a load of just a few hundred watts, sufficient EMI will result to nullify the advantages of going to zero−point switching in the first place. The thyristor to be turned on must receive gate drive exactly at the zero crossing of the applied voltage.

The most successful method of zero−point thyristor control is therefore, to have the gate signal applied before the zero crossing. As soon as the zero crossing occurs, anode voltage will be supplied and the thyristor will come on. This is effectively accomplished by using a capacitor to derive a 90° leading gate signal from the power line source. However, only one thyristor can be controlled from this phase−shifted signal, and a slaving circuit is necessary to control the other SCR to get full−wave power control. These basic ideas are illustrated in Figure 2.21. The slaving circuit fires only on the half cycle after the firing of the master SCR. This guarantees that only complete cycles of power will be applied to the load. The gate signal to the master SCR receives all the control; a convenient control method is to replace the switch with a low−power transistor, which can be controlled by bridge−sensing circuits, manually controlled potentiometers, or various other techniques.
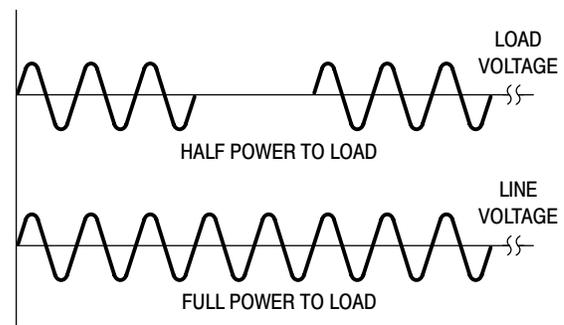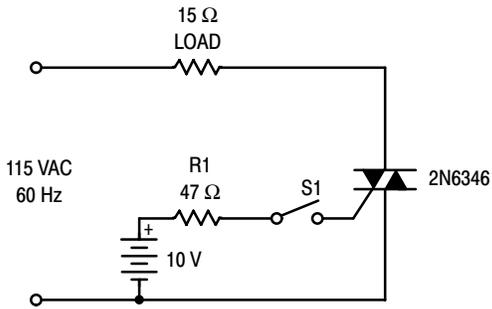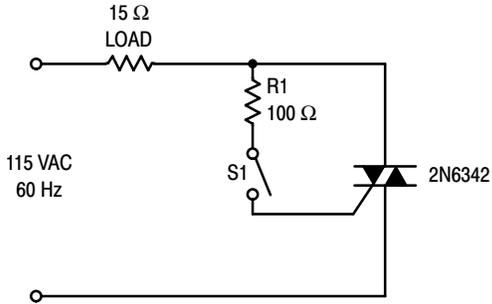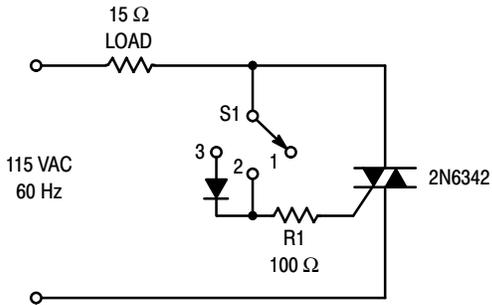

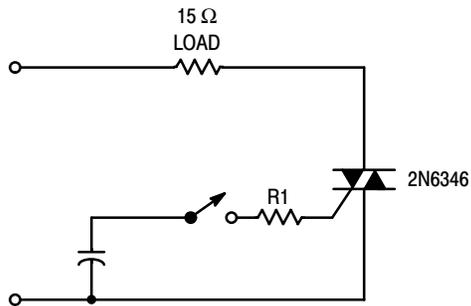**Figure 2.18. Sine Wave Showing Principles of Zero−Point Switching**

(a): Low Voltage Controlled Triac Switch

(b): Triac ac Static Contactor

(c): 3 Position Static Switch

(d): AC Controlled Triac Switch
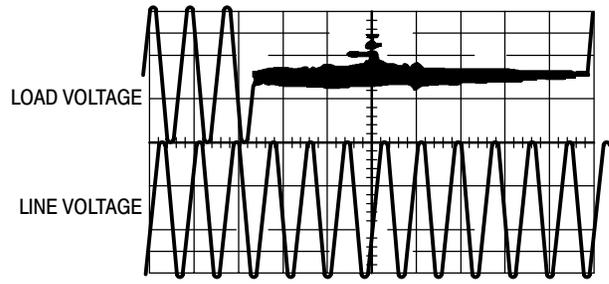
Figure 2.19. Triac Switches

Figure 2.20. Load Voltage and Line Voltage for 25% Duty Cycle

A basic SCR is very effective and trouble free. However, it can dissipate considerable power. This must be taken into account in designing the circuit and its packaging.

In the case of triacs, a slaving circuit is also usually required to furnish the gate signal for the negative half cycle. However, triacs can use slave circuits requiring less power than do SCRs as shown in Figure 2.21. Other considerations being equal, the easier slaving will some-times make the triac circuit more desirable than the SCR circuit.

Besides slaving circuit power dissipation, there is another consideration which should be carefully checked when using high–power zero–point switching. Since this is on–off switching, it abruptly applies the full load to the power line every time the circuit turns on. This may cause a temporary drop in voltage which can lead to erratic operation of other electrical equipment on the line (light dimming, TV picture shrinkage, etc.). For this reason, loads with high cycling rates should not be powered from the same supply lines as lights and other voltage–sensitive devices. On the other hand, if the load cycling rate is slow, say once per half minute, the loading flicker may not be objectionable on lighting circuits.

A note of caution is in order here. The full–wave zero–point switching control illustrated in Figure 2.21 should not be used as a half–wave control by removing the slave SCR. When the slave SCR in Figure 2.21 is removed, the master SCR has positive gate current flowing over approximately 1/4 of a cycle while the SCR itself is in the reverse–blocking state. This occurs during the negative half cycle of the line voltage. When this condition exists, Q1 will have a high leakage current with full voltage applied and will therefore be dissipating high power. This will cause excessive heating of the SCR and may lead to its failure. If it is desirable to use such a circuit as a half–wave control, then some means of clamping the gate signal during the negative half cycle must be devised to inhibit gate current while the SCR is reverse blocking. The circuits shown in Figures 2.23 and 2.24 do not have this disadvantage and may be used as half–wave controls.
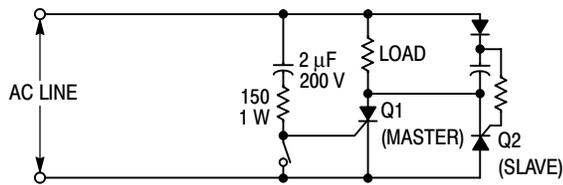
Figure 2.21. Slave and Master SCRs for Zero−Point Switching
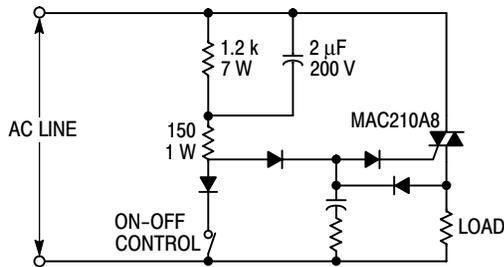
Figure 2.22. Triac Zero−Point Switch
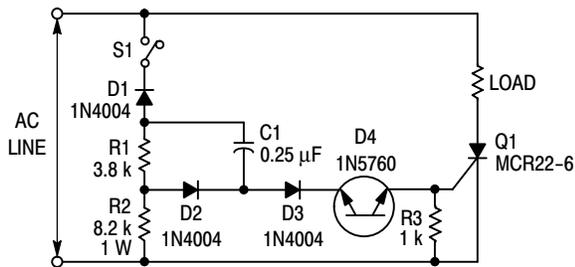
Figure 2.23. Sensitive−Gate Switch
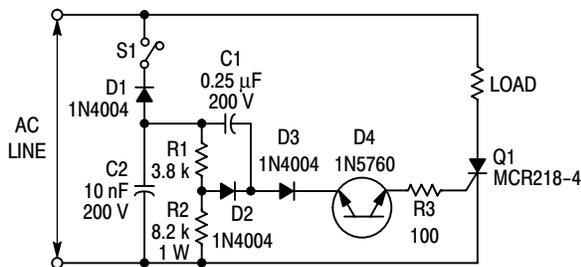
Figure 2.24. Zero−Point Switch

OPERATION

The zero−point switches shown in Figure 2.23 and 2.24 are used to insure that the control SCR turns on at the start of each positive alternation. In Figure 2.23 a pulse is generated before the zero crossing and provides a small amount of gate current when line voltage starts to go positive. This circuit is primarily for sensitive−gate SCRs. Less−sensitive SCRs, with their higher gate currents, normally require smaller values for R1 and R2 and the result can be high power dissipation in these resistors. The circuit of Figure 2.24 uses a capacitor, C2, to provide a low−impedance path around resistors R1 and R2 and can be used with less−sensitive, higher−current SCRs without increasing the dissipation. This circuit actually oscillates near the zero crossing point and provides a series of pulses to assure zero−point switching.

The basic circuit is that shown in Figure 2.23. Operation begins when switch S1 is closed. If the positive alternation is present, nothing will happen since diode D1 is reverse biased. When the negative alternation begins, capacitor C1 will charge through resistor R2 toward the limit of voltage set by the voltage divider consisting of resistors R1 and R2. As the negative alternation reaches its peak, C1 will have charged to about 40 volts. Line voltage will decrease but C1 cannot discharge because diode D2 will be reverse biased. It can be seen that C1 and three−layer diode D4 are effectively in series with the line. When the line drops to 10 volts, C1 will still be 40 volts positive with respect to the gate of Q1. At this time D4 will see about 30 volts and will trigger. This allows C1 to discharge through D3, D4, the gate of Q1, R2, and R1. This discharge current will continue to flow as the line voltage crosses zero and will insure that Q1 turns on at the start of the positive alternation. Diode D3 prevents reverse gate−current flow and resistor R3 prevents false triggering.

The circuit in Figure 2.24 operates in a similar manner up to the point where C1 starts to discharge into the gate. The discharge path will now be from C1 through D3, D4, R3, the gate of Q1, and capacitor C2. C2 will quickly charge from this high pulse of current. This reduces the voltage across D4 causing it to turn off and again revert to its blocking state. Now C2 will discharge through R1 and R2 until the voltage on D4 again becomes sufficient to cause it to break back. This repetitive exchange of charge from C1 to C2 causes a series of gate−current pulses to flow as the line voltage crosses zero. This means that Q1 will again be turned on at the start of each positive alternation as desired. Resistor R3 has been added to limit the peak gate current.

AN SCR SLAVING CIRCUIT

An SCR slaving circuit will provide full−wave control of an ac load when the control signal is available to only one of a pair of SCRs. An SCR slaving circuit is commonly used where the master SCR is controlled by zero−point switching. Zero−point switching causes the load to receive a full cycle of line voltage whenever the control signal is applied. The duty cycle of the control signal therefore determines the average amount of power supplied to the load. Zero−point switching is necessary for large loads such as electric heaters because conventional phase−shift techniques would generate an excessive amount of electro−magnetic interference (EMI).

This particular slaving circuit has two important advantages over standard RC discharge slaving circuits. It derives these advantages with practically no increase in price by using a low−cost transistor in place of the current−limiting resistor normally used for slaving. The first advantage is that a large pulse of gate current is available at the zero−crossing point. This means that it is not necessary to select sensitive−gate SCRs for controlling power. The second advantage is that this current pulse is reduced to zero within one alternation. This has a couple of good effects on the operation of the slaving SCR. It prevents gate drive from appearing while the SCR is reverse−biased, which would produce high power dissipation within the device. It also prevents the slaved SCR from being turned on for additional half cycles after the drive is removed from the control SCR.

OPERATION

The SCR slaving circuit shown in Figure 2.25 provides a single power pulse to the gate of SCR Q2 each time SCR Q1 turns on, thus turning Q2 on for the half cycle following the one during which Q1 was on. Q2 is therefore turned on only when Q1 is turned on, and the load can be controlled by a signal connected to the gate of Q1 as shown in the schematic. The control signal an be either dc or a power pulse. If the control signal is synchronized with the power line, this circuit will make an excellent zero−point switch. During the time that Q1 is on, capacitor C1 is charged through R1, D1 and Q1. While

C1 is being charged, D1 reverse−biases the base−emitter junction of Q3, thereby holding it off. The charging time constant, R1, C1, is set long enough that C1 charges for practically the entire half cycle. The charging rate of C1 follows an "S" shaped curve, charging slowly at first, then faster as the supply voltage peaks, and finally slowly again as the supply voltage decreases. When the supply voltage falls below the voltage across C1, diode D1 becomes reverse biased and the base−emitter of Q3 becomes forward biased. For the values shown, this occurs approximately 6° before the end of the half cycle conduction of Q1. The base current is derived from the energy stored in C1. This turns on Q3, discharging C1 through Q3 and into the gate of Q2. As the voltage across C1 decreases, the base drive of Q3 decreases and somewhat limits the collector current. The current pulse must last until the line voltage reaches a magnitude such that latching current will exist in Q2. The values shown will deliver a current pulse which peaks at 100 mA and has a magnitude greater than 50 mA when the anode−cathode voltage of Q2 reaches plus 10 volts. This circuit completely discharges C1 during the half cycle that Q2 is on. This eliminates the possibility of Q2 being slaved for additional half cycles after the drive is removed from Q1. The peak current and the current duration are controlled by the values of R1 and C1. The values chosen provide sufficient drive for "shorted emitter" SCRs which typically require 10 to 20 mA to fire. The particular SCR used must be capable of handling the maximum current requirements of the load to be driven; the 8 ampere, 200 V SCRs shown will handle a 1000 watt load.
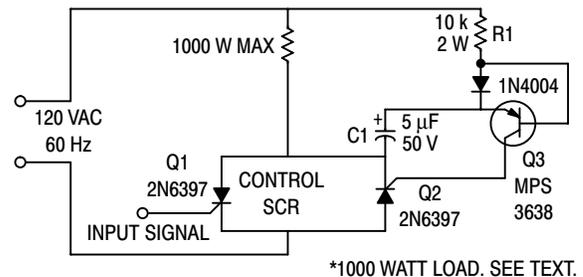

Figure 2.25. SCR Slave Circuit

SECTION 3
THYRISTOR DRIVERS AND TRIGGERING

Edited and Updated

Triggering a thyristor requires meeting its gate energy specifications and there are many ways of doing this. In general, the gate should be driven hard and fast to ensure complete gate turn on and thus minimize di/dt effects. Usually this means a gate current of at least three times the gate turn on current with a pulse rise of less than one microsecond and a pulse width greater than 10 microseconds. The gate can also be driven by a dc source as long as the average gate power limits are met.

Some of the methods of driving the gate include:
1) Direct drive from logic families of transistors
2) Opto triac drivers
3) Programmable unijunction transistors (PUTs)
4) SIDACs

In this chapter we will discuss all of these, as well as some of the important design and application considerations in triggering thyristors in general. In the chapter on applications, we will also discuss some additional considerations relating to drivers and triggers in specific applications.

PULSE TRIGGERING OF SCRs

GATE TURN–ON MECHANISM

The turn–on of PNPN devices has been discussed in many papers where it has been shown that the condition of switching is given by $\frac{dv}{di} = 0$ (i.e., $\alpha_1 + \alpha_2 = 1$, where α_1 and α_2 are the current amplification factors of the two "transistors." However, in the case of an SCR connected to a reverse gate bias, the device can have $\alpha_1 + \alpha_2 = 1$ and still stay in the blocking state. The condition of turn–on is actually $\alpha_1 + \alpha_2 > 1$.

The current amplification factor, α, increases with emitter current; some typical curves are shown in Figure 3.1. The monotonical increase of α with I_E of the device in the blocking state makes the regeneration of current (i.e., turn–on) possible.
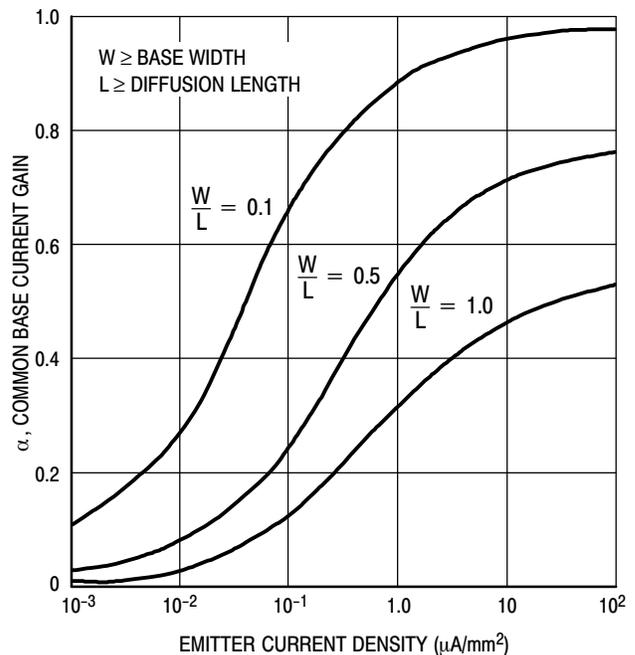
Figure 3.1. Typical Variation of Transistor α with Emitter Current Density

Using the two transistor analysis, the anode current, I_A, can be expressed as a function of gate current, I_G, as:

$$I_A = \frac{\alpha_2 I_G + I_{CS1} + I_{CS2}}{1 - \alpha_1 - \alpha_2} \tag{1}$$

Definitions and derivations are given in Appendix I. Note that the anode current, I_A, will increase to infinity as $\alpha_1 + \alpha_2 = 1$. This analysis is based upon the assumption that no majority carrier current flows out of the gate circuit. When no such assumption is made, the condition for turn–on is given by:

$$\frac{I_K}{I_A} = \frac{1 - \alpha_1}{\alpha_2} \tag{2}$$

which corresponds to $\alpha_1 + \alpha_2 > 1$ (see Appendix I).
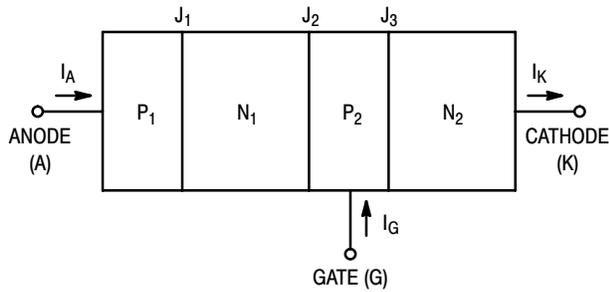
Figure 3.2. Schematic Structure of an SCR, Positive Currents Are Defined as Shown by the Arrows

Current regeneration starts when charge or current is introduced through the gate (Figure 3.2). Electrons are injected from the cathode across J_3; they travel across the P_2 "base" region to be swept out by the collector junction, J_2, and thrown into the N_1 base. The increase of majority carrier electrons in region N_1 decreases the potential in region N_1, so that holes from P_1 are injected across the junction J_1, into the N_1 "base" region to be swept across J_2, and thrown into the P_2 "base" region. The increase in the potential of region P_2 causes more electrons to be injected into P_2, thereby repeating the cycle. Since α increases with the emitter current, an increase of regeneration takes place until $\alpha_1 + \alpha_2 > 1$. Meanwhile, more carriers are collected than emitted from either of the emitters. The continuity of charge flow is violated and there is an electron build–up on the N_1 side of J_2, and a hole build–up on the P_2 side. When the inert impurity charges are compensated for by injected majority carriers, the junction J_2 becomes forward biased. The collector emits holes back to J_1 and electrons to J_3 until a steady state continuity of charge is established.

During the regeneration process, the time it takes for a minority carrier to travel across a base region is the transit time, t, which is given approximately as:

$$t_1 = \frac{W^2_i}{2D_i} \quad \begin{array}{l} \text{where } W_i = \text{ base width} \\ \\ D_i = \text{ diffusion length} \end{array} \quad (3)$$

(The subscript "i" can be either 1 or 2 to indicate the appropriate base.) The time taken from the start of the gate trigger to the turn–on of the device will be equal to some multiple of the transit time.

CURRENT PULSE TRIGGERING

Current pulse triggering is defined as supplying current through the gate to compensate for the carriers lost by recombination in order to provide enough current to sustain increasing regeneration. If the gate is triggered with a current pulse, shorter pulse widths require higher currents as shown by Figure 3.3(a). Figure 3.3(a) seems to indicate there is a constant amount of charge required to trigger on the device when I_G is above a threshold level. When the charge required for turn–on plotted versus pulse current or pulse width, there is an optimum range of current levels or pulse widths for which the charge is minimum, as shown in region A of Figure 3.3(b) and (c). Region C shows that for lower current levels (i.e., longer minimum pulse widths) more charge is required to trigger on the device. Region B shows increasing charge required as the current gets higher and the pulse width smaller.
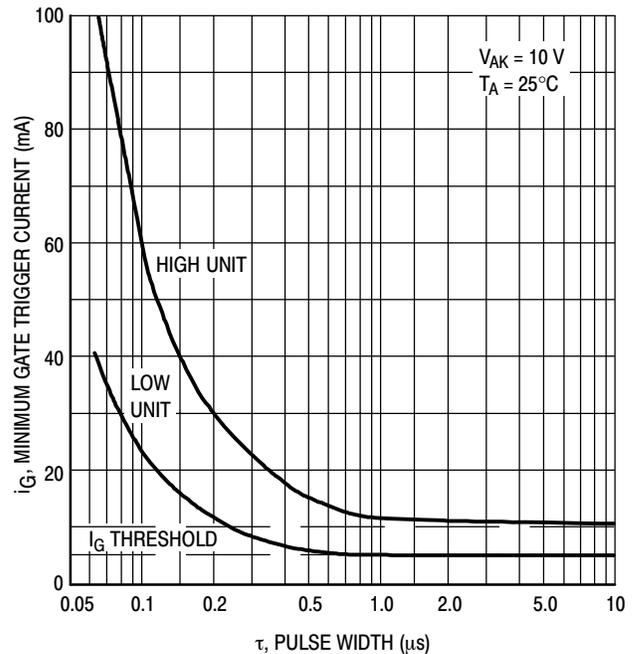
Figure 3.3(a). Typical Variation of Minimum Gate Current Required to Trigger
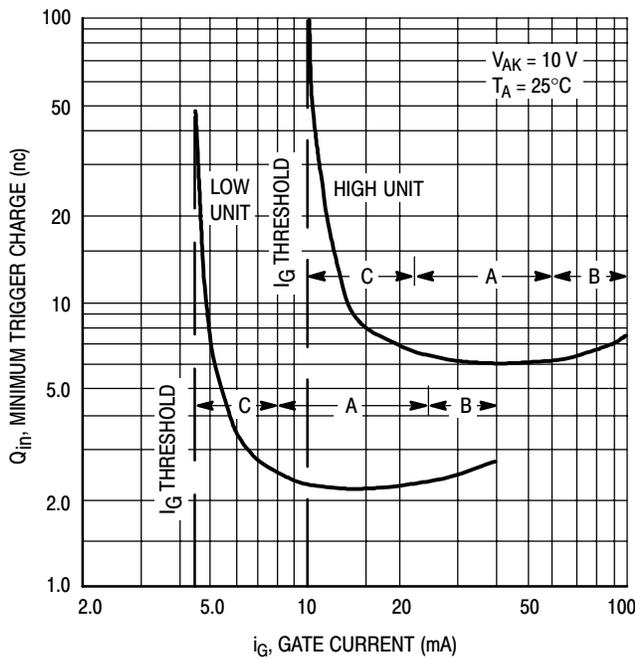
Figure 3.3(b). Variation of Charge versus Gate Current
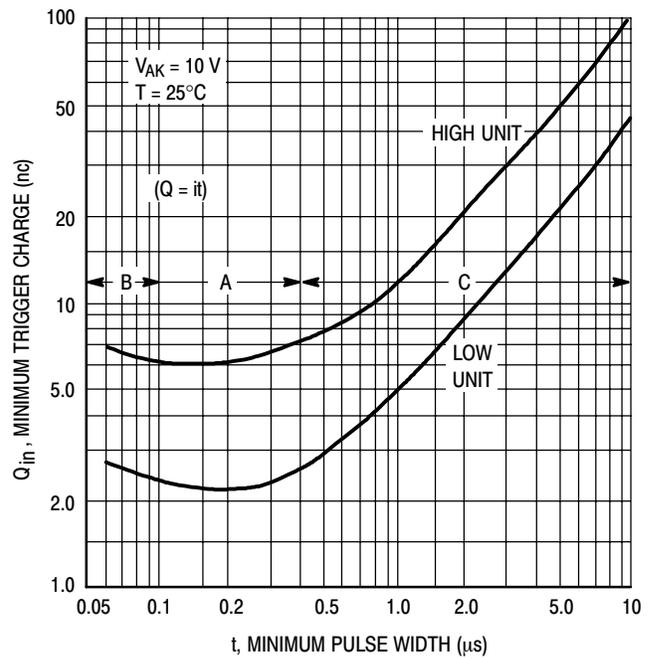
Figure 3.3(c). Variation of Charge versus Minimum Pulse Width

The charge characteristic curves can be explained qualitatively by the variation of current amplification (α_T) with respect to emitter current. A typical variation of α_1 and α_2 for a thyristor is shown in Figure 3.4(a). From Figure 3.4(a), it can be deduced that the total current amplification factor, $\alpha_T = \alpha_1 + \alpha_2$, has a characteristic curve as shown in Figure 3.4(b). (The data does not correspond to the data of Figure 3.3 — they are taken for different types of devices.)

The gate current levels in region A of Figure 3.3 correspond to the emitter (or anode) currents for which the slope of the α_T curve is steepest (Figure 3.4(b)). In region A the rate that α_T builds up with respect to changes of I_E (or I_A) is high, little charge is lost by recombination, and therefore, a minimum charge is required for turn–on.

In region C of Figure 3.3, lower gate current corresponds to small I_E (or I_A) for which the slope of α_T, as well as α_T itself, is small. It takes a large change in I_E (or $I_{A)}$ in order to build up α_T. In this region, a lot of the turn–on the device should be large enough to flood the gate to cathode junction nearly instantaneously with a

charge supplied through the gate is lost by recombination. The charge required for turn–on increases markedly as the gate current is decreased to the threshold level. Below this threshold, the device will not turn on regardless of how long the pulse width becomes. At this point, the slope of α_T is equal to zero; all of the charge supplied is lost completely in recombination or drained out through gate–cathode shunt resistance. A qualitative analysis of variation of charge with pulse width at region A and C is discussed in Appendix II.

In region B, as the gate current level gets higher and the pulse width smaller, there are two effects that contribute to an increasing charge requirement to trigger–on the device: (1) the decreasing slope of α_T and, (2) the transit time effect. As mentioned previously, it takes some multiple of the transit time for turn–on. As the gate pulse width decreases to N (t_{N1} + t_{P2}) or less, (where N is a positive real number, t_{N1} = transit time of base N_1, and t_{P2} = transit time of base P2) the amount of current required to charge which corresponds to I_E (or I_A) high enough to give $\alpha_T > 1$.
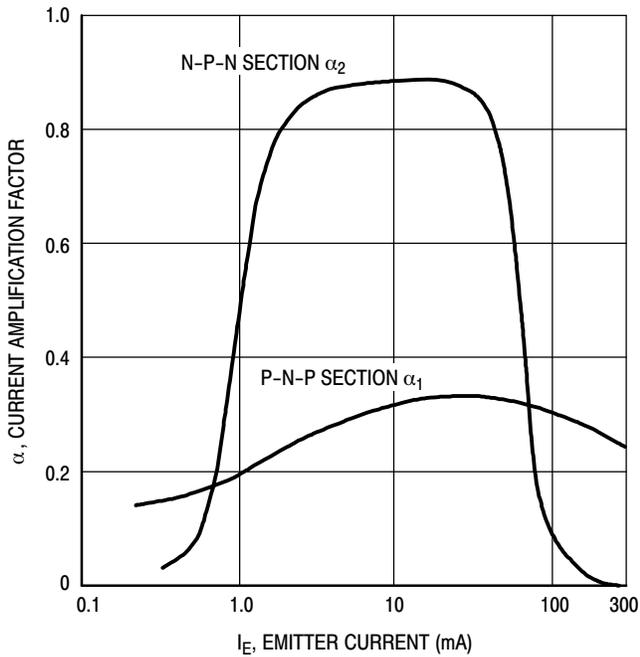
Figure 3.4(a). The Variation of α_1 and α_2 with Emitter Current for the Two Sections of Two Typical Silicon Controlled Rectifiers
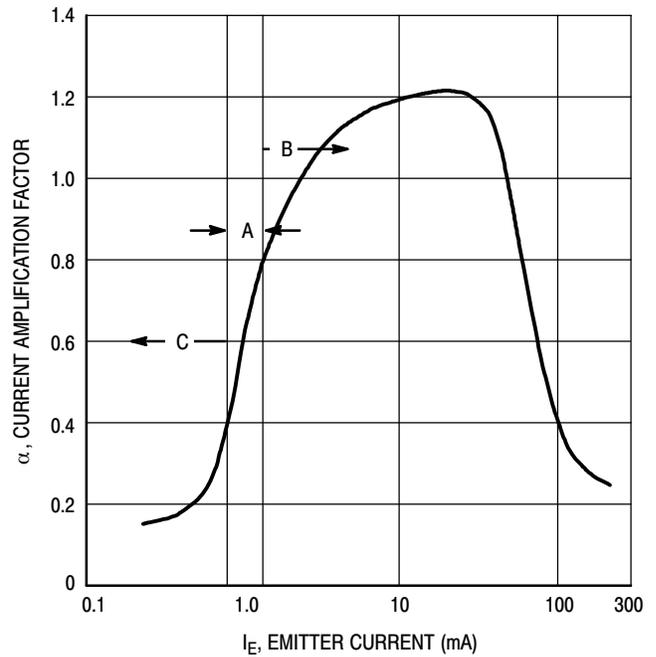
Figure 3.4(b). Typical Variation of α_T versus Emitter Current

CAPACITANCE CHARGE TRIGGERING

Using a gate trigger circuit as shown in Figure 3.5, the charge required for turn−on increases with the value of capacitance used as shown in Figure 3.7. Two reasons may account for the increasing charge characteristics:

1) An effect due to threshold current.
2) An effect due to variation of gate spreading resistance.
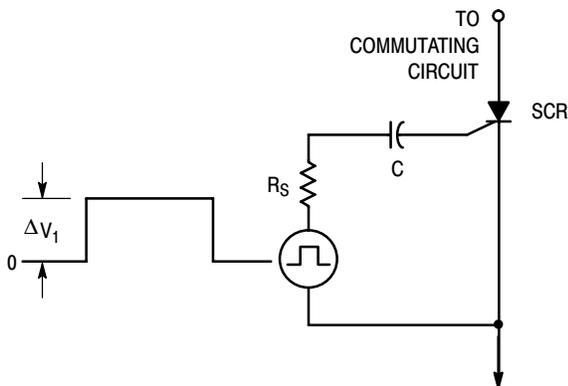
Figure 3.5. Gate Circuit of Capacitance Charge Triggering

$$t_{fi} = 2.2 \, (r'_{G1} + R_S)C_1$$

$$\text{SHADED AREA I} = |(r'_{G1} + R_S)(C_1)|(I_{thr})$$

$$\text{SHADED AREA II} = |(r'_{G2} + R_S)(C_2)|(I_{thr})$$

$$C_1 < C_2$$
$$\Delta V_1 C_1 = \Delta V_2 C_2$$

$$|(r'_{G1} + R_S)(C_1)|(I_{thr}) < |(r'_{G2} + R_S)(C_2)|(I_{thr})$$

Figure 3.6. Gate Current Waveform in Capacitance Charge Triggering

Consider the gate current waveform in Figure 3.6; the triggering pulse width is made large enough such that $\tau >> t_{fl}$; the threshold trigger current is shown as I_{thr}. All of the charge supplied at a transient current level less than I_{thr} is lost by recombination, as shown in the shaded regions.

The gate spreading resistance (r'_G) of the gate junction varies inversely with peak current; the higher the peak current, the smaller the gate spreading resistance. Variation of gate spreading resistance measured by the method of Time Domain Reflectometry is plotted in Figure 3.8.

From the data of Figure 3.7, it is clear that for larger values of capacitance a lower voltage level is required for turn−on. The peak current of the spike in Figure 3.6 is given by $I_{pk} = \dfrac{\Delta V}{R_S + r'_G}$; the smaller ΔV, the smaller I_{pk}. Smaller I_{pk} in turn yields large r'_G, so that r'_G is dependent on the value of capacitance used in capacitance charge triggering. This reasoning is confirmed by measuring the fall time of the gate trigger voltage and calculating the transient gate spreading resistance, r'_G, from: $R_S + r'_G = \dfrac{t_f}{2.2\,C}$. Results are plotted in Figure 3.9. As expected, r'_G increases with increasing values of capacitance used. Referring back to Figure 3.6, for the same amount of charge ($C\,\Delta V$), the larger the ($R_S + r'_G$)C time constant of the current spike, the more charge under the threshold level is lost in recombination. Increasing the value of C will increase the time constant more rapidly than if r'_G were invariant. Therefore, increasing the value of C should increase the charge lost as shown in Figure 3.7. Note that a two order of magnitude increase in capacitance increased the charge by less than 3:1.

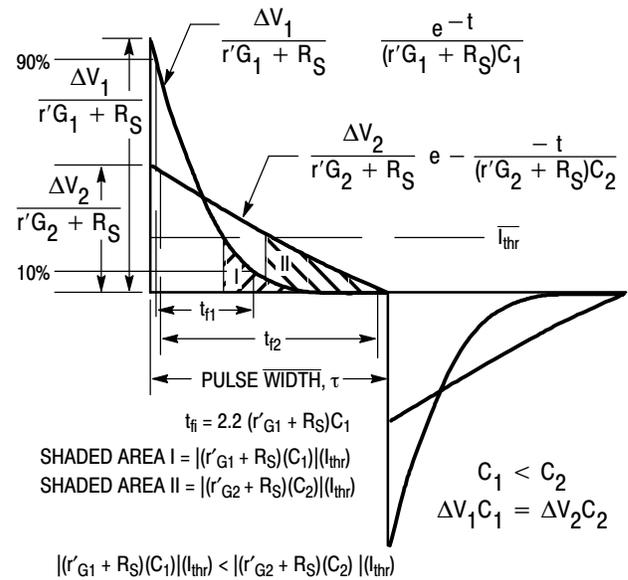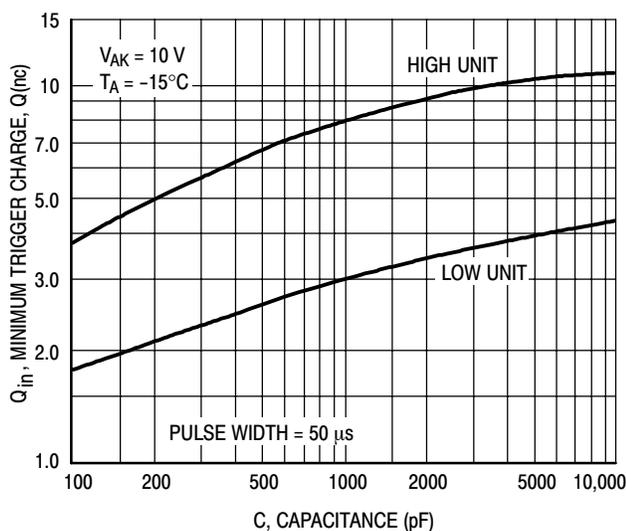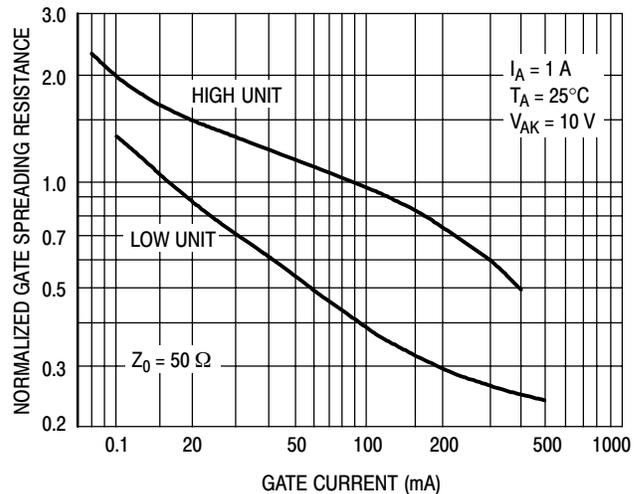**Figure 3.8. Variation of Gate Spreading Resistance versus Gate Peak Current**

EFFECT OF TEMPERATURE

The higher the temperature, the less charge required to turn on the device, as shown in Figure 3.10. At the range of temperatures where the SCR is operated the life time of minority carriers increases with temperature; therefore less charge into the gate is lost in recombination.

As analyzed in Appendix II, there are three components of charge involved in gate triggering: (1) Q_r, charge lost in recombination, (2) Q_{dr}, charge drained out through the built−in gate−cathode shunt resistance, (3) Q_{tr}, net charge for triggering. All of them are temperature dependent. Since the temperature coefficient of voltage across a p–n junction is small, Q_{dr} may be considered invariant of temperature. At the temperature range of operation, the temperature is too low to give rise to significant impurity gettering, lifetime increases with temperature causing Q_r to decrease with increasing temperature. Also, Q_{tr} decreases with increasing temperature because at a constant current the α_T of the device in the blocking state increases with temperature;[7] in other words, to attain $\alpha_T = 1$ at an elevated temperature, less anode current, hence gate current [see equation (3) of Appendix I], is needed; therefore, Q_{tr} decreases. The input charge, being equal to the sum of Q_{tr}, Q_r, and Q_{dr}, decreases with increasing temperature.

The minimum current trigger charge decreases roughly exponentially with temperature. Actual data taken on an MCR729 deviate somewhat from exponential trend (Figure 3.10). At higher temperatures, the rate of decrease is less; also for different pulse widths the rates of decrease of Q_{in} are different; for large pulse widths the recombination charge becomes more significant than that of small pulse widths. As the result, it is expected and Figure 3.10 shows that Q_{in} decreases more rapidly with temperature at high pulse widths. These effects are analyzed in

Figure 3.7. Variation of Trigger Charge versus Capacitance Used

Appendix II [equation (7), page 235]. The theory and experiment agree reasonably well.
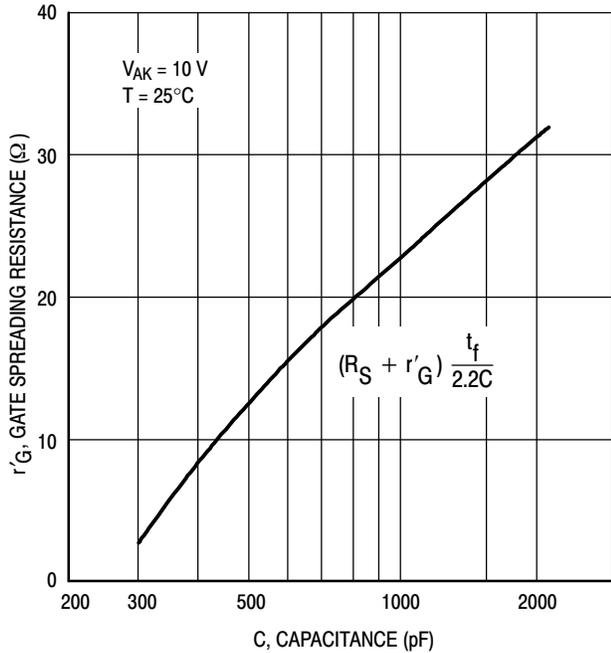
Figure 3.9. Variation of Transient Base Spreading Resistance versus Capacitance

$$(R_S + r'_G) \frac{t_f}{2.2C}$$
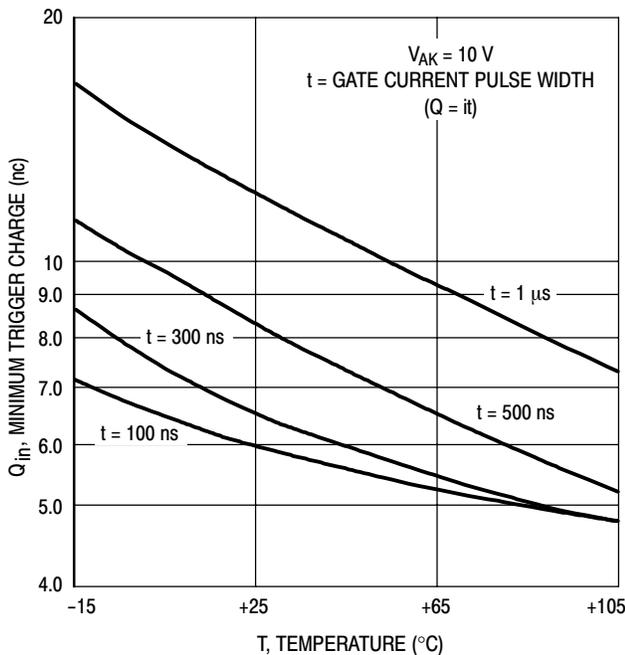
Figure 3.10. Variation of Q versus Temperature

EFFECT OF BLOCKING VOLTAGE

An SCR is an avalanche mode device; the turn−on of the device is due to multiplication of carriers in the middle collector junction. The multiplication factor is given by the empirical equation

$$M = \frac{\cdot 1}{1 - (\frac{V}{V_B})^n} \qquad (6)$$

where

M ≡ Multiplication factor

V ≡ Voltage across the middle "collector" junction (voltage at which the device is blocking prior to turn−on)

V_B ≡ Breakdown voltage of the middle "collector" junction

n ≡ Some positive number

Note as V is increased, M also increases and in turn α increases (the current amplification factor $\alpha = \gamma\delta\beta M$ where γ ≡ Emitter efficiency, β ≡ Base transport factor, and δ ≡ Factor of recombination).

The larger the V, the larger is α_T. It would be expected for the minimum gate trigger charge to decrease with increasing V. Experimental results show this effect (see Figure 3.11). For the MCR729, the gate trigger charge is only slightly affected by the voltage at which the device is blocking prior to turn−on; this reflects that the exponent, n, in equation (6) is small.

EFFECT OF GATE CIRCUIT

As mentioned earlier, to turn on the device, the total amplification factor must be greater than unity. This means that if some current is being drained out of the gate which bleeds the regeneration current, turn−on will be affected. The higher the gate impedance, the less the gate trigger charge. Since the regenerative current prior to turn−on is small, the gate impedance only slightly affects the required minimum trigger charge; but in the case of over−driving the gate to achieve fast switching time, the gate circuit impedance will have noticeable effect.

EFFECT OF INDUCTIVE LOAD

The presence of an inductive load tends to slow down the change of anode current with time, thereby causing the required charge for triggering to increase with the value of inductance. For dc or long pulse width current triggering, the inductive load has little effect, but its effect increases markedly at short pulse widths, as shown in Figure 3.12. The increase in charge occurs because at short pulse widths, the trigger signal has decreased to a negligible value before the anode current has reached a level sufficient to sustain turn−on.
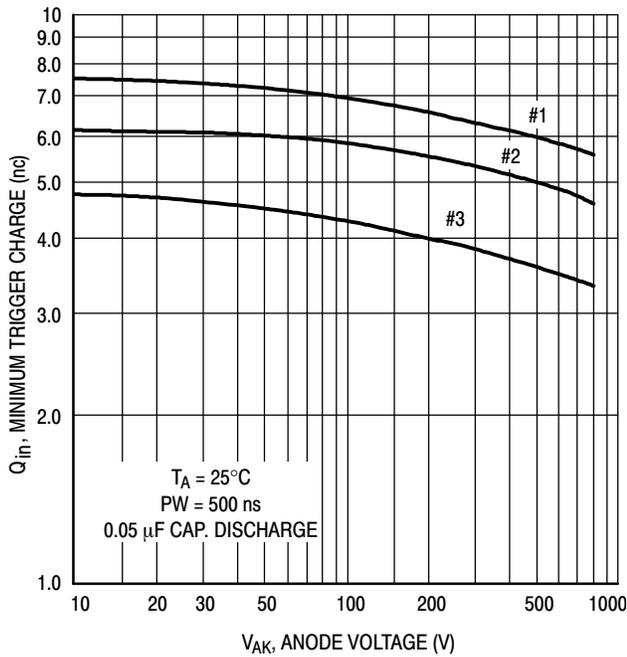
Figure 3.11. Variation of Current Trigger Charge versus Blocking Voltage Prior to Turn−On
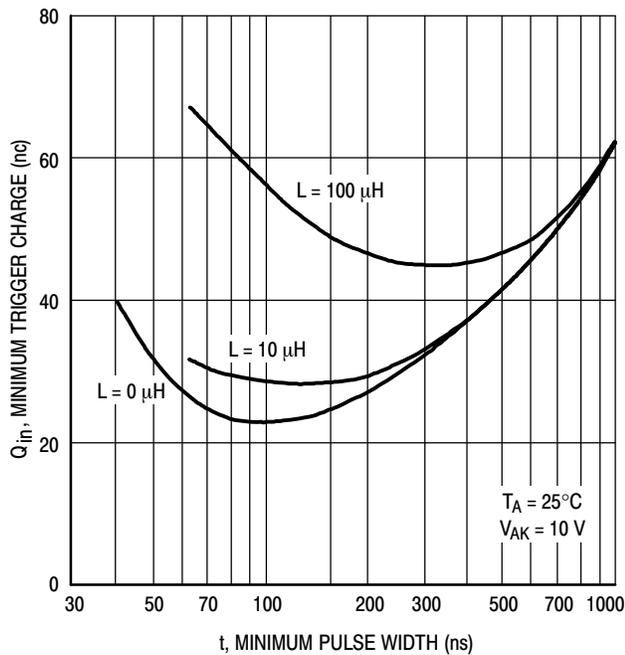
Figure 3.12. Effect of Inductance Load on Triggering Charge

USING NEGATIVE BIAS AND SHUNTING

Almost all SCR's exhibit some degree of turn−off gain. At normal values of anode current, negative gate current will not have sufficient effect upon the internal feedback loop of the device to cause any significant change in anode current. However, it does have a marked effect at low anode current levels; it can be put to advantage by using it to modify certain device parameters. Specifically, turn−off time may be reduced and hold current may be increased. Reduction of turn−off time and increase of hold current are useful in such circuits as inverters or in full−wave phase control circuits in which inductance is present.

Negative gate current may, of course, be produced by use of an external bias supply. It may also be produced by taking advantage of the fact that during conduction the gate is positive with respect to the cathode and providing an external conduction path such as a gate−to−cathode resistor. All ON Semiconductor SCR's, with the exception of sensitive gate devices, are constructed with a built in gate−to−cathode shunt, which produces the same effect as negative gate current. Further change in characteristics can be produced by use of an external shunt. Shunting does not produce as much of a change in characteristics as does negative bias, since the negative gate current, even with an external short circuit, is limited by the lateral resistance of the base layer. When using external negative bias the current must be limited, and care must be taken to avoid driving the gate into the avalanche region.

The effects of negative gate current are not shown on the device specification sheets. The curves in Figure 3.13 represent measurements made on a number of SCRs, and should therefore not be considered as spec limits. They do, however, show definite trends. For example, all of the SCRs showed an improvement in turn−off time of about one−third by using negative bias up to the point where no further significant improvement was obtained. The increase in hold current by use of an external shunt resistor ranged typically between 5 and 75 percent, whereas with negative bias, the range of improvement ran typically between 2−1/2 and 7 times the open gate value. Note that the holding current curves are normalized and are referred to the open gate value.

SPREAD OF 5 DEVICES
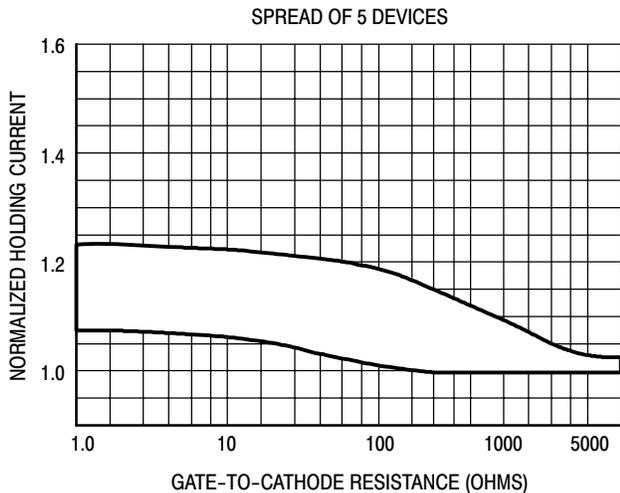
Figure 3.13(a). Normalized Holding Current versus Gate−to−Cathode Resistance

SPREAD OF 5 DEVICES
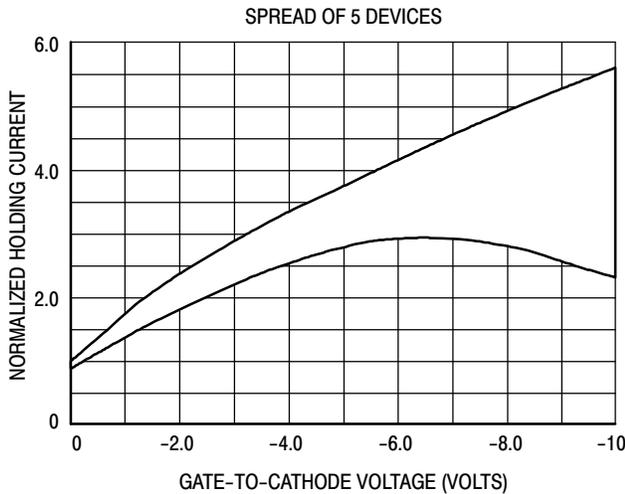
Figure 3.13(b). Normalized Holding Current versus Gate−to−Cathode Voltage

AVERAGE 10 DEVICES
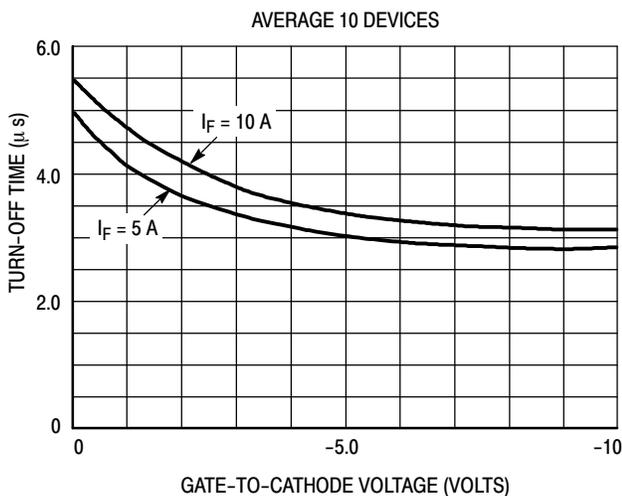
Figure 3.13(c). Turn−Off Time versus Bias

REDUCING di/dt — EFFECT FAILURES

Figure 3.14 shows a typical SCR structural cross section (not to scale). Note that the collector of transistor 1 and the base of transistor 2 are one and the same layer. This is also true for the collector of transistor 2 and the base of transistor 1. Although for optimum performance as an SCR the base thicknesses are great compared to a normal transistor, nevertheless, base thickness is still small compared to the lateral dimensions. When applying positive bias to the gate, the transverse base resistance, spreading resistance or r_b' will cause a lateral voltage drop which will tend to forward bias those parts of the transistor 1 emitter−junction closest to the base contact (gate) more heavily, or sooner than the portions more remote from the contact area. Regenerative action, consequently will start in an area near the gate contact, and the SCR will turn on first in this area. Once on, conduction will propagate across the entire junction.

LAYER	T_2	T_1
NO. 4		(E)
NO. 3	(C)	(B)
NO. 2	(B)	(C)
NO. 1	(E)	
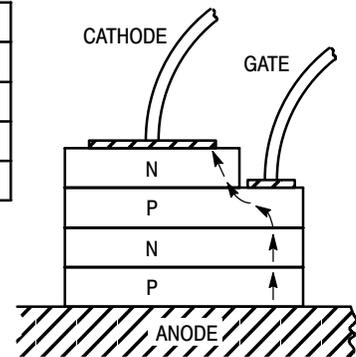
Figure 3.14. Construction of Typical SCR

The phenomenon of di/dt failure is related to the turn−on mechanism. Let us look at some of the external factors involved and see how they contribute. Curve 3.15(a) shows the fall of anode−to−cathode voltage with time. This fall follows a delay time after the application of the gate bias. The delay time and fall time together are called turn−on time, and, depending upon the device, will take anywhere from tens of nanoseconds up to a few microseconds. The propagation of conduction across the entire junction requires a considerably longer time. The time required for propagation or equalization of conduction is represented approximately by the time required for the anode−to−cathode voltage to fall from the 10 percent point to its steady state value for the particular value of anode current under consideration (neglecting the change due to temperature effects). It is during the interval of time between the start of the fall of anode−to−cathode voltage and the final equalization of conduction that the SCR is most susceptible to damage from excessive current.

Let us superimpose a current curve (b) on the anode–to–cathode voltage versus time curve to better understand this. If we allow the current to rise rapidly to a high value we find by multiplying current and voltage that the instantaneous dissipation curve (c) reaches a peak which may be hundreds of times the steady state dissipation level for the same value of current.

At the same time it is important to remember that the dissipation does not take place in the entire junction, but is confined at this time to a small volume. Since temperature is related to energy per unit volume, and since the energy put into the device at high current levels may be very large while the volume in which it is concentrated is very small, very high spot temperatures may be achieved. Under such conditions, it is not difficult to attain temperatures which are sufficient to cause localized melting of the device.

Even if the peak energy levels are not high enough to be destructive on a single–shot basis, it must be realized that since the power dissipation is confined to a small area, the power handling capabilities of the device are lessened. For pulse service where a significant percentage of the power per pulse is dissipated during the fall–time interval, it is not acceptable to extrapolate the steady state power dissipation capability on a duty cycle basis to obtain the allowable peak pulse power.
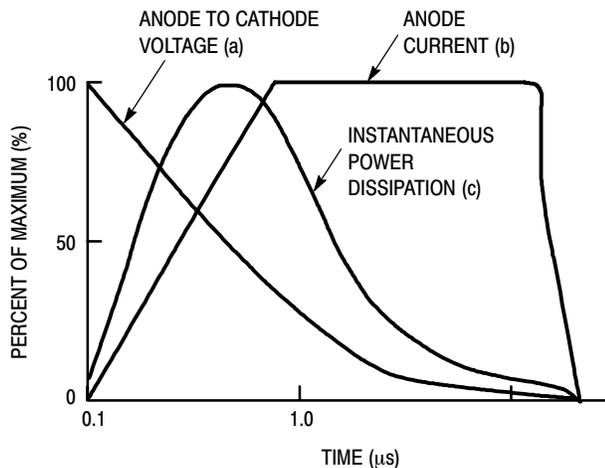
Figure 3.15. Typical Conditions — Fast–Rise, High Current Pulse

The final criterion for the limit of operation is junction temperature. For reliable operation the instantaneous junction temperature must always be kept below the maximum junction temperature as stated on the manufacturer's data sheet. Some SCR data sheets at present include information on how to determine the thermal response of the junction to current pulses. This informa-

tion is not useful, however, for determining the limitations of the device before the entire junction is in conduction, because they are based on measurements made with the entire junction in conduction.

At present, there is no known technique for making a reasonably accurate measurement of junction temperature in the time domain of interest. Even if one were to devise a method for switching a sufficiently large current in a short enough time, one would still be faced with the problem of charge storage effects in the device under test masking the thermal effects. Because of these and other problems, it becomes necessary to determine the device limitations during the turn–on interval by destructive testing. The resultant information may be published in a form such as a maximum allowable current versus time, or simply as a maximum allowable rate of rise of anode current (di/dt).

Understanding the di/dt failure mechanism is part of the problem. To the user, however, a possible cure is infinitely more important. There are three approaches that should be considered.

Because of the lateral base resistance the portion of the gate closest to the gate contact is the first to be turned on because it is the first to be forward biased. If the minimum gate bias to cause turn–on of the device is used, the spot in which conduction is initiated will be smallest in size. By increasing the magnitude of the gate trigger pulse to several times the minimum required, and applying it with a very fast rise time, one may considerably increase the size of the spot in which conduction starts. Figure 3.16(a) illustrates the effect of gate drive on voltage fall time and Figure 3.16(b) shows the improvement in instantaneous dissipation. We may conclude from this that overdriving the gate will improve the di/dt capabilities of the device, and we may reduce the stress on the device by doing so.
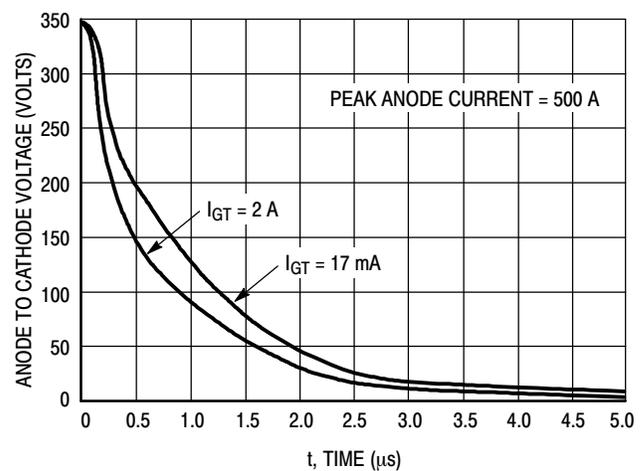
Figure 3.16(a). Effect of Gate Drive on Fall Time

A very straightforward approach is to simply slow down the rate of rise of anode current to insure that it stays within the device ratings. This may be done simply by adding some series inductance to the circuit.
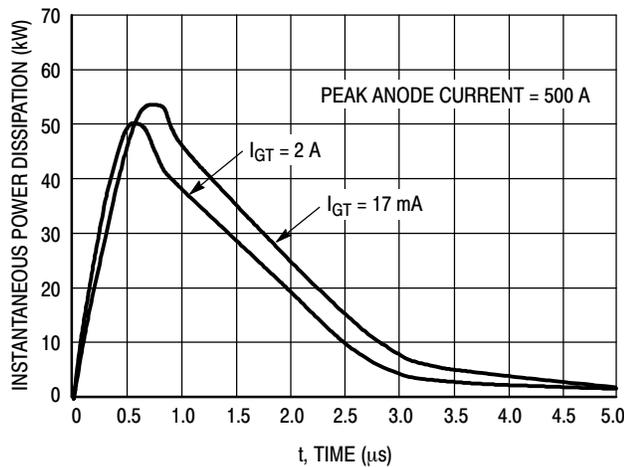
Figure 3.16(b). Effect of Gate Drive On Turn−On Dissipation

If the application should require a rate of current rise beyond the rated di/dt limit of the device, then another approach may be taken. The device may be turned on to a relatively low current level for a sufficient time for a large part of the junction to go into conduction; then the current level may be allowed to rise much more rapidly to very high levels. This might be accomplished by using a delay reactor as shown in Figure 3.17. Such a reactor would be wound on a square loop core so that it would have sharp saturation characteristic and allow a rapid current rise. It is also possible to make use of a separate saturation winding. Under these conditions, if the delay is long enough for the entire junction to go into conduction, the power handling capabilities of the device may be extrapolated on a duty cycle basis.
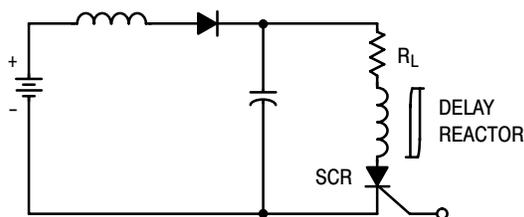

Figure 3.17. Typical Circuit Use of a Delay Reactor

WHY AND HOW TO SNUB THYRISTORS

Inductive loads (motors, solenoids, etc.) present a problem for the power triac because the current is not in phase with the voltage. An important fact to remember is that since a triac can conduct current in both directions, it has only a brief interval during which the sine wave current is passing through zero to recover and revert to its blocking state. For inductive loads, the phase shift between voltage and current means that at the time the current of the power handling triac falls below the holding current and the triac ceases to conduct, there exists a certain voltage which must appear across the triac. If this voltage appears too rapidly, the triac will resume conduction and control is lost. In order to achieve control with certain inductive loads, the rate of rise in voltage (dv/dt) must be limited by a series RC network placed in parallel with the power triac as shown in Figure 3.18. The capacitor C_S will limit the dv/dt across the triac.

The resistor R_S is necessary to limit the surge current from C_S when the triac conducts and to damp the ringing of the capacitance with the load inductance L_L. Such an RC network is commonly referred to as a "snubber."

Figure 3.19 shows current and voltage waveforms for the power triac. Commutating dv/dt for a resistive load is typically only 0.13 V/μs for a 240 V, 50 Hz line source and 0.063 V/μs for a 120 V, 60 Hz line source. For inductive loads the "turn−off" time and commutating dv/dt stress are more difficult to define and are affected by a number of variables such as back EMF of motors and the ratio of inductance to resistance (power factor). Although it may appear from the inductive load that the rate or rise is extremely fast, closer circuit evaluation reveals that the commutating dv/dt generated is restricted to some finite value which is a function of the load reactance L_L and the device capacitance C but still may exceed the triac's critical commutating dv/dt rating which is about 50 V/μs. It is generally good practice to use an RC snubber network across the triac to limit the rate of rise (dv/dt) to a value below the maximum allowable rating. This snubber network not only limits the voltage rise during commutation but also suppresses transient voltages that may occur as a result of ac line disturbances.

There are no easy methods for selecting the values for R_S and C_S of a snubber network. The circuit of Figure 3.18 is a damped, tuned circuit comprised of R_S, C_S, R_L and L_L, and to a minor extent the junction capacitance of the triac. When the triac ceases to conduct (this occurs every half cycle of the line voltage when the current falls below the holding current), the triac receives a step impulse of line voltage which depends on the power factor of the load. A given load fixes R_L and L_L; however, the circuit designer can vary R_S and C_S. Commutating dV/dt can be lowered by increasing C_S while R_S can be increased to decrease resonant "over ringing" of the tuned circuit.
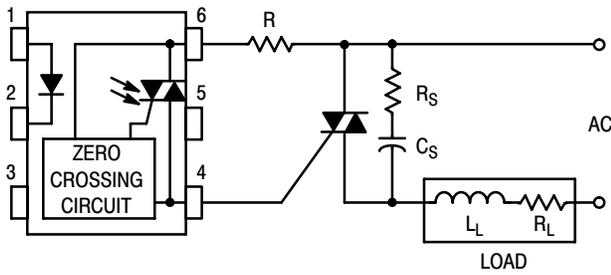
Figure 3.18. Triac Driving Circuit — with Snubber

RESISTIVE LOAD

INDUCTIVE LOAD
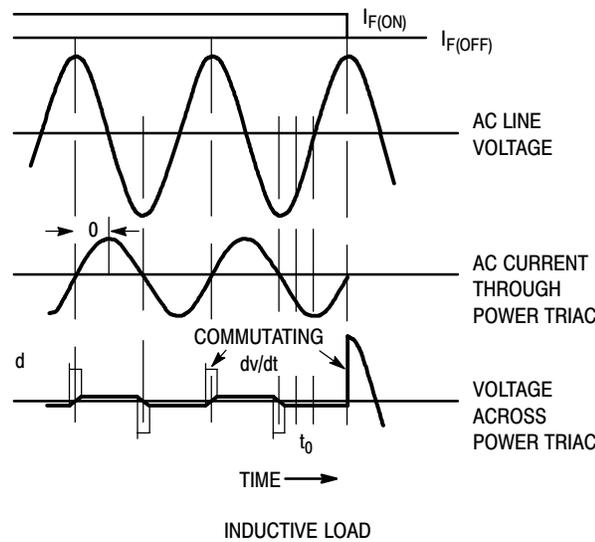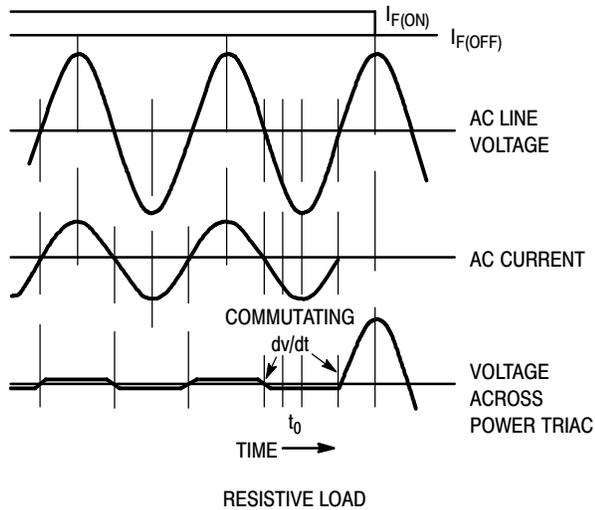
Figure 3.19. Current and Voltage Waveforms During Commutation

BASIC CIRCUIT ANALYSIS

Figure 3.20 shows an equivalent circuit used for analysis, in which the triac has been replaced by an ideal switch. When the triac is in the blocking or non–conducting state, represented by the open switch, the circuit is a standard RLC series network driven by an ac voltage source. The following differential equation can be obtained by summing the voltage drops around the circuit;

$$(R_L + R_S)\, i(t) + L\frac{di(t)}{dt} + \frac{q_c(t)}{C_S} = V_M \sin(\omega t + \phi) \quad (2)$$

in which i(t) is the instantaneous current after the switch opens, $q_c(t)$ is the instantaneous charge on the capacitor, V_M is the peak line voltage, and ϕ is the phase angle by which the voltage leads the current prior to opening of the switch. After differentiation and rearrangement, the equation becomes a standard second–order differential equation with constant coefficients.

With the imposition of the boundary conditions that $i(o) = 0$ and $q_c(o) = 0$ and with selected values for R_L, L, R_S and C_S, the equation can be solved, generally by the use of a computer. Having determined the magnitude and time of occurrence of the peak voltage across the thyristor, it is then possible to calculate the values and times of the voltages at 10% and 63% of the peak value. This is necessary in order to compute the dv/dt stress as defined by the following equation:

$$\frac{dv}{dt} = \frac{V_2 - V_1}{t_2 - t_1}$$

where V_1 and t_1 are the voltage and time at the 10% point and V_2 and t_2 are the voltage and time at the 63% point.

Solution of the differential equation for assumed load conditions will give the circuit designer a starting point for selecting R_S and C_S.

Because the design of a snubber is contingent on the load, it is almost impossible to simulate and test every possible combination under actual operating conditions. It is advisable to measure the peak amplitude and rate of rise of voltage across the triac by use of an oscilloscope, then make the final selection of R_S and C_S experimentally. Additional comments about circuit values for SCRs and Triacs are made in Chapter 6.
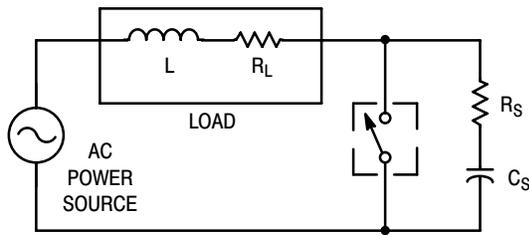
Figure 3.20. Equivalent Circuit used for Analysis

USING SENSITIVE GATE SCRs

In applications of sensitive gate SCRs such as the ON Semiconductor 2N6237, the gate–cathode resistor, R_{GK} (Figure 3.21) is an important factor. Its value affects, in varying degrees, such parameters as I_{GT}, V_{DRM}, dv/dt, I_H, leakage current, and noise immunity.
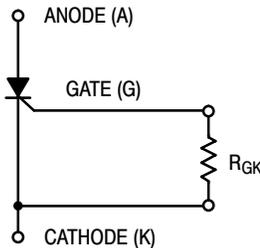
Figure 3.21. Gate–Cathode Resistor, R_{GK}

SCR CONSTRUCTION

The initial step in making an SCR is the creation, by diffusion, of P–type layers is N–type silicon base material. Prior to the advent of the all–diffused SCR, the next step was to form the gate–cathode P–N junction by alloying in a gold–antimony foil. This produced a silicon P–N junction of the regrown type over most of the junction area. However, a resistive rather than semiconductor junction would form where the molten alloy terminated at the surface. This formed an internal R_{GK}, looking in at the gate–cathode terminals, that reduced the "sensitivity" of the SCR.

Modern practice is to produce the gate–cathode junction by masking and diffusing, a much more controllable process. It produces a very clean junction over the entire junction area with no unwanted resistive paths. Good dv/dt performance by larger SCRs, however, requires resistive paths distributed over the junction area. These are diffused in as emitter shorts and naturally desensitize the device. Smaller SCRs may rely on an external R_{GK} because the lateral resistance in the gate layer is small enough to prevent leakage and dV/dt induced currents from forward biasing the cathode and triggering the SCR.

Figure 3.22(a) shows the construction of a sensitive gate SCR and the path taken by leakage current flowing out through R_{GK}. Large SCRs (Figure 3.22(b)) keep the path length small by bringing the gate layer up to contact the cathode metal. This allows the current to siphon out all–round the cathode area.

When the chip dimensions are small there is little penalty in placing the resistor outside the package. This gives the circuit designer considerable freedom in tailoring the electrical properties of the SCR. This is a great advantage when low trigger or holding current is needed. Still, there are trade–offs in the maximum allowable junction temperature and dV/dt immunity that go with larger resistor values. Verifying that the design is adequate to prevent circuit upset by heat or noise is important. The rated value for R_{GK} is usually 1 K Ohm. Lower values improve blocking and turn–off capability.

(a). SIMPLE CONSTRUCTION   (b). SHORTED EMITTER CONSTRUCTION
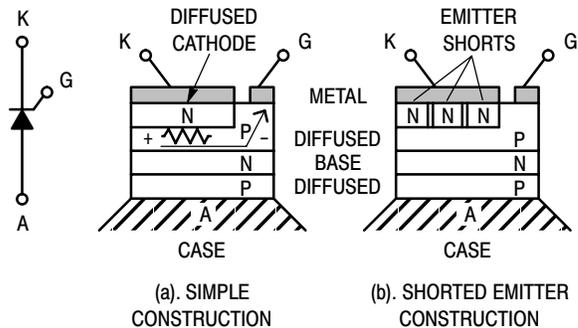
Figure 3.22. Sensitive Gate SCR Construction

The sensitive gate SCR, therefore, is an all–diffused design with no emitter shorts. It has a very high impedance path in parallel with the gate–cathode P–N diode; the better the process is the higher this impedance, until a very good device cannot block voltage in the forward direction without an external R_{GK}. This is so, because thermally generated leakage currents flowing from the anode into the gate junction are sufficient to turn on the SCR. The value for R_{GK} is usually one kilohm and its presence and value affects many other parameters.

FORWARD BLOCKING VOLTAGE AND CURRENT, V_{DRM} AND I_{DRM}

The 2N6237 family is specified to have an I_{DRM}, or anode–to–cathode leakage current, of less than 200 μA at maximum operating junction temperature and rated V_{DRM}. This leakage current increases if R_{GK} is omitted and, in fact, the device may well be able to regenerate and turn on. Tests were run on several 2N6239 devices to establish the dependency of the leakage current on R_{GK} and to determine its relationship with junction temperature, T_J, and forward voltage V_{AK} (Figure 3.23a).

Figure 3.23(a) is a plot of V_{AK}, forward voltage, versus R_{GK} taken at the maximum rated operating junction temperature of 110°C. With each device the leakage current, I_{AK}, is set for a V_{AK} of 200 V, then V_{AK} reduced and R_{GK} varied to re−establish the same leakage current. The plot shows that the leakage current is *not* strongly voltage dependent or, conversely, R_{GK} may *not* be increased for derate.

While the leakage current is not voltage dependent, it is very temperature dependent. The plot in Figure 3.23(b) of T_J, junction temperature, versus R_{GK} taken at V_{DRM}, the maximum forward blocking voltage shows this dependence. For each device (2N6329 again) the leakage current, I_{AK}, was measured at the maximum operating junction temperature of 110°C, then the junction temperature was reduced and R_{GK} varied to re−establish that same leakage current. The plot shows that the leakage current is strongly dependent on junction temperature. Conversely R_{GK} may be increased for derated temperature.

A conservative rule of thumb is that leakage doubles every 10°C. If all the current flows out through R_{GK}, triggering will not occur until the voltage across R_{GK} reaches V_{GT}. This implies an allowed doubling of the resistor for every 10° reduction in maximum junction temperature. However, this rule should be applied with caution. Static dV/dt may require a smaller resistor than expected. Also the leakage current does not always follow the 10° rule below 70°C because of surface effects.

To summarize, the leakage current in a sensitive gate SCR is much more temperature sensitive than voltage sensitive. Operation at lower junction temperatures allows an increase in the gate−cathode resistor which makes the SCR−resistor combination more "sensitive."

Figure 3.23(b). T_J versus R_{GK} (Typical) for Constant Leakage Current
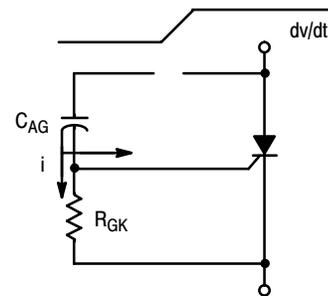
Figure 3.23(c). dv/dt Firing of an SCR

Figure 3.23(a). V_{AK} versus R_{GK} (Typical) for Constant Leakage Current
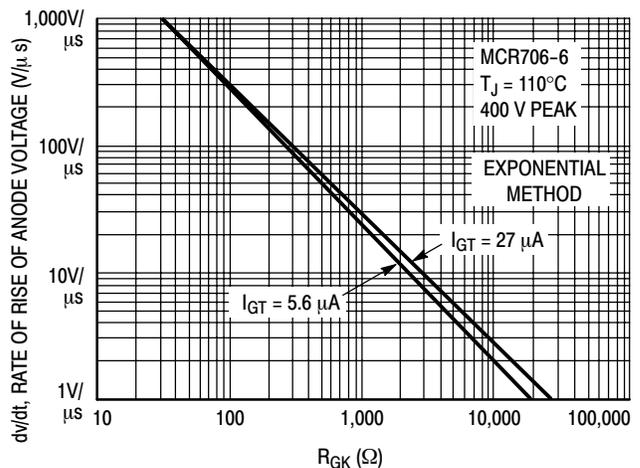
Figure 3.23(d). Static dv/dt as a function of Gate−Cathode Resistance on two devices with different sensitivity.

RATE–OF–RISE OF ANODE VOLTAGE, dv/dt

An SCR's junctions exhibit capacitance due to the separation of charge when the device is in a blocking state. If an SCR is subjected to forward dv/dt, this capacitance can couple sufficient current into the SCR's gate to turn it on, as shown in Figure 3.23(c). R_{GK} acts as a diversionary path for the dv/dt current. (In larger SCRs, where the lateral gate resistance of the device limits the influence of R_{GK}, this path is provided by the resistive emitter shorts mentioned previously.) The gate–cathode resistor, then, might be expected to have some effect on the dv/dt performance of the SCR. Figure 3.23(d) confirms this behavior. The static dV/dt for two MCR706 devices varies over several powers of ten with changes in the gate–cathode resistance. Selection of the external resistor allows the designer to trade dynamic performance with the amount of drive current provided to the resistor–SCR combination. The sensitive–gate device with low R_{GK} provides performance approaching that of an equivalent non–sensitive SCR. This strong dependence does not exist with conventional shorted emitter SCRs because of their internal resistor. The conventional SCR cannot be made more sensitive, but the sensitive–gate device attributes can be reliably set with the resistor to any desired point along the sensitivity range. Low values of resistance make the dV/dt performance more uniform and predictable. The curves for two devices with different sensitivity diverge at high values of resistance because the device response becomes more dependent on its sensitivity. The resistor is the most important factor determining the static dV/dt capability of the product. Reverse biasing the gate also improves dV/dt. A 2N6241 improved by a factor of 50 with a 1 volt bias.

GATE CURRENT, I_{GT}

The total gate current that a gating circuit must supply is the sum of the current that the device itself requires to fire and the current flowing to circuit ground through R_{GK}, as shown in Figure 3.24. I_{GT}, the current required by the device so that it may fire, is usually specified by the device manufacturer as a maximum at some temperature (for the 2N6236 series it is 500 µA maximum at –40°C). The current flowing through R_{GK} is defined by the resistor value and by the *gate–to–cathode voltage* that the SCR needs to fire. This is 1 V maximum at –40°C for the 2N6237 series, for example.
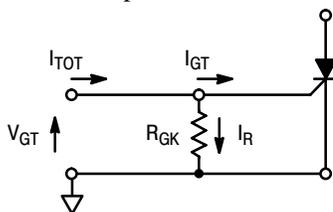
Figure 3.24. SCR and R_{GK} "Gate" Currents

GATE CURRENT, $I_{GT(min)}$

SCR manufacturers sometimes get requests for a sensitive–gate SCR specified with an $I_{GT(min)}$, that is, the maximum gate current that will *not* fire the device. This requirement conflicts with the basic function of a sensitive gate SCR, which is to fire at zero or very low gate current, $I_{GT(max)}$. Production of devices with a measurable $I_{GT(min)}$ is at best difficult and deliveries can be sporadic!

One reason for an $I_{GT(min)}$ requirement might be some measurable off–state gating circuit leakage current, perhaps the collector leakage of a driving transistor. Such current can readily be bypassed by a suitably chosen R_{GK}. The V_{GT} of the SCR at the temperature in question can be estimated from Figure 3.25, an Ohm's Law calculation made, and the resistor installed to define this "won't fire" current. This is a repeatable design well in the control of the equipment designer.

GATE TRIGGER VOLTAGE, V_{GT}

The gate–cathode junction is a p–n silicon junction. So the gate trigger voltage follows the diode law and has roughly the same temperature coefficient as a silicon diode, –2mV/C. Figure 3.25 is a plot of V_{GT} versus temperature for typical sensitive gate SCRs. They are prone to triggering by noise coupled through the gate circuit because of their low trigger voltage. The smallest noise voltage margin occurs at maximum temperature and with the most sensitive devices.
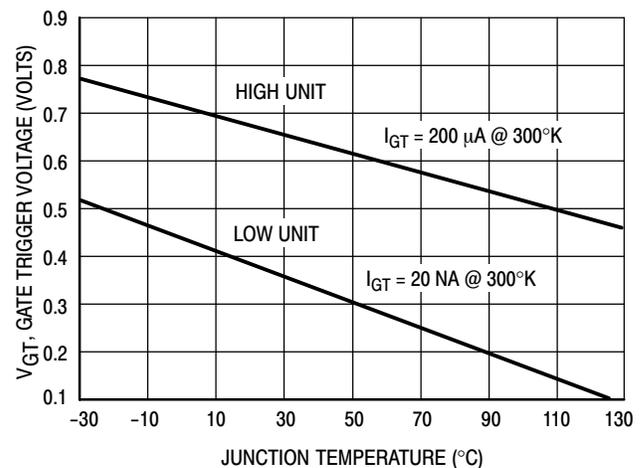
Figure 3.25. Typical V_{GT} vs T_J

HOLDING CURRENT, I_H

The holding current of an SCR is the minimum anode current required to maintain the device in the on state. It is usually specified as a maximum for a series of devices (for instance, 5 mA maximum at 25°C for the 2N6237 series). A particular device will turn off somewhere between this maximum and zero anode current and there is perhaps a 20−to−1 spread in each lot of devices.

Figure 3.26 shows the holding current increasing with decreasing R_{GK} as the resistor siphons off more and more of the regeneratively produced gate current when the device is in the latched condition.

Note that the gate−cathode resistor determines the holding current when it is less than 100 Ohms. SCR sensitivity is the determining factor when the resistor exceeds 1 meg Ohm. This allows the designer to set the holding current over a wide range of possible values using the resistor. Values typical of those in conventional non−sensitive devices occur when the external resistor is similar to their internal gate−cathode shorting resistance. The holding current uniformity also improves when the resistor is small.
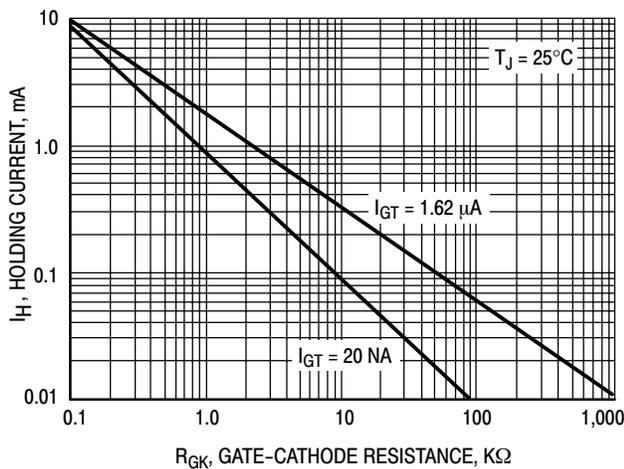
Figure 3.26. 2N5064 Holding Current

NOISE IMMUNITY

Changes in electromagnetic and electrostatic fields coupled into wires or printed circuit lines can trigger these sensitive devices, as can logic circuit glitches. The result is more serious than with a transistor since an SCR will latch on. Careful wire harness design (twisted pairs and adequate separation from high−power wiring) and printed circuit layout (gate and return runs adjacent to one another) can minimize potential problems. A gate cathode network consisting of a resistor and parallel capacitor also helps. The resistor provides a static short and is helpful with noise signals of any frequency. For example, with a

1,000 Ohm resistor, between 100 μA to 1 mA of noise current is necessary to generate enough voltage to fire the device. Adding a capacitor sized between 0.01 and 0.1 μF creates a noise filter and improves dV/dt by shunting dV/dt displacement current out through the gate terminal. These components must be placed as close as possible to the gate and cathode terminals to prevent lead inductance from making them ineffective. The use of the capacitor also requires the gate drive circuit to supply enough current to fire the SCR without excessive time delay. This is particularly important in applications with rapidly rising (di/dt > 50 A/μs) anode current where a fast rise high amplitude gate pulse helps to prevent di/dt damage to the SCR.

Reverse gate voltage can cause unwanted turn−off of the SCR. Then the SCR works like a gate turn−off thyristor. Turn−off by the gate signal is more probable with small SCRs because of the short distance between the cathode and gate regions. Whether turn−off occurs or not depends on many variables. Even if turn−off does not occur, the effect of high reverse gate current is to move the conduction away from the gate, reducing the effective cathode area and surge capability. Suppressing the reverse gate voltage is particularly important when the gate pulse duration is less than 1 microsecond. Then the part triggers by charge instead of current so halving of the gate pulse width requires double the gate current. Capacitance coupled gate drive circuits differentiate the gate pulse (Figure 3.27) leading to a reverse gate spike. The reverse gate voltage rating should not be exceeded to prevent avalanche damage.

This discussion has shown that the use of R_{GK}, the gate−cathode resistor, has many implications. Clear understanding of its need and its influence on the performance of the sensitive gate SCR will enable the designer to have better control of his circuit designs using this versatile part.
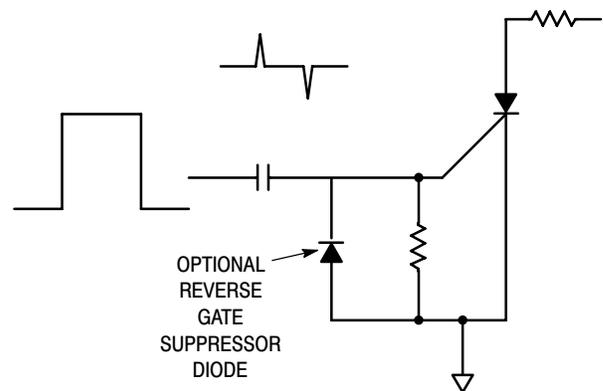
Figure 3.27. Capacitance Coupled Gate Drive

DRIVERS: PROGRAMMABLE UNIJUNCTION TRANSISTORS

The programmable unijunction transistor (PUT) is a four layer device similar to an SCR. However, gating is with respect to the anode instead of the cathode. An external resistive voltage divider accurately sets the triggering voltage and allows its adjustment. The PUT finds limited application as a phase control element and is most often used in long duration or low battery drain timer circuits where its high sensitivity permits the use of large timing resistors and small capacitors. Like an SCR, the PUT is a conductivity modulated device capable of providing high current output pulses.

OPERATION OF THE PUT

The PUT has three terminals, an anode (A), gate (G), and cathode (K). The symbol and a transistor equivalent circuit are shown in Figure 3.28. As can be seen from the equivalent circuit, the device is actually an anode–gated SCR. This means that if the gate is made negative with respect to the anode, the device will switch from a blocking state to its on state.
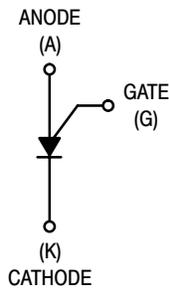
**Figure 3.28(a).
PUT Symbol**
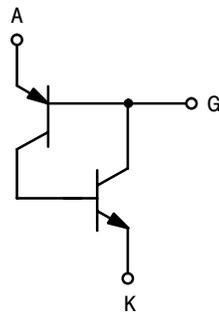
**Figure 3.28(b).
Transistor Equivalent**

The PUT is a complementary SCR when its anode is connected like an SCR's cathode and the circuit bias voltages are reversed. Negative resistance terminology describes the device characteristics because of the traditional application circuit. An external reference voltage must be maintained at the gate terminal. A typical relaxation type oscillator circuit is shown in Figure 3.29(a). The voltage divider shown is a typical way of obtaining the gate reference. In this circuit, the characteristic curve looking into the anode–cathode terminals would appear as shown in Figure 3.29(b). The peak and valley points are stable operating points at either end of a negative resistance region. The peak point voltage (V_P) is essentially the same as the external gate reference, the only difference being the gate diode drop. Since the reference is circuit and not device dependent, it may be varied, and in this way, V_P is programmable.

In characterizing the PUT, it is convenient to speak of the Thevenin equivalent circuit for the external gate voltage (V_S) and the equivalent gate resistance (R_G). The parameters are defined in terms of the divider resistors (R1 and R2) and supply voltage as follows:

$$V_S = R1 \ V1/(R1 + R2)$$
$$R_G = R1 \ R2/(R1 + R2)$$

Most device parameters are sensitive to changes in V_S and R_G. For example, decreasing R_G will cause peak and valley currents to increase. This is easy to see since R_G actually shunts the device and will cause its sensitivity to decrease.

CHARACTERISTICS OF THE PUT

Table 3.1 is a list of typical characteristics of ON Semiconductor's 2N6027/2N6028 of programmable unijunction transistors. The test circuits and test conditions shown are essentially the same as for the data sheet characteristics. The data presented here defines the static curve shown in Figure 3.29(b) for a 10 V gate reference (V_S) with various gate resistances (R_G). It also indicates the leakage currents of these devices and describes the output pulse. Values given are for 25°C unless otherwise noted.
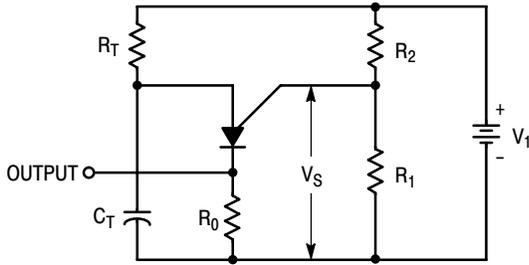
Figure 3.29(a). Typical Oscillator Circuit
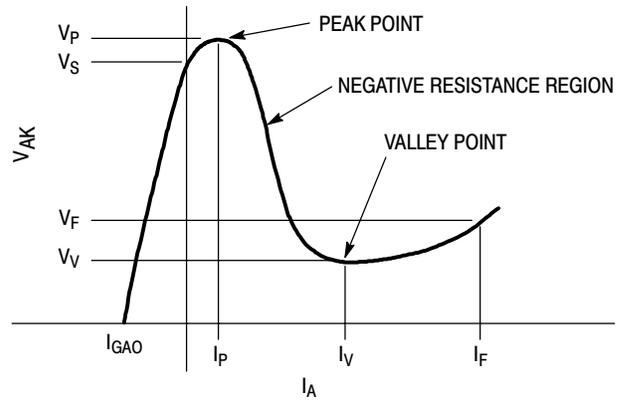
Figure 3.29(b). Static Characteristics

Table 3.1. Typical PUT Characteristics

Symbol	Test Circuit Figure	Test Conditions	2N6027	2N6028	Unit
I_P	3.30	$R_G = 1\ m\Omega$ $R_G = 10\ k\Omega$	1.25 4	0.08 0.70	μA μA
I_V	3.30	$R_G = 1\ M\Omega$ $R_G = 10\ k\Omega$	18 150	18 150	μA μA
V_{AG}		(See Figure 3.31)			
I_{GAO}		$V_S = 40\ V$	(See Figure 3.32)		
I_{GKS}		$V_S = 40\ V$	5	5	nA
V_F	Curve Tracer Used	$I_F = 50\ mA$	0.8	0.8	V
V_O	3.33		11	11	V
t_r	3.34		40	40	ns

PEAK POINT CURRENT, (I_P)

The peak point is indicated graphically by the static curve. Reverse anode current flows with anode voltages less than the gate voltage (V_S) because of leakage from the bias network to the charging network. With currents less than I_P, the device is in a blocking state. With currents above I_P, the device goes through a negative resistance region to its on state.

The charging current, or the current through a timing resistor, must be greater than I_P at V_P to insure that a device will switch from a blocking to an on state in an oscillator circuit. For this reason, maximum values of I_P are given on the data sheet. These values are dependent on V_S temperature, and R_G. Typical curves on the data sheet indicate this dependence and must be consulted for most applications.

The test circuit in Figure 3.30 is a sawtooth oscillator which uses a 0.01 μF timing capacitor, a 20 V supply, an adjustable charging current, and equal biasing resistors (R). The two biasing resistors were chosen to given an equivalent R_G of 1 MΩ and 10 kΩ. The peak point current was measured with the device off just prior to oscillation as detected by the absence of an output voltage pulse. The 2N5270 held effect transistor circuit is used as a current source. A variable gate voltage supply was used to control this current.

VALLEY POINT CURRENT, (I_V)

The valley point is indicated graphically in Figure 3.28. With currents slightly less than I_V, the device is in an unstable negative resistance state. A voltage minimum occurs at I_V and with higher currents, the device is in a stable on state.

When the device is used as an oscillator, the charging current or the current through a timing resistor must be less than I_V at the valley point voltage (V_V). For this reason, minimum values for I_V are given on the data sheet for $R_G = 10$ kΩ. With $R_G = 1$ MΩ, a reasonable "low" is 2 μA for all devices.

When the device is used in the latching mode, the anode current must be greater than I_V. Maximum values for I_V are given with $R_G = 1$ MΩ. All devices have a reasonable "high" of 400 μA I_V with $R_G = 10$ kΩ.

PEAK POINT VOLTAGE, (V_P)

The unique feature of the PUT is that the peak point voltage can be determined externally. This programmable feature gives this device the ability to function in voltage controlled oscillators or similar applications. The triggering or peak point voltage is approximated by

$$V_P \approx V_T + V_S,$$

where V_S is the unloaded divider voltage and V_T is the offset voltage. The actual offset voltage will always be higher than the anode–gate voltage V_{AG}, because I_P flows out of the gate just prior to triggering. This makes $V_T = V_{AG} + I_P R_G$. A change in R_G will affect both V_{AG} and $I_P R_G$ but in opposite ways. First, as R_G increases, I_P decreases and causes V_{AG} to decrease. Second, since I_P does not decrease as fast as R_G increases, the $I_P R_G$ product will increase and the actual V_T will increase. These second order effects are difficult to predict and measure. Allowing V_T to be 0.5 V as a first order approximation gives sufficiently accurate results for most applications.

The peak point voltage was tested using the circuit in Figure 3.30 and a scope with 10 MΩ input impedance across the PUT. A Tektronix, Type W plug–in was used to determine this parameter.

FORWARD ANODE–GATE VOLTAGE, (V_{AG})

The forward anode–to–gate voltage drop affects the peak point voltage as was previously discussed. The drop is essentially the same as a small signal silicon diode and is plotted in Figure 3.31. The voltage decreases as current decreases, and the change in voltage with temperature is greater at low currents. At 10 nA the temperature coefficient is about −2.4 V/°C and it drops to about −1.6 mV/°C at 10 mA. This information is useful in applications where it is desirable to temperature compensate the effect of this diode.

GATE–CATHODE LEAKAGE CURRENT, (I_{GKS})

The gate–to–cathode leakage current is the current that flows from the gate to the cathode with the anode shorted to the cathode. It is actually the sum of the open circuit gate–anode and gate–cathode leakage currents. The shorted leakage represents current that is shunted away from the voltage divider.

NOTES: 1) VARIOUS SENSE RESISTORS (R_S) ARE USED TO KEEP THE SENSE VOLTAGE NEAR 1 Vdc.
2) THE GATE SUPPLY (V_G) IS ADJUSTED FROM ABOUT −0.5 V TO +20 V.

Figure 3.30. Test Circuit for I_P, V_P and I_V

GATE–ANODE LEAKAGE CURRENT, (I_{GAO})

The gate–to–anode leakage current is the current that flows from the gate to the anode with the cathode open. It is important in long duration timers since it adds to the charging current flowing into the timing capacitor. The typical leakage currents measured at 40 V are shown in Figure 3.32. Leakage at 25°C is approximately 1 nA and the current appears to double for about every 10°C rise in temperature.

FORWARD VOLTAGE, (V_F)

The forward voltage (V_F) is the voltage drop between the anode and cathode when the device is biased on. It is the sum of an offset voltage and the drop across some internal dynamic impedance which both tend to reduce the output pulse. The typical data sheet curve shows this impedance to be less than 1 ohm for up to 2 A of forward current.

PEAK OUTPUT VOLTAGE, (V_O)

The peak output voltage is not only a function of V_P, V_F and dynamic impedance, but is also affected by switching speed. This is particularly true when small capacitors (less than 0.01 μF) are used for timing since they lose part of their charge during the turn on interval. The use of a relatively large capacitor (0.2 μF) in the test circuit of Figure 3.33 tends to minimize this last effect. The output voltage is measured by placing a scope across the 20 ohm resistor which is in series with the cathode lead.

RISE TIME, (t_r)

Rise time is a useful parameter in pulse circuits that use capacitive coupling. It can be used to predict the amount of current that will flow between these circuits. Rise time is specified using a fast scope and measuring between 0.6 V and 6 V on the leading edge of the output pulse.

MINIMUM AND MAXIMUM FREQUENCY

In actual tests with devices whose parameters are known, it is possible to establish minimum and maximum values of timing resistors that will guarantee oscillation. The circuit under discussion is a conventional RC relaxation type oscillator.

To obtain maximum frequency, it is desirable to use low values of capacitance (1000 pF) and to select devices and bias conditions to obtain high I_V. It is possible to use stray capacitance but the results are generally unpredictable. The minimum value of timing resistance is obtained using the following rule of thumb:

$$R_{(min)} = 2(V_1 - V_V)/I_V$$

where the valley voltage (V_V) is often negligible.

To obtain minimum frequency, it is desirable to use high values of capacitance (10 μF) and to select devices and bias conditions to obtain low I_P. It is important that the capacitor leakage be quite low. Glass and mylar dielectrics are often used for these applications. The maximum timing resistor is as follows:

$$R_{(max)} = (V_I - V_P)/2I_P$$

In a circuit with a fixed value of timing capacitance, our most sensitive PUT, the 2N6028, offers the largest dynamic frequency range. Allowing for capacitance and bias changes, the approximate frequency range of a PUT is from 0.003 Hz to 2.5 kHz.
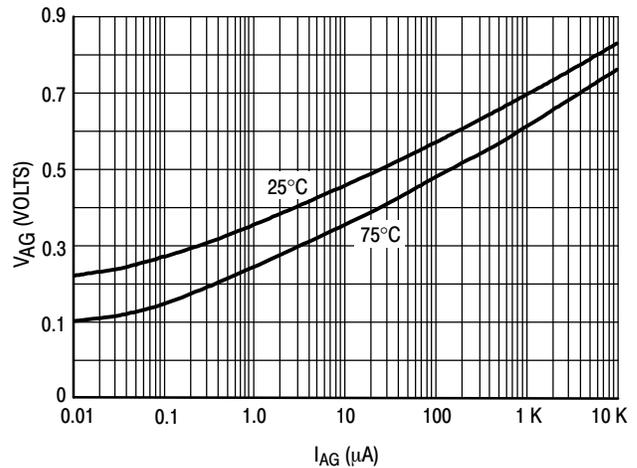
Figure 3.31. Voltage Drop of 2N6027 Series
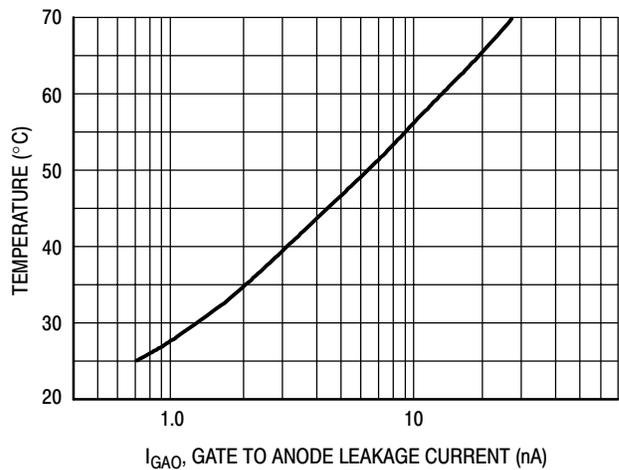
Figure 3.32. Typical Leakage Current of the 2N6027, 2N6028 Reverse Voltage Equals 40 V
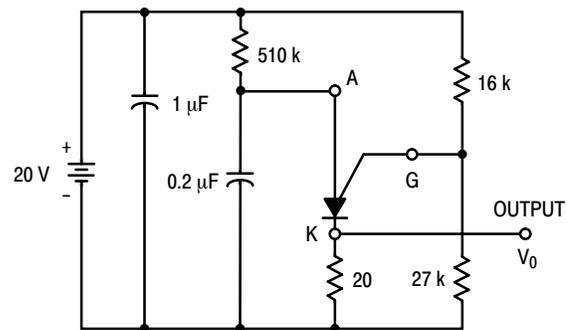
Figure 3.33. PUT Test Circuit for Peak Output Voltage (V_o)
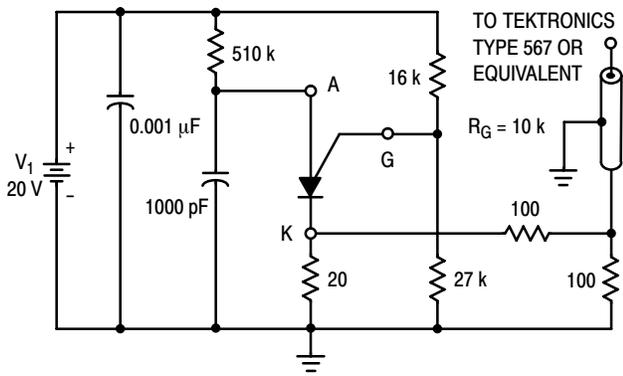
Figure 3.34. t_r Test Circuit for PUTs

length of the output pulse as temperature increases is responsible for this result. Since this parameter has not been characterized, it is obvious that temperature compensation is more practical with relatively low frequency oscillators.

Various methods of compensation are shown in Figure 3.36. In the low cost diode–resistor combination of 3.36(a), the diode current is kept small to cause its temperature coefficient to increase. In 3.36(b), the bias current through the two diodes must be large enough so that their total coefficient compensates for V_{AG}. The transistor approach in 3.36(c) can be the most accurate since its temperature coefficient can be varied independently of bias current.

Figure 3.35. Uncompensated Oscillator

TEMPERATURE COMPENSATION

The PUT with its external bias network exhibits a relatively small frequency change with temperature. The uncompensated RC oscillator shown in Figure 3.35 was tested at various frequencies by changing the timing resistor R_T. At discrete frequencies of 100, 200, 1000 and 2000 Hz, the ambient temperature was increased from 25° to 60°C. At these low frequencies, the negative temperature coefficient of V_{AG} predominated and caused a consistent 2% increase in frequency. At 10 kHz, the frequency remained within 1% over the same temperature range. The storage time phenomenon which increases the

(a) DIODE–RESISTOR

(b) DUAL–DIODE   (c) TRANSISTOR

Figure 3.36. Temperature Compensation Techniques

SECTION 4
THE SIDAC, A NEW HIGH VOLTAGE BILATERAL TRIGGER

Edited and Updated

The SIDAC is a high voltage bilateral trigger device that extends the trigger capabilities to significantly higher voltages and currents than have been previously obtainable, thus permitting new, cost-effective applications. Being a bilateral device, it will switch from a blocking state to a conducting state when the applied voltage of either polarity exceeds the breakover voltage. As in other trigger devices, (SBS, Four Layer Diode), the SIDAC switches through a negative resistance region to the low voltage on-state (Figure 4.1) and will remain on until the main terminal current is interrupted or drops below the holding current.

SIDAC's are available in the large MKP3V series and economical, easy to insert, small MKP1V series axial lead packages. Breakdown voltages ranging from 104 to 280 V are available. The MKP3V devices feature bigger chips and provide much greater surge capability along with somewhat higher RMS current ratings.

The high-voltage and current ratings of SIDACs make them ideal for high energy applications where other trigger devices are unable to function alone without the aid of additional power boosting components.

The basic SIDAC circuit and waveforms, operating off of ac are shown in Figure 4.2. Note that once the input voltage exceeds $V_{(BO)}$, the device will switch on to the forward on-voltage V_{TM} of typically 1.1 V and can conduct as much as the specified repetitive peak on-state current I_{TRM} of 20 A (10 μs pulse, 1 kHz repetition frequency).

$$R_S = \frac{(V_{(BO)} - V_S)}{(I_S - I_{(BO)})}$$
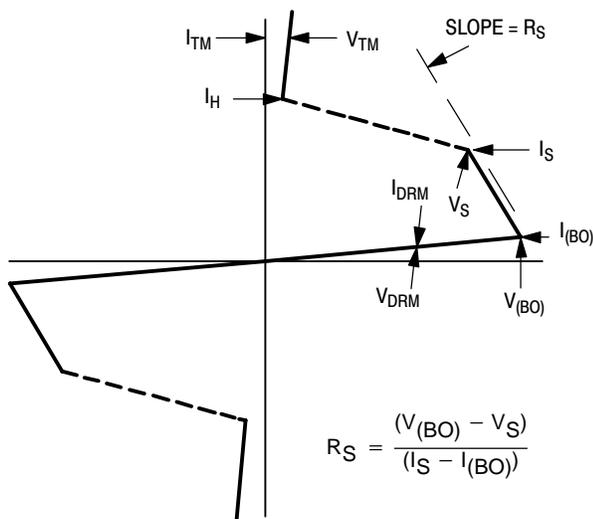
Figure 4.1(a). Idealized SIDAC V-I Characteristics
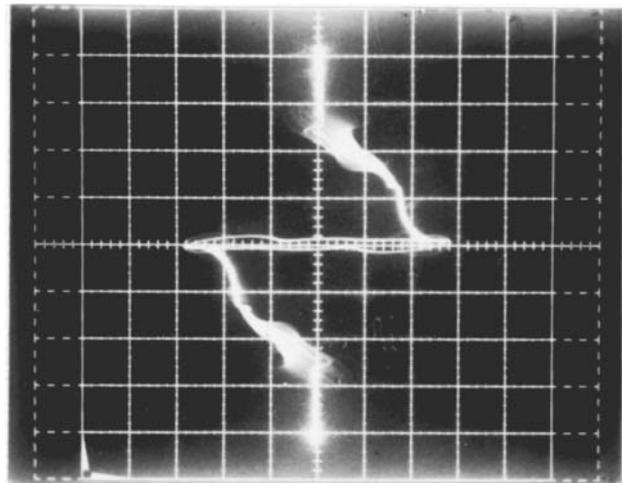
Figure 4.1(b). Actual MKP1V130 V-I Characteristic. Horizontal: 50 V/Division. Vertical: 20 mA/Division. (0,0) at Center. R_L = 14 k Ohm.
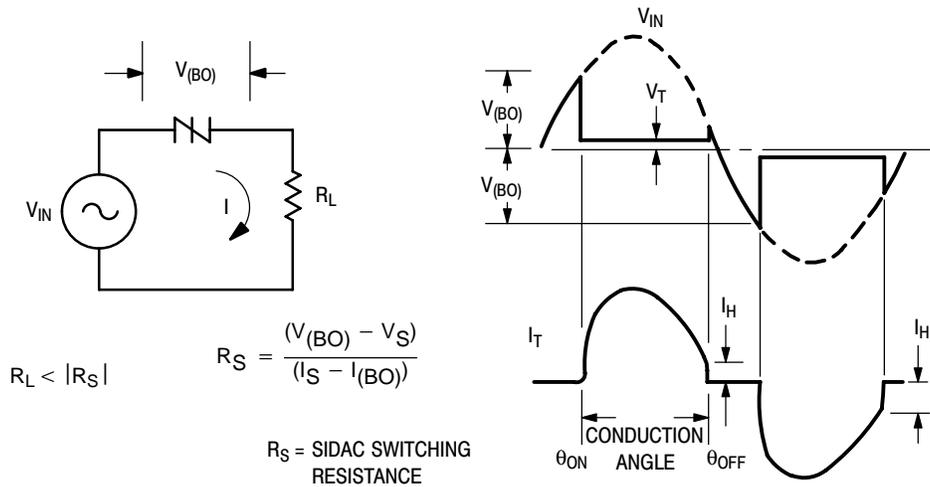
Figure 4.2. Basic SIDAC Circuit and Waveforms

Operation from an AC line with a resistive load can be analyzed by superimposing a line with slope $= -1/R_L$ on the device characteristic. When the power source is AC, the load line can be visualized as making parallel translations in step with the instantaneous line voltage and frequency. This is illustrated in Figure 4.3 where v_1 through v_5 are the instantaneous open circuit voltages of the AC generator and i_1 through i_5 are the corresponding short circuit currents that would result if the SIDAC was not in the circuit. When the SIDAC is inserted in the circuit, the current that flows is determined by the intersection of the load line with the SIDAC characteristic. Initially the SIDAC blocks, and only a small leakage current flows at times 1 through 4. The SIDAC does not turn-on until the load line supplies the breakover current ($I_{(BO)}$) at the breakover voltage ($V_{(BO)}$).

If the load resistance is less than the SIDAC switching resistance, the voltage across the device will drop quickly as shown in Figure 4.2. A stable operating point (V_T, I_T) will result if the load resistor and line voltage provide a current greater than the latching value. The SIDAC remains in an "on" condition until the generator voltage causes the current through the device to drop below the holding value (I_H). At that time, the SIDAC switches to the point (V_{off}, I_{off}) and once again only a small leakage current flows through the device.
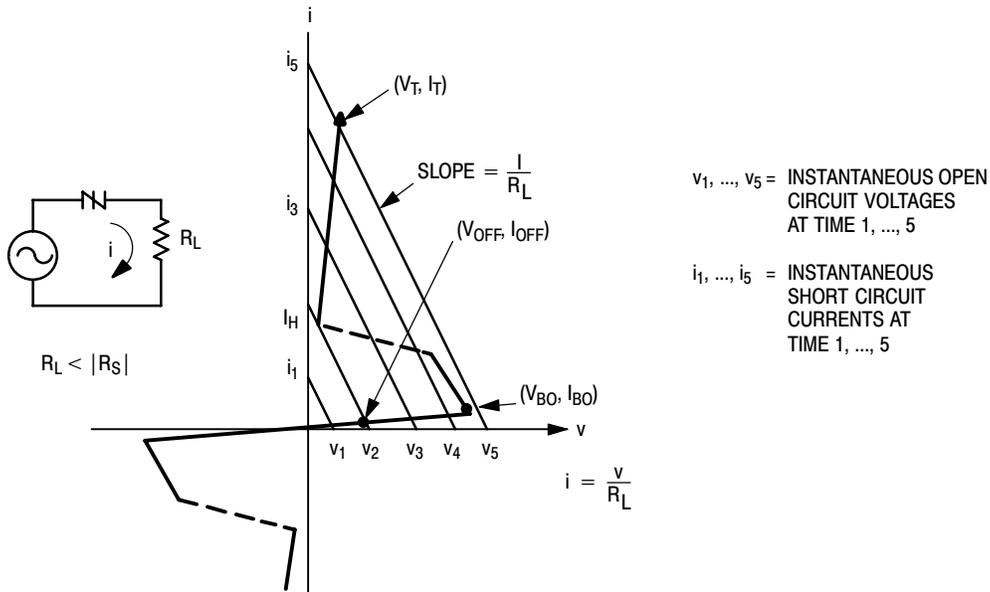
Figure 4.3. Load Line for Figure 4.2. (1/2 Cycle Shown.)

Figure 4.4 illustrates the result of operating a SIDAC with a resistive load greater than the magnitude of its switching resistance. The behavior is similar to that described in Figures 4.2 and 4.3 except that the turn-on and turn-off of the SIDAC is neither fast nor complete. Stable operating points on the SIDAC characteristics between $(V_{(BO)}, I_{(BO)})$ and (V_S, I_S) result as the generator voltage increases from v_2 to v_4. The voltage across the SIDAC falls only partly as the loadline sweeps through this region. Complete turn-on of the SIDAC to (V_T, I_T) does not occur until the load line passes through the point (V_S, I_S). The load line illustrated in Figure 4.4 also results in incomplete turn-off. When the current drops below I_H, the operating point switches to (V_{off}, I_{off}) as shown on the device characteristic.
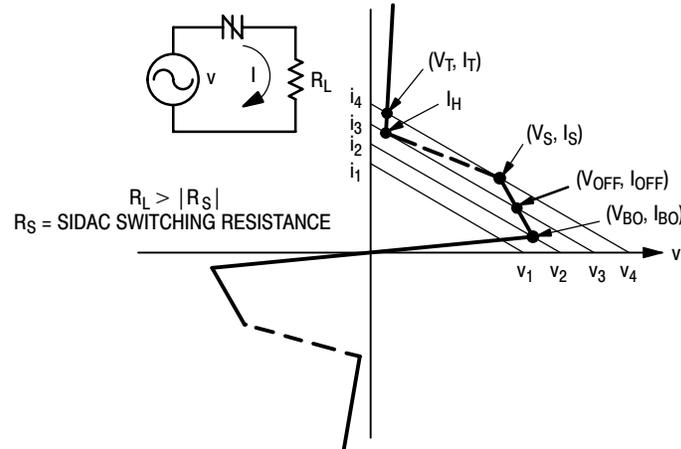
Figure 4.4. High Resistance Load Line with Incomplete Switching

The switching current and voltage can be 2 to 3 orders of magnitude greater than the breakover current and on-state voltage. These parameters are not as tightly specified as V_{BO} and I_{BO}. Consequently operation of the SIDAC in the state between fully on and fully off is undesirable because of increased power dissipation, poor efficiency, slow switching, and tolerances in timing.

Figure 4.5 illustrates a technique which allows the use of the SIDAC with high impedance loads. A resistor can be placed around the load to supply the current required to latch the SIDAC. Highly inductive loads slow the current rise and the turn-on of the SIDAC because of their L/R time constant. The use of shunt resistor around the load will improve performance when the SIDAC is used with inductive loads such as small transformers and motors.

The SIDAC can be used in oscillator applications. If the load line intersects the device characteristic at a point where the total resistance $(R_L + R_S)$ is negative, an unstable operating condition with oscillation will result. The resistive load component determines steady-state behavior. The reactive components determine transient behavior. Figure 4.10 shows a SIDAC relaxation oscillator application. The wide span between I_{BO} and I_H makes the SIDAC easy to use. Long oscillation periods can be achieved with economical capacitor sizes because of the low device $I_{(BO)}$.

Z1 is typically a low impedance. Consequently the SIDAC's switching resistance is not important in this application. The SIDAC will switch from a blocking to full on-state in less than a fraction of a microsecond.

The timing resistor must supply sufficient current to fire the SIDAC but not enough current to hold the SIDAC in an on-state. These conditions are guaranteed when the timing resistor is selected to be between R_{max} and R_{min}.

For a given time delay, capacitor size and cost is minimized by selecting the largest allowable timing resistor. R_{max} should be determined at the lowest temperature of operation because $I_{(BO)}$ increases then. The load line corresponding to R_{max} passes through the point $(V_{(BO)}, I_{(BO)})$ allowing the timing resistor to supply the needed breakover current at the breakover voltage. The load line for a typical circuit design should enclose this point to prevent sticking in the off state.

Requirements for higher oscillation frequencies and greater stored energy in the capacitor result in lower values for the timing resistor. R_{min} should be determined at the highest operating temperature because I_H is lower then. The load line determined by R and V_{in} should pass below I_H on the device characteristic or the SIDAC will stick in the on-state after firing once. I_H is typically more than 2 orders of magnitude greater than I_{BO}. This makes the SIDAC well suited for operation over a wide temperature span.

SIDAC turn-off can be aided when the load is an under-damped oscillatory CRL circuit. In such cases, the SIDAC current is the sum of the currents from the timing resistor and the ringing decay from the load. SIDAC turn-off behavior is similar to that of a TRIAC where turn-off will not occur if the rate of current zero crossing is high. This is a result of the stored charge within the volume of the device. Consequently, a SIDAC cannot be force commuted like an SCR. The SIDAC will pass a ring wave of sufficient amplitude and frequency. Turn-off requires the device current to approach the holding current gradually. This is a complex function of junction temperature, holding current magnitude, and the current wave parameters.

$R_{SL} < |R_S|$

TYPICAL:
R_{SL} = 2.7 k OHM
      10 WATT
R_S = 3 k OHM

R_{SL} = TURN-ON SPEED UP RESISTOR
R_S = SIDAC SWITCHING RESISTANCE
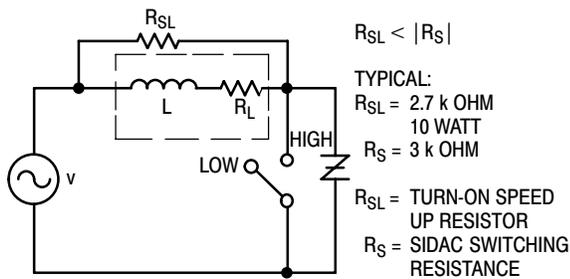
Figure 4.5. Inductive Load Phase Control

The simple SIDAC circuit can also supply switchable load current. However, the conduction angle is not readily controllable, being a function of the peak applied voltage and the breakover voltage of the SIDAC. As an example, for peak line voltage of about 170 V, at $V_{(BO)}$ of 115 V and a holding current of 100 mA, the conduction angle would be about 130°. With higher peak input voltages (or lower breakdown voltages) the conduction angle would correspondingly increase. For non-critical conduction angle, 1 A rms switching applications, the SIDAC is a very cost-effective device.

Figure 4.7 shows an example of a SIDAC used to phase control an incandescent lamp. This is done in order to lower the RMS voltage to the filament and prolong the life of the bulb. This is particularly useful when lamps are used in hard to reach locations such as outdoor lighting in signs where replacement costs are high. Bulb life span can be extended by 1.5 to 5 times depending on the type of lamp, the amount of power reduction to the filament, and the number of times the lamp is switched on from a cold filament condition.

The operating cost of the lamp is also reduced because of the lower power to the lamp; however, a higher wattage bulb is required for the same lumen output. The maximum possible energy reduction is 50% if the lamp wattage is not increased. The minimum

conduction angle is 90° because the SIDAC must switch on before the peak of the line voltage. Line regulation and breakover voltage tolerances will require that a conduction angle longer than 90° be used, in order to prevent lamp turn-off under low line voltage conditions. Consequently, practical conduction angles will run between 110° and 130° with corresponding power reductions of 10% to 30%.

In Figure 4.2 and Figure 4.7, the SIDAC switching angles are given by:

$$\theta_{ON} = SIN^{-1} (V_{(BO)}/V_{pk})$$

where V_{pk} = Maximum Instantaneous Line Voltage

$$\theta_{OFF} = 180 - SIN^{-1} \left(\frac{(I_H \cdot R_L) + V_T}{V_{pk}} \right)$$

where θ_{ON}, θ_{OFF} = Switching Angles in degrees
       V_T = 1 V = Main Terminal Voltage at $I_T = I_H$

Generally the load current is much greater than the SIDAC holding current. The conduction angle then becomes 180° minus $\theta_{(on)}$.

Rectifiers have also been used in this application to supply half wave power to the lamp. SIDAC's prevent the flicker associated with half-wave operation of the lamp. Also, full wave control prevents the introduction of a DC component into the power line and improves the color temperature of the light because the filament has less time to cool during the off time.

The fast turn-on time of the SIDAC will result in the generation of RFI which may be noticeable on AM radios operated in the vicinity of the lamp. This can be prevented by the use of an RFI filter. A possible filter design is shown in Figure 4.5. This filter causes a ring wave of current through the SIDAC at turn-on time. The filter inductor must be selected for resonance at a frequency above the upper frequency limit of human hearing and as low below the start of the AM broadcast band as possible for maximum harmonic attenuation. In addition, it is important that the filter inductor be non-saturating to prevent dI/dT damage to the SIDAC. For additional information on filter design see page 92.
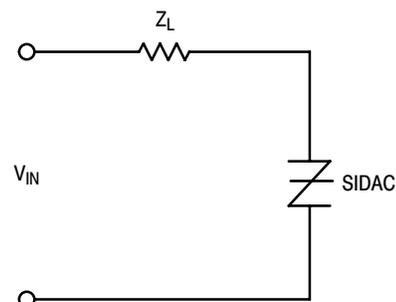
Figure 4.6. SIDAC Circuit
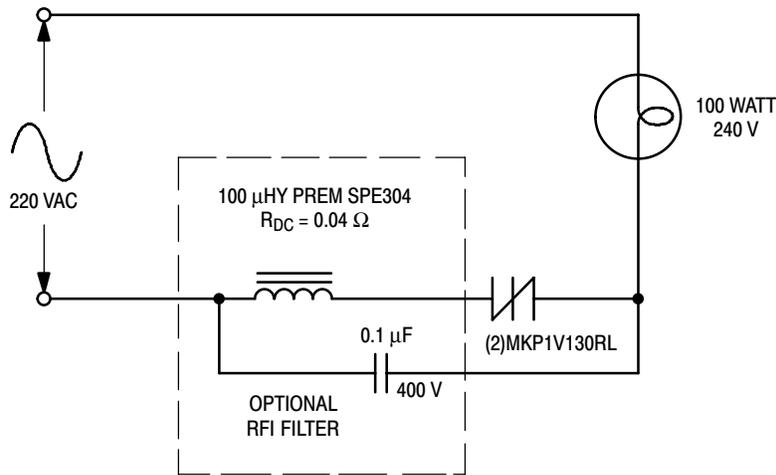
Figure 4.7. Long-Life Circuit for Incandescent Lamp

The sizing of the SIDAC must take into account the RMS current of the lamp, thermal properties of the SIDAC, and the cold start surge current of the lamp which is often 10 to 20 times the steady state load current. When lamps burn out, at the end of their operating life, very high surge currents which could damage the SIDAC are possible because of arcing within the bulb. The large MKP3V device is recommended if the SIDAC is not to be replaced along with the bulb.

Since the MKP3V series of SIDACs have relatively tight $V_{(BO)}$ tolerances (104 V to 115 V for the −115 device), other possible applications are over-voltage protection (OVP) and detection circuits. An example of this, as illustrated in Figure 4.8, is the SIDAC as a transient protector in the transformer-secondary of the medium voltage power supply, replacing the two more expensive back-to-back zeners or an MOV. The device can also be used across the output of the regulator (< 100 V) as a simple OVP, but for this application, the regulator must have current foldback or a circuit breaker (or fuse) to minimize the dissipation of the SIDAC.

Another example of OVP is the telephony applications as illustrated in Figure 4.9. To protect the Subscriber Loop Interface Circuit (SLIC) and its associated electronics from voltage surges, two SIDACs and two rectifiers are used for secondary protection (primary protection to 1,000 V is provided by the gas discharge tube across the lines). As an example, if a high positive voltage transient appeared on the lines, rectifier D1 (with a P.I.V. of 1,000 V) would block it and SIDAC D4 would conduct the surge to ground. Conversely, rectifier D2 and SIDAC D3 would protect the SLIC for negative transients. The SIDACs will not conduct when normal signals are present.

Being a negative resistance device, the SIDAC also can be used in a simple relaxation oscillator where the frequency is determined primarily by the RC time constant (Figure 4.10). Once the capacitor voltage reaches the SIDAC breakover voltage, the device will fire, dumping the charged capacitor. By placing the load in the discharge path, power control can be obtained; a typical load could be a transformer-coupled xeon flasher, as shown in Figure 4.12.
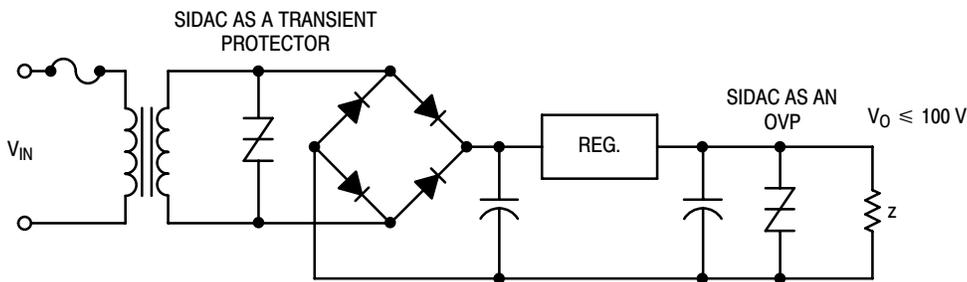
Figure 4.8. Typical Application of SIDACs as a Transient Protector and OVP in a Regulated Power Supply
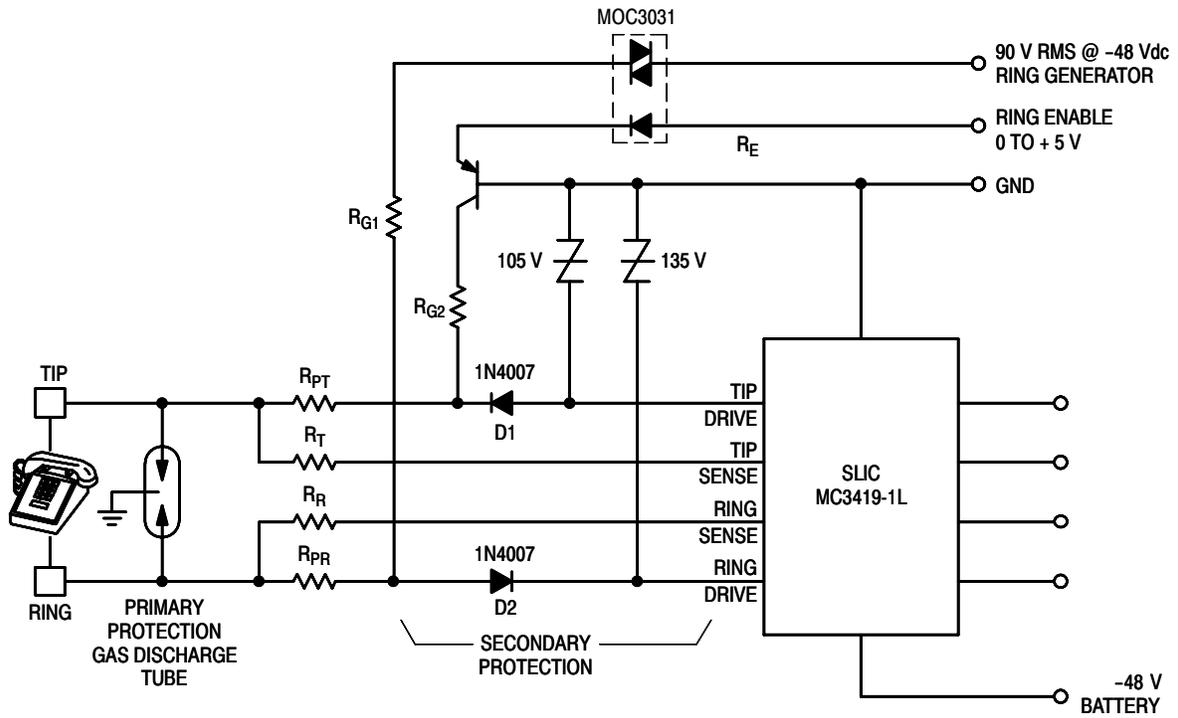
Figure 4.9. SIDACs Used for OVP in Telephony Applications

$$R_{MAX} \leq \frac{V_{IN} - V_{(BO)}}{I_{(BO)}}$$

$$R_{MIN} \geq \frac{V_{IN} - V_{TM}}{I_H}$$

$$t \cong RC \ln \left(\frac{I}{I - \dfrac{V_{BO}}{V_{IN}}} \right)$$
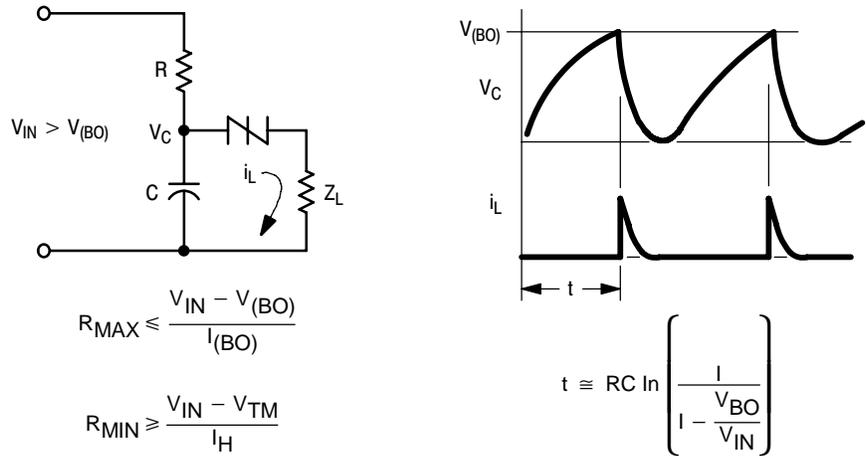
Figure 4.10. Relaxation Oscillator Using a SIDAC

SIDAC's provide an economical means for starting high intensity high pressure gas discharge lamps. These lamps are attractive because of their long operating life and high efficiency. They are widely used in outdoor lighting for these reasons.

Figure 4.13 illustrates how SIDAC's can be used in sodium vapor lamp starters. In these circuits, the SIDAC is used to generate a short duration (1 to 20 μs) high-voltage pulse of several KV or more which is timed by means of the RC network across the line to occur near the peak of the AC input line voltage. The high voltage pulse strikes the arc which lights the lamp.

In these circuits, an inductive ballast is required to provide a stable operating point for the lamp. The lamp is a negative resistance device whose impedance changes with current, temperature, and time over the first few minutes of operation. Initially, before the lamp begins to conduct, the lamp impedance is high and the full line voltage appears across it. This allows C to charge to the breakover voltage of the SIDAC, which then turns on discharging the capacitor through a step-up transformer generating the high voltage pulse. When the arc strikes, the voltage across the lamp falls reducing the available charging voltage across RC to the point where V_C no longer exceeds $V_{(BO)}$ and the SIDAC remains off. The low duty cycle lowers average junction temperature improving SIDAC reliability. Normal operation approximates non-repetitive conditions. However, if the lamp fails or is removed during replacement, operation of the SIDAC will be at the 60 Hz line frequency. The design of the circuit should take into account the resulting steady state power dissipation.
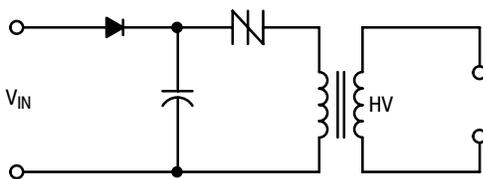
Figure 4.11. Typical Capacitor Discharge SIDAC Circuit
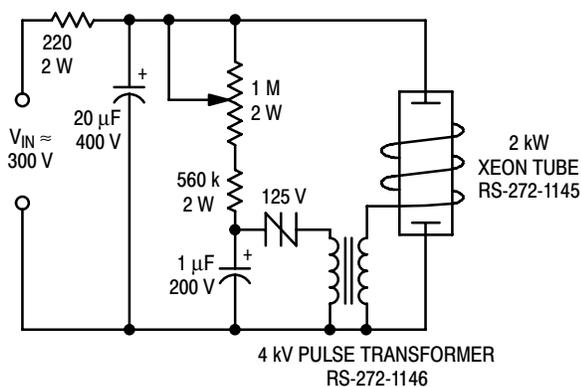
Figure 4.12. Xeon Flasher Using a SIDAC
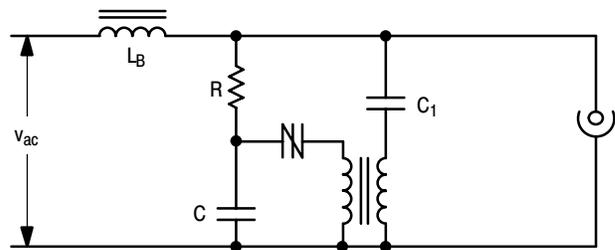
(a). Conventional HV Transformer
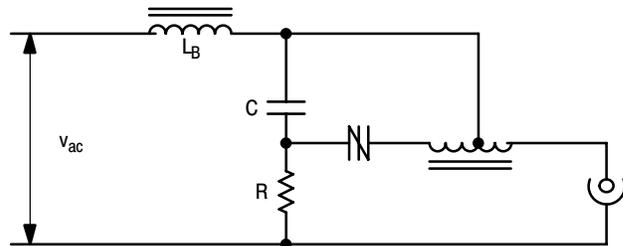
(b). H.V. Auto-Transformer
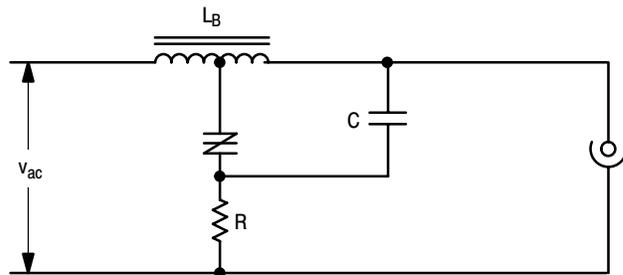
(c). Tapped Ballast Auto Transformer

Figure 4.13. Sodium Vapor Lamp Starter Circuits

Figure 4.14 illustrates a solid state fluorescent lamp starter using the SIDAC. In this circuit the ballast is identical to that used with the conventional glow-tube starter shown in Figure 4.15.

The glow tube starter consists of a bimetallic switch placed in series with the tube filaments which closes to energize the filaments and then opens to interrupt the current flowing through the ballast inductor thereby generating the high-voltage pulse necessary for starting. The mechanical glow-tube starter is the circuit component most likely to cause unreliable starting.
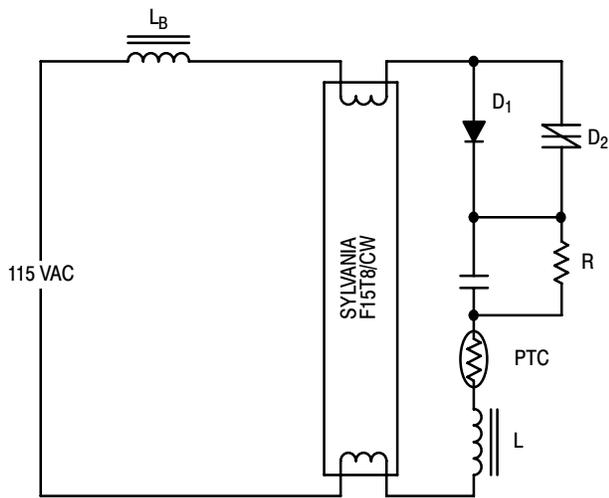
L_B	UNIVERSAL MFG CORP CAT200-H2 14-15-20-22 WATT BALLAST 325 mHY 28.9 Ω DCR
D1	1N4005 RECTIFIER
D2	(2) MKP1V130RL SIDAC
C	3 VFD 400 V
R	68 k OHMS 112 WATT
PTC	KEYSTONE CARBON COMPANY RL3006-50-40-25-PTO 50 OHMS/25°C
L	MICROTRAN QIL 50-F 50 mHY 11 OHMS

Figure 4.14. Fluorescent Starter Using SIDAC

The heating of the filaments causes thermonic emission of electrons from them. These electrons are accelerated along the length of the tube causing ionization of the argon gas within the tube. The heat generated by the starting current flow through the tube vaporizes the mercury droplets within the tube which then become ionized themselves causing the resistance and voltage across the tube to drop significantly. The drop in voltage across the tube is used to turn off the starting circuit and prevent filament current after the lamp is lit.

The SIDAC can be used to construct a reliable starter circuit providing fast, positive lamp ignition. The starter shown in Figure 4.14 generates high voltage by means of a series CRL charging circuit. The circuit is roughly analogous to a TRIAC snubber used with an inductive load, except for a lower damping factor and higher Q. The size of C determines the amount of filament heating current by setting the impedance in the filament circuit before ionization of the tube.

The evolution of this circuit can be understood by first considering an impractical circuit (Figure 4.16).

If L_B and C are adjusted for resonance near 60 Hz, the application of the AC line voltage will result in a charging current that heats the filaments and a voltage across the capacitor and tube that grows with each half-cycle of the AC line until the tube ionizes. Unfortunately, C is a large capacitor which can suddenly discharge through the tube causing high current pulses capable of destroying the tube filament. Also C provides a permanent path for filament current after starting. These factors cause short tube operating life and poor efficiency because of filament power losses. The impractical circuit must be modified to:

(1) Switch off the filament current after starting.

(2) Limit capacitor discharge current spikes.

In Figure 4.14 a parallel connected rectifier and SIDAC have been added in series with the capacitor C. The breakover voltage of the SIDAC is higher than the peak of the line voltage. Diode D1 is therefore necessary to provide a current path for charging C.

On the first half-cycle, C resonant charges through diode D1 to a peak voltage of about 210 V, and remains at that value because of the blocking action of the rectifier and SIDAC. During this time, the bleeder resistor R has negligible effect on the voltage across C because the RC time constant is long in comparison to the line period. When the line reverses, the capacitor voltage boosts the voltage across the SIDAC until breakover results. This results in a sudden step of voltage across the inductor L, causing resonant charging of the capacitor to a higher voltage on the 2nd half-cycle.
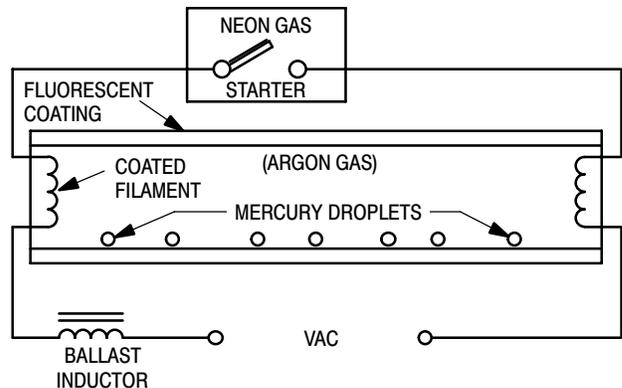
Figure 4.15. Fluorescent Lamp with Glow Tube Starter

$$f_O = \frac{1}{2a\sqrt{LC}} = 60 \text{ Hz}$$

$$Q = \frac{X_{LB}}{R_{TOTAL}}$$

$$V_{max} = Q\ VAC\ \sqrt{2} \qquad V_{START} < V_{MAX}$$
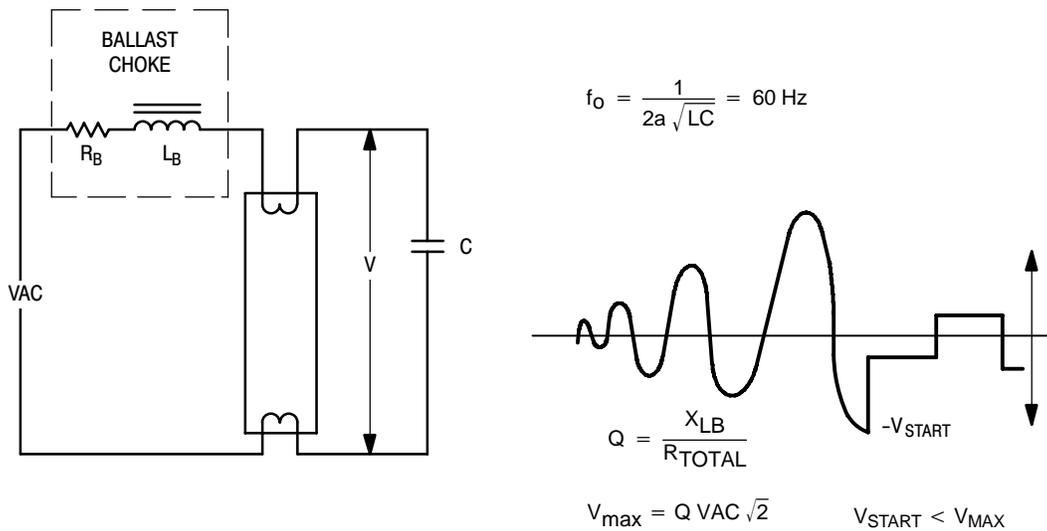
Figure 4.16. Impractical Starter Circuit
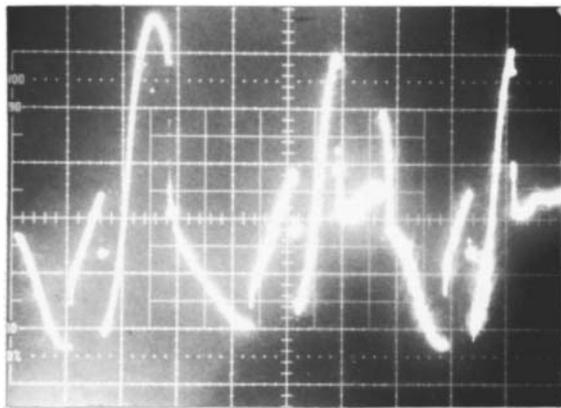
(a). 5 ms/DIVISION
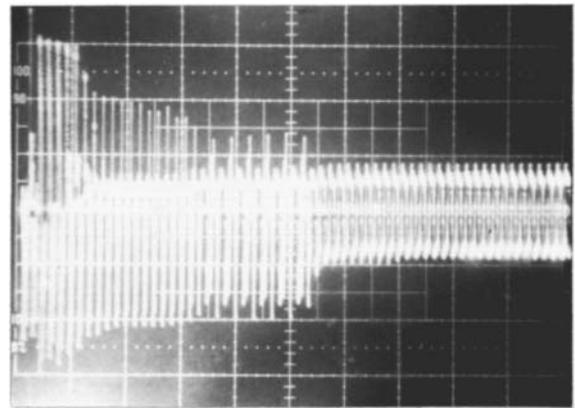
(b). 100 ms/DIVISION

Figure 4.17. Starting Voltage Across Fluorescent Tube 100 V/DIV
0 V AT CENTER
V_{Line} = 110 V

Several cycles of operation are necessary to approach steady state operating conditions. Figure 4.17 shows the starting voltage waveform across the tube.

The components R, PTC, and L serve the dual role of guarantying SIDAC turn-off and preventing capacitor discharge currents through the tube.

SIDAC's can also be used with auto-transformer ballasts. The high voltage necessary for starting is generated by the leakage autotransformer. The SIDAC is used to turn-on the filament transformer initially and turn it off after ionization causes the voltage across the tube to drop.

Figure 4.18 illustrates this concept. The resistor R can be added to aid turn-off of the SIDAC by providing a

small idle current resulting in a voltage drop across the impedance Z. The impedance Z could be a saturable reactor and or positive temperature coefficient thermistor. These components help to insure stability of the system comprised of the negative resistance SIDAC and negative resistance tube during starting, and promote turn off of the SIDAC.

The techniques illustrated in Figure 4.13 are also possible methods for generation of the necessary high-voltage required in fluorescent starting. The circuits must be modified to allow heating of the fluorescent tube cathodes if starting is to simulate the conditions existing when a glow tube is used.
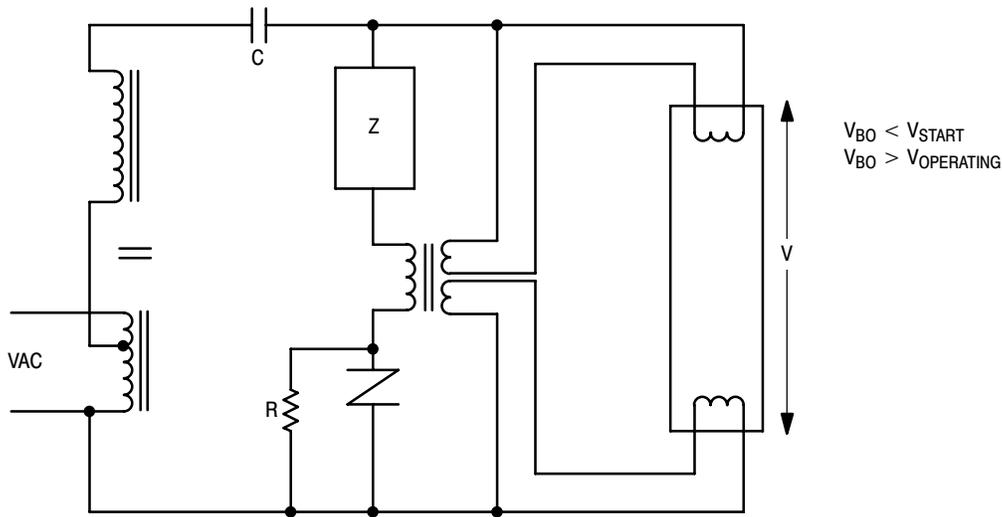
Figure 4.18. Fluorescent Starter Using SIDAC and Autotransformer Ballast

$V_{BO} < V_{START}$
$V_{BO} > V_{OPERATING}$

Table 4.1. Possible Sources for Thermistor Devices

Fenwal Electronics, 63 Fountain Street
Framingham MA 01701

Keystone Carbon Company, Thermistor Division
St. Marys, PA 15857

Thermometrics, 808 U.S. Highway 1
Edison, N.J. 08817

Therm-O-Disc, Inc. Micro Devices Product Group
1320 South Main Street, Mansfield, OH 44907

Midwest Components Inc., P.O Box 787
1981 Port City Boulevard, Muskegon, MI 49443

Nichicon (America) Corp., Dept. G
927 E. State Pkwy, Schaumburg, IL 60195

Thermistors are useful in delaying the turn-on or insuring the turn-off of SIDAC devices. Table 4.1 shows possible sources of thermistor devices.

Other high voltage nominal current trigger applications are:

• Gas or oil igniters
• Electric fences
• HV electrostatic air filters
• Capacitor Discharge ignitions

Note that all these applications use similar circuits where a charged capacitor is dumped to generate a high transformer secondary voltage (Figure 4.11).

In many cases, the SIDAC current wave can be approximated by an exponential or quasi-exponential current wave (such as that resulting from a critically damped or slightly underdamped CRL discharge circuit). The ques-

tion then becomes; how much "real world" surge current can the SIDAC sustain? The data sheet defines an I_{TSM} of 20 A, but this is for a 60 Hz, one cycle, peak sine wave whereas the capacitor discharge current waveform has a fast-rise time with an exponential fall time.

To generate the surge current curve of peak current versus exponential discharge pulse width, the test circuit of Figure 4.19 was implemented. It simulates the topology of many applications whereby a charged capacitor is dumped by means of a turned-on SIDAC to produce a current pulse. Timing for this circuit is derived from the nonsymmetrical CMOS astable multivibrator (M.V.) gates G1 and G2. With the component values shown, an approximate 20 second positive-going output pulse is fed to the base of the NPN small-signal high voltage transistor Q1, turning it on. The following high voltage PNP transistor is consequently turned on, allowing capacitor C1 to be charged through limiting resistor R1 in about 16 seconds. The astable M.V. then changes state for about 1.5 seconds with the positive going pulse from Gate 1 fed through integrator R2-C2 to Gate 3 and then Gate 4. The net result of about a 100 μs time delay from G4 is to ensure non-coincident timing conditions. This positive going output is then differentiated by C3-R3 to produce an approximate 1 ms, leading edge, positive going pulse which turns on NPN transistor Q3 and the following PNP transistor Q4. Thus, an approximate 15 mA, 1 ms pulse is generated for turning on SCR Q5 about 100 μs after capacitor charging transistor Q2 is turned off. The SCR now fires, discharging C1 through the current limiting resistor R4 and the SIDAC Device Under Test (D.U.T.). The peak current and its duration is set by the voltage V_C across capacitor C1 and current limiting resistor R4. The circuit has about a 240 V capability limited by C1, Q1 and Q2 (250 V, 300 V and 300 V respectively).
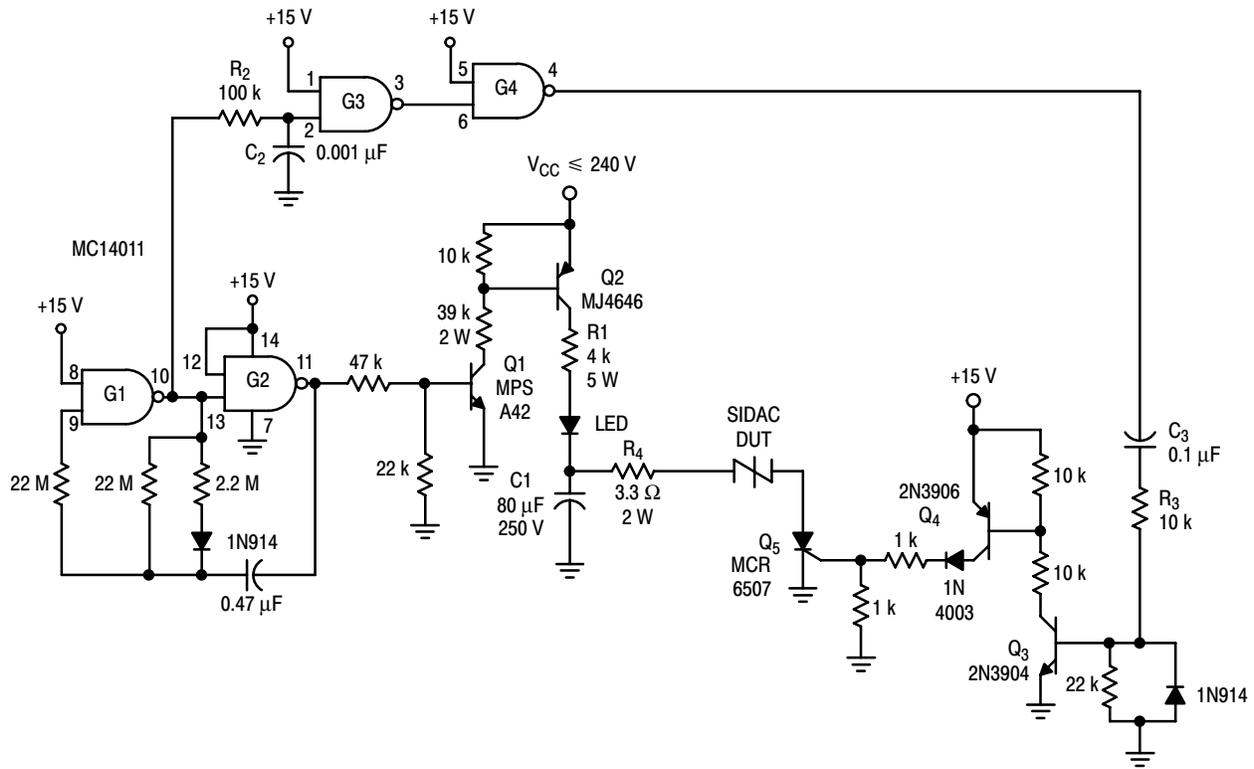
Figure 4.19. SIDAC Surge Tester

The SCR is required to fire the SIDAC, rather than the breakover voltage, so that the energy to the D.U.T. can be predictably controlled.

By varying V_C, C1 and R4, the surge current curve of Figure 4.20 was derived. Extensive life testing and adequate derating ensure that the SIDAC, when properly used, will reliably operate in the various applications.
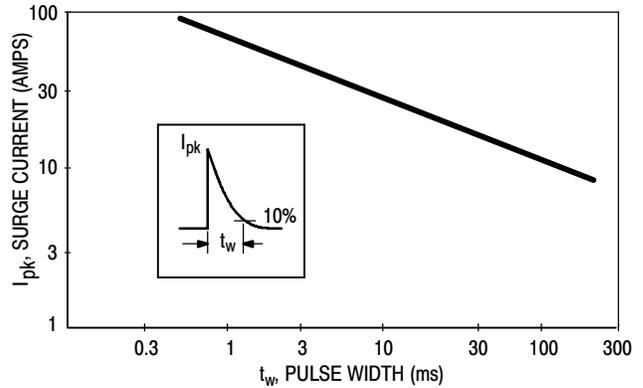
Figure 4.20. Exponential Surge Current Capability of the MKP3V SIDAC. Pulse Width versus Peak Current

SECTION 5
SCR CHARACTERISTICS

SCR TURN–OFF CHARACTERISTICS

In addition to their traditional role of power control devices, SCRs are being used in a wide variety of other applications in which the SCR's turn–off characteristics are important. As in example — reliable high frequency inverters and converter designs (<20 kHz) require a known and controlled circuit–commutated turn–off time (t_q). Unfortunately, it is usually difficult to find the turn–off time of a particular SCR for a given set of circuit conditions.

This section discusses t_q in general and describes a circuit capable of measuring t_q. Moreover, it provides data and curves that illustrate the effect on t_q when other parameters are varied, to optimize circuit performance.

SCR TURN–OFF MECHANISM

The SCR, being a four layer device (P–N–P–N), is represented by the two interconnected transistors, as shown in Figure 5.1. This regenerative configuration allows the device to turn on and remain on when the gate trigger is removed, as long as the loop gain criteria is satisfied; i.e., when the sum of the common base current gains (α) of both the equivalent NPN transistor and PNP transistor, exceed one. To turn off the SCR, the loop gain must be brought below unity, whereby the on–state principal current (anode current i_T) limited by the external circuit impedance, is reduced below the holding current (I_H). For ac line applications, this occurs automatically during the negative going portion of the waveform. However, for dc applications (inverters, as an example), the anode current must be interrupted or diverted; (diversion of the anode current is the technique used in the t_q test fixture described later in this application note).

SCR TURN–OFF TIME t_q

Once the anode current in the SCR ceases, a period of time must elapse before the SCR can again block a forward voltage. This period is the SCR's turn–off time, t_q, and is dependent on temperature, forward current, and other parameters. The turn–off time phenomenon can be understood by considering the three junctions that make up the SCR. When the SCR is in the conducting state, each of the three junctions is forward biased and the N and P regions (base regions) on either side of J2 are heavily saturated with holes and electrons (stored charge). In order to turn off the SCR in a minimum amount of time, it is necessary to apply a negative (reverse) voltage to the device anode, causing the holes and electrons near the two end junctions, J1 and J3, to diffuse to these junctions. This causes a reverse current to flow through the SCR. When the holes and electrons near junctions J1 and J3 have been removed, the reverse current will cease and junctions J1 and J3 will assume a blocking state. However, this does not complete the recovery of the SCR since a high concentration of holes and electrons still exist near the center junction, J2. This concentration decreases by the recombination process and is largely independent of the external circuit. When the hole and electron concentration near junction J2 has reached some low value, junction J2 will assume its blocking condition and a forward voltage can, after this time, be applied without the SCR switching back to the conduction state.

P–N–P–N STRUCTURE

TWO TRANSISTOR MODEL
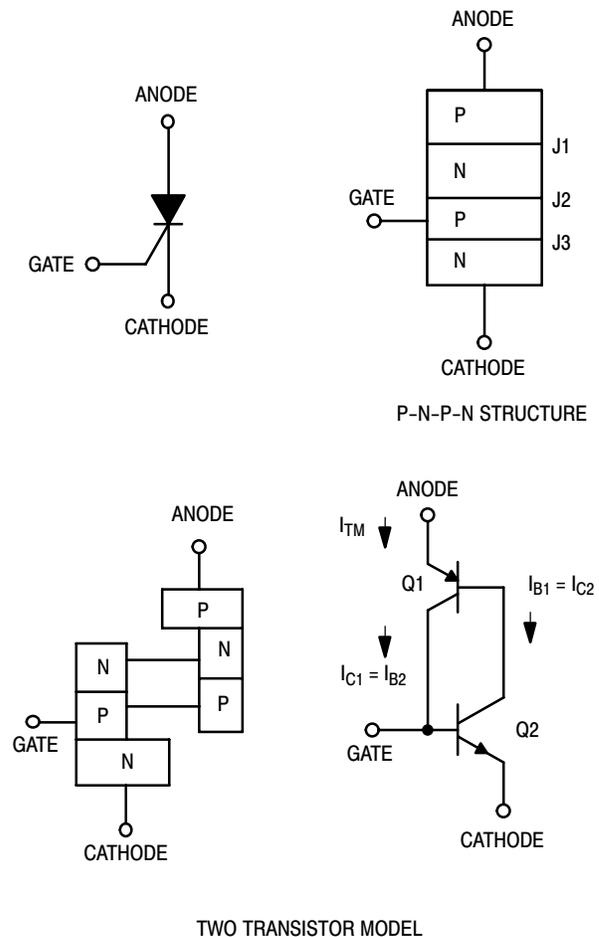
Figure 5.1. Two Transistor Analogy of an SCR

t_q MEASUREMENT

When measuring SCR turn−off time, t_q, it is first necessary to establish a forward current for a period of time long enough to ensure carrier equilibrium. This must be specified, since I_{TM} has a strong effect on the turn−off time of the device. Then, the SCR current is reversed at a specified di/dt rate, usually by shunting the SCR anode to some negative voltage through an inductor. The SCR will then display a "reverse recovery current," which is the charge clearing away from the junctions. A further waiting time must then elapse while charges recombine, before a forward voltage can be applied. This forward voltage is ramped up a specified dv/dt rate. The dv/dt delay time is reduced until a critical point is reached where the SCR can no longer block the forward applied voltage ramp. In effect, the SCR turns on and consequently, the ramp voltage collapses. The elapsed time between this critical point and the point at which the forward SCR current passes through zero and starts to go negative (reverse recovery phase), is the t_q of the SCR. This is illustrated by the waveforms shown in Figure 5.2.

t_q GENERAL TEST FIXTURE

The simplified circuit for generating these waveforms is schematically illustrated in Figure 5.3. This circuit is implemented with as many as eight transformers including variacs, and in addition to being very bulky, has been known to be troublesome to operate. However, the configuration is relevent and, in fact, is the basis for the design, as described in the following paragraphs.

t_q TEST FIXTURE BLOCK DIAGRAMS AND WAVEFORMS

The block diagram of the tq Test Fixture, illustrated in Figure 5.4, consists of four basic blocks: A Line Synchronized Pulse Generator establishes system timing; a Constant Current Generator (variable in amplitude) powers the Device Under Test (DUT); a di/dt Circuit controls the rate of change of the SCR turn−off current; and the dv/dt Circuit reapplies a controlled forward blocking voltage. Note from the waveforms illustrated that the di/dt circuit, in parallel with the DUT, diverts the constant current from the DUT to produce the described anode current I_{TM}.

t_q TEST FIXTURE CHARACTERISTICS

The complete schematic of the t_q Test Fixture and the important waveforms are shown in Figures 5.5 and 5.6, respectively.

A CMOS Gate is used as the Line Synchronized Pulse Generator, configured as a wave shaping Schmitt trigger, clocking two cascaded monostable multivibrators for delay and pulse width settings (Gates 1C to 1F). The result is a pulse generated every half cycle whose width and position (where on the cycle it triggers) are adjustable by means of potentiometers R2 and R3, respectively. The output pulse is normally set to straddle the peak of the ac line, which not only makes the power supplies more efficient, but also allows a more consistent oscilloscope display. This pulse shown in waveform A of Figure 5.6 initiates the t_q test, which requires approximately 0.5 ms to assure the device a complete turn on. A fairly low duty cycle results, (approximately 5%) which is important in minimizing temperature effects. The repetitive nature of this test permits easy oscilloscope viewing and allows one to readily "walk in" the dv/dt ramp. This is accomplished by adjusting the appropriate potentiometer (R7) which, every 8.33 ms (every half cycle) will apply the dv/dt ramp at a controlled time delay.
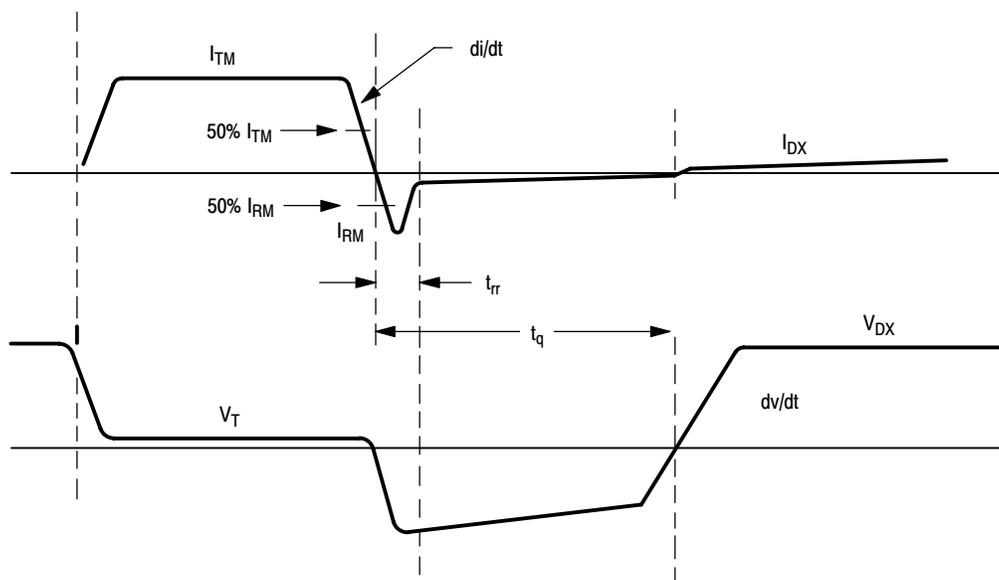
Figure 5.2. SCR Current and Voltage Waveforms During Circuit−Commutated Turn−Off
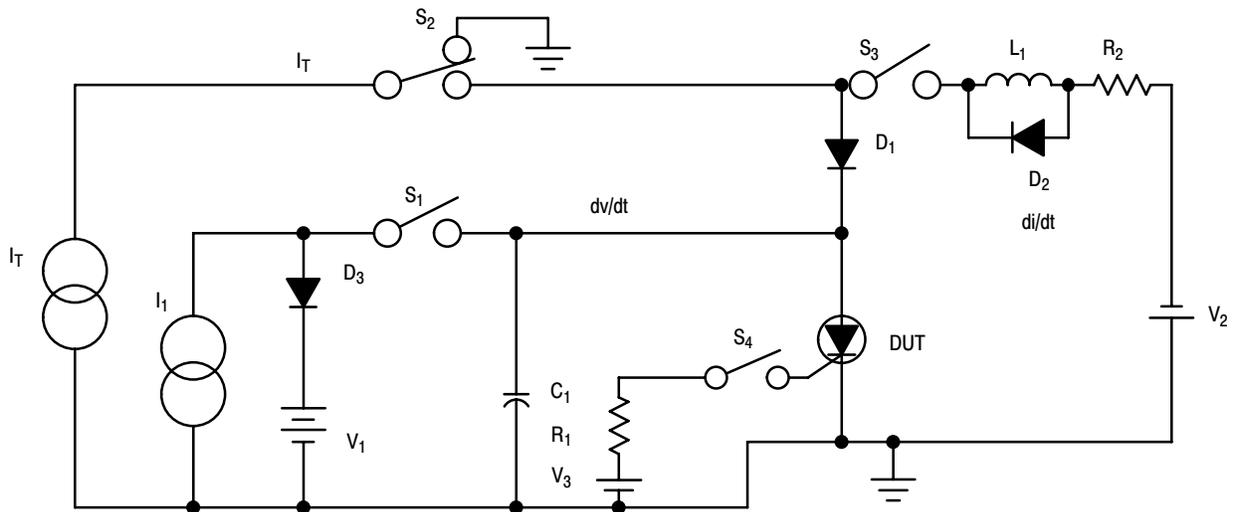
Figure 5.3. Simplified t_q Test Circuit

To generate the appropriate system timing delays, four RC integrating network/comparators are used, consisting of op–amps U2, U5 and U6.

Op–amp U2A, along with transistor Q2, opto–coupler U4 and the following transistors Q6 and Q7, provide the gate drive pulse to the DUT (see waveforms B, C and D of Figure 5.6). The resulting gate current pulse is about 50 μs wide and can be selected, by means of switch S2, for an I_{GT} of from about 1 mA to 90 mA. Opto–coupler U4, as well as U1 in the Constant Current Circuit, provide electrical isolation between the power circuitry and the low level circuitry.

The Constant Current Circuit consists of an NPN Darlington Q3, connected as a constant current source driving a PNP tri–Darlington (Darlington Q4, Bipolar Q5). By varying the base voltage of Q3 (with Current Control potentiometer R4), the collector current of Q3 and thus the base voltage of Q4 will also vary. The PNP output transistor Q5 (MJ14003) (rated at 70 A), is also configured as a constant current source with four, parallel connected emitter resistors (approximately 0.04 ohms, 200 W), thus providing as much as 60 A test current. Very briefly, the circuit operates as follows: — CMOS Gate 1E is clocked high, turning on, in order, a) NPN transistor Q16, b) PNP transistor Q1, c) optocoupler U3, and d) transistors Q3, Q4 and Q5. The board mounted Current Set potentiometer R5, sets the maximum output current and R4, the Current Control, is a front panel, multiturn potentiometer.
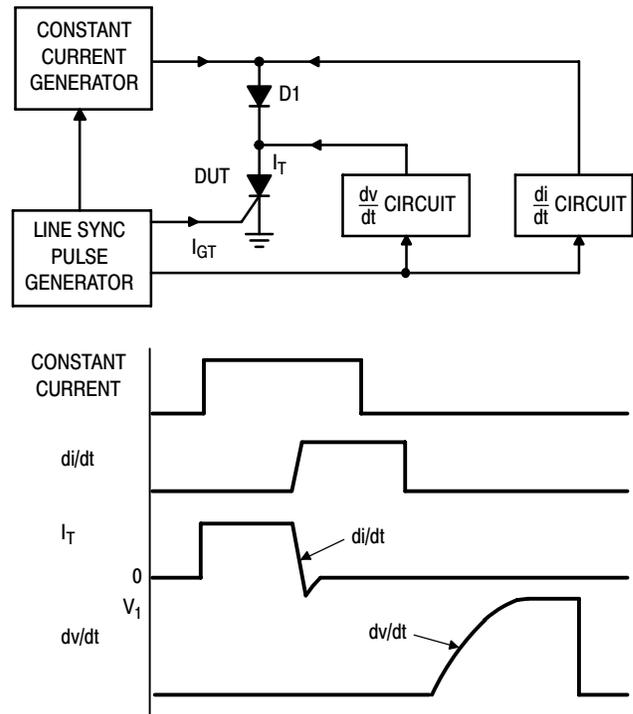
Figure 5.4. Block Diagram of the t_q Test Fixture and Waveforms

LINE SYNCHRONIZED PULSE GENERATOR

Figure 5.5. t_q Test Fixture
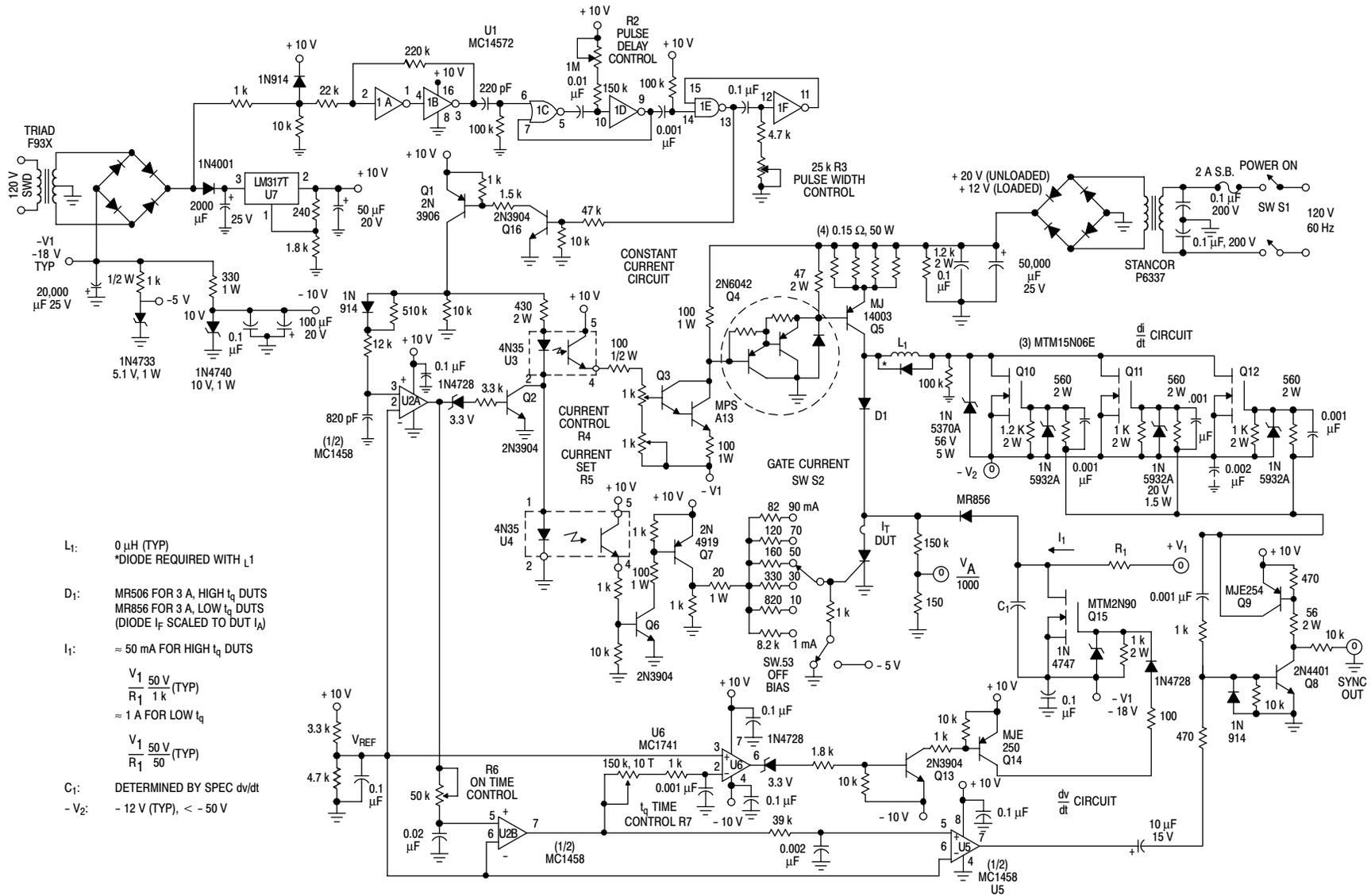
L_1: 0 μH (TYP)
  *DIODE REQUIRED WITH $_L$1

D_1: MR506 FOR 3 A, HIGH t_q DUTS
  MR856 FOR 3 A, LOW t_q DUTS
  (DIODE I_F SCALED TO DUT I_A)

I_1: ≈ 50 mA FOR HIGH t_q DUTS

  $\dfrac{V_1}{R_1} \dfrac{50\,V}{1\,k}$ (TYP)

  ≈ 1 A FOR LOW t_q

  $\dfrac{V_1}{R_1} \dfrac{50\,V}{50}$ (TYP)

C_1: DETERMINED BY SPEC dv/dt

$-V_2$: -12 V (TYP), < -50 V

Time delay for the di/dt Circuit is derived from cascaded op–amps U2B and U5 (waveforms F and G of Figure 5.6). The output gate, in turn, drives NPN transistor Q8, followed by PNP transistor Q9, whose output provides the gate drive for the three parallel connected N–channel power MOSFET transistors Q10–Q12 (waveforms H of Figure 5.6). These three FETs (MTM15N06), are rated at 15 A continuous drain current and 40 A pulsed current and thus can readily divert the maximum 60 A constant current that the Fixture can generate. The results of this diversion from the DUT is described by waveforms E, H and I of Figure 5.6, with the di/dt of of I_{TM} dictated by the series inductance L1. For all subsequent testing, the inductor was a shorting bar, resulting in very little inductance and consequently, the highest di/dt (limited primarily by wiring inductance). When a physical inductor L1 is used, a clamp diode, scaled to the diverted current, should be placed across L1 to limit "inductive kicks."

dv/dt CIRCUIT

The last major portion of the Fixture, the dv/dt Circuit, is variable time delayed by the multi–turn, front panel t_q Time Control potentiometer R7, operating as part of an integrator on the input of comparator U6. Its output (waveform J of Figure 5.6) is used to turn–off, in order, a) normally on NPN transistor Q13, b) PNP transistor Q14 and c) N–channel power MOSFET Q15 (waveform L of Figure 5.6). This FET is placed across ramp generating capacitor C1, and when unclamped (turned off), the capacitor is allowed to charge through resistor R1 to the supply voltage $+V_1$. Thus, the voltage appearing on the drain will be an exponentially rising voltage with a dv/dt dictated by R1, C1, whose position in time can be advanced or delayed. This waveform is then applied through a blocking diode to the anode of the DUT for the forward blocking voltage test.

Another blocking diode, D1, also plays an important role in t_q measurements and must be properly selected. Its purpose is to prevent the dv/dt ramp from feeding back into the Current Source and di/dt Circuit and also to momentarily apply a reverse blocking voltage (a function of $-V_2$ of the di/dt circuit) to the DUT. Consequently, D1 must have a reverse recovery time t_{rr} greater than the DUT, but less than the t_q time. When measuring standard recovery SCRs, its selection — fast recovery rectifiers or standard recovery — is not that critical, however, for fast recovery, low t_q SCRs, the diode must be tailored to the DUT to produce accurate results. Also, the current rating of the diode must be compatible with the DUT test current. These effects are illustrated in the waveforms shown in Figure 5.7 where both a fast recovery rectifier and standard recovery rectifier were used in measuring t_q of a standard 2N6508 SCR. Although the di/dt's were the same, the reverse recovery current I_{RM} and t_{rr} were greater with the standard recovery rectifier, resulting in a somewhat shorter t_q (59 μs versus 63 μs). In fact, t_q is affected by the initial conditions (I_{TM}, di/dt, I_{RM}, dv/dt, etc.) and these conditions should be specified to maintain measurement repeatability. This is later described in the published curves and tables.

Finally, the resistor R1 and the resultant current I_1 in the dv/dt circuit must meet certain criteria: I_1 should be greater than the SCR holding current so that when the DUT does indicate t_q limitation, it latches up, thus suppressing the dv/dt ramp voltage; and, for fast SCRs (low t_q), I_1 should be large enough to ensure measurement repeatability. Typical values of I_1 for standard and fast SCRs may be 50 mA and 500 mA, respectively. Obviously, for high forward blocking voltage $+V_1$ tests, the power requirements must be met.

EFFECTS OF GATE BIAS ON t_q

Examples of the effects of I_1 on t_q are listed in Table 5.III whereby standard and fast SCRs were tested with about 50 mA and 1 A, respectively. Note that the low t_q SCR's required fast recovery diodes and high I_1 current.

TEST FIXTURE POWER SUPPLIES

Most of the power supplies for the system are self contained, including the $+12$ V supply for the Constant Current Circuit. This simple, unregulated supply furnishes up to 60 A peak pulsed current, primarily due to the line synchronized operation of the system. Power supplies $+V_1$ and $-V_2$, for this exercise, were external supplies, since they are variable, but they can be incorporated in the system. The reverse blocking voltage to the DUT is supplied by $-V_2$ and is typically set for about -10 V to -20 V, being limited to the breakdown voltage of the diverting power MOSFETS ($V_{DSS} = 60$ V). The $+12$ V unregulated supply can be as high as $+20$ V when unloaded; therefore, $-V_2$ (MAX), in theory, would be -40 V but should be limited to less than -36 V due to the 56 V protective Zener across the drain–source of the FETs. Also, $-V_2$ must be capable of handling the peak 60 A, diverting current, if so required.

The reapplied forward blocking voltage power supply $+V_1$, may be as high as the DUT V_{DRM} which conceivably can be 600 V, 1,000 V or greater and, since this supply is on most of the time, must be able to supply the required I_1. Due to the sometimes high power requirements, $+V_1$ test conditions may have to be reduced for extremely fast SCRs.

PARAMETERS AFFECTING t_q

To see how the various circuit parameters can affect t_q, one condition at a time is varied while the others are held constant. The parameters to be investigated are a) forward current magnitude (I_{TM}), b) forward current duration, c) rate of change of turn−off current (di/dt), d) reverse−current magnitude (I_{RM}), e) reverse voltage (V_{RM}), f) rate of reapplied forward voltage (dv/dt), g) magnitude limit of reapplied voltage, h) gate−cathode resistance and i) gate drive magnitude (I_{GT}).

Typical data of this kind, taken for a variety of SCRs, including standard SCRs, high speed SCRs, is con-densed and shown in Table 5.1. The data consists of the different conditions which the particular SCR types were subjected to; ten SCRs of each type were serialized and tested to each condition and the ten t_q's were averaged to yield a "typical t_q."

The conditions listed in Column A in Table 5.1, are typical conditions that might be found in circuit opera-tion. Columns B through J in Table 5.1, are in order of increasing t_q; the conditions listed in these columns are only the conditions that were modified from those in Column A and if a parameter is not listed, it is the same as in Column A.
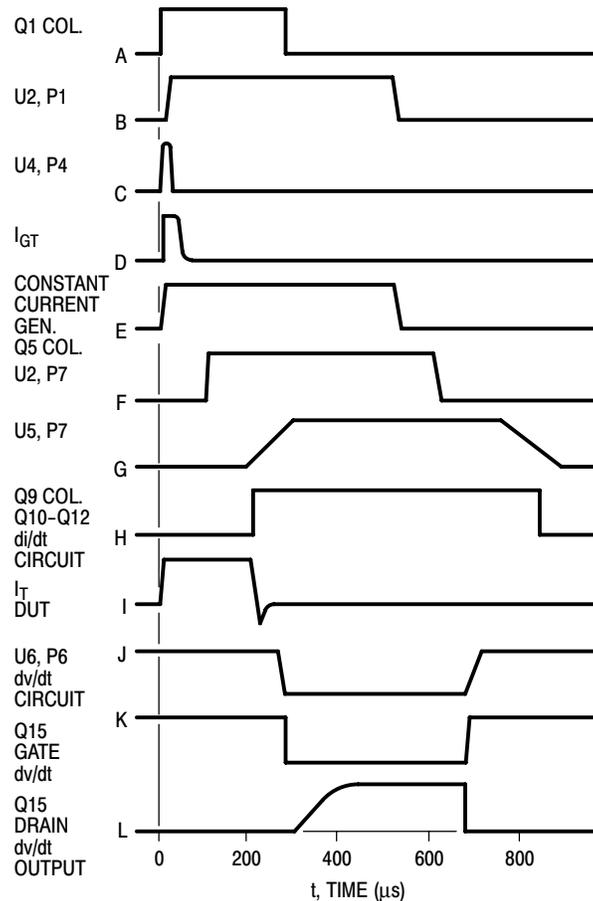
Figure 5.6. t_q Test Fixture System Waveforms

I = 2 A/Div

0 A

V = 10 V/Div

0 V

t_q = 63 µs   t = 50 µs/Div   t = 1 µs/Div
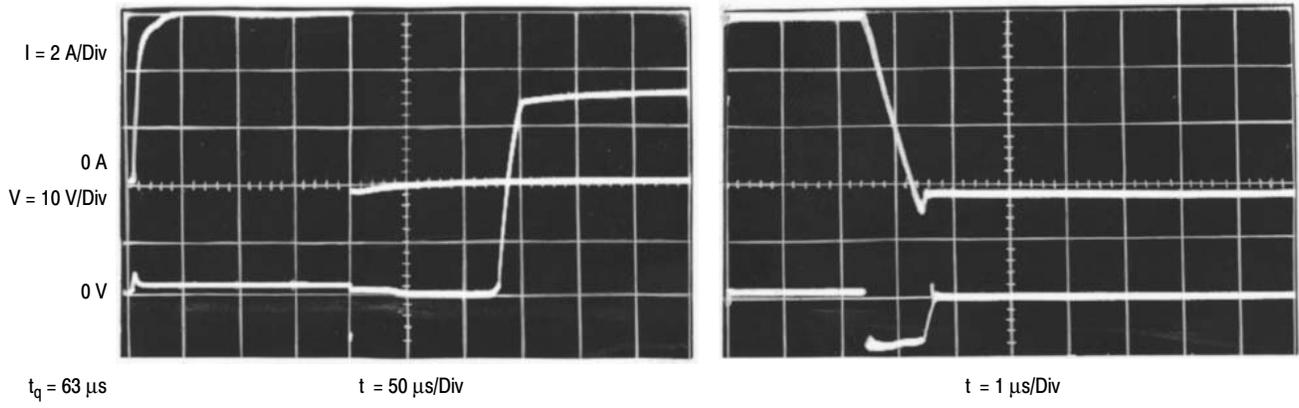
D1 = MR856, FAST RECOVERY RECTIFIER

I = 2 A/Div

0 A

V = 10 V/Div

0 V

t_q = 59 µs   t = 50 µs/Div   t = 1 µs/Div
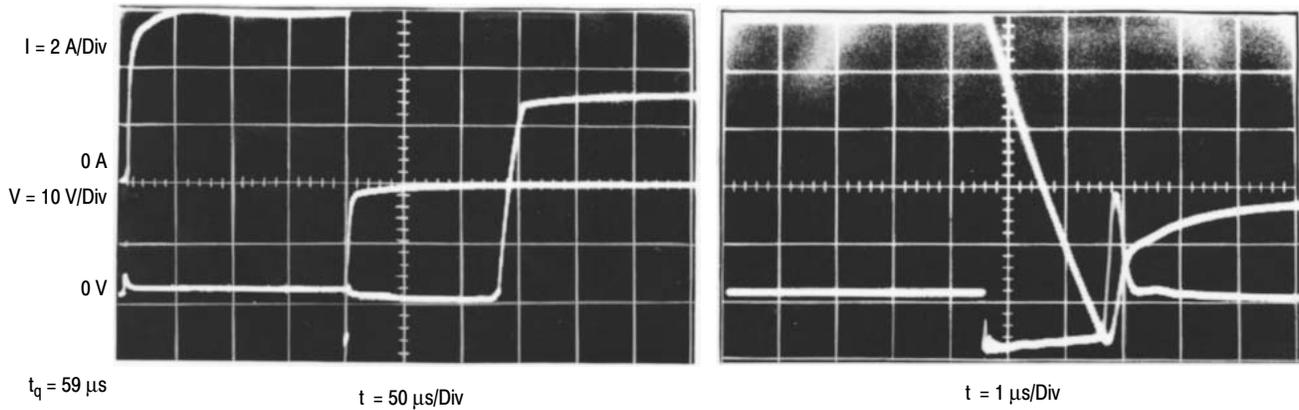
D1 = 1N5402, STANDARD RECOVERY RECTIFIER

Figure 5.7. The Effects of Blocking Diode D1 on t_q of a 2N6508 SCR

Table 5.1. Parameters Affecting t_q

Device	A	B	C	D	E	F	G	H	I
2N6508 25 A 600 V	R_{GK} = 1 k dv/dt = 15 V/µs I_{TM} = 25 A I_{RM} = 14 A di/dt = − 100 A/µs I_{TM} duration = 275 µs I_{GT} = 30 mA	R_{GK} = 100 dv/dt = 2.4 V/µs I_{TM} = 1 A I_{RM} = 1.8 A di/dt = 32 A/µs	R_{GK} = 100 dv/dt = 2.4 V/µs I_{TM} = 2 A I_{RM} = 50 mA di/dt = 0.5 µs	R_{GK} = 100 dv/dt = 2.4 V/µs I_{RM} = 50 mA di/dt = 0.45 A/µs	R_{GK} = 100 dv/dt = 2.4 V/µs	R_{GK} = ∞ dv/dt = 2.4 V/µs	R_{GK} = 100 dv/dt = 2.4 V/µs I_{TM} = 37 A	R_{GK} = 100	I_{GT} = 90 mA
	typ t_q = 68 µs	typ t_q = 42 µs	typ t_q = 45 µs	typ t_q = 49 µs	typ t_q = 60 µs	typ t_q = 64 µs	typ t_q = 64 µs	typ t_q = 65 µs	typ t_q = 68 µs
2N6399 12 A	R_{GK} = 1 k dv/dt = 90 V/µs I_{TM} = 12 A I_{RM} = 11 A di/dt = − 100 A/µs I_{TM} duration = 275 µs I_{GT} = 30 mA	R_{GK} = 100 dv/dt = 2.5 V/µs I_{TM} = 1 A I_{RM} = 50 mA di/dt = − 0.5 A/µs	R_{GK} = 100 dv/dt = 2.5 V/µs I_{TM} = 1 A I_{RM} = 2.7 A di/dt = 56 A/µs	R_{GK} = 100 dv/dt = 2.5 V/µs I_{RM} = 50 mA di/dt = 32 A/µs	R_{GK} = 100 dv/dt = 2.5 V/µs I_{TM} = 18 A I_{RM} = 50 mA di/dt = 0.3 A/µs	R_{GK} = ∞ dv/dt = 2.5 V/µs I_{RM} = 50 mA di/dt = 0.35 A/µs	R_{GK} = 100	I_{GT} = 90 mA	
	typ t_q = 48 µs	typ t_q = 30 µs	typ t_q = 31 µs	typ t_q = 32 µs	typ t_q = 33 µs	typ t_q = 35.5 µs	typ t_q = 45 µs	typ t_q = 48 µs	

Table 5.1. Continued

Device	A	B	C	D	E	F	G	H	I
C106B 4 A	I_{GT} = 1 mA R_{GK} = 1 k dv/dt = 5 V/μs I_{TM} = 4A I_{RM} = 4A di/dt = 50 A/μs I_{TM} duration = 275 μs V_{DX} = 50 V typ t_q = 28 μs	I_{TM} = 2 A I_{RM} = 2.5 A di/dt = −30 A/μs V_{DX} = 50 V typ t_q = 25 μs	I_{TM} = 6 A I_{RM} = −1 A/μs di/dt = −1 A/μs V_{DX} = 150 V typ t_q = 26 μs	I_{TM} = 6 A I_{RM} = 0.1 A di/dt = −1 A/μs V_{DX} = 50 V typ t_q = 26 μs	dv/dt = 1.4 V/μs I_{TM} = 2 A I_{RM} = 0.2 A di/dt = −1.4 A/μs typ t_q = 26 μs	−V_2 = 35 V I_{RM} = 0.2 A di/dt = −1.4 A/μs typ t_q = 27 μs	I_{RM} = 0.15 A −V_2 = 4 V di/dt = −1.4 A/μs typ t_q = 27 μs	dv/dt = 1.4 V/μs I_{RM} = 0.15 A di/dt = 1.4 A/μs typ t_q = 27 μs	I_{GT} = 90 mA dv/dt = 1.4 V/μs I_{RM} = 2 A di/dt = −1.4 A/μs typ t_q = 27 μs
2N6240 4 A	R_{GK} = 1 k dv/dt = 40 V/μs I_{TM} = 4 A I_{RM} = 4 A di/dt = 50 A/μs I_{TM} duration = 275 μs I_{GT} = 1 mA V_{DX} = 50 V typ t_q = 44.8 μs	R_{GK} = 100 dv/dt = 1.3 V/μs I_{TM} = 1 A I_{RM} = 50 mA di/dt = −0.5 A/μs I_{GT} = 90 mA V_{DX} = 150 V typ t_q = 26 μs	R_{GK} = 100 dv/dt = 1.75 V/μs I_{TM} = 1 A I_{RM} = 50 mA di/dt = −0.5 A/μs I_{GT} = 90 mA typ t_q = 26.2 μs	R_{GK} = 100 dv/dt = 1.75 V/μs I_{RM} = 50 mA di/dt = −0.5 A/μs I_{GT} = 90 mA typ t_q = 27.7 μs	dv/dt = 1.75 V/μs R_{GK} = 100 I_{TM} = 6 A I_{RM} = 50 mA di/dt = −0.5 A/μs I_{GT} = 90 mA typ t_q = 28.6 μs	R_{GK} = 100 I_{RM} = 50 mA di/dt = −0.5 A/μs I_{GT} = 90 mA typ t_q = 30 μs	R_{GK} = 100 I_{GT} = 900 mA typ t_q = 32.7 μs	R_{GK} = ∞ dv/dt = 1.75 V/μs I_{TM} = 1 A I_{RM} = 50 mA di/dt = −0.5 A/μs I_{GT} = 90 mA typ t_q = 37.2 μs	I_{GT} = 90 mA typ t_q = 41.4 μs
MCR100–6 0.8 A	R_{GK} = 1 k dv/dt = 160 V/μs I_{TM} = 0.8 A I_{RM} = 0.8 A di/dt = 12 A/μs V_{DX} = 50 V I_{TM} duration = 275 μs typ t_q = 14.4 μs	dv/dt = 30 V/μs I_{TM} = 0.25 A I_{RM} = 40 mA di/dt = −0.6 A/μs typ t_q = 12.7 μs	dv/dt = 30 V/μs Ir = 40 mA di/dt = −0.8 A/μs typ t_q = 13.5 μs	−V_2 = 9 V I_{RM} = 20 mA di/dt = −0.4 A/μs typ t_q = 13.7 μs	−V_2 = 1 V Ir = 40 mA di/dt = −0.8 A/μs typ t_q = 13.9 μs	dv/dt = 30 V/μs I_{TM} = 1.12 A I_{RM} = 40 mA di/dt = −0.8 A/μs typ t_q = 14.4 μs	dv/dt = 30 V/μs I_{TM} = 1.12 A I_{RM} = 40 mA di/dt = −0.8 A/μs V_{DX} = 100 V typ t_q = 14.4 μs		
2N5064 0.8 A	R_{GK} = 1 k dv/dt = 30 V/μs I_{TM} = 0.8 A I_{RM} = 0.8 A di/dt = 12 A/μs I_{TM} duration = 275 μs V_{DX} = 50 V typ t_q = 28.9 μs	dv/dt = 5 V/μs I_{TM} = 0.2 A I_{RM} = 50 mA di/dt = −0.6 A/μs typ t_q = 27/μs	dv/dt = 5 V/μs I_{RM} = 50 mA di/dt = −0.8 A/μs typ t_q = 30/μs	dv/dt = 5 V/μs I_{TM} = 1.12 A I_{RM} = 50 mA di/dt = −0.8 A/μs typ t_q = 31 μs	I_{RM} = 40 mA −V_2 = 9 V di/dt = −0.45 A/μs typ t_q = 31.2 μs	I_{RM} = 40 mA −V_2 = 1 V di/dt = −0.8 A/μs typ t_q = 31.4 μs	V_{DX} = 100 V dv/dt = 5 V/μs I_{TM} = 1.12 A I_{RM} = 50 mA di/dt = −0.8 A typ t_q = 31.7 μs		
2N5061 0.8 A	dv/dt = 10 V/μs I_{TM} = 0.8 A I_{RM} = 0.8 A di/dt = 18 A/μs I_{TM} duration = 275 μs R_{GK} = 1 k V_{DX} = 30 V typ t_q = 31.7 μs	dv/dt = 3.5 V/μs I_{TM} = 0.25 A I_{RM} = 40 mA di/dt = −0.7 A/μs typ t_q = 19.1 μs	dv/dt = −3.5 V/μs I_{RM} = 40 mA di/dt = −0.8 A/μs typ t_q = 19/μs	dv/dt = 3.5 V/μs I_{TM} = 1.12 A I_{RM} = 40 mA di/dt = −0.8 A/μs V_{DX} = 60 V typ t_q = 19.8 μs	dv/dt = 3.58/μs I_{TM} = 1.12 A I_{RM} = 40 mA di/dt = −0.7 A/μs typ t_q = 20.2 μs	−V_2 = 4 V I_{RM} = 20 mA di/dt = −0.2 A/μs typ t_q = 30 μs	−V_2 = 1 V I_{RM} = 40 mA di/dt = −0.8 A/μs typ t_q = 30.2 μs		

Table 5.2 is a condensed summary of Table 5.1 and shows what happens to the t_q of the different devices when a parameter is varied in one direction or the other.

THE EFFECT OF CHANGING PARAMETERS ON t_q

From Tables 5.1 and 5.2, it is clear that some parameters affect t_q more than others. The following discussion describes the effect on t_q of the various parameters.

FORWARD CURRENT MAGNITUDE (I_{TM})

Of the parameters that were investigated, forward−current magnitude and the di/dt rate have the strongest effect on t_q. Varying the I_{TM} magnitude over a realistic range of I_{TM} conditions can change the measured t_q by about 30%. The change in t_q is attributed to varying current densities (stored charge) present in the SCR's junctions as the I_{TM} magnitude is changed. Thus, if a large SCR must have a short t_q when a low I_{TM} is present, a large gate trigger pulse (I_{GT} magnitude) would be advantageous. This turns on a large portion of the SCR to minimize the high current densities that exists if only a small portion of the SCR were turned on (by a weak gate pulse) and the low I_{TM} did not fully extend the turned on region.

In general, the SCR will exhibit longer t_q times with increasing I_{TM}. Increasing temperature also increases the t_q time.

di/dt RATE

Varying the turn−off rate of change of anode current di/dt does have some effect on the t_q of SCRs. Although the increase in t_q versus increasing di/dt was nominal for the SCRs illustrated, the percentage change for the fast SCRs was fairly high (about 30−40%).

REVERSE CURRENT MAGNITUDE (I_{RM})

The reverse current is actually due to the stored charge clearing out of the SCR's junctions when a negative voltage is applied to the SCR anode. I_{RM} is very closely related to the di/dt rate; an increasing di/dt rate causing an increase of I_{RM} and a decreasing di/dt rate causing a lower I_{RM}.

Parameter Changed	Device	Columns	1st (μs)	2nd (μs)
I_{GT} Increase	2N6508	AI	68	68
	2N6399	AG	48	48
	2N6240	AI	44.8	41.4
	C106F	HI	27	27
Decrease R_{GK} 1 k to 100 ohms	2N6508	AH	68	65
	2N6399	AG	48	45
	2N6240	GI	41.4	32.7
Increase R_{GK} 1 k to ∞	2N6508	EF	60	64
	2N6399	DF	32	35.5
	2N6240	CH	26.2	37.2
V_{DX}	C106F	DC	26	26
	2N6240	BC	26.2	26
	MCR100−6	FG	14.4	14.4
	2N5064	DG	31	31.7
	2N5061	DE	20.2	19.8
Decrease dv/dt Rate	2N6508	EH	65	60
	C106F	HJ	29	27
	2N6240	DF	30	27.7
Increase I_{TM}	2N6508	EG	60	64
	2N6399	DE	32	33
	C106F	EH	26	27
	2N6240	DC	26.2	27.7
		DE	27.7	28.6
		CE	26.2	28.6
	MCR100−6	CF	13.5	14.4
	2N5064	CD	30.7	31
	2N5061	BE	19.1	20.7

Table 5.2. The Effects of Changing Parameters on t_q

By using different series inductors and changing the negative anode turn−off voltage, it is possible to keep the di/dt rate constant while changing I_{RM}. It was found that I_{RM} has little or no effect on t_q when it is the only variable changed (see Table 5.1 C106F, Columns F and G, for example).

REVERSE ANODE VOLTAGE (V_{RM})

Reverse anode voltage has a strong effect on the I_{RM} magnitude and the di/dt rate, but when V_{RM} alone is varied, with I_{RM} and di/dt held constant, little or no change in t_q time was noticed. V_{RM} must always be within the reverse voltage of the device.

Device	Gate Bias		Conditions		+ V$_1$	RI	dv/dt (v/μs)
	0V	– 5 V	– V$_2$ = –10 V, I$_F$ = 3 A		50 V	1 k/50	2.5/50
	t$_q$^{1}	t$_q$^{2}	Diode DI	dv/dt (V/μs)	Remarks		
2N6508	40 μs	30 μs	Slow MR502	2.5	Slow diode faster than fast diode, (lower t$_q$)		
2N6240	16 μs	9 μs	Slow	2.5	Slow diode faster. 2.5 V/μs faster than 50 V/μs		
2N6399	30 μs	25 μs	Slow	2.5	Tested slow diode only		
C106F	13 μs	8 μs	Slow	2.5	Tested slow diode only		

Table 5.3 The Effects of Gate Bias on t$_q$
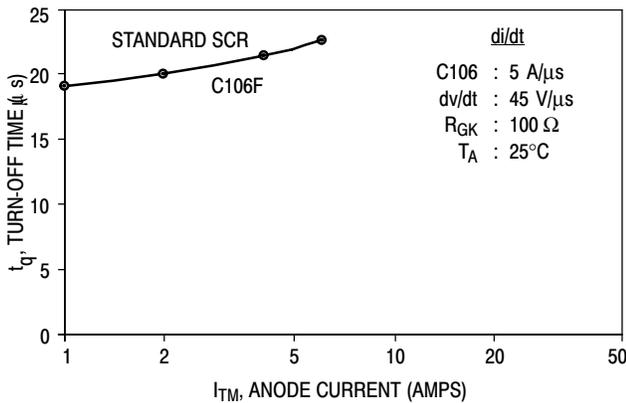
Figure 5.8. Standard SCR Turn–Off Time t$_q$ as a Function of Anode Current I$_{TM}$

REAPPLIED dv/dt RATE

Varying the reapplied dv/dt rate across the range of dv/dt's commonly encountered can vary the t$_q$ of a given SCR by more than 10%. The effect of the dv/dt rate on t$_q$ is due to the Anode–Gate capacitance. The dv/dt applied at the SCR anode injects current into the gate through this capacitance (i$_{GT}$ = C dv/dt). As the dv/dt rate increased, the gate current also increases and can trigger the SCR on. To complicate matters, this injected current also adds to the current due to leakage or stored charge left in the junctions just after turn–off.

The stored charge remaining in the center junction is the main reason for long t$_q$ times and, for the most part, the charge is removed by the recombination process. If the reapplied dv/dt rate is high, more charge is injected into this junction and prevents it from returning to the blocking state, as soon as if it were a slow dv/dt rate. The higher the dv/dt rate, the longer the t$_q$ times will be.

MAGNITUDE LIMIT OF REAPPLIED dv/dt (V$_{DX}$)

Changing the magnitude limit of the reapplied dv/dt voltage has little or no effect on a given SCR's t$_q$ time when the maximum applied voltage is well below the voltage breakdown of the SCR. The t$_q$ times will lengthen if the SCR is being used near its voltage breakdown, since the leakage present near breakdown is higher than at lower voltage levels. The leakage will lengthen the time it takes for the charge to be swept out of the SCR's center junction, thus lengthening the time it takes for this junction to return to the blocking state.

GATE CATHODE RESISTANCE (R$_{GK}$)

In general, the lower the R$_{GK}$ is, the shorter the t$_q$ time will be for a given SCR. This is because low R$_{GK}$ aids in the removal of stored charge in the SCR's junctions. An approximate 15% change in the t$_q$ time is seen by changing R$_{GK}$ from 100 ohms to 1000 ohms for the DUTs.

GATE DRIVE MAGNITUDE (I$_{GT}$)

Changing the gate drive magnitude has little effect on a SCR's t$_q$ time unless it is grossly overdriven or underdriven. When it is overdriven, there is an unnecessary large amount of charge in SCR's junction. When underdriven, it is possible that only a small portion of the chip at the gate region turns on. If the anode current is not large enough to spread the small turned on region, there is a high current and charge density in this region that consequently lengthens the t$_q$ time.

FORWARD CURRENT DURATION

Forward current duration had no measurable effect on t$_q$ time when varied from 100 μs to 300 μs, which were the limits of the ON Semiconductor t$_q$ Tester. Longer I$_{TM}$ durations heat up the SCR which causes temperature effects; very short I$_{TM}$ durations affect the t$_q$ time due to the lack of time for the charges in the SCR's junctions to reach equilibrium, but these effects were not seen in the range tested.

REVERSE GATE BIAS VOLTAGE

As in transistor operation, reverse biasing the gate of the SCR decreases the turn–off time, due to the rapid "sweeping out" of the stored charge. The reduction in t_q for standard SCRs is quite pronounced, approaching perhaps 50% in some cases; for fast SCRs, only nominal improvement might result. Table 5.3 shows this effect on six SCRs where the gate bias was set for 0 V and – 5 V, respectively (the 1 k gate resistor of the DUT was either grounded or returned to – 5 V). Due to the internal, monolithic resistor of most SCRs, the actual reverse bias voltage between the gate–cathode is less than the reverse bias supply.

CHARACTERIZING SCRs FOR CROWBAR APPLICATIONS

The use of a crowbar to protect sensitive loads from power supply overvoltage is quite common and, at the first glance, the design of these crowbars seems like a straightforward, relatively simple task. The crowbar SCR is selected so as to handle the overvoltage condition and a fuse is chosen at 125 to 250% of the supply's rated full–load line current. However, upon further investigation, other questions and problems are encountered.

How much overvoltage and for how long (energy) can the load take this overvoltage? Will the crowbar respond too slowly and thus not protect the load or too fast resulting in false, nuisance triggering? How much energy can the crowbar thyristor (SCR) take and will it survive until the fuse opens or the circuit breaker opens? How fast will the fuse open, and at what energy level? Can the fuse adequately differentiate between normal current levels — including surge currents — and crowbar short circuit conditions?

It is the attempt of this section to answer these questions — to characterize the load, crowbar, and fuse and thus to match their characteristics to each other.

The type of regulator of most concern is the low voltage, series pass regulator where the filter capacitors to be crowbarred, due to 60 Hz operation, are relatively large and the charge and energy stored correspondingly large. On the other hand, switching regulators operating at about 20 kHz require smaller capacitors and thus have lower crowbar constraints.

These regulators are quite often line–operated using a high voltage, two–transistor inverter, half bridge or full bridge, driving an output step–down transformer. If a transistor were to fail, the regulator–transformed power would be less and the output voltage would drop, not rise, as is the case for the linear series regulator with a shorted pass transistor. Thus, the need for overvoltage protection of these types of switching regulators is minimized.

This premise, however, does not consider the case of the lower power series switching regulator where a shorted transistor would cause the output voltage to rise. Nor does it take into account overvoltage due to transients on the output bus or accidental power supply hookup. For these types of operations, the crowbar SCR should be considered.

HOW MUCH OVERVOLTAGE CAN THE LOAD TAKE?

Crowbar protection is most often needed when ICs are used, particularly those requiring a critical supply voltage such as TTL or expensive LSI memories and MPUs.

If the load is 5 V TTL, the maximum specified continuous voltage is 7 V. (CMOS, with its wide power supply range of 3 to 18 V, is quite immune to most overvoltage conditions.) But, can the TTL sustain 8 V or 10 V or 15 V and, if so, for how long and for how many power cycles? Safe Operating Area (SOA) of the TTL must be known. Unfortunately, this information is not readily available and has to be generated.
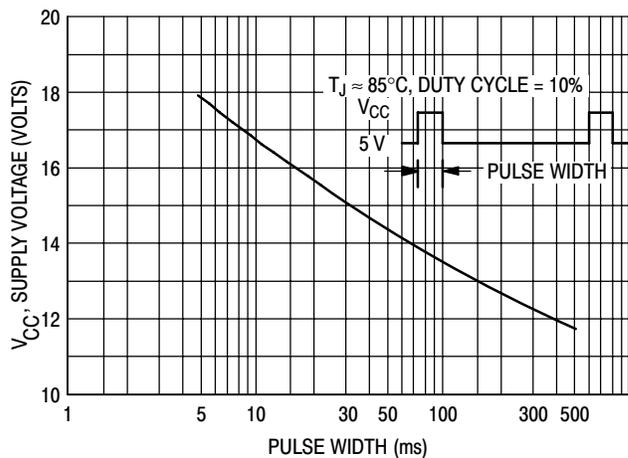
Figure 5.9. Pulsed Supply Voltage versus Pulse Width

Using the test circuit illustrated in Appendix III, a quasi–SOA curve for a typical TTL gate was generated (Figure 5.9). Knowing the overvoltage–time limit, the crowbar and fuse energy ratings can be determined.

The two possible configurations are illustrated in Figure 5.10, the first case shows the crowbar SCR across the input of the regulator and the second, across the output. For both configurations, the overvoltage comparator senses the load voltage at the remote load terminals, particularly when the I_R drop of the supply leads can be appreciable. As long as the output voltage is less than that of the comparator reference, the crowbar SCR will be in an off state and draw no supply current. When an over–voltage condition occurs, the comparator will produce a gate trigger to the SCR, firing it, and thus clamping the regulator input, as in the first case — to the SCRs on–state drop of about 1 to 1.5 V, thereby protecting the load.

(a). SCR Across Input of Regulator

(b). SCR Across Output of Regulator

*NEEDED IF SUPPLY NOT CURRENT LIMITED
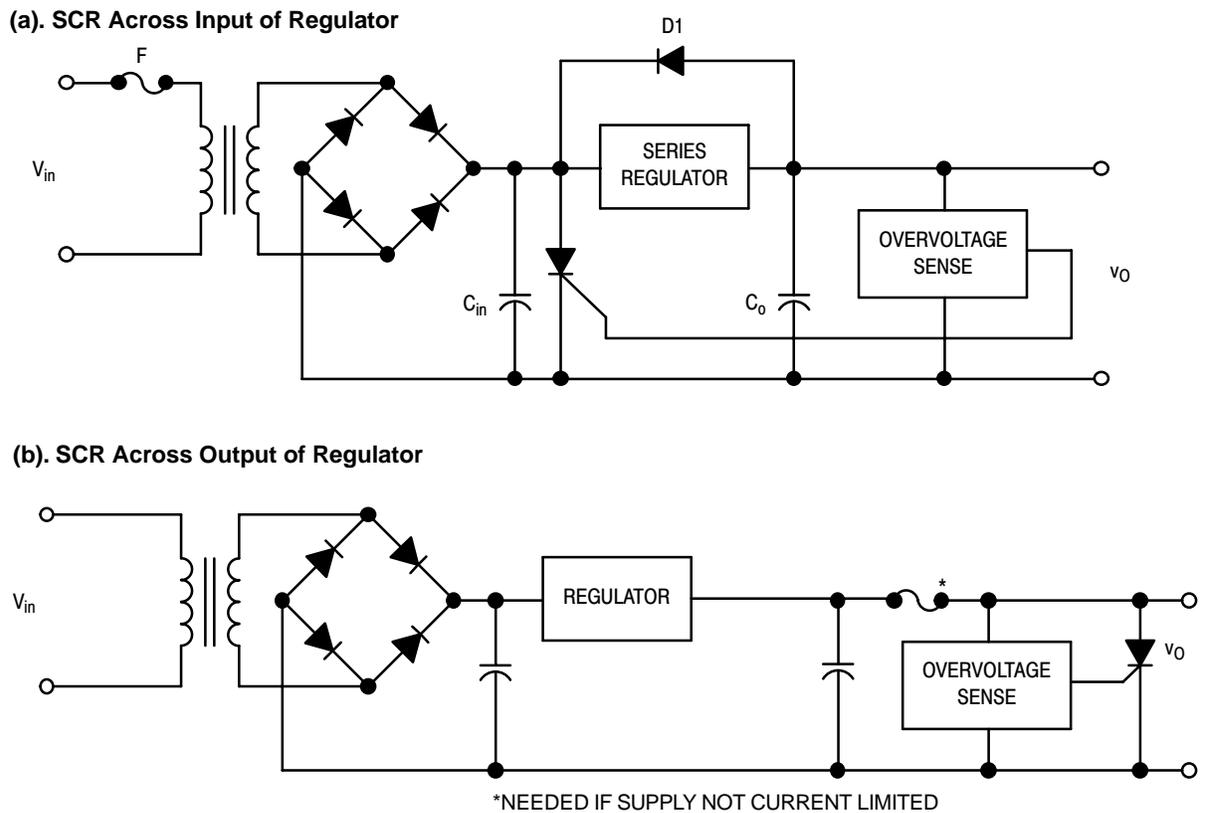
Figure 5.10. Typical Crowbar Configurations

Placing the crowbar across the input filter capacitors, although effectively clamping the output, has several disadvantages.

1. There is a stress placed on the input rectifiers during the crowbarring short circuit time before the line fuse opens, particularly under repeated operation.

2. Under low line conditions, the minimum short circuit current can be of the same magnitude as the maximum primary line current at high line, high load, making the proper fuse selection a difficult choice.

3. The capacitive energy to be crowbarred (input and output capacitor through rectifier D1) can be high.

When the SCR crowbar and the fuse are placed in the dc load circuit, the above problems are minimized. If crowbarring occurs due to an external transient on the line and the regulator's current limiting is working properly, the SCR only has to crowbar the generally smaller output filter capacitor and sustain the limited regulator current.

If the series pass devices were to fail (short), even with current limiting or foldback disabled, the crowbarred energy would generally be less than of the previous case. This is due to the higher impedance of the shorted regulator (due to emitter sharing and current sensing resistors) relative to that of rectifier D1.

Fuse selection is much easier as a fault will now give a greater percentage increase in dc load current than when measuring transformer primary or secondary rms current. The disadvantage, however, of placing the fuse in the dc load is that there is no protection for the input rectifier, capacitor, and transformer, if one of these components were to fail (short). Secondly, the one fuse must protect not only the load and regulator, but also have adequate clearing time to protect the SCR, a situation which is not always readily accomplished. The input circuitry can be protected with the addition of a primary fuse or a circuit breaker.

HOW MUCH ENERGY HAS TO BE CROWBARRED?

This is dictated by the power supply filter capacitors, which are a function of output current. A survey of several linear power supply manufacturers showed the output filter capacitor size to be from about 100 to 400 microfarads per ampere with about 200 μF/A being typical. A 30 A regulator might therefore have a 6000 μF output filter capacitor.

Additionally, the usually much larger input filter capacitor will have to be dumped if the regulator were to short, although that energy to be dissipated will be dependent on the total resistance in the circuit between that capacitor and the SCR crowbar.

The charge to be crowbarred would be

$$Q = CV = I_T,$$

the energy,

$$E = 1/2\ CV^2$$

and the peak surge current

$$i_{pk} = \frac{V_C}{R_T}$$

When the SCR crowbars the capacitor, the current waveform will be similar to that of Figure 5.11, with the peak surge current, i_{pk}, being a function of the total impedance in the circuit (Figure 5.12) and will thus be limited by the Equivalent Series Resistance (ESR) and inductance (ESL) of the capacitor plus the dynamic impedance of the SCR, any external current limiting resistance, (and inductance) of the interconnecting wires and circuit board conductors.

The ESR of computer grade capacitors, depending on the capacitor size and working voltage, might vary from 10 to 1000 milliohms (mΩ). Those used in this study were in the 25 to 50 mΩ range.

The dynamic impedance of the SCR (the slope of the on−state voltage, on−state current curve), at high currents, might be in the 10 to 20 mΩ range. As an example, from the on−state characteristics of the MCR70, 35 A rms SCR, the dynamic impedance is

$$r_d = \frac{\Delta V_F}{\Delta I_F} = \frac{(4.5 - 3.4)V}{(300 - 200)A} = \frac{1.1\ V}{100\ A} \cong 11\ m\Omega.$$

The interconnecting wire might offer an additional 5 mΩ (#20 solid copper wire $\cong$ 20 mΩ/ft) so that the total circuit resistance, without additional current limiting, might be in the 40 to 70 mΩ range. The circuit inductance was considered low enough to ignore so far as i_{pk} is concerned for this exercise, being in hundreds of nano-henry range (ESL $\cong$ 3 nH, L wire $\cong$ 500 nH/ft). However, di/dt will be affected by the inductance.

HOW MUCH ENERGY CAN THE CROWBAR SCR SUSTAIN?

There are several factors which contribute to possible SCR failures or degradation — the peak surge current, di/dt, and a measure of the device's energy capability, I^2t.

If the peak current and/or duration of the surge is large, destruction of the device due to excessive dissipation can occur. Obviously, the i_{pk} can be reduced by inserting additional impedance in the crowbar path, at an increase in dump time. However, this time, which is a measure of how long the overvoltage is present, should be within the SOA of the load.

The energy stored in the capacitor being a constant for a particular voltage would suggest that the I^2t integral for any limiting resistance is also a constant. In reality, this is not the case as the thermal response of the device must be taken into consideration. It has been shown that the dissipation capability of a device varies as to the $\sqrt{t}$ for the first tens of milliseconds of the thermal response and, in effect, the measure of a device's energy capability would be closer to $i^2\sqrt{t}$. This effect is subsequently illustrated in the empirically derived i_{pk} versus time derating curves being a non−linear function. However, for comparison with fuses, which are rated in I^2t, the linear time base, "t," will be used.

The di/dt of the current surge pulse is also a critical parameter and should not exceed the device's ratings (typically about 200 A/μs for 50 A or less SCRs). The magnitude of di/dt that the SCR can sustain is controlled by the device construction and, to some extent, the gate drive conditions. When the SCR gate region is driven on, conduction across the junction starts in a small region and progressively propagates across the total junction. Anode current will initially be concentrated in this small conducting area, causing high current densities which can degrade and ultimately destroy the device. To minimize this di/dt effect, the gate should be turned on hard and fast such that the area turned on is initially maximized. This can be accomplished with a gate current pulse approach-ing five times the maximum specified continuous gate current, I_{gt}, and with a fast rise time (< 1 μs). The gate current pulse width should be greater than the propagation time; a figure of 10 μs minimum should satisfy most SCRs with average current ratings under 50 A or so.

The wiring inductance alone is generally large enough to limit the di/dt. Since most SCRs are good for over 100 A/μs, this effect is not too large a problem. However, if the di/dt is found excessive, it can be reduced by placing an inductance in the loop; but, again, this increases the circuit's response time to an overvoltage and the trade−off should be considered.

CROWBAR CURRENT TERMS

t = 0.5 ms/Div

t = 10 μs/Div

I = 200 A/Div	$R_S = 0$
MCR69	$V_C = 30$ V
C = 22,000 μF	$I_{GT} = 200$ mA
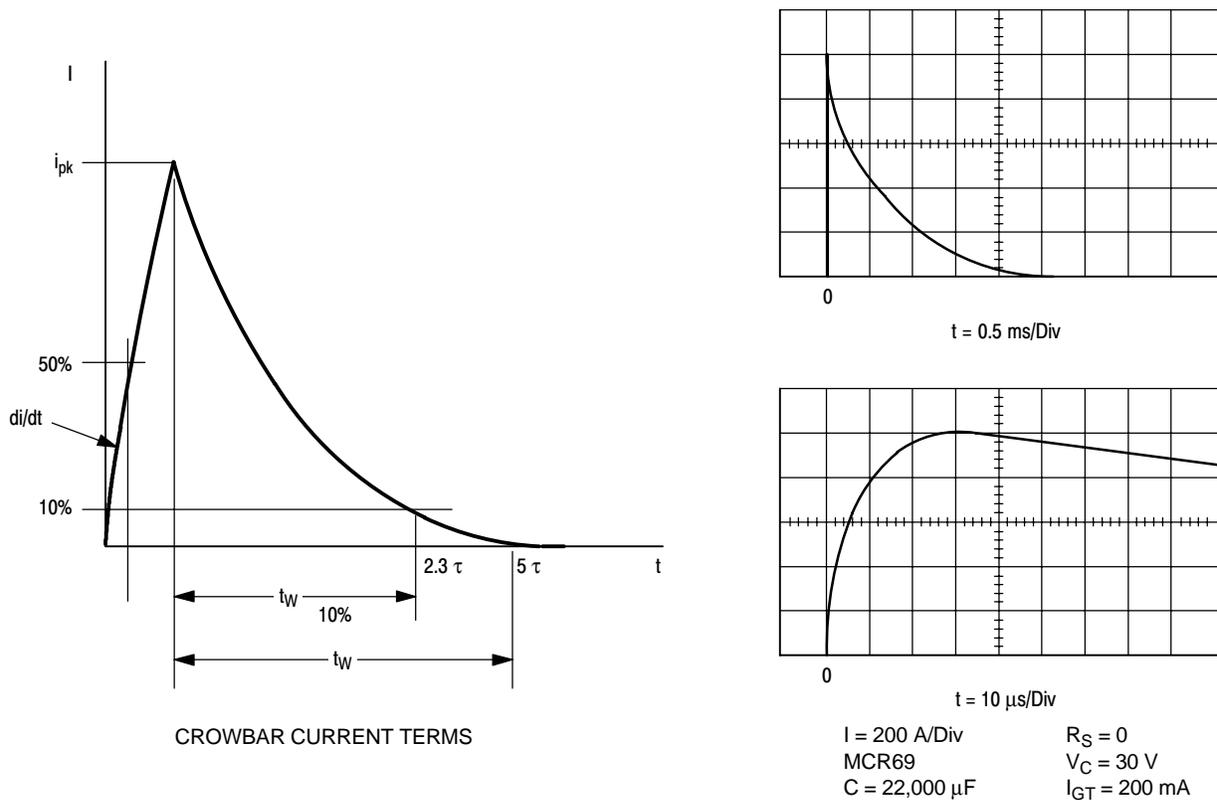
Figure 5.11. Typical SCR Crowbar Waveform
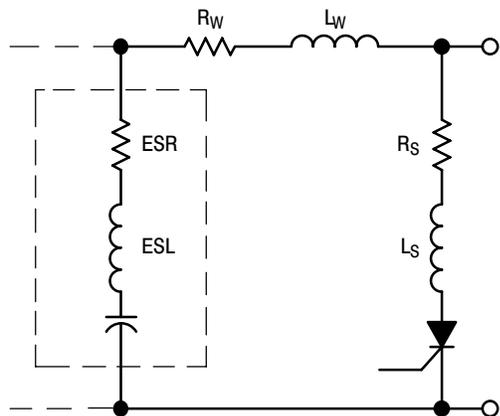
R_W, L_W: INTERCONNECTING WIRE IMPEDANCE
R_S, L_S: CURRENT LIMITING IMPEDANCE

**Figure 5.12. Circuit Elements Affecting SCR
Surge Current**

Since many SCR applications are for 60 Hz line operation, the specified peak non–repetitive surge current I_{TSM} and circuit fusing I^2t are based on 1/2 cycle (8.3 ms) conditions. For some SCRs, a derating curve based on up to 60 or 100 cycles of operation is also published. This rating, however, does not relate to crowbar applications. To fully evaluate a crowbar system, the SCR must be characterized with the capacitor dump exponential surge current pulse.

A simple test circuit for deriving this pulse is shown in Figure 5.13, whereby a capacitor is charged through a limiting resistor to the supply voltage, V, and then the charge is dumped by the SCR device under test (DUT). The SCR gate pulse can be varied in magnitude, pulse width, and rise time to produce the various I_{GT} conditions. An estimate of the crowbar energy capability of the DUT is determined by first dumping the capacitor charged to low voltage and then progressively increasing the voltage until the DUT fails. This is repeated for several devices to establish an average and minimum value of the failure points cluster.
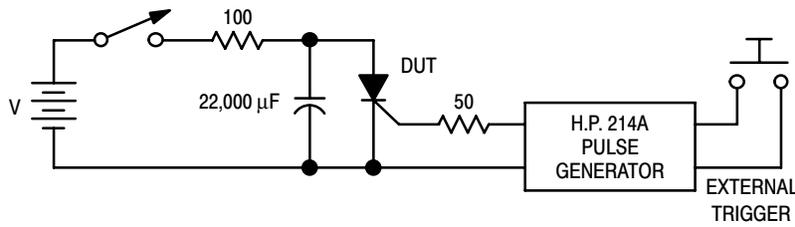
Figure 5.13

This procedure was used to test several different SCRs of which the following Table 5.4 describes several of the pertinent energy specifications and also the measured crowbar surge current at the point of device failure.

This one−shot destruct test was run with a gate current of five $I_{GT(MAX)}$ and a 22,000 μF capacitor whose ESR produced the exponentially decaying current pulse about 1.5 ms wide at its 10% point. Based on an appropriate derating, ten devices of each line where then successfully tested under the following conditions.

Device	V_C	i_{pk}	t
2N6397	12 V	250 A	1.5 ms
2N6507	30 V	800 A	1.5 ms

To determine the effect of gate drive on the SCRs, three devices from each line were characterized at non−destruct levels using three different capacitors (200, 6,000, and 22,000 μF), three different capacitor voltages (10, 20, and 30 V), and three different gate drives (IGT(MAX), 5 IGT(MAX), and a ramp IGT(MAX) with a di/dt of about 1 mA/μs). Due to its energy limitations, the MCR68 was tested with only 10 V across the larger capacitors.

The slow ramp, I_{GT}, was used to simulate overvoltage sense applications where the gate trigger rise time can be slow such as with a coupling zener diode.

No difference in SCR current characteristics were noted with the different gate current drive conditions; the peak currents were a function of capacitor voltage and circuit impedance, the fall times related to RTC, and the rise times, tr, and di/dt, were more circuit dependent (wiring inductance) and less device dependent (SCR turn−on time, ton). Since the wiring inductance limits, tr, the effect of various IGTs was masked, resulting in virtually identical waveforms.

The derated surge current, derived from a single (or low number) pulse test, does not truly reflect what a power supply crowbar SCR might have to see over the life of the supply. Life testing over many cycles have to be performed; thus, the circuit described in Appendix IV was developed. This life test fixture can simultaneously test ten SCRs under various crowbar energy and gate drive conditions.

Table 5.4. Specified and Measured Current Characteristics of Three SCRs

Device	Case	Maximum Specified Values					Measured Crowbar Surge Current I_{pk}		
		$I_{T(rms)}$ (A)	$I_{T(AV)}$ (A)	I_{TSM*} (A)	I^2t (A^{2}s)	I_{GT}(Max) (mA)	Min (A)	Max (A)	Ave (A)
2N6397	TO−220	12	8	100	40	30	380	750	480
2N6507	TO−220	25	16	300	375	40	1050	1250	1100

* I_{TSM} = Peak Non−Repetitive Surge Current, 1/2 cycle sine wave, 8.3 ms.

Each of the illustrated SCRs of Figure 5.14(a) were tested with as many as four limiting resistors (0, 50, 100, and 240 mΩ) and run for 1000 cycles at a nominal energy level. If no failures occurred, the peak current was progressively increased until a failure(s) resulted. Then the current was reduced by 10% and ten new devices were tested for 2000 cycles (about six hours at 350 cycles/hour). If this test proved successful, the data was further derated by 20% and plotted as shown on log–log paper with a slope of − 1/4. This theoretical slope, due to the $I^2\sqrt{t}$ one–dimensional heat–flow relationship (see Appendix VI), closely follows the empirical results. Of particular interest is that although the peak current increases with decreasing time, as expected, the I^2t actually decreases.
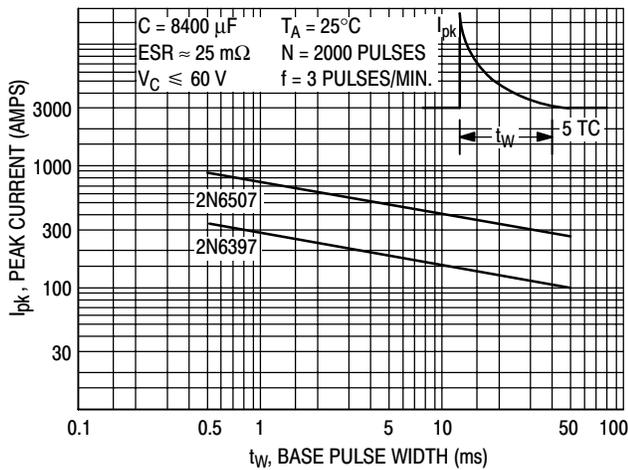
Figure 5.14(a). Peak Surge Current versus Pulse Width

(b). Peak Surge Current versus Ambient Temperature

Figure 5.14(b) shows the effect of elevated ambient temperature on the peak current capability of the illustrated SCRs.

FUSE CHARACTERISTICS

SCRs, like rectifiers, are generally rated in terms of average forward current, $I_{T(AV)}$, due to their half–wave operation. Additionally, an rms forward current, $I_{T(rms)}$, a peak forward surge current, I_{TSM}, and a circuit–fusing energy limit, I^2t, may be shown. However, these specifications, which are based one–half cycle 60 Hz operation, are not related to the crowbar current pulse and some means must be established to define their relationship. Also, fuses which must ultimately match the SCR and the load, are rated in rms currents.

The crowbar energy curves are based on an exponentially decaying surge current waveform. This can be converted* to I_{rms} by the equation.

$$I_{rms} = 0.316 \, i_{pk}$$

which now allows relating the SCR to the fuse.

*See Appendix V

The logic load has its own overvoltage SOA as a function of time (Figure 5.9). The crowbar SCR must clamp the overvoltage within a specified time, and still be within its own energy rating; thus, the series–limiting resistance, R_S, in the crowbar path must satisfy both the load and SCR energy limitations. The overvoltage response time is set by the total limitations. The overvoltage response time is set by the total limiting resistance and dumped capacitor(s) time constant. Since the SOA of the TTL used in this exercise was derived by a rectangular overvoltage pulse (in effect, over–energy), the energy equivalent of the real–world exponentially falling voltage waveform must be made. An approximation can be made by using an equivalent rectangular pulse of 0.7 times the peak power and 0.7 times the base time.

Once an overvoltage is detected and the crowbar is enabled, in addition to sustaining the peak current, the SCR must handle the regulator short–circuit current for the time it takes to open the fuse.

Thus, all three elements are tied together — the load can take just so much overvoltage (over–energy) and the crowbar SCR must repeatedly sustain for the life of the equipment an rms equivalent current pulse that lasts for the fuse response time.

It would seem that the matching of the fuse to the SCR would be straightforward — simply ensure that the fuse rms current rating never exceed the SCR rms current rating (Figure 5.15), but still be sufficient to handle steady–state and normal overload currents. The more exact relationship would involve the energy dissipated in the system $\int I^2Rdt$, which on a comparative basis, can be reduced to I^2t. Thus, the "let–through" I^2t of the fuse should not exceed I^2t capability of the SCR under all operating conditions. These conditions are many, consisting of "available fault current," power factor of the load, supply voltage, supply frequency, ambient temperature, and various fuse factors affecting the I^2t.

There has been much detailed information published on fuse characteristics and, rather than repeat the text which would take many pages, the reader is referred to those sources. Instead, the fuse basics will be defined and an example of matching the fuse to the SCR will be shown.

In addition to interrupting high current, the fuse should limit the current, thermal energy, and overvoltage due to the high current. Figure 5.16 illustrates the condition of the fuse at the moment the over–current starts. The peak let–through current can be assumed triangular in shape for a first–order approximation, lasting for the clearing time of the fuse. This time consists of the melting or pre–arcing time and the arcing time. The melting time is an inverse function of over–current and, at the time that the fuse element is opened, an arc will be formed causing the peak arc voltage. This arc voltage is both fuse and circuit dependent and under certain conditions can exceed the

peak line voltage, a condition the user should ensure does not overstress the electronics.

The available short–circuit current is the maximum current the circuit is capable of delivering and is generally limited by the input transformer copper loss and reactance when the crowbar SCR is placed at the input to the regulator or the regulator current limiting when placed at the output. For a fuse to safely protect the circuit, it should limit the peak let–through current and clear the fault in a short time, usually less than 10 ms.
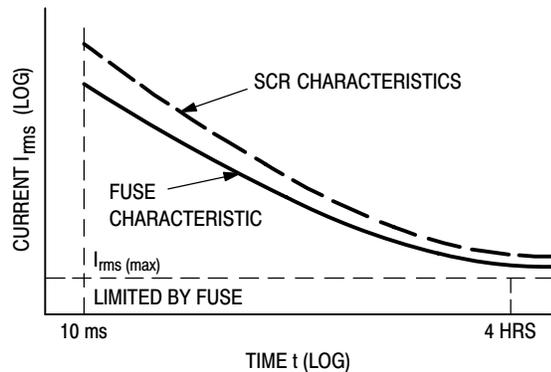
Figure 5.15. Time–Current Characteristic Curves of a Crowbar SCR and a Fuse
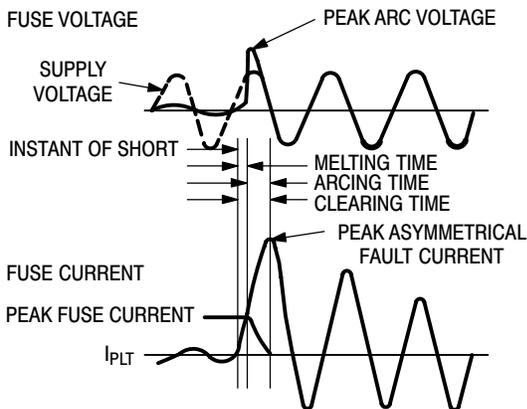
Figure 5.16. Typical Fuse Timing Waveforms During Short Circuit

Fuse manufacturers publish several curves for characterizing their products. The current–time plot, which describes current versus melting time (minimum time being 10 ms), is used in general industrial applications, but is not adequate for protecting semiconductors where the clearing time must be in the subcycle range. Where protection is required for normal multicycle overloads, this curve is useful.

Two other useful curves, the total clearing I^2t characteristic and the peak let–through current I_{PLT} characteristic, are illustrated in Figures 5.17 and 5.18 respectively. Some vendors also show total clearing time curves (overlayed on Figure 5.17 as dotted lines) which then allows direct comparison with the SCR energy limits. When this clearing time information is not shown, then the designer should determine the I_{PLT} and I^2t from the respective curves and then solve for the clearing time from the approximate equation relating these two parameters. Assuming a triangular waveform for I_{PLT}, the total clearing time, t_c, would then approximately be

$$t_c \approx \frac{3\, I^2t}{I_{PLT}^2}$$

Once t_c of the fuse is known, the comparison with the SCR can readily be made. As long as the I^2t of the fuse is less than the I^2t of the SCR, the SCR is protected. It should be pointed out that these calculations are predicated on a known value of available fault current. By inspection of Figure 5.18, it can be seen that I_{PLT} can vary greatly with available fault current, which could have a marked effect on the degree of protection. Also, the illustrated curves are for particular operating conditions; the curves will vary somewhat with applied voltage and frequency, initial loading, load power factor, and ambient temperature. Therefore, the reader is referred to the manufacturer's data sheet in those cases where extrapolation will be required for other operating conditions. The final proof is obtained by testing the fuse in the actual circuit under worst–case conditions.

CROWBAR EXAMPLE

To illustrate the proper matching of the crowbar SCR to the load and the fuse, consider the following example. A 50 A TTL load, powered by a 60 A current limited series regulator, has to be protected from transients on the supply bus by crowbarring the regulator output. The output filter capacitor of 10,000 μF (200 μF/A) contributes most of the energy to be crowbarred (the input capacitor is current limited by the regulator). The transients can reach 18 V for periods 100 ms.

Referring to Figure 5.9, it is seen that this transient exceeds the empirically derived SOA. To ensure safe operation, the overvoltage transient must be crowbarred within 5 ms. Since the TTL SOA is based on a rectangular power pulse even though plotted in terms of voltage, the equivalent crowbarred energy pulse should also be derived. Thus, the exponentially decaying voltage waveform should be multiplied by the exponentially decaying current to result in an energy waveform proportional to e^{-2x}. The rectangular equivalent will have to be determined and then compared with the TTL SOA. However, for simplicity, by using the crowbarred exponential waveform, a conservative rating will result.
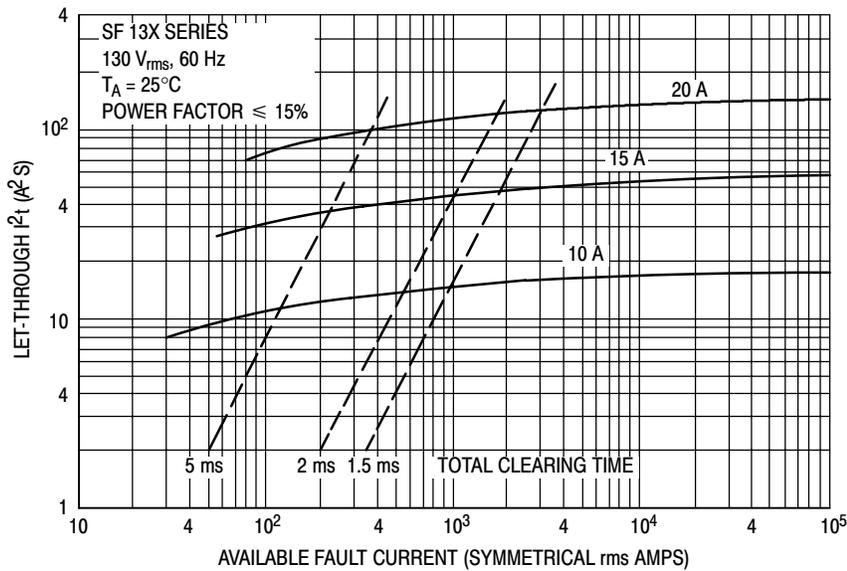
Figure 5.17. Maximum Clearing I²t Characteristics for 10 to 20 A Fuses

To protect the SCR, a fuse must be chosen that will open before the SCR's I^2t is exceeded, the current being the regulator limiting current which will also be the available fault current to the fuse.

The fuse could be eliminated by using a 60 A SCR, but the cost versus convenience trade−off of not replacing the fuse is not warranted for this example. A second fuse or circuit breaker will protect the rectifiers and regulator for internal faults (shorts), but its selection, which is based on the respective energy limits of those components, is not part of this exercise.

If a crowbar discharge time of 3 ms were chosen, it would not only be within the rectangular pulsed SOA, but also be well within the derived equivalent rectangular model of the exponential waveform. It would also require about 1.3 time constants for the overvoltage to decay from 18 V to 5 V; thus, the RC time constant would be 3 ms/1.3 or 2.3 ms.

The limiting resistance, R_S would simply be

$$R_S = \frac{2.3 \text{ ms}}{10,000 \ \mu F} = 0.23 \ \Omega \cong 0.2 \ \Omega$$
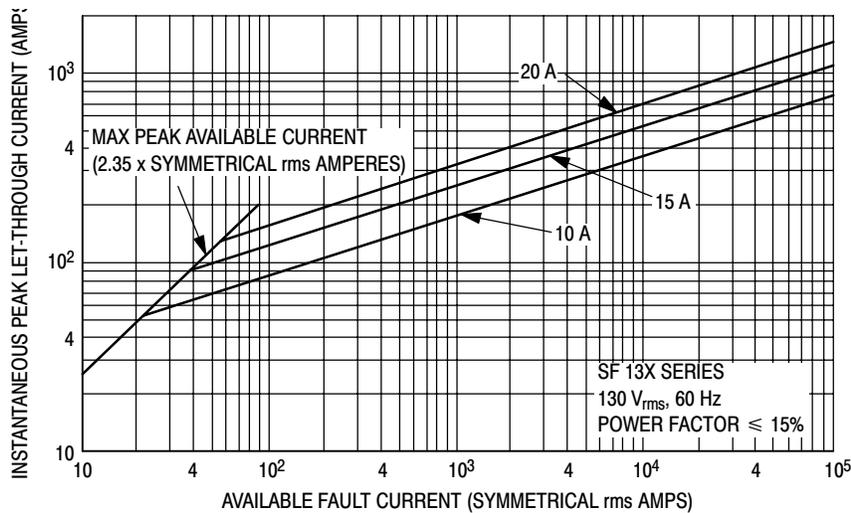
Figure 5.18. Peak Let−Through Current versus Fault Current for 10 to 20 A Fuses

Since the capacitor quickly charges up to the over–voltages V_{CC1} of 18 V, the peak capacitor discharge current would be

$$I_{pk} = \frac{V_{CC1}}{R_S} = \frac{18 \text{ V}}{0.2 \text{ } \Omega} = 90 \text{ A}$$

The rms current equivalent for this exponentially decaying pulse would be

$$I_{rms} = 0.316 \, I_{pk} = 0.316(90) = 28.4 \text{ A rms}$$

Now referring to the SCR peak current energy curves (Figure 5.14), it is seen that the MCR68 can sustain 210 A peak for a base time of 3 ms. This 12 A SCR must also sustain the 60 A regulator limited current for the time required to open the fuse. The MCR68 has a specified peak forward surge current rating of 100 A (1/2 cycle, sine wave, 60 Hz, non–repetitive) and a circuit fusing rating of 40 A^2s.

The non–repetitive rating implies that the device can sustain 100 occurrences of this 1/2 cycle surge over the life of the device; the SCR crowbar surge current curves were based on 2000 cycles.

For the 3 ms time frame, the $I_1^2 t_1$ for the exponential waveform is

$$I_1^2 t_1 = (28.4 \text{ A})^2 (3 \text{ ms}) = 2.4 \text{ A}^2\text{s}$$

Assuming that the fuse will open within 6 ms, the approximate energy that the SCR must sustain would be 60 A for an additional 3 ms. By superposition, this would amount to

$$I_2^2 t_2 = (60 \text{ A})^2 (6 \text{ ms}) = 21.6 \text{ A}^2\text{s}$$

which, when added to the exponential energy, would result in 24 A^2.

The MCR68 has a 40 A^2s rating based on a 1/2 cycle of 8.3 ms. Due to the one–dimensional heat flow in the device, the energy capability is not linearly related to time, but varies as to the $\sqrt{t}$. Therefore, with a 6 ms 1/2–cycle sine wave, the 40 A^2t rating would now decrease to approximately (see Appendix VI for derivation).

$$I_2^2 t_2 = I_1^2 t_1 \left(\frac{t_2}{t_1}\right)^{1/2}$$

$$= 40 \text{ A}^2\text{s} \left(\frac{6 \text{ ms}}{8.3 \text{ ms}}\right)^{1/2}$$

$$= 34 \text{ A}^2\text{s}$$

Although the 1/2 cycle extrapolated rating is greater than the actual crowbar energy, it is only characterized for 100 cycles of operation.

To ensure 2000 cycles of operation, at a somewhat higher cost, the 25 A MCR69 could be chosen. Its exponential peak current capability, at 3 ms, is about 560 A and has a specified I_{TSM} of 300 A for 8.3 ms. The I^2t rating is not specified, but can be calculated from the equation

$$I^2 t = \frac{(I_{TSM})^2}{2} \, t = \frac{(300 \text{ A})^2}{2} (8.3 \text{ ms}) = 375 \text{ A}^2\text{s}$$

Extrapolating to 6 ms results in about 318 A^2s, an I^2t rating much greater than the circuit 24 A^2s value.

The circuit designer can then make the cost/performance trade–offs.

All of these ratings are predicated on the fuse operating within 6 ms.

With an available fault current of 60 A, Figure 5.17 shows that a 10 A (SF13X series) fuse will have a let–through I^2t of about 10 A^2s and a total clearing time of about 6 ms, satisfying the SCR requirements, that is,

$$I^2 t \text{ fuse} < I^2 t \text{ SCR}$$

$$t_c \leq 6 \text{ ms}$$

Figure 5.18 illustrates that for the same conditions, instantaneous peak let–through current of about 70 A would result. For fuse manufacturers that don't show the clearing time information, the approximate time can be calculated from the triangular model, as follows

$$t_c = \frac{3 \, I^2 t}{I_{PLT}^2} = \frac{3(10)}{(70)^2} = 6.1 \text{ ms}$$

The fuse is now matched to the SCR which is matched to the logic load. Other types of loads can be similarly matched, if the load energy characteristics are known.

CHARACTERIZING SWITCHES AS LINE–TYPE MODULATORS

In the past, hydrogen thyratrons have been used extensively as discharge switches for line type modulators. In general, such devices have been highly satisfactory from an electrical performance standpoint, but they have some major drawbacks including relatively large size and weight, low efficiency (due to filament power requirements), and short life expectancy compared with semiconductor devices, now can be eliminated through the use of silicon controlled rectifiers.

A line type modulator is a modulator whose output–pulse characteristics are determined by a lumped–constant transmission line (pulse forming network) and by the proper match of the line impedance (PFN) to the load impedance.

A switch for this type modulator should only initiate conduction and should have no effect on pulse characteristics. This is in contrast to a hard switch modulator where output pulse characteristics are determined by the "hard" relationship of grid (base) control of conduction through a vacuum tube (transistor) switch.

Referring to the schematic (Figure 5.25), when the power supply is first turned on, no charge exists in the PFN, and energy is transferred from the power supply to the PFN via the resonant circuit comprising the charging choke and PFN capacitors. At the time that the voltage

across the PFN capacitors reaches twice the power supply voltage, current through the charging choke tries to reverse and the power supply is disconnected due to the back biased impedance of the hold−off diode. If we assume this diode to be perfect, the energy remains stored in the PFN until the discharge switch is triggered to its on state. When this occurs, assuming that the pulse transformer has been designed to match the load impedance to the PFN impedance, all energy stored in the PFN reactance will be transferred to the load if we neglect switch losses. Upon completion of the transfer of energy the switch must return to its off condition before allowing transfer of energy once again from the power supply to the PFN storage element.

OPTIMUM SWITCH CHARACTERISTICS

FORWARD BREAKOVER VOLTAGE

Device manufacturers normally apply the variable−amplitude output of a half−wave rectifier across the SCR. Thus, forward voltage is applied to the device for only a half cycle and the rated voltage is applied only as an ac peak. While this produces a satisfactory rating for ac applications, it does not hold for dc.

An estimated 90% of devices tested for minimum breakover voltage (V_{BO}) in a dc circuit will not meet the data sheet performance specifications. A switch designed for the pulse modulator application should therefore specify a minimum continuous forward breakover voltage at rated maximum leakage current for maximum device temperatures.

THE OFF SWITCH

The maximum forward leakage current of the SCR must be limited to a low value at maximum device temperature. During the period of device nonconduction it is desired that the switch offer an off impedance in the range of megohms to hundreds of megohms. This is required for two reasons: (1) to prevent diminishing the efficiency of recharge by an effective shunt path across the PFN, and (2) to prevent the bleeding off of PFN charge during the interpulse period. This second factor is especially important in the design of radar tansponders wherein the period between interrogations is variable. Change of the PFN voltage during the interpulse period could result in frequency shift, pulse instabilities, and loss of power from the transmitter being modulated.

THE ON SWITCH

At present, SCR design is more limited in the achievable maximum forward sustaining voltage than in the current that the device will conduct. For this reason modulators utilizing SCRs can be operated at lower impedance levels than comparable thyratron circuits of yesterday. It is not uncommon for the characteristic impedance of the pulse forming network to be in the order of 5 to 10 ohms or less. Operating the SCR at higher current to switch the same equivalent pulse power as a thyratron requires the SCR on impedance to be much lower so that the I^2R loss is a reasonable value, in order to maintain circuit efficiency. Low switch loss, moreover, is mandatory because internal power dissipation can be directly translated into junction−temperature−rise and associated leakage current increase which, if excessive, could result in thermal runaway.

TURN−ON TIME

In radar circuits the *pulse−power* handling capability of an SCR, rather than the normally specified *average−power* capability, is of primary importance.

For short pulses at high PRFs the major portion of semiconductor dissipation occurs during the initial turn−on during the time that the anode rises from its forward leakage value to its maximum value. It is necessary, therefore, that turn−on time be as short as possible to prevent excessive power dissipation.

The function of radar is to provide distance information measured as a function of time. It is important, therefore, that any delay introduced by a component be fixed in relation to some variable parameter such as signal strength or temperature. For radar pulse modulator applications, a minimal delay variation versus temperature is required and any such variation must be repetitive from SCR to SCR, in production lots, so that adequate circuit compensation may be provided.

PULSE GATE CURRENT TO FIRE

The time of delay, the time of rise, and the delay variation versus temperature associated with SCR turn−on are functions of the gate triggering current available and the trigger pulse duration. In order to predict pulse circuit operation of the SCR, the pulse gate current required to turn the device on when switching the low−impedance modulator should be specified and the limits of turn−on−time variation for the specified pulse trigger current and collector load should be given at the high and low operating temperature extremes.

RECOVERY TIME

After the cessation of forward conducting current in the on device, a time of SCR circuit isolation must be provided to allow the semiconductor to return to its off state. Recovery time cannot be given as an independent parameter of device operation, but must include factors as determined by the external circuit, such as: (1) pulse current and rate of decay; (2) availability of an inverse voltage immediately following pulse−current conduction; (3) level of base bias following pulse current conduction; (4) rate of rise of reapplied positive voltage and its amplitude in relation to SCR breakover voltage; and (5) maximum circuit ambient temperature.

In the reverse direction the controlled rectifier behaves like a conventional silicon diode. Under worst circuit conditions, if an inverse voltage is generated through the existence of a load short circuit, the current available will be limited only by the impedance of the pulse forming network and SCR inverse characteristics. The reverse current is able to sweep out some of the carriers from the SCR junctions. Intentional design of the load impedance to something less than the network impedance allows development of an inverse voltage across the SCR immediately after pulse conduction, enhancing switch turn−off time. Careful use of a fast clamp diode in series with a fast zener diode, the two in shunt across the SCR, allows application of a safe value of circuit−inverse−voltage without preventing the initial useful reverse current. Availability of a negative base−bias following pulse current conduction provides a similar enhancement of switch turn−off time.

If removal of carriers from the SCR junction enables a faster switch recovery time, then, conversely, operation of the SCR at high temperatures with large forward currents and with slow rate of current decay all increase device recovery time.

HOLDING CURRENT

One of the anomalies that exist in the design of a pulse SCR is the requirement for a high holding current. This need can be determined by examining the isolation component that disconnects the power supply from the discharge circuit during the time that PFN energy is being transferred to the transmitter and during the recovery time of the discharge switch. An inductance resonating with the PFN capacitance at twice the time of recharge is normally used for power supply isolation. Resonant charging restricts the initial flow of current from the power supply, thereby maximizing the time at which power supply current flow will exceed the holding current of the SCR. If the PFN recharge current from the power supply exceeds the holding current of the SCR before it has recovered, the SCR will again conduct without the application of a trigger pulse. As a result continuous conduction occurs from the power supply through the low impedance path of the charging choke and on switch. This lock−on condition can completely disable the equipment employing the SCR switch.

The charging current passed by the inductance is given as (the PFN inductance is considered negligible):

$$i_c(t) = \frac{E_{bb} - V_n(0)}{\sqrt{L_c/C_n}} \left(\frac{\cos \dfrac{T_r - 2t}{2\sqrt{L_c C_n}}}{\sin \dfrac{T_r}{2\sqrt{L_c C_n}}} \right)$$

Where

E_{bb} = power supply voltage

$V_n(0)$ = 0 volts if the PFN employs a clamp diode or is matched to the load

T_r = time of resonant recharge and is usually equal to $\dfrac{1}{PRF}$

L_c = value of charging inductance

C_n = value of total PFN capacity

For a given radar pulse modulator design, the values of power supply voltage, time of resonant recharge, charging choke inductance, and PFN capacitance are established. If the time (t) represents the recovery time of the SCR being used as the discharge switch, i_c then represents the minimum value of holding current required by the SCR to prevent power supply lock−on. Conversely, if the modulator design is about an existing SCR where holding current, recovery time, and forward breakover voltage are known, the charge parameters can be derived by rewriting the above formula as follows:

$$i_H = \frac{V_{BO} - V_n(0)}{\sqrt{L_c/C_n}} \left(\frac{\cos \dfrac{T_r - 2(\text{recovery time})}{2\sqrt{L_c C_n}}}{\sin \dfrac{T_r}{2\sqrt{L_c C_n}}} \right)$$

The designer may find that for the chosen SCR the desired characteristics of modulator pulse width and pulse repetition frequency are not obtainable.

One means of increasing the effective holding current of an SCR is for the semiconductor to exhibit some turn−off gain characteristic for the residual current flow at the end of the modulator pulse. The circuit designer then can provide turn−off base current, making the SCR more effective as a pulse circuit element.

THE SCR AS A UNIDIRECTIONAL SWITCH

When triggered to its on state, the SCR, like the hydrogen thyratron, is capable of conducting current in one direction. A load short circuit could result in an inverse voltage across the SCR due to the reflection of voltage from the pulse forming network. The circuit designer may wish to provide an intentional load−to−PFN mismatch such that some inverse voltage is generated across the SCR to enhance its turn−off characteristics. Nevertheless, since the normal circuit application is unidirectional, the semiconductor device designer could take advantage of this fact in restricting the inverse−voltage rating that the SCR must withstand. The circuit designer, in turn, can accommodate this lack of peak−inverse−voltage rating by use of a suitable diode clamp across the PFN or across the SCR.

SCRs TESTS FOR PULSE CIRCUIT APPLICATION

The suitability for pulse circuit applications of SCRs not specifically characterized for such purposes can be determined from measurements carried out with relatively simple test circuits under controlled conditions. Applicable test circuits and procedures are outlined in the following section.

FORWARD BLOCKING VOLTAGE AND LEAKAGE CURRENT

Mount the SCRs to a heat sink and connect the units to be tested as shown in Figure 5.21. Place the assembly in an oven and stabilize at maximum SCR rated temperature. Turn on the power supply and raise the voltage to rated V_{BO}. Allow units to remain with the voltage applied for minimum of four hours. At the end of the temperature soak, determine if any units exhibit thermal runaway by checking for blown fuses (without removing the power). Reject any units which have blown circuit fuses. The forward leakage current, I_{LF}, of the remaining units may be calculated after measuring the voltage V_L, across resistor R2. Any units with a leakage current greater than manufacturer's rating should be rejected.
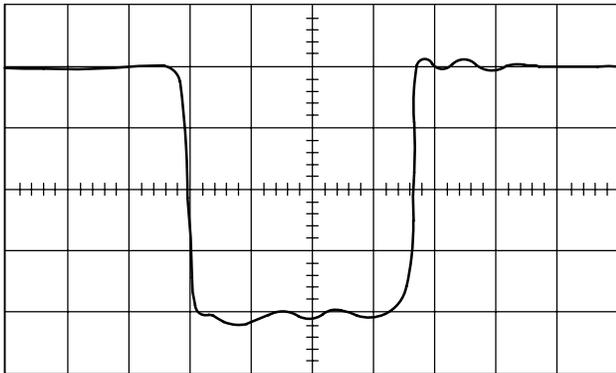
Figure 5.20. Vertical Set to 4 cm, Horizontal 0.2 μs/cm. Detected RF Magnetron Pulse

TURN–ON TIME, VARIATION AND ON IMPEDANCE

This circuit assumes that the pulse gate current required to switch a given modulator load current is specified by the manufacturer or that the designer is able to specify the operating conditions. Typical operating values might be:

Time of trigger pulse t = 1 μs
Pulse gate current I_G = 200 mA
Forward blocking voltage V_{BO} = 400 V
Load current I_{Load} = 30 A

To measure turn–on time using a Tektronix 545 oscilloscope (or equivalent) with a dual trace type CA plug–in, connect probes of Channels A and B to Test Points A and B. Place the Mode selector switch in the Added Algebraically position and the Channel B Polarity switch in the Inverted position. Adjust the HR212A pulse generator to give a positive pulse 1 μs wide (100 pps) as viewed at Test Point A. Adjust the amplitude of the "added" voltage across the 100–ohm base resistor for the specified pulse gate current (200 mA in this example).

Switch the Mode selector knob to the alternate position. Connect Channel A to Test Point D. Leave the oscilloscope probe, Channel B, at Test Point B, thereby displaying the input trigger waveform. Measure the time between the 50 percent voltage amplitudes of the two waveforms. This is the Turn–On Time ($t_D + t_R$).

To measure turn–on time versus temperature, place the device to be tested on a suitable heat sink and place the assembly in a temperature chamber. Stabilize the chamber at minimum rated (cold) temperature. Repeat the above measurements. Raise the chamber temperature to maximum rated (hot) temperature and stabilize. Repeat the measurements above.
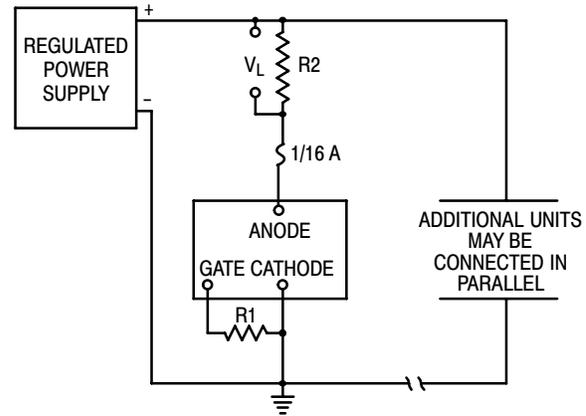
Figure 5.21. Test Setup for SCR Forward Blocking Voltage and Leakage Current Measurements

RESISTOR R1 IS USED ONLY IF MANUFACTURER CALLS FOR BIAS RESISTOR BETWEEN GATE AND CATHODE. RESISTOR R2 CAN HAVE ANY SMALL VALUE WHICH, WHEN MULTIPLIED BY MAXIMUM ALLOWABLE LEAKAGE CURRENT, WILL PROVIDE A CONVENIENT READING OF VOLTAGE V_L.

To measure the turn−on impedance for the specified current load, the on impedance can be measured as an SCR forward voltage drop. The point in time of measurement shall be half the output pulse width. For a 1 μs output pulse, the measurement procedure would be:

Connect the oscilloscope probe, Channel B, to Point D shown in Figure 5.22. Use the oscilloscope controls Time/CM and Multiplier to a setting of 0.5 μs per centimeter or faster. With the Amplitude Control set to view 100 volts per centimeter (to prevent amplifier overloading) measure the amplitude of the voltage drop, V_F, across the SCR 0.5 μs after the PFN voltage waveform has dropped to half amplitude. It may be necessary to check ground reference several times during this test to provide the needed accuracy of measurement.
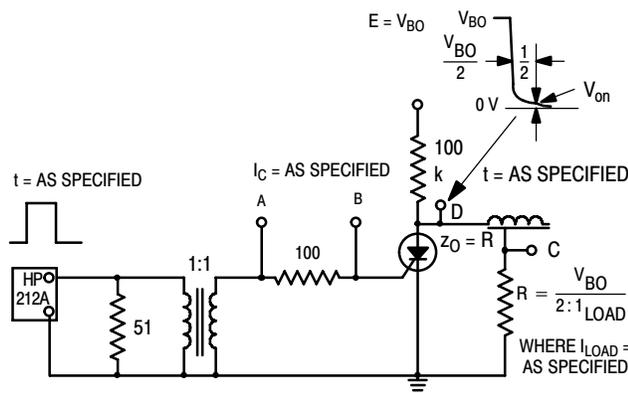
Figure 5.22. Suggested Test Circuit for SCR "On" Measurements

HOLDING CURRENT

The SCR holding current can be measured with or without a gate turn−off current, according to the position of switch S2. The ON Semiconductor Trigger Pulse Generator is a transistor circuit capable of generating a 1.5 μs turn−on pulse followed by a variable−duration turn−off pulse. Measurements should be made at the maximum expected temperature of operation. Resistor R1 should be chosen to allow an initial magnitude of current flow at the device pulse current rating.

To measure holding current, connect the SCRs under test as illustrated in Figure 5.23. Place SCRs in oven and stabilize at maximum expected operating temperature. View the waveform across R1 by connecting the oscilloscope probe (Tektronix 2465) Channel A to Point A, and Channel B to Point B. Place the Mode Selector switch in the Added Algebraically position. Place the Polarity swich of Channel B in the Inverted position. Adjust both Volts/CM switches to the same scale factor, making sure that each Variable knob is in its Calibrated position. Adjust pulse generator for a positive pulse, 1 μs wide, and 1,000 pps pulse repetition frequency. Adjust power supply voltage to rated V_{BO}. Adjust input pulse amplitude until unit fully triggers. Measure amplitude of voltage drop across R1, $V(A - B)$, and calculate holding current in mA from the equation

$$mA = \frac{V(A - B)}{R1} + \frac{V_{BO}}{100 \text{ k}\Omega}$$

Any unit which turns on but does not turn off has a holding current of less than

$$\frac{V_{BO} \text{ V}}{100 \text{ k}\Omega}$$

The approximate voltage setting to view the amplitude of the holding current will be 10 or 20 volts per centimeter. The approximate sweep speed will be 2 to 5 μs per centimeter. These settings will, of course, vary, depending upon the holding current of the unit under test.

SCR recovery time is greatly dependent upon the circuit in which the device is used. However, any test of SCR recovery time should suffice to compare devices of various manufacturers, as long as the test procedure is standardized. Further evaluation of the selected devices could be made in an actual modulator circuit tester wherein techniques conducive to SCR turn−off are used. The circuit setup shown in Figures 5.24 and 5.25 can be employed for such tests. A slight load to PFN mismatch is called for to generate an inverse voltage across the SCR at the termination of the output pulse. An SCR gate turn−off pulse is used. The recharge component is a charging choke, providing optimized conditions of reapplied voltage to the PFN (and across the SCR). Adequate heat sinking of the SCR should be provided.
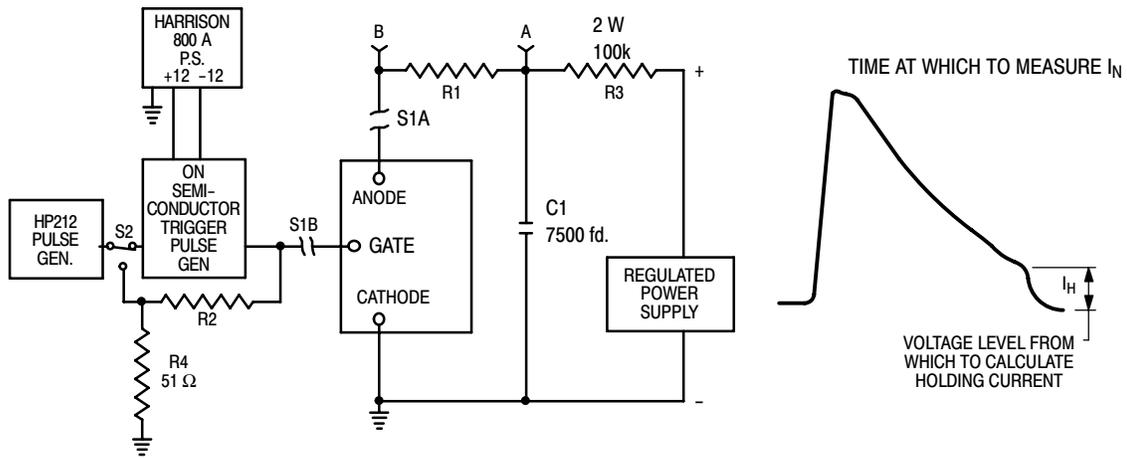
NOTE: ADDITIONAL UNITS MAY BE TESTED BY SWITCHING THE
ANODE AND GATE CONNECTIONS TO SIMILARLY
MOUNTED SCRs. SHORT LEAD LENGTHS ARE DESIRABLE.

Figure 5.23. Test Setup for Measuring Holding Current
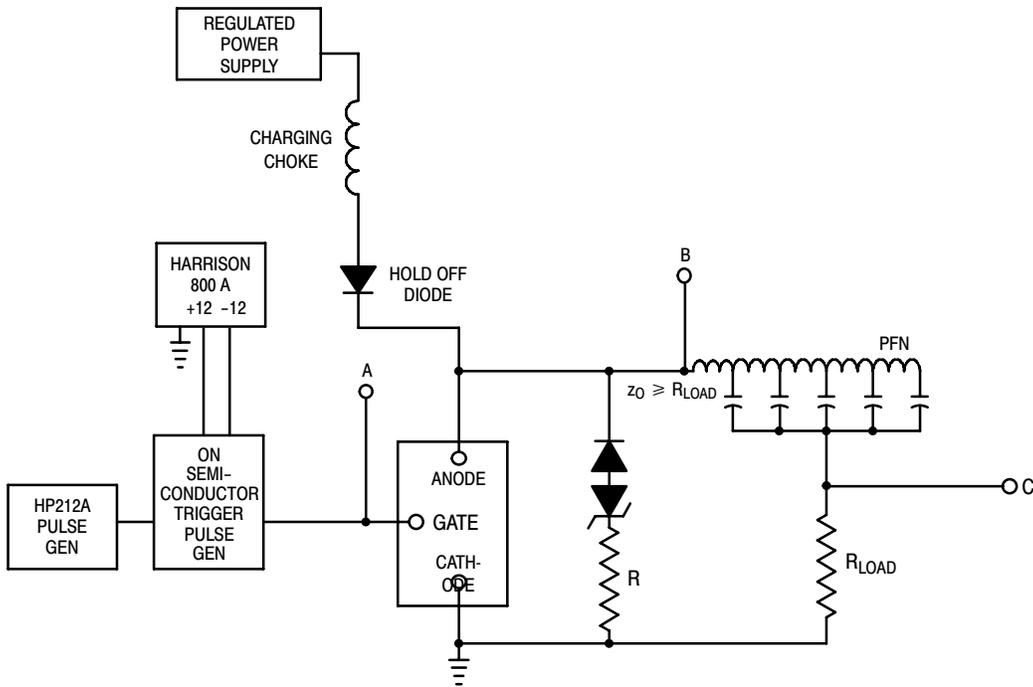
Figure 5.24. Modulator Circuit for SCR Tests
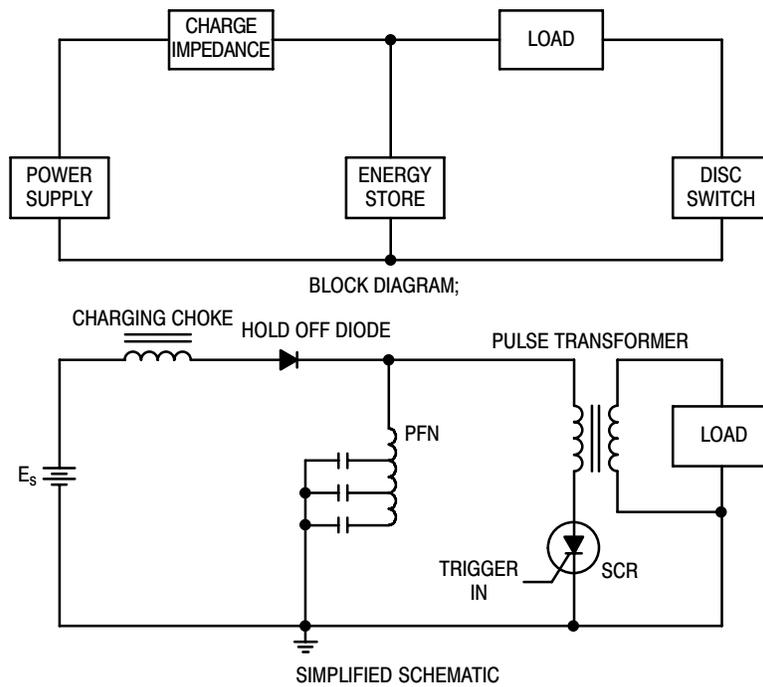
Figure 5.25. Radar Modulator, Resonant Line Type

PARALLEL CONNECTED SCRs

When an application requires current capability in excess of a single economical SCR, it can be worthwhile to consider paralleling two or more devices. To help determine if two or more SCRs in parallel are more cost effective than one high current SCR, some of the advantages and disadvantages are listed for parallel devices.

Advantages
1. Less expensive to purchase
2. Less expensive to mount
3. Less expensive to replace, in case of failure
4. Ease of mounting
5. Ease of isolation from sink

Disadvantages
1. Increased SCR count
2. Selected or matched devices
3. Increased component count
4. Greater R & D effort

There are several factors to keep in mind in paralleling and many are pertinent for single SCR operations as well.

GATE DRIVE

The required gate current (I_{GT}) amplitude can vary greatly and can depend upon SCR type and load being switched. As a general rule for parallel SCRs, I_{GT} should be at least two or three times the $I_{GT(MAX)}$ specification on the data sheet and ideally close to, but never exceeding, the maximum specified gate power dissipation or peak current. Adequate gate current is necessary for rapid turn−on of all the parallel SCRs and to ensure simultaneous turn−on without excessive current crowding across any of the individual die. The rise time of the gate drive pulse should be fast, ideally ≤ 100 ns. Each gate should be driven from a good current source and through its own resistor, even if transformer drive is used. Gate pulse width requirements vary but should be of sufficient width to ensure simultaneous turn−on and last well beyond the turn−on delay of the slowest device, as well as beyond the time required for latching of all devices. Ideally, gate current would flow for the entire conduction period to ensure latching under all operating conditions.

With low voltage switching, which includes conduction angles near 180° and near zero degrees, the gate drive requirements can be more critical and special emphasis may be required of gate pulse amplitude and width.

PARAMETER MATCHING

For reliable current sharing with parallel SCRs, there are certain device parameters that should be matched or held within close tolerances. The degree of matching required varies and can be affected by type of load (resistive, inductive, incandescent lamp or phase con-trolled loads) being switched.

The most common device parameters that can effect current sharing are:

1. t_d — turn−on delay time
2. t_r — turn−on rise time of anode current
3. $V_{A(MIN)}$ — minimum anode voltage at which device will turn on
4. Static on−state voltage and current
5. I_L — Latching current

The four parameters shown in Table 5.6 were measured with a curve tracer and are:

I_L, latching current; V_{TM}, on−state voltage; I_{GT} and V_{GT}, minimum gate current and voltage for turn on.
Of the four parameters, I_L and V_{TM} can greatly affect current sharing.

The latching current of each SCR is important at turn−on to ensure each device turns on and will stay on for the entire conduction period. On−state voltage determines how well the SCRs share current when cathode ballasting is not used.

Table 5.5 gives turn−on delay time (t_d) and turn−on rise time (t_r) of the anode−cathode voltage and the minimum forward anode voltage for turn−on. These parameters were measured in the circuits shown in Figures 5.28 and 5.29. One SCR at a time was used in the circuit shown in Figure 5.28.

Turn−on delay on twenty−five SCRs was measured (only ten are shown in Table 5.5) and they could be from one or more production lots. The variation in t_d was slight and ranged from 35 to 44 ns but could vary considerably on other production lots and this possible variation in t_d would have to be considered in a parallel application.

Waveforms for minimum forward anode voltage for turn−on are shown in Figure 5.26. The trailing edge of the gate current pulse is phase delayed (R_3) so that the SCR is not turned on. The width of the gate current pulse is now increased (R_5) until the SCR turns on and the forward anode voltage switches to the on−state at about 0.73 V. This is the minimum voltage at which this SCR will turn on with the circuit conditions shown in Figure 5.28.

For dynamic turn−on current sharing, t_d, t_r and $V_{A(MIN)}$ are very important. As an example, with a high wattage incandescent lamp load, it is very important that the inrush current of the cold filament be equally shared by the parallel SCRs. The minimum anode voltage at which a device turns on is also very important. If one of the parallel devices turns on before the other devices and its on−state voltage is lower than the required minimum anode voltage for turn−on of the unfired devices, they therefore cannot turn on. This would overload the device which

turned on, probably causing failure from over−current and excessive junction temperature.

Table 5.5. MCR12D Turn−On Delay, Rise Time and Minimum Forward Anode Voltage For Turn−On

Device	Turn−On Delay and Rise Time Off−State Voltage = 8 V Peak R_L = 10 Ohms, $I_A \cong$ 6.5 A Peak I_G = 100 mA (PW = 100 μs) Conduction Angle 90 Degrees		Minimum Anode Voltage For Turn−On Off−State Voltage = 4 V Peak R_L = 0.5 Ohm I_A = 5A I_G = 100 mA
	$t_{d(ns)}$	$t_{r(\mu s)}$	(Volts)
1	35	0.80	0.70
2	38	0.95	0.81
3	45	1	0.75
4	44	1	0.75
5	44	0.90	0.75
6	43	0.85	0.75
7	38	1.30	0.75
8	38	1.25	0.70
9	38	1	0.75
10	37	0.82	0.70

Figure 5.26. Minimum Anode Voltage For Turn−On Off−State Voltage = 4 V Peak, R_L = 0.5 Ohm, $I_A \approx$ 5 A, I_G = 75 mA

Turn−off time — t_q is important in higher frequency applications which require the SCR to recover from the forward conduction period and be able to block the next cycle of forward voltage. Thus, t_q matching for high frequency operation can be as important as t_d, t_r and $V_{A(MIN)}$ matching for equal turn−on current sharing.

Due to the variable in t_q measurement, no further attempt will be made here to discuss this parameter and the reader is referred to Application Note AN914.

The need for on−state matching of current and voltage is important, especially in unforced current sharing circuits.

UNFORCED CURRENT SHARING

When operating parallel SCRs without forced current sharing, such as without cathode ballasting using resistors or inductors, it is very important that the device parameters be closely matched. This includes t_d, t_r, minimum forward anode voltage for turn−on and on−state voltage matching. The degree of matching determines the success of the circuit.

In circuits without ballasting, it is especially important that physical layout, mounting of devices and resistance paths be identical for good current sharing, even with on−state matched devices.

Figure 5.27 shows how anode current can vary on devices closely matched for on−state voltage (1, 3 and 4) and a mismatched device (2). Without resistance ballasting, the matched devices share peak current within one ampere and device 2 is passing only nine amps, seven amps lower than device 1. Table 5.6 shows the degree of match or mismatch of V_{TM} of the four SCRs.

With unforced current sharing ($R_K = 0$), there was a greater tendency for one device (1) to turn−on, preventing the others from turning on when low anode switching voltage (≤ 10 V rms) was tried. Table 5.5 shows that the minimum anode voltage for turn−on is from 7 to 14% lower for device 1 than on 2, 3 and 4. Also, device 1 turn−on delay is 35 ns versus 38, 45 and 44 ns for devices 2, 3 and 4.

The tendency for device 1 to turn on, preventing the other three from turning on, is most probably due to its lower minimum anode voltage requirement and shorter turn on delay. The remedy would be closer matching of the minimum anode voltage for turn−on and driving the gates hard (but less than the gate power specifications) and increasing the width of the gate current pulse.

FORCED CURRENT SHARING

Cathode ballast elements can be used to help ensure good static on−state current sharing. Either inductors or resistors can be used and each has advantages and disadvantages. This section discusses resistive ballasting, but it should be kept in mind that the inductor method is usually better suited for the higher current levels. Although they are more expensive and difficult to design, there is less power loss with inductor ballasting as well as other benefits.

The degree of peak current sharing is shown in Figure 5.27 for four parallel MCR12D SCRs using cathode resistor ballasting with an inductive anode load. With devices 1, 3 and 4, on−state voltage is matched within 10 mV at an anode current of 15 A (See Table 5.6) and are within 1A of each other in Figure 5.27, with cathode resistance (R_K) equal to zero. As R_K increases, the current sharing becomes even closer. The unmatched device 2, with a V_{TM} of 1.41 V (Table 5.6), is not carrying

its share of current (Figure 5.29) with R_K equal zero. As R_K increases, device 2 takes a greater share of the total current and with R_K around 0.25 ohm, the four SCRs are sharing peak current quite well. The value of R_K depends on how close the on−state voltage is matched on the SCRs and the degree of current sharing desired, as well as the permissible power dissipation in R_K.
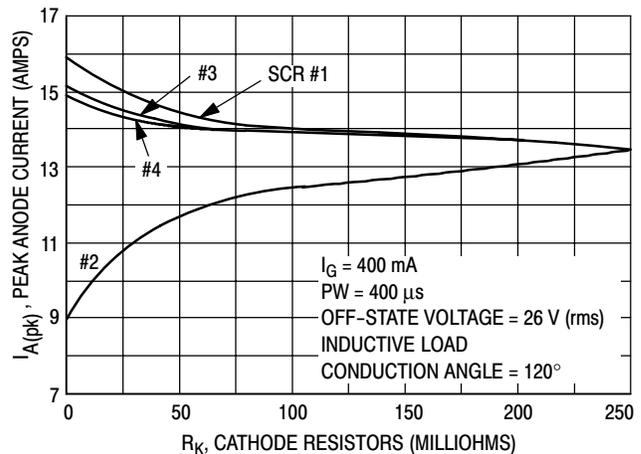
Figure 5.27. Effects Of Cathode Resistor On Anode Current Sharing

Table 5.6. MCR12D Parameters Measured On Curve Tracer, $T_C = 25°C$

Device #	I_L, Latching Current $V_D = 12$ Vdc $I_G = 100$ mA	V_{TM}, On−State Voltage $I_A = 15$ A PW = 300 µs	Minimum Gate Current & Voltage for Turn−On $V_D = 12$ Vdc, $R_L = 140 \ \Omega$	
			I_{GT}	V_{GT}
1	13 mA	1.25 V	5.6 mA	0.615 V
2	27	1.41	8.8	0.679
3	28	1.26	12	0.658
4	23	1.26	9.6	0.649
5	23	1.28	9.4	0.659
6	23	1.26	9.6	0.645
7	18	1.25	7.1	0.690
8	19	1.25	7	0.687
9	19	1.25	8.4	0.694
10	16	1.25	6.9	0.679

LINE SYNCHRONIZED DRIVE CIRCUIT

Gate drive for phase control of the four parallel SCRs is accomplished with one complementary MOS hex gate, MC14572, and two bipolar transistors (Figure 5.28). This adjustable line−synchronized driver permits SCR conduction from near zero to 180 degrees. A Schmitt trigger clocks a delay monostable multivibrator that is followed by a pulse−width monostable multivibrator.

Line synchronization is achieved through the half–wave section of the secondary winding of the full–wave, center–tapped transformer (A). This winding also supplies power to the circuit through rectifiers D_1 and D_2.

The full–wave signal is clipped by diode D_5, referenced to a + 15 volt supply, so that the input limit of the CMOS chip is not exceeded. The waveform is then shaped by the Schmitt trigger, which is composed of inverters U_{1-a} and U_{1-b}. A fast switching output signal B results.

The positive–going edge of this pulse is differentiated by the capacitive–resistive network of C_1 and R_2 and triggers the delay multivibrator that is composed of U_{1-c} and U_{1-d}. As a result, the normally high output is switched low. The trailing edge of this pulse (C) then triggers the following multivibrator, which is composed of NAND gate U_{1-e} and inverter U_{1-f}. The positive going output pulse (waveform D) of this multivibrator, whose width is set by potentiometer R_6, turns on transistors Q_1 and Q_2, which drives the gates of the four SCRs. Transistor Q_2 supplies about 400 mA drive current to each gate through 100 ohm resistors and has a rise time of ≤ 100 ns.
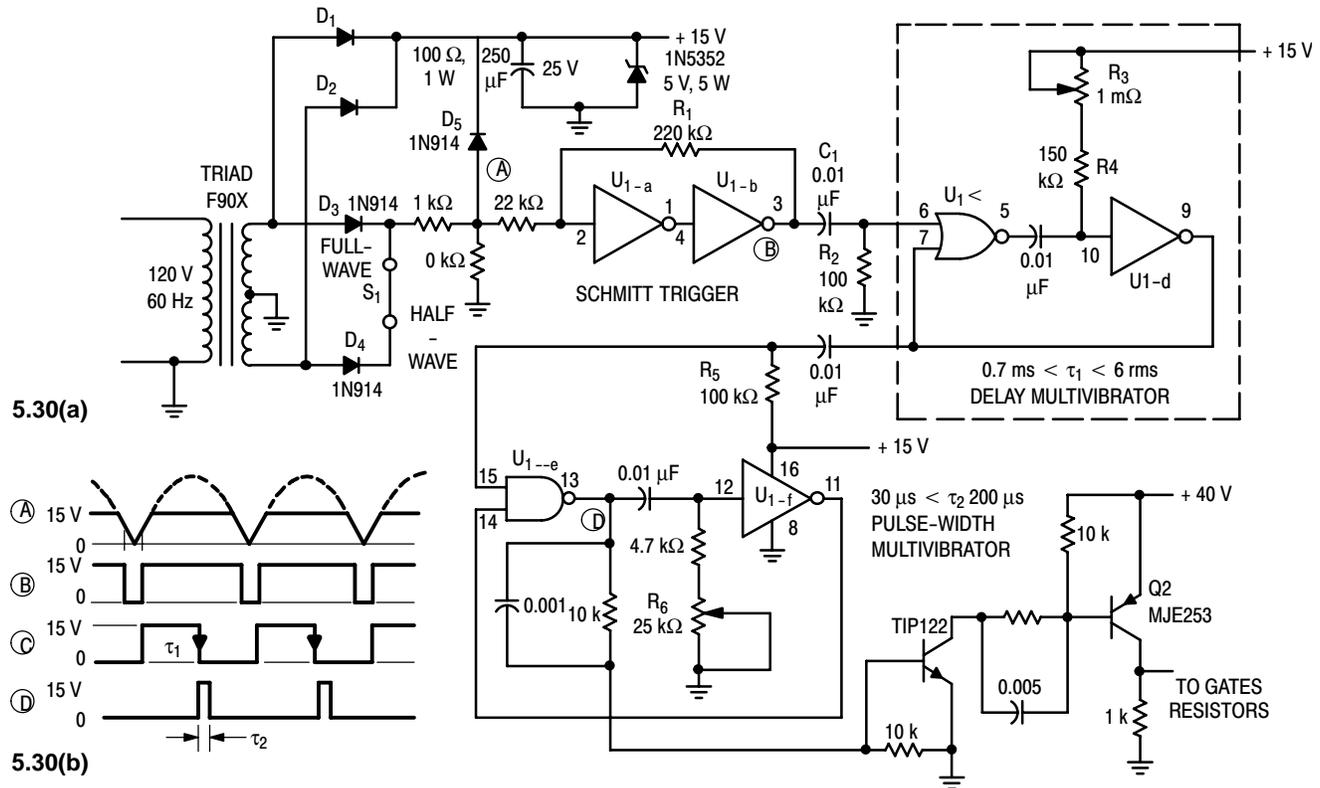
Figure 5.28. Line–Synchronized Gate Driver

PARALLEL SCR CIRCUIT

The four SCRs are MCR12Ds, housed in the TO–220 package, rated at 12 A rms, 50 V and are shown schematically in Figure 5.29. Due to line power limitations, it was decided to use a voltage step down transformer and not try working directly from the 120 V line. Also, line isolation was desirable in an experiment of this type.

The step down transformer ratings were 120 V rms primary, 26 V rms secondary, rated at 100 A, and was used with a variable transformer for anode voltage adjustment.

The inductive load consisted of four filter chokes in parallel (Stancor #C–2688 with each rated at 10 mH, 12.5 Adc and 0.11 ohm).

For good current sharing with parallel SCRs, symmetry in layout and mounting is of primary importance. The four SCRs were mounted on a natural finish aluminum heat sink and torqued to specification which is 8 inch pounds. Cathode leads and wiring were identical, and when used, the cathode resistors R_K were matched within 1%. An RC snubber network (R_7 and C_2) was connected across the anodes–cathodes to slow down the rate–of–rise of the off–state voltage, preventing unwanted turn–on.

LOAD: FOUR STANCOR FILTER CHOKES (#C–2688) IN PARALLEL
EACH RATED AT: 10 mH @ 12.5 Adc AND 0.11 OHMS
ALL ANODES COMMON TO HEAT SINK
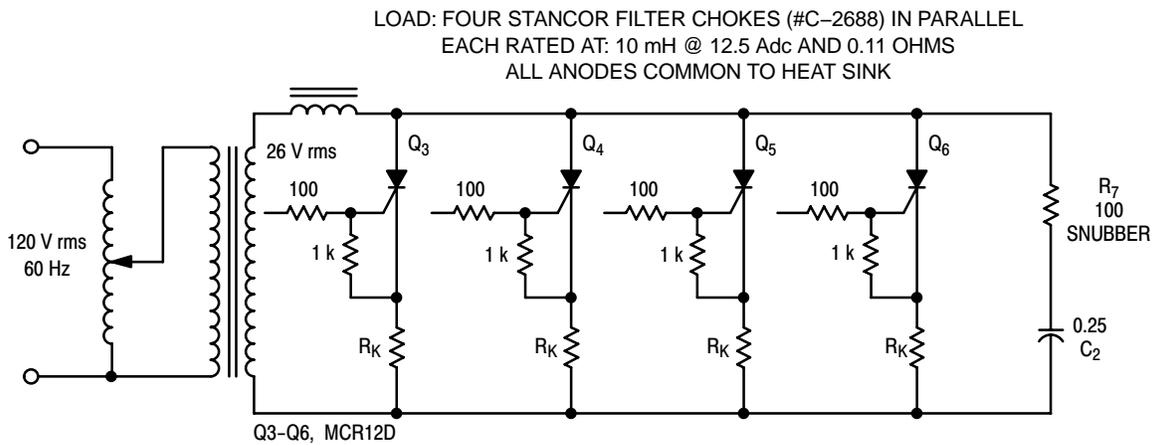
Figure 5.29. Parallel Thyristors

CHARACTERIZING RFI SUPPRESSION IN THYRISTOR CIRCUITS

In order to understand the measures for suppression of EMI, characteristics of the interference must be explored first. To have interference at all, we must have a transmitter, or creator of interference, and a receiver, a device affected by the interference. Neither the transmitter nor the receiver need be related in any way to those circuits commonly referred to as radio–frequency circuits. Common transmitters are opening and closing of a switch or relay contacts, electric motors with commutators, all forms of electric arcs, and electronic circuits with rapidly changing voltages and currents. Receivers are generally electronic circuits, both low and high impedance which are sensitive to pulse or high frequency energy. Often the very circuits creating the interference are sensitive to similar interference from other circuits nearby or on the same power line.

EMI can generally be separated into two categories — radiated and conducted. Radiated interference travels by way of electro–magnetic waves just as desirable RF energy does. Conducted interference travels on power, communications, or control wires. Although this separation and nomenclature might seem to indicate two neat little packages, independently controllable, such is not the case. The two are very often interdependent such that in some cases control of one form may completely eliminate the other. In any case, both interference forms must be considered when interference elimination steps are taken.

Phase control circuits using thyristors (SCRs, triacs, etc.) for controlling motor speed or resistive lighting and heating loads are particularly offensive in creating interference. They can completely obliterate most stations on any AM radio nearby and will play havoc with another control on the same power line. These controls are generally connected in one of the two ways shown in the block diagrams of Figure 5.30.

A common example of the connection of 5.30(a) is the wall mounted light dimmer controlling a ceiling mounted lamp. A motorized appliance with a built–in control such as a food mixer is an example of the connection shown in 5.30(b).

Figure 5.30(a) may be re–drawn as shown in Figure 5.31, illustrating the complete circuit for RF energy. The switch in the control box represents the thyristor, shown in its blocking state. In phase control operation, this switch is open at the beginning of each half cycle of the power line alternations. After a delay determined by the remainder of the control circuitry, the switch is closed and remains that way until the instantaneous current drops to zero. This switch is the source from which the RF energy flows down the power lines and through the various capacitors to ground.
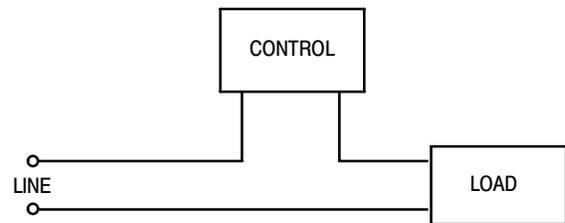
(a). Separately Mounted Control
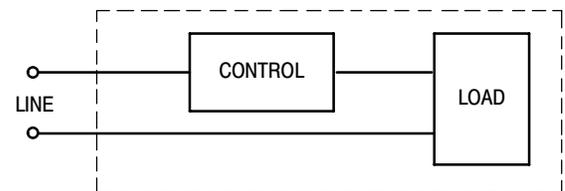
(b). Control and Load in the Same Enclosure

Figure 5.30. Block Diagram of Control Connections

If the load is passive, such as a lamp or a motor which does not generate interference, it may be considered as an impedance bypassed with the wire–to–wire capacitance of its leads. If it is another RF energy source, however, such as a motor with a commutator, it must be treated separately to reduce interference from that source. The power supply may be considered as dc since the interference pulse is extremely short (10 μs) compared to the period of the power line frequency (16 ms for 60 Hz). The inductance associated with the power source comes from two separate phenomena. First is the leakage impedance of the supply transformer, and second is the self–inductance of the wires between the power line transformer and the load.

One of the most difficult parameters to pin down in the system is the effect of grounding. Most industrial and commercial wiring and many homes use a grounded conduit system which provides excellent shielding of radiated energy emanating from the wiring. However, a large number of homes are being wired with two to three wire insulated cable without conduit. In three–wire systems, one wire is grounded independently of the power system even though one of the power lines is already grounded. The capacitances to ground shown in Figure 5.31 will be greatly affected by the type of grounding used. Of course, in any home appliance, filtering must be provided suitable for all three different systems.

Before the switch in the control is closed, the system is in a steady–state condition with the upper line of the power line at the system voltage and the bottom line and the load at ground potential. When the switch is closed, the upper line potential instantaneously falls due to the line and source inductance, then it rises back to its original value as the line inductance is charged. While the upper line is rising, the line from the control to the load also rises in potential. The effect of both of these lines increasing in potential together causes an electro–static field change which radiates energy. In addition, any other loads connected across the power lines at point A, for example, would be affected by a temporary loss of voltage created by the closing of the switch and by the line and source inductance. This is a form of conducted interference.

A second form of radiated interference is inductive coupling in which the power line and ground form a one–turn primary of an air core transformer. In this mode, an unbalanced transient current flows down the power lines with the difference current flowing to ground through the various capacitive paths available. The secondary is the radio antenna or the circuit being affected. This type of interference is a problem only when the receiver is within about one wavelength of the transmitter at the offending frequency.

Radiated interference from the control circuit proper is of little consequence due to several factors. The lead lengths in general are so short compared to the wave-lengths in question that they make extremely poor antenna. In addition, most of these control circuits are mounted in metal enclosures which provide shielding for radiated energy generated within the control circuitry.

A steel box will absorb radiated energy at 150 kHz such that any signal inside the box is reduced 12.9 dB per mil of thickness of the box. In other words, a 1/16 inch thick steel box will attenuate radiated interference by over 800 dB! A similar aluminum box will attenuate 1 dB per mil or 62.5 dB total. Thus, even in an aluminum box, the control circuitry will radiate very little energy.

Both forms of radiated interference which are a problem are a result of conducted interference on the power lines which is in turn caused by a rapid rise in current. Thus, if this current rise is slowed, all forms of interference will be reduced.

RFI SOLUTIONS

Since the switch in Figure 5.31, when it closes, provides a very low impedance path, a capacitor in parallel with it will show little benefit in slowing down the rise of current. The capacitor will be charged to a voltage determined by the circuit constants and the phase angle of the line voltage just before the switch closes. When the switch closes, the capacitor will discharge quickly, its current limited only by its own resistance and the resistance of the switch. However, a series inductor will slow down the current rise in the load and thus reduce the voltage transient on all lines. A capacitor connected as shown in Figure 5.32 will also help slow down the current rise since the inductor will now limit the current out of the capacitor. Thus, the capacitor voltage will drop slowly and correspondingly the load voltage will increase slowly.

Although this circuit will be effective in many cases, the filter is unbalanced, providing an RF current path through the capacitances to ground. It has, therefore, been found advantageous to divide the inductor into two parts and to put half in each line to the control. Figure 5.33 illustrates this circuit showing the polarity marks of two coils which are wound on the same core.

A capacitor at point A will help reduce interference further. This circuit is particularly effective when used with the connection of Figure 5.30(b) where the load is not always on the grounded side of the power line. In this case, the two halves of the inductor would be located in the power line leads, between the controlled circuit and the power source.
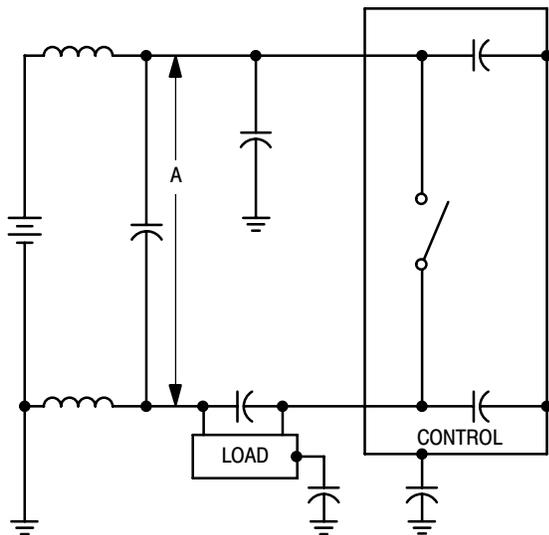
Figure 5.31. RF Circuit for Figure 5.30(a)
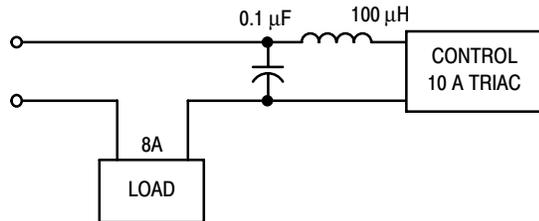
Figure 5.32. One Possible EMI Reduction Circuit

Where the control circuit is sensitive to fast rising line transients, a capacitor at point B will do much to eliminate this problem. The capacitor must charge through the impedance of the inductor, thus limiting the rate of voltage change (dv/dt) applied to the thyristor while it is in the blocking state.

DESIGN CRITERIA

Design equations for the split inductor have been developed based on parameters which should be known before attempting a design. The most difficult to determine is t_r, the minimum allowable current rise time which will not cause objectionable interference. The value of this parameter must be determined empirically in each situation if complete interference reduction is needed. ON Semiconductor has conducted extensive tests using an AM radio as a receiver and a 600 Watt thyristor lamp dimmer as a transmitter. A rate of about 0.35 Amp per μs seems to be effective in eliminating objectionable interference as well as materially reducing false triggering of the thyristor due

to line transients. The value of t_r may be calculated by dividing the peak current anticipated by the allowable rate of current rise.

Ferrite core inductors have proved to be the most practical physical configuration. Most ferrites are effective; those with highest permeability and saturation flux density are preferred. Those specifically designed as high frequency types are not necessarily desirable.

Laminated iron cores may also be used; however, they require a capacitor at point A in Figure 5.33 to be at all effective. At these switching speeds, the iron requires considerable current in the windings before any flux change can take place. We have found currents rising to half their peak value in less than one μs before the inductance begins to slow down the rise. The capacitor supplies this current for the short period without dropping in voltage, thus eliminating the pulse on the power line.

Once a core material has been selected, wire size is the next decision in the design problems. Due to the small number of turns involved (generally a single layer) smaller sizes than normally used in transformers may be chosen safely. Generally, 500 to 800 circular mills per ampere is acceptable, depending on the enclosure of the filter and the maximum ambient temperature expected.

An idea of the size of the core needed may be determined from the equation:

$$(1) \quad A_c A_w = \frac{26 \, A_{wire} \, E_{rms} \, t_r}{B_{MAX}}$$

where:

A_c = the effective cross-sectional area of the core in in^2

A_w = available core window area in in^2

A_{wire} = wire cross section in circular mils

B_{MAX} = core saturation flux density in gauss

t_r = allowable current rise time in seconds

E_{rms} = line voltage

(A factor of 3 has been included in this equation to allow for winding space factor.) Once a tentative core selection has been made, the number of turns required may be found from the equation:

$$(2) \quad N = \frac{11 \, E_{rms} \, t_r \times 10^6}{B_{MAX} A_c}$$

where:

N = the total number of turns on the core

The next step is to check how well the required number of turns will fit onto the core. If the fit is satisfactory, the core design is complete; if not, some trade-offs will have to be made.
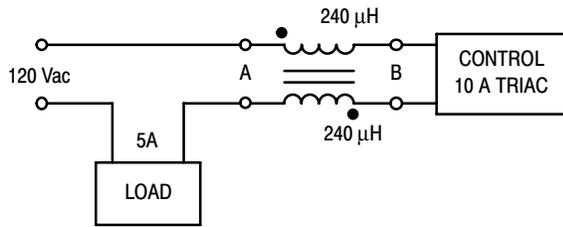
Figure 5.33. Split Inductor Circuit

In most cases, the inductor as designed at this point will have far too much inductance. It will support the entire peak line voltage for the time selected as t_r and will then saturate quickly, giving much too fast a current rise. The required inductance should be calculated from the allowable rise time and load resistance, making the rise time equal to two time constants. Thus:

$$(3) \qquad \frac{2L}{R} = t_r \quad \text{or} \quad L = \frac{R\,t_r}{2}$$

Paper or other insulating material should be inserted between the core halves to obtain the required inductance by the equation:

$$(4) \qquad I_g = \frac{3.19\,N^2\,A_c \times 10^{-8}}{L} - \frac{I_c}{\mu}$$

where:

I_g = total length of air gap in inches

μ = effective ac permeability of the core material at the power line frequency

I_c = effective magnetic path length of the core in inches

A_c = effective cross sectional area of the core in square inches

L = inductance in henries

DESIGN EXAMPLE

Consider a 600 watt, 120 Volt lamp dimmer using an ON Semiconductor 2N6348A triac. Line current is $\frac{600}{120} =$ 5 amperes. #16 wire will provide about 516 circular mils per ampere.

For core material, type 3C5 of Ferroxcube Corporation of America, Saugerties, New York, has a high B_{max} and μ. The company specifies $B_{MAX} = 3800$ gauss and $\mu = 1900$ for material.

As was previously mentioned, a current rise rate of about 0.35 ampere per μs has been found to be acceptable for interference problems with ac–dc radios in most wiring situations. With 5 amperes rms, 7 amperes peak,

$$t_r = \frac{7}{0.35} = 20\ \mu s$$

Then the equation (1):

$$A_cA_w = \frac{26 \times 2580 \times 120 \times 20 \times 10^{-6}}{3800\ \text{gauss}} = 0.044$$

Core part number 1F30 of the same company in a U–1 configuration has an A_cA_w product of 0.0386, which should be close enough.

$$N = \frac{10.93 \times 120 \times 20 \times 10^{-6} \times 10^6}{3800 \times 0.137} = 42\ \text{turns}$$

Two coils of 21 turns each should be wound on either one or two legs and be connected as shown in Figure 5.33.

The required inductance of the coil is found from equation (3).

$$L = \frac{R\,t_r}{2} = \frac{E_{rated}}{I_{rated}} \times \frac{t_r}{2} = \frac{120}{5} \times \frac{20}{2} \times 10^{-6} = 240 \times 10^{-6}$$
$$L = 240\ \mu H$$

To obtain this inductance, the air gap should be

$$I_g = \frac{3.19 \times 42^2 \times 0.137 \times 10^{-8}}{240 \times 10^{-6}} - \frac{3.33}{1900} = 0.0321 - 0.00175$$
$$I_g = 0.03035$$

Thus, 15 mils of insulating material in each leg will provide the necessary inductance.

If a problem still exists with false triggering of the thyristor due to conducted interference, a capacitor at point B in Figure 5.33 will probably remedy the situation.

SECTION 6
APPLICATIONS

Edited and Updated

Because they are reliable solid state switches, thyristors have many applications, especially as controls.

One of the most common uses for thyristors is to control ac loads such as electric motors. This can be done either by controlling the part of each ac cycle when the circuit conducts current (phase control) or by controlling the number of cycles per time period when current is conducted (cycle control).

In addition, thyristors can serve as the basis of relaxation oscillators for timers and other applications. Most of the devices covered in this book have control applications.

PHASE CONTROL WITH THYRISTORS

The most common method of electronic ac power control is called *phase control*. Figure 6.1 illustrates this concept. During the first portion of each half-cycle of the ac sine wave, an electronic switch is opened to prevent the current flow. At some specific phase angle, α, this switch is closed to allow the full line voltage to be applied to the load for the remainder of that half-cycle. Varying α will control the portion of the total sine wave that is applied to the load (shaded area), and thereby regulate the power flow to the load.

The simplest circuit for accomplishing phase control is shown in Figure 6.2. The electronic switch in this case is a triac (Q) which can be turned on by a small current pulse to its gate. The TRIAC turns off automatically when the current through it passes through zero. In the circuit shown, capacitor C_T is charged during each half-cycle by the current flowing through resistor R_T and the load. The fact that the load is in series with R_T during this portion of the cycle is of little consequence since the resistance of R_T is many times greater than that of the load. When the voltage across C_T reaches the breakdown voltage of the DIAC bilateral trigger (D), the energy stored in capacitor C_T is released. This energy produces a current pulse in the DIAC, which flows through the gate of the TRIAC and turns it on. Since both the DIAC and the TRIAC are bidirectional devices, the values of R_T and C_T will determine the phase angle at which the TRIAC will be triggered in both the positive and negative half-cycles of the ac sine wave.
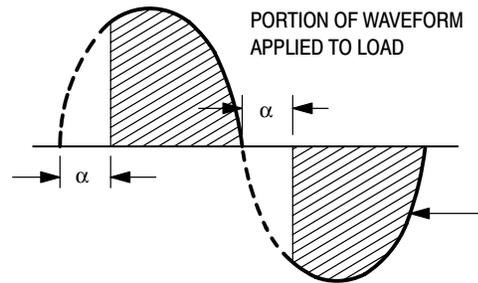
Figure 6.1. Phase Control of AC Waveform
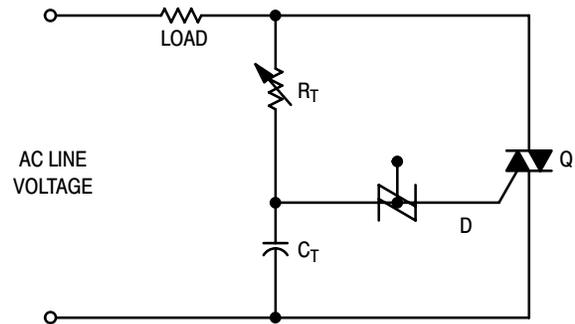
Figure 6.2. Simplest Circuit for Phase Control
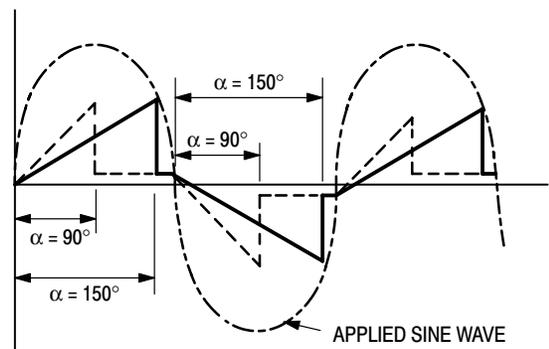
Figure 6.3. Waveforms of Capacitor Voltage at Two Phase Angles

The waveform of the voltage across the capacitor for two typical control conditions ($\alpha = 90°$ and $150°$) is shown in Figure 6.3. If a silicon controlled rectifier is used in this circuit in place of the TRIAC, only one half-cycle of the waveform will be controlled. The other half-cycle will be blocked, resulting in a pulsing dc output whose average value can be varied by adjusting R_T.

CONTROL OF INDUCTION MOTORS

Shaded-pole motors driving low-starting-torque loads such as fans and blowers may readily be controlled using any of the previously described full-wave circuits. One needs only to substitute the winding of the shaded-pole motor for the load resistor shown in the circuit diagrams.

Constant-torque loads or high-starting-torque loads are difficult, if not impossible, to control using the voltage controls described here. Figure 6.4 shows the effect of varying voltage on the speed-torque curve of a typical shaded-pole motor. A typical fan-load curve and a constant-torque-load curve have been superimposed upon this graph. It is not difficult to see that the torque developed by the motor is equal to the load torque at two different points on the constant-torque-load curve, giving two points of equilibrium and thus an ambiguity to the speed control. The equilibrium point at the lower speed is a condition of high motor current because of low counter EMF and would result in burnout of the motor winding if the motor were left in this condition for any length of time. By contrast, the fan speed-torque curve crosses each of the motor speed-torque curve crosses each of the motor speed-torque curves at only one point, therefore causing no ambiguities. In addition, the low-speed point is one of low voltage well within the motor winding's current-carrying capabilities.

Permanent-split-capacitor motors can also be controlled by any of these circuits, but more effective control is achieved if the motor is connected as shown in Figure 6.5. Here only the main winding is controlled and the capacitor winding is continuously connected to the entire ac line voltage. This connection maintains the phase shift between the windings, which is lost if the capacitor phase is also controlled. Figure 6.6(a) shows the effect of voltage on the speed-torque characteristics of this motor and a superimposed fan-load curve.
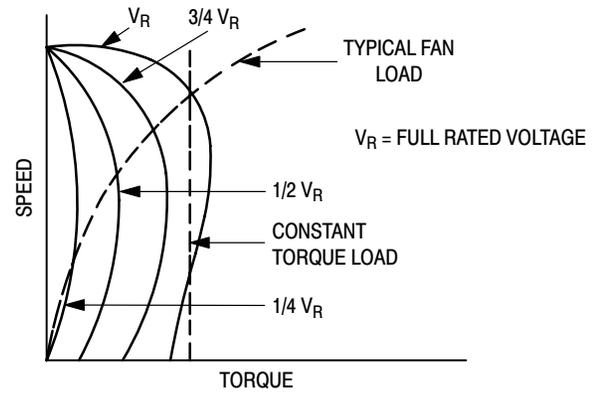
Figure 6.4. Characteristics of Shaded-Pole Motors at Several Voltages
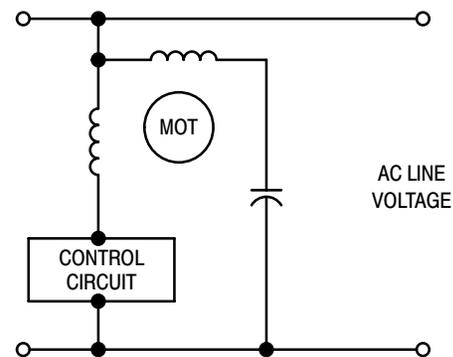
Figure 6.5. Connection Diagram for Permanent-Split-Capacitor Motors

Not all induction motors of either the shaded-pole or the permanent-split-capacitor types can be controlled effectively using these techniques, even with the proper loads. Motors designed for the highest efficiencies and, therefore, low slip also have a very low starting torque and may, under certain conditions, have a speed-torque characteristic that could be crossed twice by a specific fan-load speed-torque characteristic. Figure 6.6(b) shows motor torque-speed characteristic curves upon which has been superimposed the curve of a fan with high starting torque. It is therefore desirable to use a motor whose squirrel-cage rotor is designed for medium-to-high impedance levels and, therefore, has a high starting torque. The slight loss in efficiency of such a motor at full rated speed and load is a small price to pay for the advantage of speed control prevents the TRIAC from turning on due to line transients and inductive switching transients.
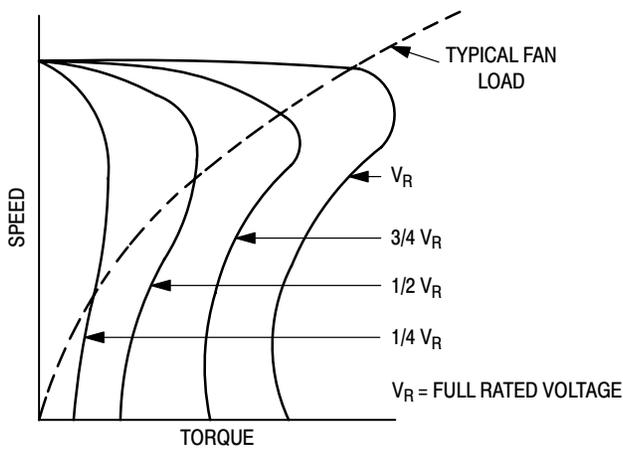
(a). High-Starting-Torque Motor
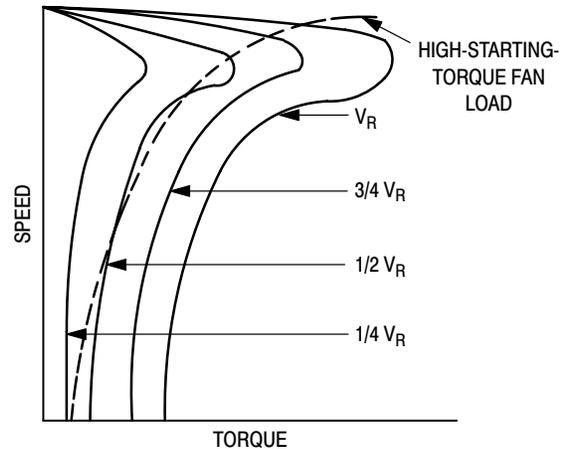
(b). High-Efficiency Motor

Figure 6.6. Speed–Torque Curves for a Permanent–Split–Capacitor Motors at Various Applied Voltages

A unique circuit for use with *capacitor-start motors* in explosive or highly corrosive atmospheres, in which the arcing or the corrosion of switch contacts is severe and undesirable, is shown in Figure 6.7. Resistor R1 is connected in series with the main running winding and is of such a resistance that the voltage drop under normal full-load conditions is approximately 0.2 V peak. Since starting currents on these motors are quite high, this peak voltage drop will exceed 1 V during starting conditions, triggering the TRIAC, which will cause current to flow in the capacitor winding. When full speed is reached, the current through the main winding will decrease to about 0.2 V, which is insufficient to trigger the TRIAC — thus the capacitor winding will no longer be energized. Resistor R2 and capacitor C2 form a dv/dt suppression network; this prevents the TRIAC from turning on due to line transients and inductive switching transients.

CONTROL OF UNIVERSAL MOTORS

Any of the half-wave or full-wave controls described previously can be used to control universal motors. *Non-feedback,* manual controls, such as those shown in Figure 6.2, are simple and inexpensive, but they provide very little torque at low speeds. A comparison of typical speed-torque curves using a control of this type with those of *feedback* control is shown in Figure 6.8.

These motors have some unique characteristics which allow their speed to be controlled very easily and efficiently with a feedback circuit such as that shown in Figure 6.9. This circuit provides phase-controlled half-wave power to the motor; that is, on the negative half-cycle, the SCR blocks current flow in the negative direction causing the motor to be driven by a pulsating direct current whose amplitude is dependent on the phase control of the SCR.

Figure 6.7. Circuit Diagram for Capacitor-Start Motor

(A) NON-FEEDBACK CONTROL
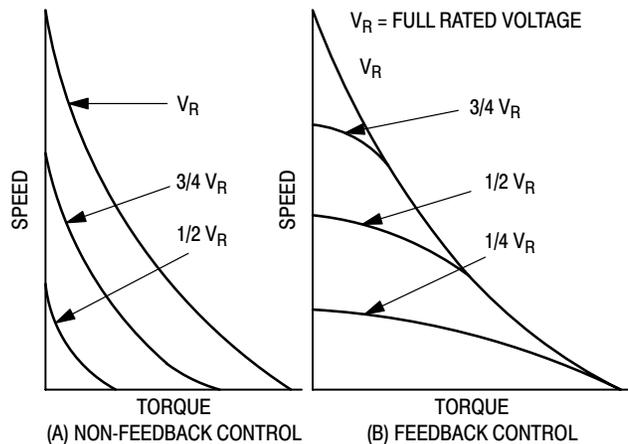
(B) FEEDBACK CONTROL

Figure 6.8. Comparison of Feedback Control with Non-Feedback Control

The theory of operation of this control circuit is not at all difficult to understand. Assuming that the motor has been running, the voltage at point A in the circuit diagram must be larger than the forward drop of Diode D1, the gate-to-cathode drop of the SCR, and the EMF generated by the residual MMF in the motor, to get sufficient current flow to trigger the SCR.

The waveform at point A (V_A) for one positive half-cycle is shown in 6.9(b), along with the voltage levels of the SCR gate (V_{SCR}), the diode drop (V_D), and the motor-generated EMF (V_M). The phase angle (α) at which the SCR would trigger is shown by the vertical dotted line. Should the motor for any reason speed up so that the generated motor voltage would increase, the trigger point would move upward and to the right along the curve so that the SCR would trigger later in the half-cycle and thus provide less power to the motor, causing it to slow down again.

Similarly, if the motor speed decreased, the trigger point would move to the left and down the curve, causing the TRIAC to trigger earlier in the half-cycle providing more power to the motor, thereby speeding it up.

Resistors R1, R2, and R3, along with diode D2 and capacitor C1 form the ramp-generator section of the circuit. Capacitor C1 is changed by the voltage divider R1, R2, and R3 during the positive half-cycle. Diode D2 prevents negative current flow during the negative half-cycle, therefore C1 discharges through only R2 and R3 during that half-cycle. Adjustment of R3 controls the amount by which C1 discharges during the negative half-cycle. Because the resistance of R1 is very much larger than the ac impedance of capacitor C1, the voltage waveform on C1 approaches that of a perfect cosine wave with a dc component. As potentiometer R2 is varied, both the dc and the ac voltages are divided, giving a family of curves as shown in 6.9(c).
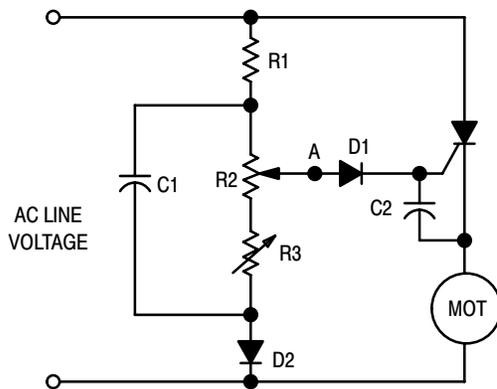
Figure 6.9. (a). Speed-Control Scheme for Universal Motors

The gain of the system, that is, the ratio of the change of effective SCR output voltage to the change in generator EMF, is considerably greater at low speed settings than it is at high speed settings. This high gain coupled with a motor with a very low residual EMF will cause a condition sometimes known as cycle skipping. In this mode of operation, the motor speed is controlled by skipping entire cycles or groups of cycles, then triggering one or two cycles early in the period to compensate for the loss in speed. Loading the motor would eliminate this condition; however, the undesirable sound and vibration of the motor necessitate that this condition be eliminated. This can be done in two ways.

The first method is used if the motor design is fixed and cannot be changed. In this case, the impedance level of the voltage divider R1, R2 and R3 can be lowered so that C1 will charge more rapidly, thus increasing the slope of the ramp and lowering the system gain. The second method, which will provide an overall benefit in improved circuit performance, involves a redesign of the motor so that the residual EMF becomes greater. In general, this means using a lower grade of magnetic steel for the laminations. As a matter of fact, some people have found that ordinary cold-rolled steel used as rotor laminations makes a motor ideally suited for this type of electronic control.

Another common problem encountered with this circuit is that of thermal runaway. With the speed control set at low or medium speed, at high ambient temperatures the speed may increase uncontrollably to its maximum value. This phenomenon is caused by an excessive impedance in the voltage-divider string for the SCR being triggered. If the voltage-divider current is too low, current will flow into the gate of the SCR without turning it on, causing the waveform at point A to be as shown in 6.9(d). The flat portion of the waveform in the early part of the half-cycle is caused by the SCR gate current loading the voltage divider before the SCR is triggered. After the SCR is triggered, diode D1 is back-biased and a load is no longer on the voltage divider so that it jumps up to its unloaded voltage. As the ambient temperature increases, the SCR becomes more sensitive, thereby requiring less gate current to trigger, and is triggered earlier in the half-cycle.This early triggering causes increased current in the SCR, thereby heating the junction still further and increasing still further the sensitivity of the SCR until maximum speed has been reached.

The solutions to this problem are the use of the most sensitive SCR practical and a voltage divider network of sufficiently low impedance. As a rough rule of thumb, the average current through the voltage divider during the positive half-cycle should be approximately three times the current necessary to trigger the lowest-sensitivity (highest gate current) SCR being used.
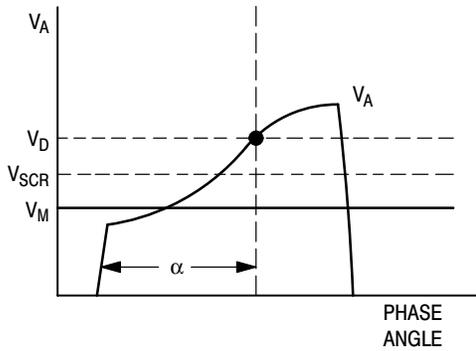
(b). Waveform for One Positive Half-Cycle of Circuit
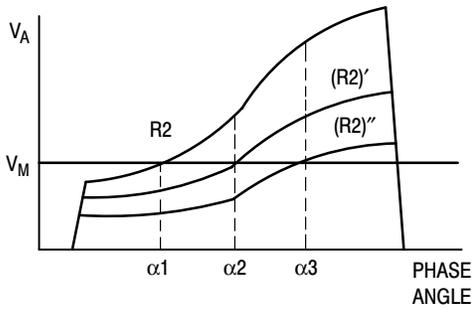
(c). Voltage Waveform at Point "A" for Three Settings of Potentiometer R2
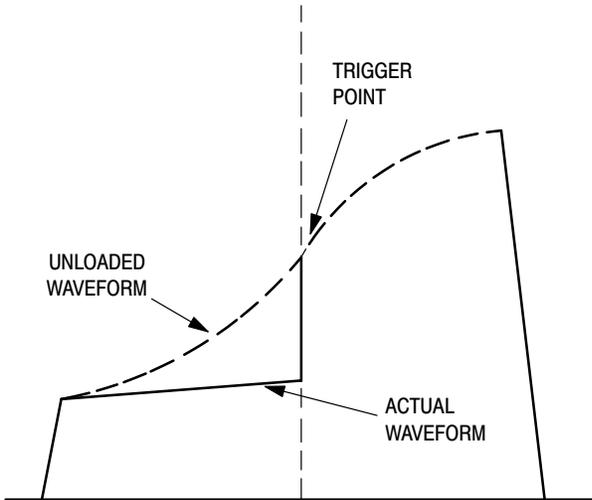
(d). Point "A" Voltage with Excessive Resistance R1

In addition to the type of steel used in the motor laminations, consideration should also be given to the design of motors used in this half-wave speed control. Since the maximum rms voltage available to the motor under half-wave conditions is 85 V, the motor should be designed for use at that voltage to obtain maximum speed. However, U.L. requirements state that semiconductor devices used in appliance control systems must be able to

be short-circuited without causing danger. Many designers have found it advantageous, therefore, to use 115 V motors with this system and provide a switch to apply full-wave voltage to the motor for high-speed operation. Figure 6.10 shows the proper connection for this switch. If one were to simply short-circuit the SCR for full-speed operation, a problem could arise. If the motor were operating at full speed with the switch closed, and the switch were then opened during the negative half-cycle, the current flowing in the inductive field of the motor could then break down the SCR in the negative direction and destroy the control. With the circuit as shown, the energy stored in the field of the motor is dissipated in the arc of the switch before the SCR is connected into the circuit.
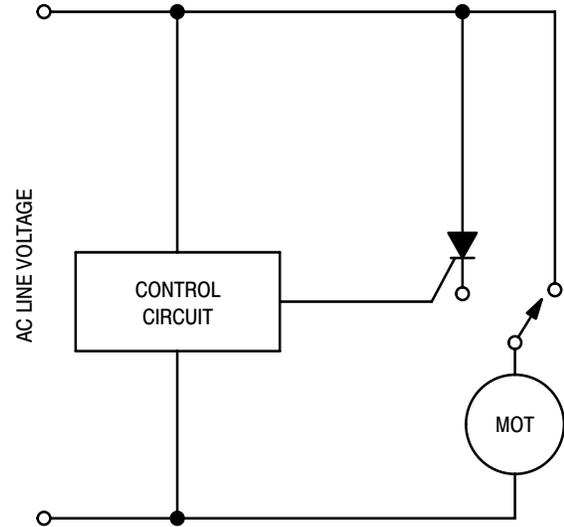
Figure 6.10. Switching Scheme for Full-Wave Operation

CONTROL OF PERMANENT-MAGNET MOTORS

As a result of recent developments in ceramic permanent-magnet materials that can be easily molded into complex shapes at low cost, the permanent-magnet motor has become increasingly attractive as an appliance component. Electronic control of this type of motor can be easily achieved using techniques similar to those just described for the universal motor. Figure 6.11 is a circuit diagram of a control system that we have developed and tested successfully to control permanent-magnet motors presently being used in blenders. Potentiometer R3 and diode D1 form a dc charging path for capacitor C1; variable resistor R1 and resistor R2 form an ac charging path which creates the ramp voltage on the capacitor. Resistor R4 and diode D2 serve to isolate the motor control circuit from the ramp generator during the positive and negative half-cycles, respectively.
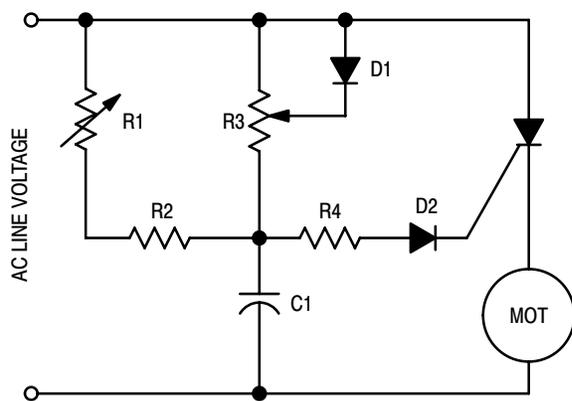
Figure 6.11. Circuit Diagram for Controlling Permanent-Magnet Motors

A small amount of cycle skipping can be experienced at low speeds using this control, but not enough to necessitate further development work. Since the voltage generated during off time is very high, the thermal runaway problem does not appear at all. Typical speed-torque curves for motors of this type are shown in Figure 6.12.
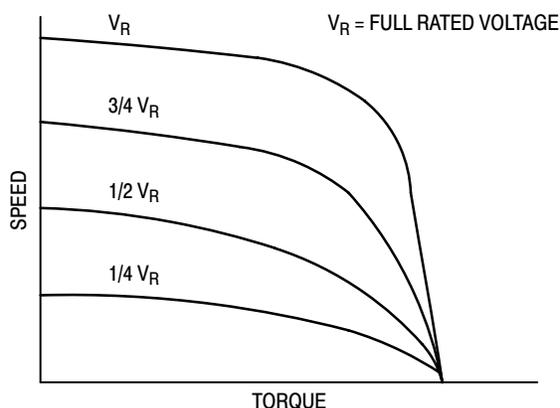
Figure 6.12. Speed-Torque Characteristic of Permanent-Magnet Motors at Various Applied Voltages

MOTOR SPEED CONTROL WITH FEEDBACK

While many motor speed control circuits have used SCRs, the TRIAC has not been very popular in this application. At first glance, it would appear that the TRIAC would be perfect for speed control because of its bilateral characteristics. There are a couple of reasons why this is not true. The major difficulty is the TRIAC's dv/dt characteristic. Another reason is the difficulty of obtaining a feedback signal because of the TRIAC's bilatera nature.

While the TRIAC has its disadvantages, it does offer some advantages. In a SCR speed control either two SCRs must be used, or the line voltage must be full-wave rectified using relatively high current rectifiers, or the control must be limited to half-wave. The TRIAC eliminates all these difficulties. By using a TRIAC the part count, package size, and cost can be reduced. Figure 6.13 shows a TRIAC motor speed control circuit that derives its feedback from the load current and does not require separate connections to the motor field and armature windings. Therefore, this circuit can be conveniently built into an appliance or used as a separate control.

The circuit operates as follows: When the TRIAC conducts, the normal line voltage, less the drop across the TRIAC and resistor R5, is applied to the motor. By delaying the firing of the TRIAC until a later portion of the cycle, the rms voltage applied to the motor is reduced and its speed is reduced proportionally. The use of feedback maintains torque at reduced speeds.

Diodes D1 through D4 form a bridge which applies full-wave rectified voltage to the phase-control circuit. Phase control of the TRIAC is obtained by the charging of capacitor C1 through resistors R2 and R3 from the voltage level established by zener diode D5. When C1 charges to the firing voltage of PUT Q1, the TRIAC triggers by transformer T1. C1 discharges through the emitter of Q1. While the TRIAC is conducting, the voltage drop between points A and B falls below the breakdown voltage of D5. Therefore, during the conduction period, the voltage on C1 is determined by the voltage drop from A to B and by resistors R1, R2, and R3. Since the voltage between A and B is a function of motor current due to resistor R5, C1 is charged during the conduction period to a value which is proportional to the motor current. The value of R5 is chosen so that C1 cannot charge to a high enough voltage to fire Q1 during the conduction period. However, the amount of charging required to fire Q1 has been decreased by an amount proportional to the motor current. Therefore, the firing angle at which Q1 will fire has been advanced in proportion to the motor current. As the motor is loaded and draws more current, the firing angle of Q1 is advanced even more, causing a proportionate increase in the rms voltage applied to the motor, and a consequent increase in its available torque.

Since the firing voltage of Q1 depends on the voltage from base one to base two, it is necessary to support the base two voltage during the conduction portion of the cycle to prevent the feedback voltage from firing Q1. D6 and C2 perform this function.

Because the motor is an inductive load, it is necessary to limit the commutation dv/dt for reliable circuit operation. R6 and C3 perform this function.
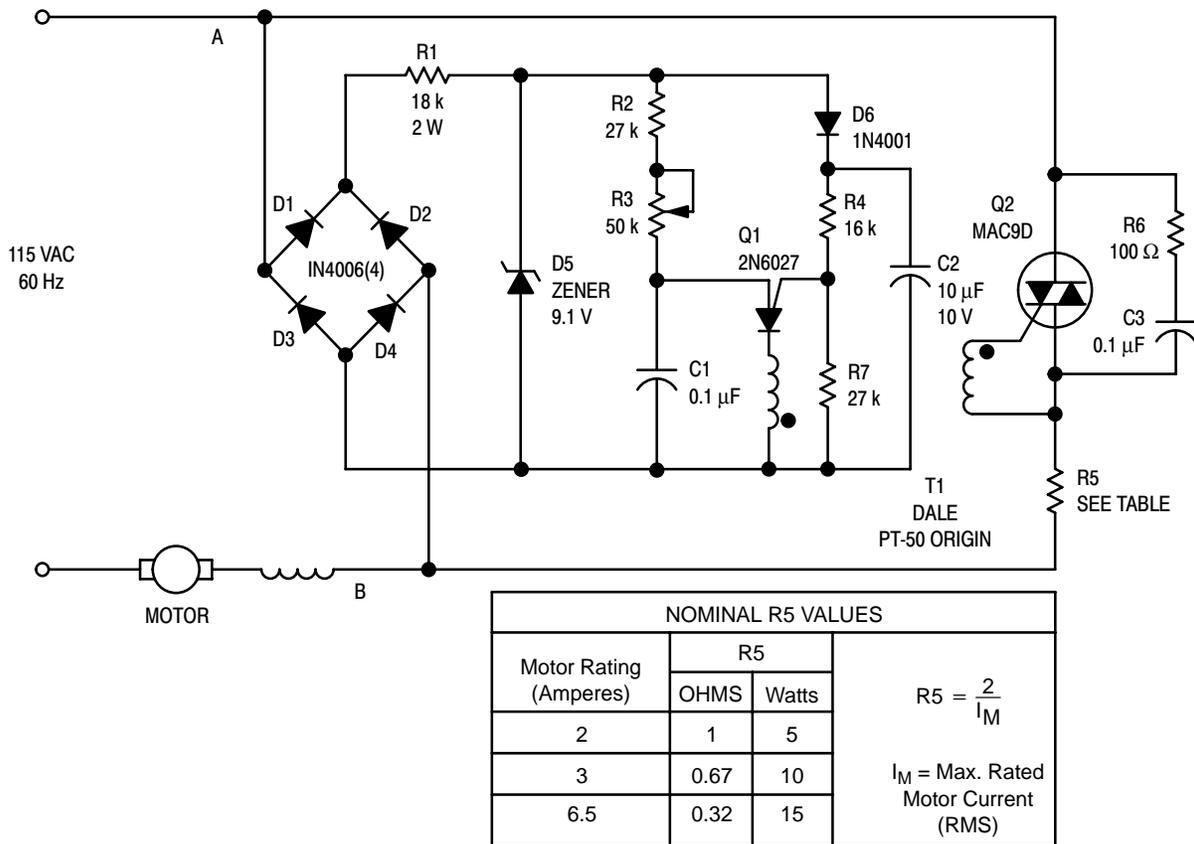
Figure 6.13. Motor Speed Control with Feedback

NOMINAL R5 VALUES			
Motor Rating (Amperes)	R5		$R5 = \dfrac{2}{I_M}$
	OHMS	Watts	
2	1	5	
3	0.67	10	I_M = Max. Rated Motor Current (RMS)
6.5	0.32	15	

Nominal values for R5 can be obtained from the table or they can be calculated from the equation given. Exact values for R5 depend somewhat on the motor characteristics. Therefore, it is suggested that R5 be an adjustable wirewound resistor which can be calibrated in terms of motor current, and the speed control can be adapted to many different motors. If the value of R5 is too high, feedback will be excessive and surging or loss of control will result. If the value is too low, a loss of torque will result. The maximum motor current flows through R5, and its wattage must be determined accordingly.

This circuit has been operated successfully with 2 and 3 ampere 1/4-inch drills and has satisfactorily controlled motor speeds down to 1/3 or less of maximum speed with good torque characteristics. to the motor, and a consequent increase in its available torque.

AN INTEGRATED CIRCUIT FEEDBACK CONTROL

The TDA1185A TRIAC phase angle controller (Figure 6.14) generates controlled triac triggering pulses and applies positive current feedback to stabilize the speed of universal motors. A ramp voltage synchronized to the ac line half cycle and compared to an external set voltage determines the firing angle. Negative gate pulses drive the triac in quadrants two and three.

Because the speed of a universal motor decreases as torque increases, the TDA1185A lengthens the triac conduction angle in proportion to the motor current, sensed through resistor R9.

The TDA1185A is the best solution for low cost applications tolerating 5% motor speed variation. Open loop systems do not have a tachometer or negative feedback and consequently cannot provide perfect speed compensation.

CONSTANT SPEED MOTOR CONTROL USING TACHOMETER FEEDBACK

Tachometer feedback sensing rotor speed provides excellent performance with electric motors. The principal advantages to be gained from tachometer feedback are the ability to apply feedback control to shaded-pole motors, and better brush life in universal motors used in feedback circuits. This latter advantage results from the use of full-wave rather than half-wave control, reducing the peak currents for similar power levels.

Figure 6.14. TDA 1185-A Universal Motor Speed Control — Internal Block Diagram/Pin Assignment

THE TACHOMETER

The heart of this system is, of course, the speed-sensing tachometer itself. Economy being one of the principal goals of the design, it was decided to use a simple magnetic tachometer incorporating the existing motor fan as an integral part of the magnetic circuit. The generator consists of a coil wound on a permanent magnet which is placed so that the moving fan blades provide a magnetic path of varying reluctance as they move past the poles of the magnet. Several possible configurations of the magnetic system are shown in Figure 6.15.

Flux in a magnetic circuit can be found from the "magnetic Ohm's law":

$$\phi = \frac{MMF}{R},$$

where ϕ = the flux,

MMF = the magnetomotive force (strength of the magnet), and

R = the reluctance of the magnetic path.

Assuming the MMF of the permanent magnet to be constant, it is readily apparent that variations in reluctance will directly affect the flux. The steel fan blades provide a low-reluctance path for the flux once it crosses the air gap between them and the poles of the magnet. If the magnet used has a horseshoe or U shape, and is placed so that adjacent fan blades are directly opposite each pole in one position of the motor armature, the magnetic path will be of

relatively low reluctance; then as the motor turns the reluctance will increase until one fan blade is precisely centered between the poles of the magnet. As rotation continues, the reluctance will then alternately increase and decrease as the fan blades pass the poles of the magnet. If a bar- or L-shaped magnet is used so that one pole is close to the shaft or the frame of the motor and the other is near the fan blades, the magnetic path reluctance will vary as each blade passes the magnet pole near the fan. In either case the varying reluctance causes variations in the circuit flux and a voltage is generated in the coil wound around the magnet. The voltage is given by the equation:

$$e = -N \frac{d\phi}{dt} \times 10^{-8},$$

where   e = the coil voltage in volts,

N = the number of turns in the coil, and

$\frac{d\phi}{dt}$ = the rate of change of flux in lines per second.

In a practical case, a typical small horseshoe magnet wound with 1000 turns of wire generated a voltage of about 0.5 volts/1000 rpm when mounted in a blender.

Since both generated voltage and frequency are directly proportional to the motor speed, either parameter can be used as the feedback signal. However, circuits using voltage sensing are less complex and therefore less expensive. Only that system will be discussed here.

Figure 6.15. (a). Locations for Magnetic Sensing Tachometer Generator Using a Horseshoe Magnet

(b). Locations for Magnetic Sensing Tachometer Generator Using an "L" or Bar Magnet

THE ELECTRONICS

In one basic circuit, which is shown in Figure 6.16, the generator output is rectified by rectifier D1, then filtered and applied between the positive supply voltage and the base of the detector transistor Q1. This provides a negative voltage which reduces the base-voltage on Q1 when the speed increases.

The emitter of the detector transistor is connected to a voltage divider which is adjusted to the desired tachometer output voltage. In normal operation, if the tachometer voltage is less than desired, the detector transistor, Q1, is turned on by current through R1 into its base. Q1 then turns on Q2 which causes the timing capacitor for programmable unijunction transistor Q3 to charge quickly.

As the tachometer output approaches the voltage desired, the base-emitter voltage of Q1 is reduced to the point at which Q1 is almost cut off. Thereby, the collector current of Q2, which charges the PUT timing capacitor, reduces, causing it to charge slowly and trigger the thyristor later in the half cycle. In this manner, the average power to the motor is reduced until just enough power to maintain the desired motor speed is allowed to flow.

Input circuit variations are used when the tachometer output voltage is too low to give a usable signal with a silicon rectifier. In the variation shown in Figure 6.16(b), the tachometer is connected between a voltage divider and the base of the amplifier transistor. The voltage divider is set so that with no tachometer output the transistor is just barely in conduction. As the tachometer output increases, Q_T is cut off on negative half cycles and conducts on positive half cycles. Resistors R9 and R10 provide a fixed gain for this amplifier stage, providing the h_{FE} of Q_T is much greater than the ratio of R9 to R10. Thus the output of the amplifier is a fixed multiple of the positive values of the tachometer waveform. The rectifier diode D1 prevents C1 from discharging through R9 on negative half cycles of the tachometer. The remainder of the filter and control circuitry is the same as the basic circuit.

In the second variation, shown in 6.16(c), R8 has been replaced by a semiconductor diode, D2. Since the voltage and temperature characteristics more closely match those of the transistor base-to-emitter junction, this circuit is easier to design and needs no initial adjustments as does the circuit in 6.16(b). The remainder of this circuit is identical to that of Figure 6.15.

In the second basic circuit, which is shown in Figure 6.17, the rectified and filtered tachometer voltage is added to the output voltage of the voltage divider formed by R1 and R2. If the sum of the two voltages is less than $V1 - V_{BE \ Q1}$ (where $V_{BE \ Q1}$ is the base-emitter voltage of Q1), Q1 will conduct a current proportional to $V1 - V_{BE \ Q1}$, charging capacitor C. If the sum of the two voltages is greater than $V1 - V_{BE \ Q1}$, Q1 will be cut off and no current will flow into the capacitor. The operation of the remainder of the circuit is the same as the previously described circuits.
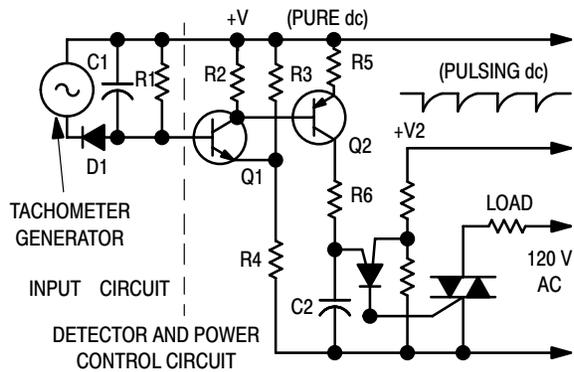
Figure 6.16. (a). Basic Tachometer Control Circuit
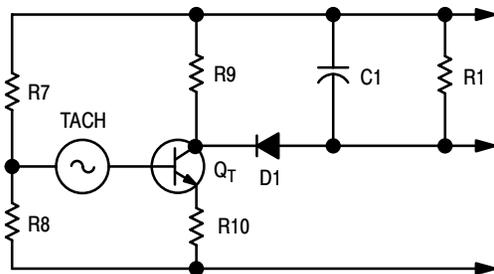
(b). Variation Used when the Tachometer Output is Too Low for Adequate Control
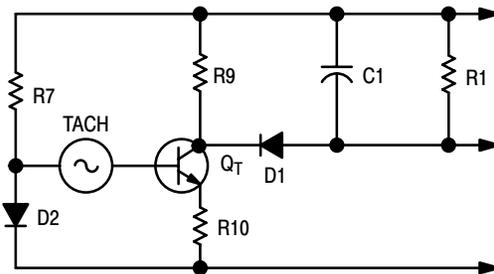
(c). Variation Providing Better Temperature Tracking and Easier Initial Adjustment

PHASE CONTROL WITH TRIGGER DEVICES

Phase control using thyristors is one of the most common means of controlling the flow of power to electric motors, lamps, and heaters. With an ac voltage applied to the circuit, the gated thyristor (SCR, TRIAC, etc.) remains in its off-state for the first portion of each half cycle of the power line, then, at a time (phase angle) determined by the

control circuit, the thyristor switches on for the remainder of the half cycle. By controlling the phase angle at which the thyristor is switched on, the relative power in the load may be controlled.

PHASE CONTROL WITH PROGRAMMABLE UNIJUNCTION TRANSISTORS

PUTs provide a simple, convenient means for obtaining the thyristor trigger pulse synchronized to the ac line at a controlled phase angle.
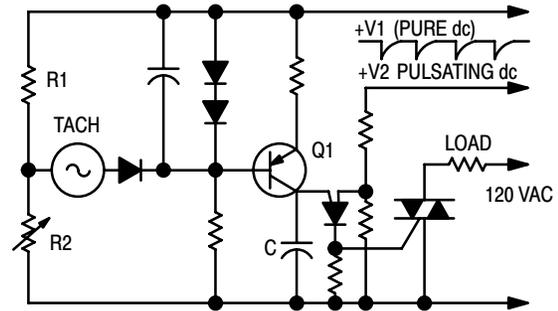
Figure 6.17. Another Basic Tachometer Circuit

These circuits are all based on the simple relaxation oscillator circuit of Figure 6.18. R_T and C_T in the figure form the timing network which determines the time between the application of voltage to the circuit (represented by the closing of S1) and the initiation of the pulse. In the case of the circuit shown, with V_s pure dc, the oscillator is free running, R_T and C_T determine the frequency of oscillation. The peak of the output pulse voltage is clipped by the forward conduction voltage of the gate to cathode diode in the thyristor. The principal waveforms associated with the circuit are shown in Figure 6.18(b).

Operation of the circuit may best be described by referring to the capacitor voltage waveform. Following power application, C_T charges at the rate determined by its own capacitance and the value of R_T until its voltage reaches the peak point voltage of the PUT. Then the PUT switches into conduction, discharging C_T through R_{GK} and the gate of the thyristor. With V_s pure dc, the cycle then repeats immediately; however, in many cases V_s is derived from the anode voltage of the thyristor so that the timing cycle cannot start again until the thyristor is blocking forward voltage and once again provides V_s.
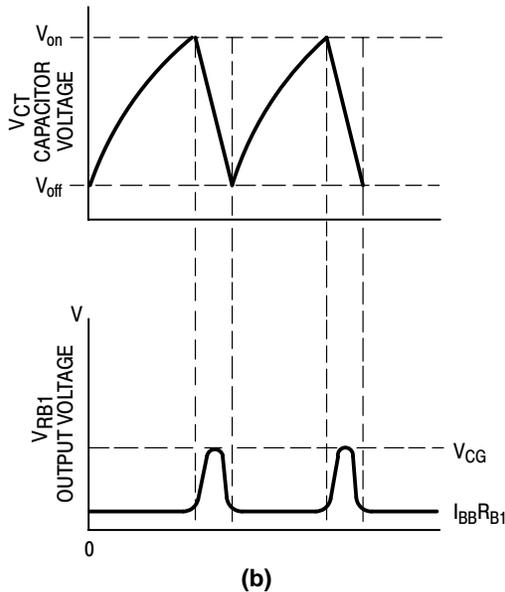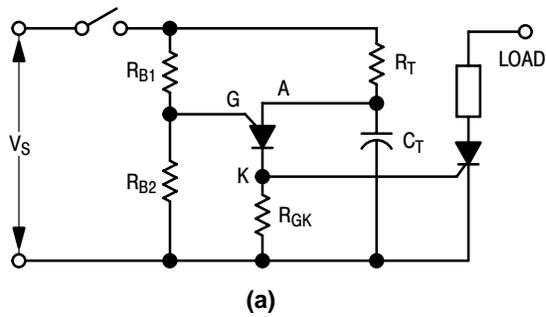
Figure 6.18. Basic Relaxation Oscillator Circuit (a) and Waveforms (b)

It is often necessary to synchronize the timing of the output pulses to the power line voltage zero-crossing points. One simple method of accomplishing synchronization is shown in Figure 6.19. Zener diode D1 clips the rectified supply voltage resulting in a V_s as shown in 6.19(b). Since V_S, and therefore the peak point voltage of the PUT drops to zero each time the line voltage crosses zero, C_T discharges at the end of every half cycle and begins each half cycle in the discharged state. Thus, even if the PUT has not triggered during one half cycle, the capacitor begins the next half cycle discharged. Consequently, the values of R_T and C_T directly control the phase angle at which the pulse occurs on each half cycle. The zener diode also provides voltage stabilization for the timing circuit giving the same pulse phase angle regardless of normal line voltage fluctuations.

APPLICATIONS

The most elementary application of the PUT trigger circuit, shown in Figure 6.20, is a half-wave control circuit.

In this circuit, R_D is selected to limit the current through D_1 so that the diode dissipation capability is not exceeded. Dividing the allowable diode dissipation by one-half the zener voltage will give the allowable positive current in the diode since it is conducting in the voltage regulating mode only during positive half cycles. Once the positive half-cycle current is found, the resistor value may be calculated by subtracting 0.7 times the zener voltage from the rms line voltage and dividing the result by the positive current:

$$R_D = \frac{Erms - 0.7\,Vz}{I_{positive}}$$

The power rating of R_D must be calculated on the basis of full wave conduction as D1 is conducting on the negative half cycle acting as a shunt rectifier as well as providing V_s on the positive half cycle.
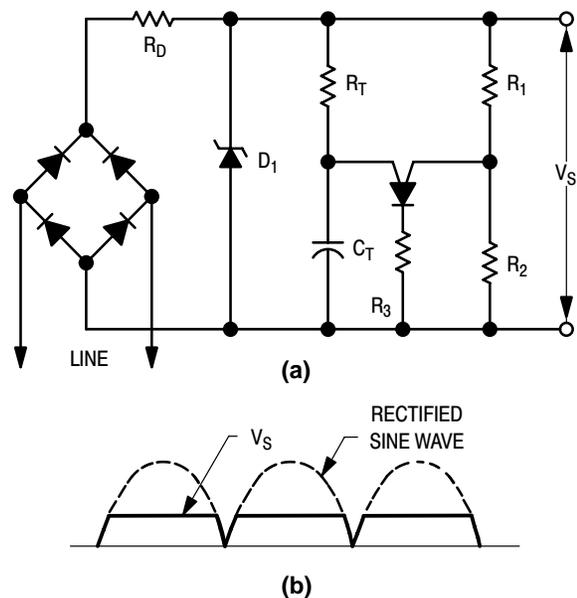
Figure 6.19. Control Circuit (a) with Zener Clipped, Rectified Voltage (b)
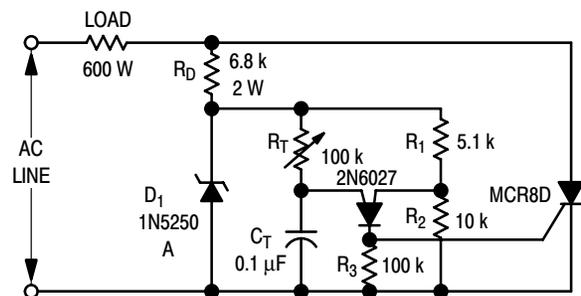
Figure 6.20. Half Wave Control Circuit with Typical Values for a 600 Watt Resistive Load

The thyristor is acting both as a power control device and a rectifier, providing variable power to the load during the positive half cycle and no power to the load during the negative half cycle. The circuit is designed to be a two terminal control which can be inserted in place of a switch. If full wave power is desired as the upper extreme of this control, a switch can be added which will short circuit the SCR when R_T is turned to its maximum power position. The switch may be placed in parallel with the SCR if the load is resistive; however, if the load is inductive, the load must be transferred from the SCR to the direct line as shown in Figure 6.21.

(a). Resistive Load

(b). Inductive Load
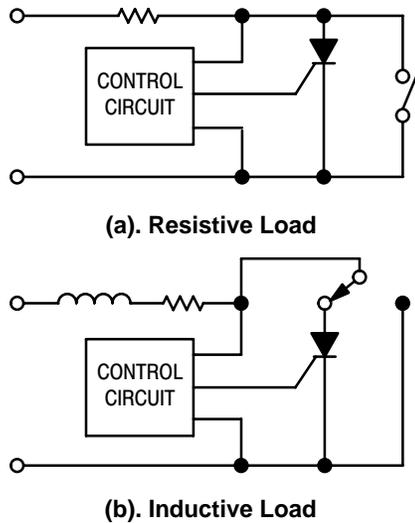
Figure 6.21. Half Wave Controls with Switching for Full Wave Operation
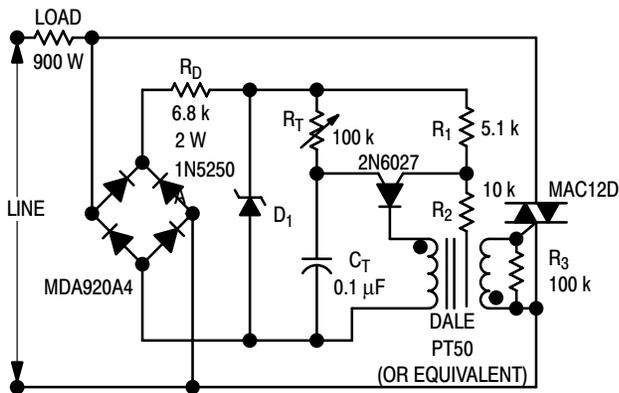
Figure 6.22. A Simple Full Wave Trigger Circuit with Typical Values for a 900 Watt Resistive Load

Full wave control may be realized by the addition of a bridge rectifier, a pulse transformer, and by changing the thyristor from an SCR to a TRIAC, shown in Figure 6.22.

Occasionally a circuit is required which will provide constant output voltage regardless of line voltage changes. Adding potentiometer P1, as shown in Figure 6.23, to the circuits of Figures 6.20 and 6.22, will provide an approximate solution to this problem. The potentiometer is adjusted to provide reasonably constant output over the desired range of line voltage. As the line voltage increases, so does the voltage on the wiper of P1 increasing V_S and thus the peak point voltage of the PUT. The increased peak point voltage results in C_T charging to a higher voltage and thus taking more time to trigger. The additional delay reduces the thyristor conduction angle and maintains the average voltage at a reasonably constant value.

FEEDBACK CIRCUITS

The circuits described so far have been manual control circuits; i.e., the power output is controlled by a potentiometer turned by hand. Simple feedback circuits may be constructed by replacing R_T with heat or light-dependent sensing resistors; however, these circuits have no means of adjusting the operating levels. The addition of a transistor to the circuits of Figures 6.20 and 6.22 allows complete control.
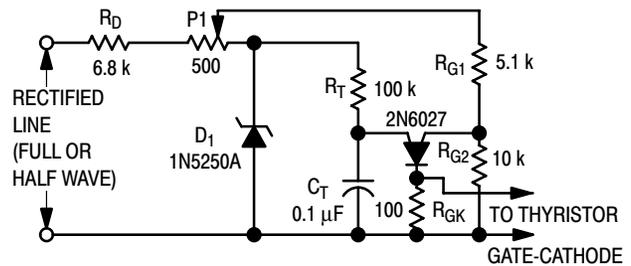
Figure 6.23. Circuit for Line Voltage Compensation
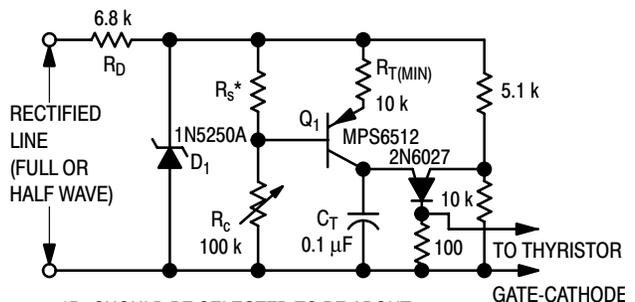
*R_s SHOULD BE SELECTED TO BE ABOUT 3 k TO 5 k OHMS AT THE DESIRED OUTPUT LEVEL

Figure 6.24. Feedback Control Circuit

Figure 6.24 shows a feedback control using a sensing resistor for feedback. The sensing resistor may respond to any one of many stimuli such as heat, light, moisture, pressure, or magnetic field. R_s is the sensing resistor and R_c is the control resistor that establishes the desired operating point. Transistor Q_1 is connected as an emitter follower such that an increase in the resistance of R_s decreases the voltage on the base of Q_1, causing more current to flow. Current through Q_1 charges C_T, triggering the PUT at a delayed phase angle. As R_s becomes larger, more charging current flows, causing the capacitor voltage to increase more rapidly. This triggers the PUT with less phase delay, boosting power to the load. When R_s decreases, less power is applied to the load. Thus, this circuit is for a sensing resistor which decreases in response to too much power in the load. If the sensing resistor increases with load power, then R_s and R_c should be interchanged.

If the quantity to be sensed can be fed back to the circuit in the form of an isolated, varying dc voltage such as the output of a tachometer, it may be inserted between the voltage divider and the base of Q1 with the proper polarity. In this case, the voltage divider would be a potentiometer to adjust the operating point. Such a circuit is shown in Figure 6.25.
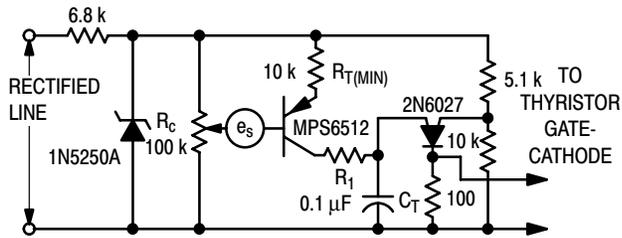
Figure 6.25. Voltage Feedback Circuit

In some cases, average load voltage is the desired feedback variable. In a half wave circuit this type of feedback usually requires the addition of a pulse transformer, shown in Figure 6.26. The RC network, R_1, R_2, C_1, averages load voltage so that it may be compared with the set point on R_s by Q_1. Full wave operation of this type of circuit requires dc in the load as well as the control circuit. Figure 6.27 is one method of obtaining this full wave control.

Each SCR conducts on alternate half-cycles and supplies pulsating dc to the load. The resistors (Rg) insure sharing of the gate current between the simultaneously driven SCRs. Each SCR is gated while blocking the line voltage every other half cycle. This momentarily increases reverse blocking leakage and power dissipation. However, the leakage power loss is negligible due to the low line voltage and duty cycle of the gate pulse.

There are, of course, many more sophisticated circuits which can be derived from the basic circuits discussed here. If, for example, very close temperature control is desired, the circuit of Figure 6.24 might not have sufficient

gain. To solve this problem a dc amplifier could be inserted between the voltage divider and the control transistor gate to provide as close a control as desired. Other modifications to add multiple inputs, switched gains, ramp and pedestal control, etc., are all simple additions to add sophistication.
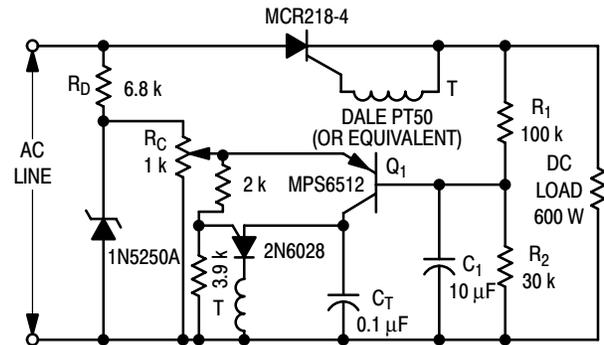
Figure 6.26. Half Wave, Average Voltage Feedback
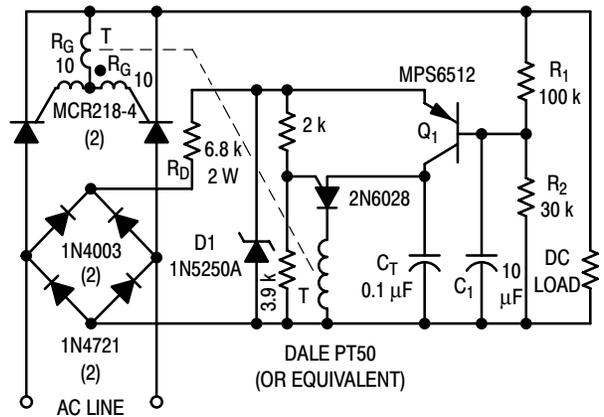
Figure 6.27. Full Wave, Average Voltage Feedback Control

CLOSED LOOP UNIVERSAL MOTOR SPEED CONTROL

Figure 6.28 illustrates a typical tachometer stabilized closed feedback loop control using the TDA1285A integrated circuit. This circuit operates off the ac line and generates a phase angle varied trigger pulse to control the triac. It uses inductive or hall effect speed sensors, controls motor starting acceleration and current, and provides a 1 to 2% speed variation for temperature and load variations.

CYCLE CONTROL WITH OPTICALLY ISOLATED TRIAC DRIVERS

In addition to the phase control circuits, TRIAC drivers can also be used for ac power control by on-off or burst control, of a number of ac cycles. This form of power control allows logic circuits and microprocessors to easily control ac power with TRIAC drivers of both the zero-crossing and non zero-crossing varieties.
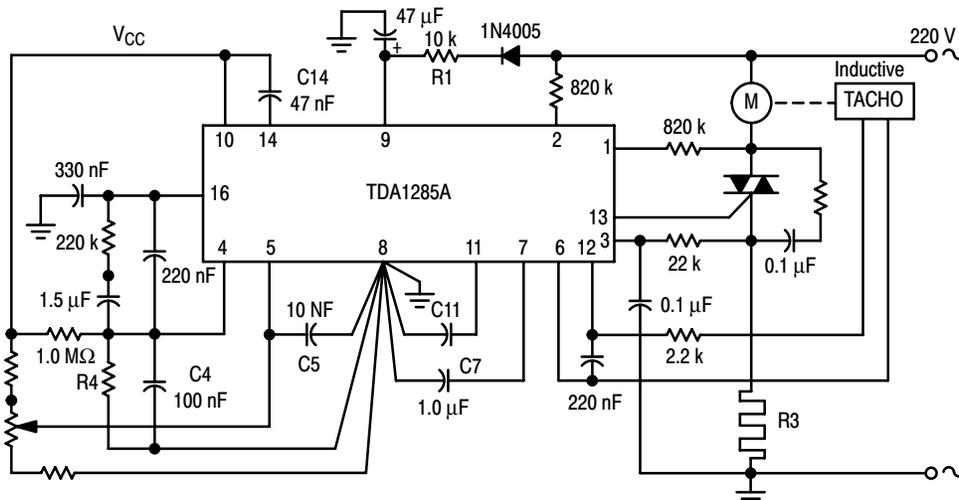
Figure 6.28. (a). Motor Control Circuit

NOTES:

Frequency to Voltage converter
—Max. motor speed 30,000 rpm

—Tachogenerator 4 pairs of poles: max. frequency = $\dfrac{30,000}{60}$ x 4 = 2 kHz

—C11 = 680 pF. R4 adjusted to obtain $V_{Pin\,4}$ = 12 V at max. speed: 68 kΩ
—Power Supply
with V_{mains} = 120 Vac, R_1 = 4.7 kΩ. Perfect operation
will occur down to 80 Vac.
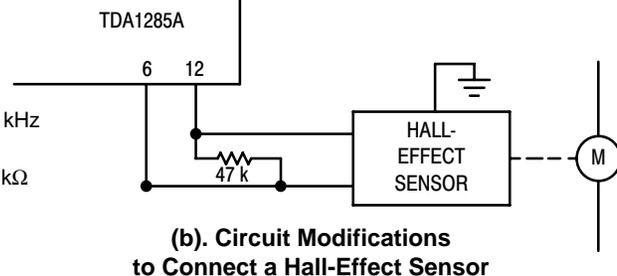
**(b). Circuit Modifications
to Connect a Hall-Effect Sensor**

USING NON-ZERO CROSSING OPTICALLY ISOLATED TRIAC DRIVERS

USING THE MOC3011 ON 240 VAC LINES

The rated voltage of a MOC3011 is not sufficiently high for it to be used directly on 240 V line; however, the designer may stack two of them in series. When used this way, two resistors are required to equalize the voltage dropped across them as shown in Figure 6.29.

REMOTE CONTROL OF AC VOLTAGE

Local building codes frequently require all 115 V light switch wiring to be enclosed in conduit. By using a MOC3011, a TRIAC, and a low voltage source, it is possible to control a large lighting load from a long distance through low voltage signal wiring which is completely isolated from the ac line. Such wiring usually is not required to be put in conduit, so the cost savings in installing a lighting system in commercial or residential buildings can be considerable. An example is shown in Figure 6.29. Naturally, the load could also be a motor, fan, pool pump, etc.
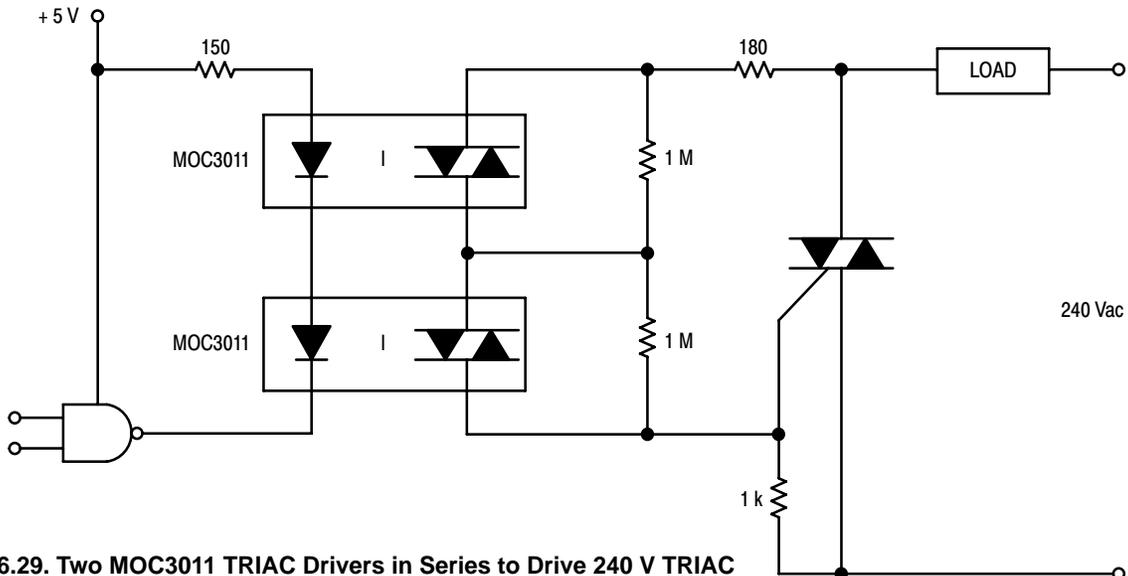
Figure 6.29. Two MOC3011 TRIAC Drivers in Series to Drive 240 V TRIAC
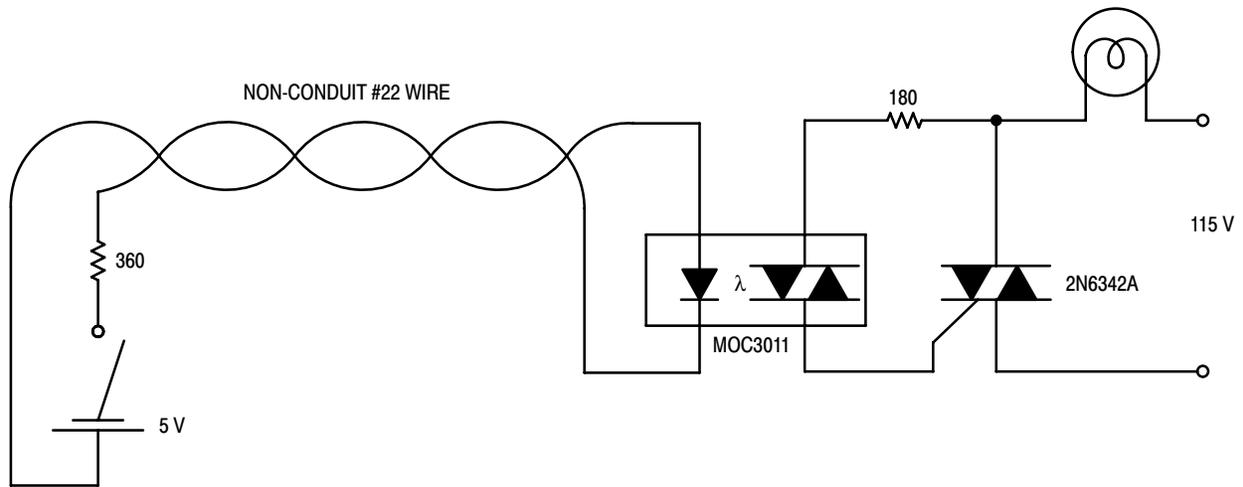
Figure 6.30. Remote Control of AC Loads Through Low Voltage Non-Conduit Cable

SOLID STATE RELAY

Figure 6.30 shows a complete general purpose, solid state relay snubbed for inductive loads with input protection. When the designer has more control of the input and output conditions, he can eliminate those components which are not needed for his particular application to make the circuit more cost effective.

INTERFACING MICROPROCESSORS TO 115 VAC PERIPHERALS

The output of a typical microcomputer input-output (I/O) port is a TTL-compatible terminal capable of driving one or two TTL loads. This is not quite enough to drive the MOC3011, nor can it be connected directly to an SCR or TRIAC, because computer common is not normally referenced to one side of the ac supply. Standard 7400 series gates can provide an input compatible with the output of an MC6821, MC6846 or similar peripheral interface adaptor and can directly drive the MOC3011. If

the second input of a 2 input gate is tied to a simple timing circuit, it will also provide energization of the TRIAC only at the zero crossing of the ac line voltage as shown in Figure 6.32. This technique extends the life of incandescent lamps, reduces the surge current strains on the TRIAC, and reduces EMI generated by load switching. Of course, zero crossing can be generated within the microcomputer itself, but this requires considerable software overhead and usually just as much hardware to generate the zero-crossing timing signals.

APPLICATIONS USING THE ZERO CROSSING TRIAC DRIVER

For applications where EMI induced, non-zero crossing-load switching is a problem, the zero crossing TRIAC driver is the answer. This TRIAC driver can greatly simplify the suppression of EMI for only a nominal increased cost. Examples of several applications using the MOC3031, 41 follows.
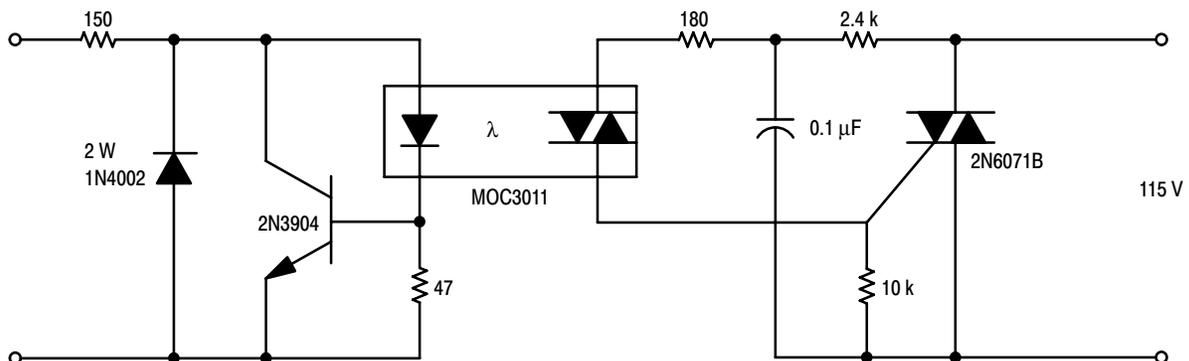
Figure 6.31. Solid-State Relay
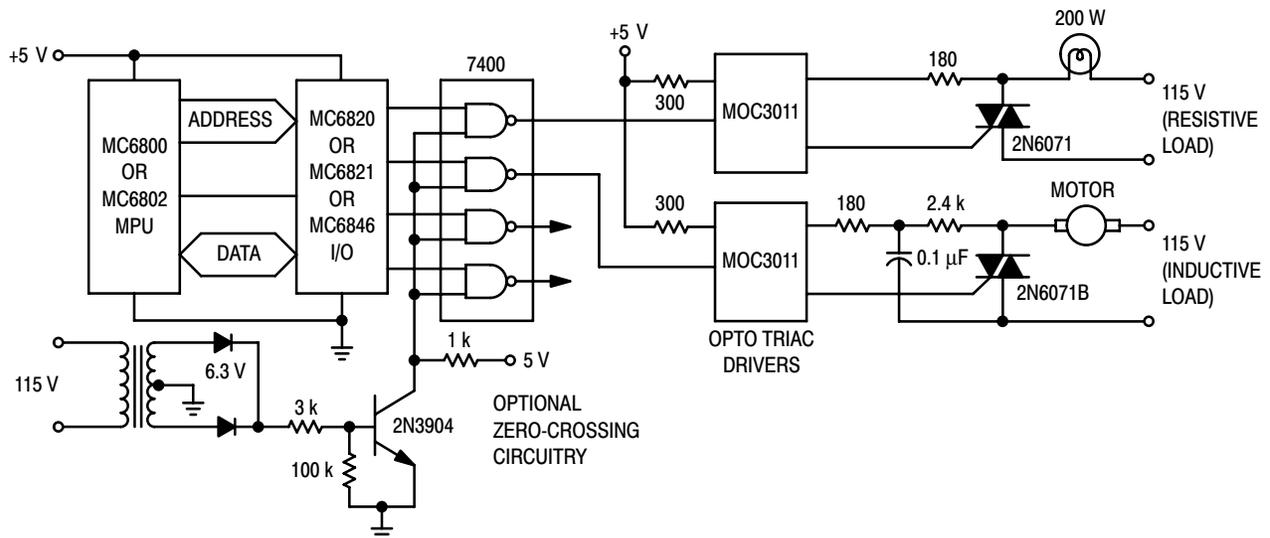
Figure 6.32. Interfacing an M6800 Microcomputer System to 115 Vac Loads

MATRIX SWITCHING

Matrix, or point-to-point switching, represents a method of controlling many loads using a minimum number of components. On the 115 V line, the MOC3031 is ideal for this application; refer to Figure 6.33. The large static dv/dt rating of the MOC3031 prevents unwanted loads from being triggered on. This might occur, in the case of non-zero crossing TRIAC drivers, when a TRIAC driver on a vertical line was subjected to a large voltage ramp due to a TRIAC on a horizontal line being switched on. Since non-zero crossing TRIAC drivers have lower static dv/dt ratings, this ramp would be sufficiently large to trigger the device on.

R is determined as before:

$$R_{(min)} = \frac{V_{in(pk)}}{I_{TSM}}$$

$$= \frac{170 \text{ V}}{1.2 \text{ A}} = 150 \text{ ohms}$$
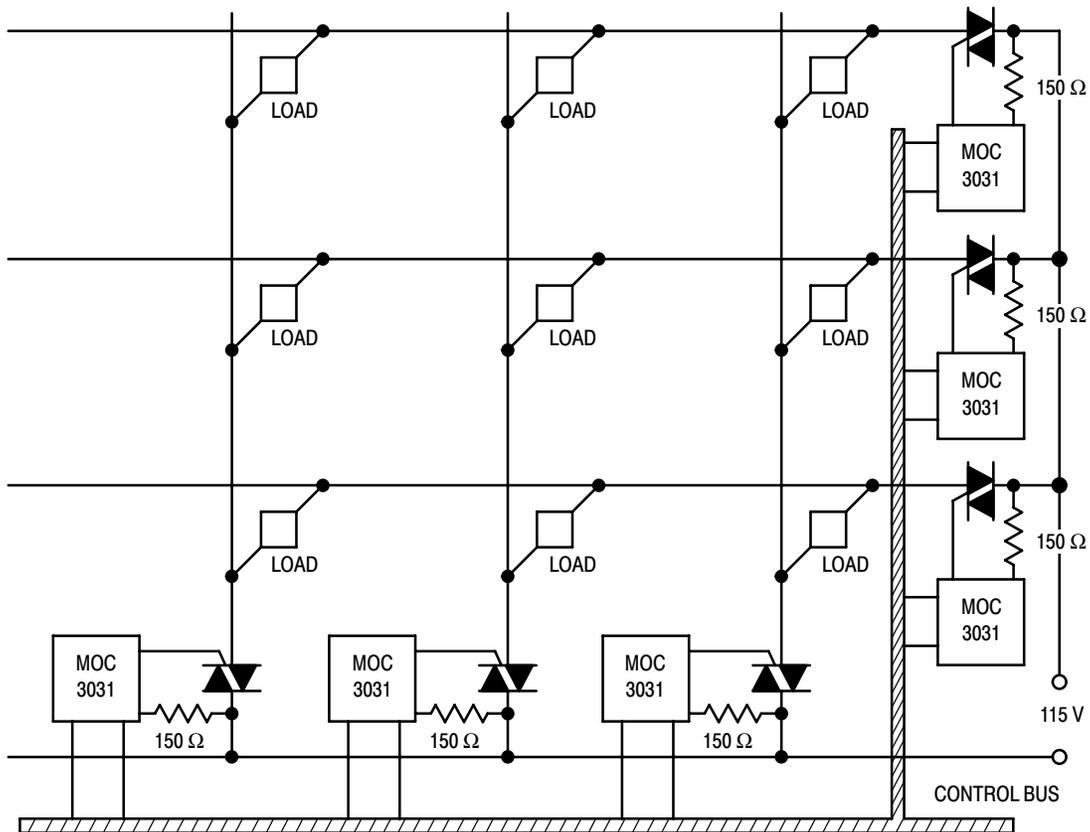
Figure 6.33. Matrix Switching
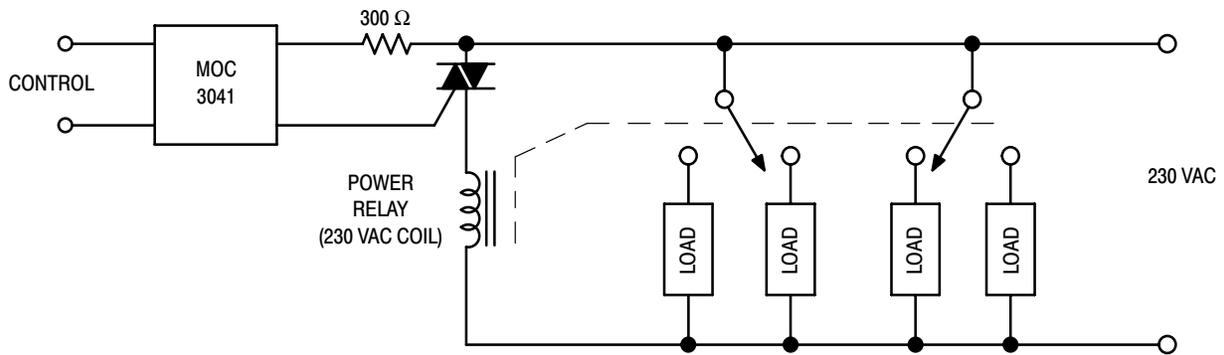
Figure 6.34. Power Relay Control

POWER RELAYS

The use of high-power relays to control the application of ac power to various loads is a very widespread practice. Their low contact resistance causes very little power loss and many options in power control are possible due to their multipole-multithrow capability. The MOC3041 is well suited to the use of power relays on the 230 Vac line; refer to Figure 6.34. The large static dv/dt of this device makes a snubber network unnecessary, thus reducing component count and the amount of printed circuit board space required. A non-zero crossing TRAIC driver (MOC3021) could be used in this application, but its lower static dv/dt rating would necessitate a snubber network.

MICROCOMPUTER INTERFACE

The output of most microcomputer input/output (I/O) ports is a TTL signal capable of driving several TTL gates. This is insufficient to drive a zero-crossing TRIAC driver. In addition, it cannot be used to drive an SCR or TRIAC directly, because computer common is not usually referenced to one side of the ac supply. However, standard 7400 NAND gates can be used as buffers to accept the output of the I/O port and in turn, drive the MOC3031 and/or MOC3041; refer to Figure 6.35.

The zero-crossing feature of these devices extends the life of incandescent lamps, reduces inrush currents and minimizes EMI generated by load switching.

AC MOTORS

The large static dv/dt rating of the zero-crossing TRIAC drivers make them ideal when controlling ac motors. Figure 6.36 shows a circuit for reversing a two phase motor using the MOC3041. The higher voltage MOC3041 is required, even on the 115 Vac line, due to the mutual and self-inductance of each of the motor windings, which may cause a voltage much higher than 115 Vac to appear across the winding which is not conducting current.

DETERMINING LIMITING RESISTOR R FOR A HIGH-WATTAGE INCANDESCENT LAMP

Many high-wattage incandescent lamps suffer shortened lifetimes when switched on at ac line voltages other than zero. This is due to a large inrush current destroying the filament. A simple solution to this problem is the use of the MOC3041 as shown in Figure 6.37. The MOC3041 may be controlled from a switch or some form of digital logic.
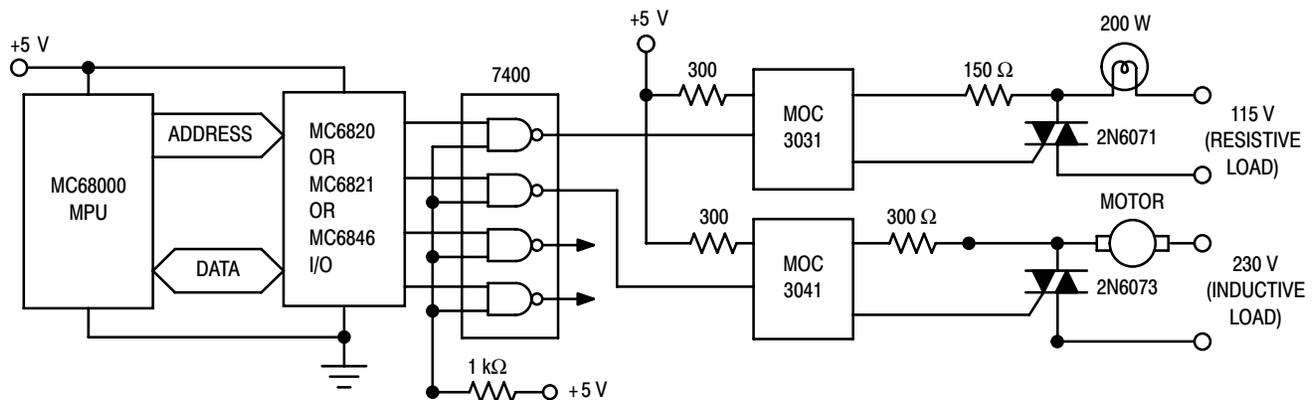
Figure 6.35. M68000 Microcomputer Interface
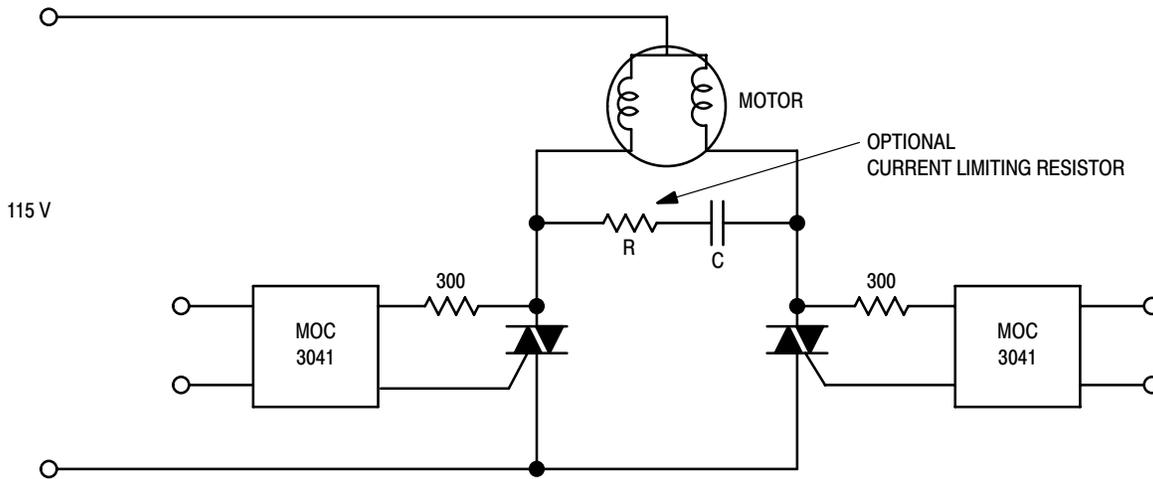
Figure 6.36. Reversing Motor Circuit

The minimum value of R is determined by the maximum surge current rating of the MOC3041 (I_{TSM}):

$$R_{(min)} = \frac{V_{in(pk)}}{I_{TSM}}$$

$$= \frac{V_{in(pk)}}{1.2\ A}$$

(10)

On a 230 Vac Line:

$$R_{(min)} = \frac{340\ V}{1.2\ A} = 283\ ohms$$

(11)

In reality, this would be a 300 ohm resistor.

AC POWER CONTROL WITH SOLID-STATE RELAYS

The Solid-State Relay (SSR) as described below, is a relay function with:

a. Four Terminals (Two Input, Two Output)
b. DC or AC Input
c. Optical Isolation Between Input and Output
d. Thyristor (SCR or TRIAC) Output

e. Zero Voltage Switching Output
   (Will Only Turn On Close to Zero Volts)
f. AC Output (50 or 60 Hz)

Figure 6.38 shows the general format and waveforms of the SSR. The input on/off signal is conditioned (perhaps only by a resistor) and fed to the Light-Emitting-Diode (LED) of an optoelectronic-coupler. This is ANDed with a go signal that is generated close to the zero-crossing of the line, typically ≤ 10 Volts. Thus, the output is not gated on via the amplifier except at the zero-crossing of the line voltage. The SSR output is then re-gated on at the beginning of every half-cycle until the input on signal is removed. When this happens, the thyristor output stays on until the load current reaches zero, and then turns off.

ADVANTAGES AND DISADVANTAGES OF SSRs

The SSR has several advantages that make it an attractive choice over its progenitor, the Electromechanical Relay (EMR) although the SSR generally costs more than its electromechanical counterpart. These advantages are:
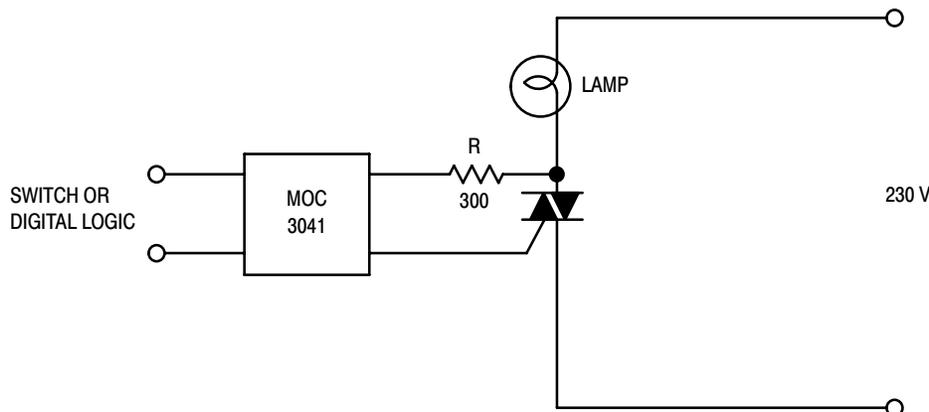
Figure 6.37. High-Wattage Lamp Control
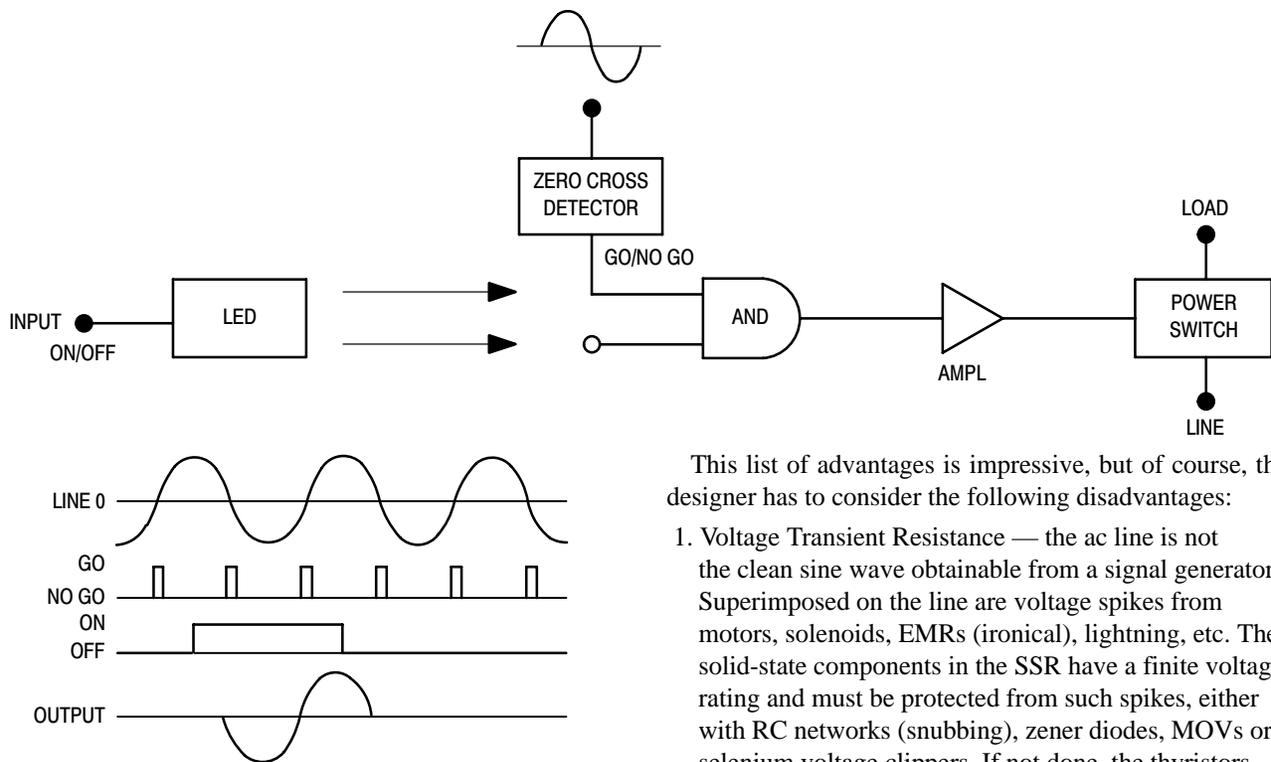
Figure 6.38. SSR Block Diagram

1. No Moving Parts — the SSR is all solid-state. There are no bearing surfaces to wear, springs to fatigue, assemblies to pick up dust and rust. This leads to several other advantages.
2. No Contact Bounce — this in turn means no contact wear, arcing, or Electromagnetic Interference (EMI) associated with contact bounce.
3. Fast Operation — usually less than 10 μs. Fast turn-on time allows the SSR to be easily synchronized with line zero-crossing. This also minimizes EMI and can greatly increase the lifetime of tungsten lamps, of considerable value in applications such as traffic signals.
4. Shock and Vibration Resistance — the solid-state contact cannot be "shaken open" as easily as the EMR contact.
5. Absence of Audible Noise — this devolves from the lack of moving mechanical parts.
6. Output Contact Latching — the thyristor is a latching device, and turns off only at the load current zero-crossing, minimizing EMI.
7. High Sensitivity — the SSR can readily be designed to interface directly with TTL and CMOS logic, simplifying circuit design.
8. Very Low Coupling Capacitance Between Input and Output. This is a characteristic inherent in the optoelectronic-coupler used in the SSR, and can be useful in areas such as medical electronics where the reduction of stray leakage paths is important.

This list of advantages is impressive, but of course, the designer has to consider the following disadvantages:

1. Voltage Transient Resistance — the ac line is not the clean sine wave obtainable from a signal generator. Superimposed on the line are voltage spikes from motors, solenoids, EMRs (ironical), lightning, etc. The solid-state components in the SSR have a finite voltage rating and must be protected from such spikes, either with RC networks (snubbing), zener diodes, MOVs or selenium voltage clippers. If not done, the thyristors will turn on for part of a half cycle, and at worst, they will be permanently damaged, and fail to block voltage. For critical applications a safety margin on voltage of 2 to 1 or better should be sought.

The voltage transient has at least two facets — the first is the sheer amplitude, already discussed. The second is its frequency, or rate-of-rise of voltage (dv/dt). All thyristors are sensitive to dv/dt to some extent, and the transient must be snubbed, or "soaked up," to below this level with an RC network.[1] Typically this rating ("critical" or "static" dv/dt) is 50 to 100 V/μs at maximum temperature. Again the failure mode is to let through, to a half-cycle of the line, though a high energy transient can cause permanent damage. Table 6.1 gives some starting points for snubbing circuit values. The component values required depend on the characteristics of the transient, which are usually difficult to quantify. Snubbing across the line as well as across the SSR will also help.

Table 6.1. Typical Snubbing Values

Load Current A rms	Resistance Ω	Capacitance μF
5	47	0.047
10	33	0.1
25	10	0.22
40	22	0.47

1. For a more thorough discussion of snubbers, see page 38.
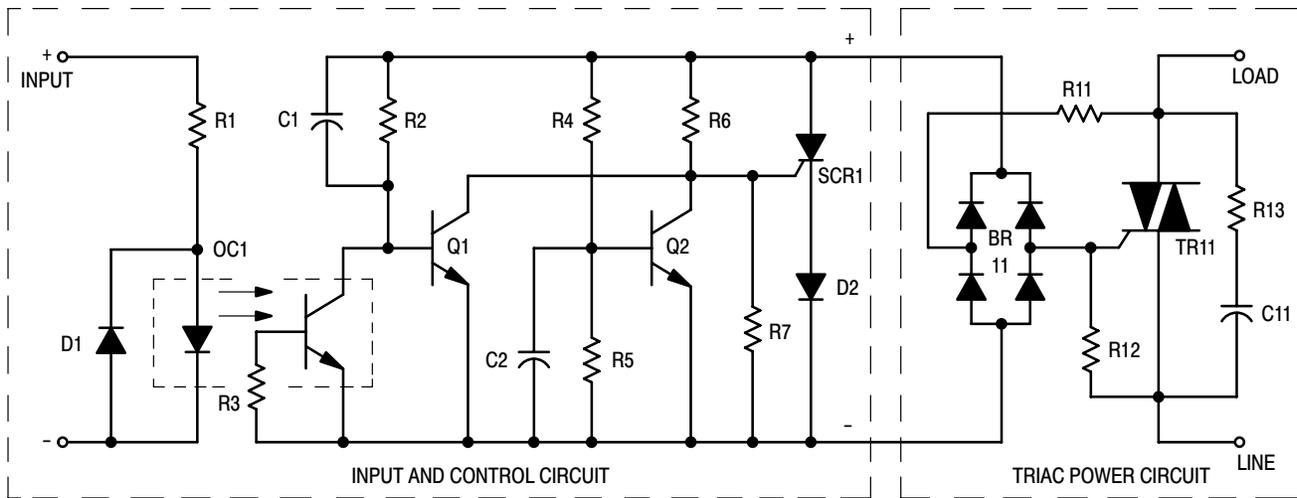
Figure 6.39 (a). TRIAC SSR Circuit

2. Voltage Drop — The SSR output contact has some offset voltage — approximately 1 V, depending on current, causing dissipation. As the thyristor has an operating temperature limit of +125°C, this heat must be removed, usually by conduction to air via a heat sink or the chassis.

3. Leakage Current — When an EMR is open, no current can flow. When an SSR is open however, it does not have as definite an off condition. There is always some current leakage through the output power switching thyristor, the control circuitry, and the snubbing network. The total of this leakage is usually 1 to 10 mA rms — three or four orders of magnitude less than the on-state current rating.

4. Multiple Poles — are costly to obtain in SSRs, and three phase applications may be difficult to implement.

5. Nuclear Radiation — SSRs will be damaged by nuclear radiation.

TRIAC SSR CIRCUIT

Many SSR circuits use a TRIAC as the output switching device. Figure 6.39(a) shows a typical TRIAC SSR circuit. The control circuit is used in the SCR relay as well, and is defined separately. The input circuit is TTL compatible. Output snubbing for inductive loads will be described later.

A sensitive-gate SCR (SCR1) is used to gate the power TRIAC, and a transistor amplifier is used as an interface between the optoelectronic-coupler and SCR1. (A sensitive-gate SCR and a diode bridge are used in preference to a sensitive gate TRIAC because of the higher sensitivity of the SCR.)

CONTROL CIRCUIT OPERATION

The operation of the control circuit is straightforward. The AND function of Figure 6.38 is performed by the wired-NOR collector configuration of the small-signal transistors Q1 and Q2. Q1 clamps the gate of SCR1 if optoelectronic-coupler OC1 is off. Q2 clamps the gate if there is sufficient voltage at the junction of the potential divider R4,R5 to overcome the V_{BE} of Q2. By judicious selection of R4 and R5, Q2 will clamp SCR1's gate if more than approximately 5 Volts appear at the anode of SCR1; i.e., Q2 is the zero-crossing detector.

Table 6.2. Control Circuit Parts List

Line Voltage

Part	120 V rms	240 V rms
C1	220 pF, 20%, 200 Vdc	100 pF, 20%, 400 Vdc
C2	0.022 µF, 20%, 50 Vdc	0.022 µF, 20%, 50 Vdc
D1	1N4001	1N4001
D2	1N4001	1N4001
OC1	MOC1005	MOC1005
Q1	MPS5172	MPS5172
Q2	MPS5172	MPS5172
R1	1 kΩ, 10%, 1 W	1 kΩ, 10%, 1 W
R2	47 kΩ, 5%, 1/2 W	100 kΩ, 5%, 1 W
R3	1 MΩ, 10%, 1/4 W	1 MΩ, 10%, 1/4 W
R4	110 kΩ, 5%, 1/2 W	220 kΩ, 5%, 1/2 W
R5	15 kΩ, 5%, 1/4 W	15 kΩ, 5%, 1/4 W
R6	33 kΩ, 10%, 1/2 W	68 kΩ, 10%, 1 W
R7	10 kΩ, 10%, 1/4 W	10 kΩ, 10%, 1/4 W
SCR1	2N5064	2N6240

If OC1 is on, Q1 is clamped off, and SCR1 can be turned on by current flowing down R6, only if Q2 is also off — which it is only at zero crossing.
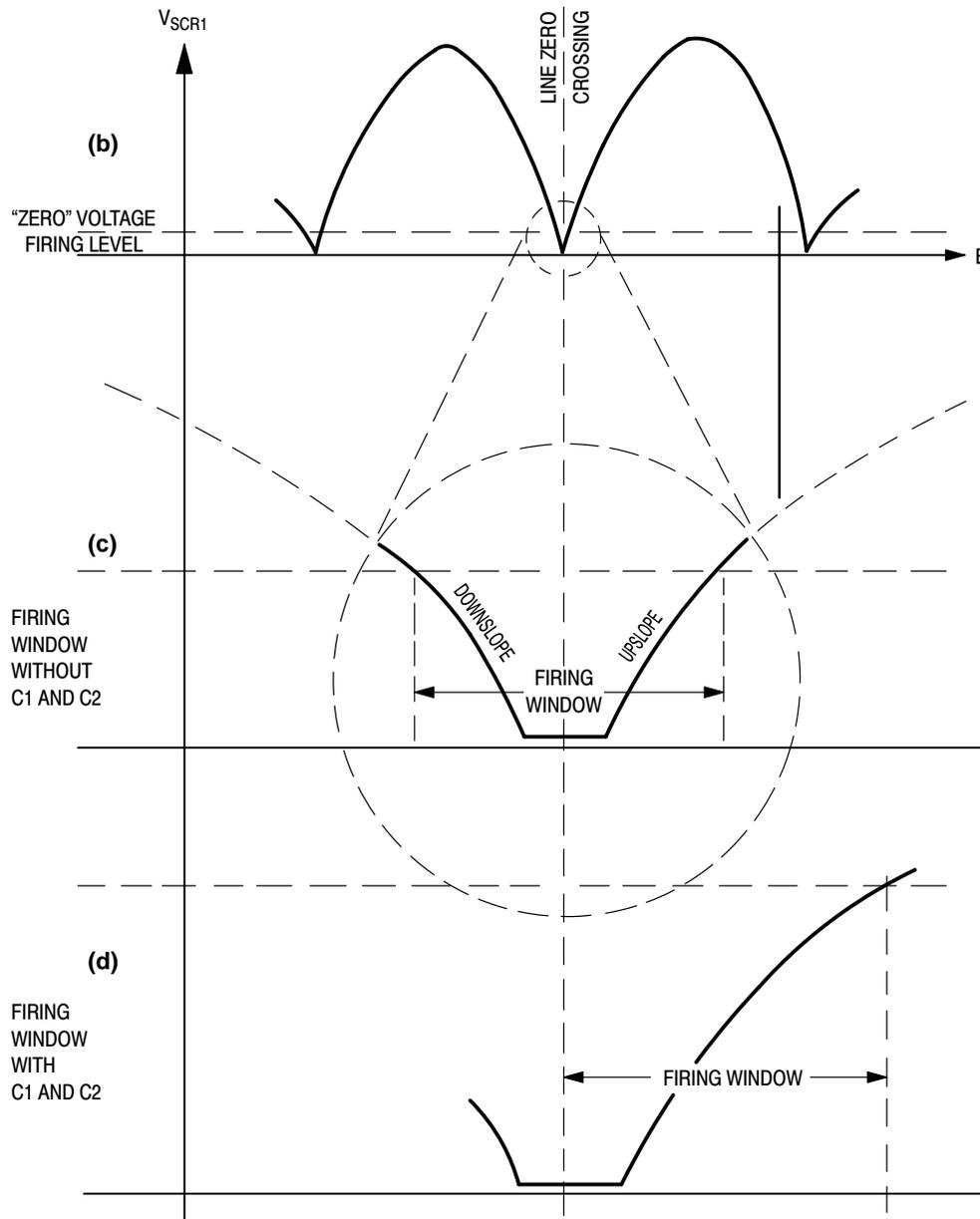
Figure 6.39. Firing Windows

The capacitors are added to eliminate circuit race conditions and spurious firing, time ambiguities in operation. Figure 6.39(b) shows the full-wave rectified line that appears across the control circuit. The zero voltage firing level is shown in 6.39(b) and 6.39(c), expanded in time and voltage. A race condition exists on the up-slope of the second half-cycle in that SCR1 may be triggered via R6 before Q1 has enough base current via R2 to clamp SCR1's gate. C1 provides current by virtue of the rate of change of the supply voltage, and Q1 is turned on firmly as the supply voltage starts to rise, eliminating any possibility of unwanted firing of the SSR; thus eliminating the race condition.

This leaves the possibility of unwanted firing of the SSR on the down-slope of the first half cycle shown. C2 provides a phase shift to the zero voltage potential divider, and Q2 is held on through the real zero-crossing. The resultant window is shown in 6.39(d).

CONTROL CIRCUIT COMPONENTS

The parts list for the control circuit at two line voltages is shown in Table 6.2.

R1 limits the current in the input LED of OC1. The input circuit will function over the range of 3 to 33 Vdc.

D1 provides reverse voltage protection for the input of OC1.

D2 allows the gate of SCR1 to be reverse biased, providing better noise immunity and dv/dt performance.

R7 eliminates pickup on SCR1's gate through the zero-crossing interval.

SCR1 is a sensitive gate SCR; the 2N5064 is a TO-92 device, the 2N6240 is a Case 77 device.

Alternatives to the simple series resistor (R1) input circuit will be described later.

POWER CIRCUIT COMPONENTS

The parts list for the TRIAC power circuit in Figure 6.39(a) is shown in Table 6.3 for several rms current ratings, and two line voltages. The metal TRIACs are in the half-inch pressfit package in the isolated stud configuration; the plastic TRIACs are in the TO-220 Thermowatt package. R12 is chosen by calculating the peak control circuit off-state leakage current and ensuring that the voltage drop across R12 is less than the $V_{GT(MIN)}$ of the TRIAC.

C11 must be an ac rated capacitor, and with R13 provides some snubbing for the TRIAC. The values shown for this network are intended more for inductive load commutating dv/dt snubbing than for voltage transient suppression. Consult the individual data sheets for the dissipation, temperature, and surge current limits of the TRIACs.

Table 6.3. TRIAC Power Circuit Parts List

Voltage	120 V rms				240 V rms			
rms Current Amperes	8	12	25	40	8	12	25	40
BR11	IN4004(4)	IN4004(4)	IN4004(4)	IN4004(4)	IN4004(4)	IN4004(4)	IN4004(4)	IN4004(4)
C11, µF (10%, line voltage ac rated)	0.047	0.047	0.1	0.1	0.047	0.047	0.1	0.1
R11 (10%, 1 W)	39	39	39	39	39	39	39	39
R12 (10%, 1/2 W)	18	18	18	18	18	18	18	18
R13 (10%, 1/2 W)	620	620	330	330	620	620	330	330
TR11 Plastic	2N6344	2N6344A	—	—	2N6344	2N6344A	—	—

TRIACs AND INDUCTIVE LOADS

The TRIAC is a single device which to some extent is the equivalent of two SCRs inverse parallel connected; certainly this is so for resistive loads. Inductive loads however, can cause problems for TRIACs, especially at turn-off.

A TRIAC turns off every line half-cycle when the line current goes through zero. With a resistive load, this coincides with the line voltage also going through zero. The TRIAC must regain blocking-state before there are more than 1 or 2 Volts of the reverse polarity across it — at 120 V rms, 60 Hz line this is approximately 30 µs. The TRIAC has not completely regained its off-state characteristics, but does so as the line voltage increases at the 60 Hz rate.

Figure 6.40 indicates what happens with an inductive or lagging load. The on signal is removed asynchronously and the TRIAC, a latching device, stays on until the next current zero. As the current is lagging the applied voltage, the line voltage at that instant appears across the TRIAC. It is this rate-of-rise of voltage, the commutating dv/dt, that must be limited in TRIAC circuits, usually to a few volts per microsecond. This is normally done by use of a snubber network R_S and C_S as shown in Figure 6.41.

SCRs have less trouble as each device has a full half-cycle to turn off and, once off, can resist dv/dt to the critical value of 50 to 100 V/µs.

CHOOSING THE SNUBBING COMPONENTS[1]

There are no easy methods for selecting the values of R_S and C_S in Figure 6.41 required to limit commutating dv/dt. The circuit is a damped tuned circuit comprised by R_S, C_S, R_L and L_L, and to a minor extent the junction capacitance of the TRIAC. At turn-off this circuit receives a step impulse of line voltage which depends on the power factor of the load. Assuming the load is fixed, which is normally the case, the designer can vary R_S and C_S. C_S can be increased to decrease the commutating dv/dt; R_S can be increased to decrease the resonant over-ring of the tuned circuit — to increase damping. This can be done empirically, beginning with the values for C11 and R13 given in Table 6.3, and aiming at close to critical damping and the data sheet value for commutating dv/dt. Reduced temperatures, voltages, and off-going di/dt (rate-of-change of current at turn-off) will give some safety margin.

1. For a more thorough discussion of snubbers, see page 38.
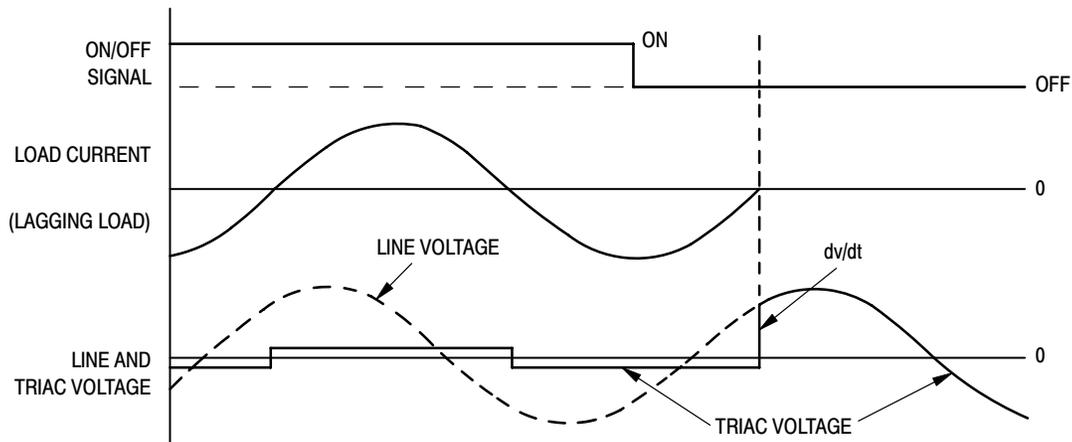
Figure 6.40. Commutating dv/dt

Table 6.4. SCR Power Circuit Parts List

Voltage		120 V rms				240 V rms			
rms Current Amperes		5	11	22	49	5	11	22	49
C21 (10%, line voltage ac rated)		SEE TEXT							
D21-24		1N4003	1N4003	1N4003	1N4003	1N4004	1N4004	1N4004	1N4004
R21 (10%, 1 W)		39	39	39	39	39	39	39	39
R22, 23 (10%, 1/2 W)		18	18	18	18	18	18	18	18
R24		SEE TEXT							
SCR21, 22	Plastic	2N6240	2N6397	2N6402	—	2N6240	2N6397	2N6403	—
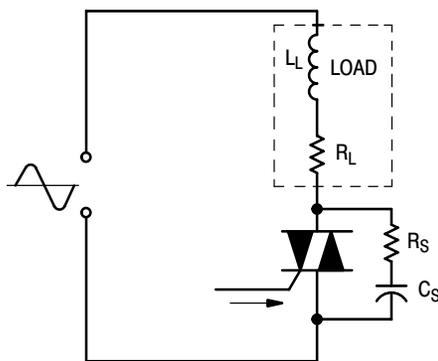
Figure 6.41. TRIAC with Snubber Network

SCR SSR CIRCUIT

The inverse parallel connected Silicon Controlled Rectifier (SCR) pair (shown in Figure 6.42) is less sensitive to commutating dv/dt. Other advantages are the improved thermal and surge characteristics of having two devices; the disadvantage is increased cost.

The SCR power circuit can use the same control circuit as the TRIAC Circuit shown in Figure 6.39(a). In Figure 6.42, for positive load terminal and when the control circuit is gated on, current flows through the load, D21, R21, SCR1, D22, the gate of SCR21 and back to the line, thus turning on SCR21. Operation is similar for the other line polarity. R22 and R23 provide a path for the off-state leakage of the control circuit and are chosen so that the voltage dropped across them is less than the $V_{GT(MIN)}$ of the particular SCR. R24 and C21 provide snubbing and line transient suppression, and may be chosen from Table 6.4 or from the C11, R13 rows of Table 6.3. The latter values will provide less transient protection but also less off-state current, with the capacitor being smaller. Other circuit values are shown in Table 6.46.
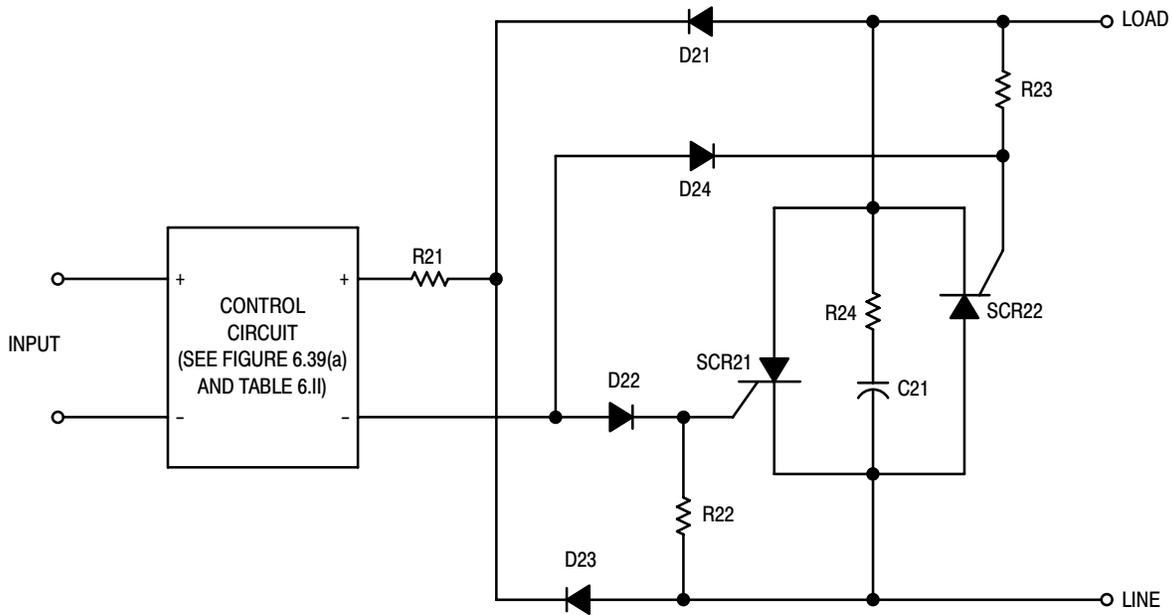
Figure 6.42. SCR SSR Circuit

Consult the individual data sheets for packages and dissipation, temperature, and surge current limits.

While the SCRs have much higher dv/dt commutation ability, with inductive loads, attention should be paid to maintaining the dv/dt below data sheet levels.

ALTERNATE INPUT CIRCUITS

CMOS COMPATIBLE

The 1 kΩ resistor, R1, shown in Figure 6.39(a) and Table 6.2, provide an input that is compatible with the current that a TTL gate output can sink. The resistor R1 must be changed for CMOS compatibility, aiming at 2 mA in the LED for adequate performance to 100°C. At 2 mA do not use the CMOS output for any other function, as a LOGIC 0 or 1 may not be guaranteed. Assume a forward voltage drop of 1.1 V for the LED, and then make the Ohm's Law calculation for the system dc supply voltage, thus defining a new value for R1.

TTL/CMOS COMPATIBLE

To be TTL compatible at 5 Volts and CMOS compatible over 3 to 15 Volts, a constant current circuit is required, such as the one in Figure 6.43. The current is set by the V_{BE} of Q31 and the resistance of the R32, R33, and thermistor TH31 network, and is between 1 and 2 mA, higher at high temperatures to compensate for the reduced transmission efficiency of optoelectronic-couplers at higher temperature. The circuit of Figure 6.43 gives an equivalent impedance of approximately 50 kΩ. The circuit performs

adequately over 3 to 33 Vdc and −40 to +100°C. Note that though the SSR is protected against damage from improperly connected inputs, the external circuit is not, as D31 acts as a bypass for a wrongly connected input driver.
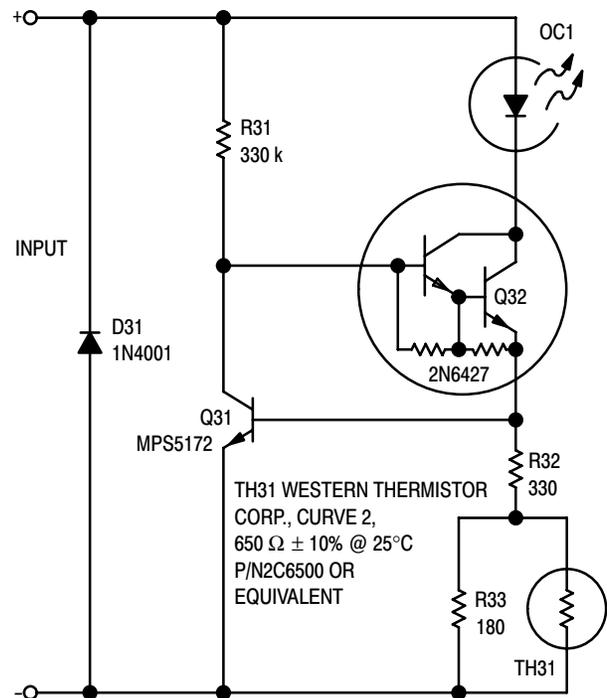
Figure 6.43. TTL/CMOS Compatible Input

AC LINE COMPATIBLE

To use SSRs as logic switching elements is inefficient, considering the availability and versatility of logic families such as CMOS. When it is convenient to trigger from ac, a circuit such as shown in Figure 6.44 may be used. The capacitor C41 is required to provide current to the LED of OC1 through the zero-crossing time. An in-phase input voltage gives the worst case condition. The circuit gives 2 mA minimum LED current at 75% of nominal line voltage.

INVERSE PARALLEL SCRs FOR POWER CONTROL

TRIACs are very useful devices. They end up in solid state relays, lamp drivers, motor controls, sensing and detection circuits; just about any industrial full-wave application. But in high-frequency applications or those requiring high voltage or current, their role is limited by their present physical characteristics, and they become very expensive at current levels above 40 amperes rms.

SCRs can be used in an inverse-parallel connection to bypass the limitations of a TRIAC. A simple scheme for doing this is shown in Figure 6.45. The control device can take any of many forms, shown is the reed relay (Figure 6.45). TRIACs and Opto couplers can be inserted at point A–A to replace the reed relay.

	R41
120 V	22 kΩ, 10%, 1 W
240 V	47 kΩ, 10%, 2 W

Figure 6.44. AC Compatible Input

Compared to a TRIAC, an inverse-parallel configuration has distinct advantages. Voltage and current capabilities are dependent solely on SCR characteristics with ratings today of over a thousand volts and several hundred amps. Because each SCR operates only on a half-wave basis, the system's rms current rating is $\sqrt{2}$ times the SCR's rms current rating (see Suggested SCR chart). The system has the same surge current rating as the SCRs do. Operation at 400 Hz is also no problem. While turn-off time and dv/dt limits control TRIAC operating speed, the recovery characteristics of an SCR need only be better than the appropriate half-wave period.

$$R \geq \frac{\sqrt{2}\,V}{I_{GP}} - (R_L + R_C)$$

WHERE I_{GP} IS PEAK GATE CURRENT RATING OF SCR
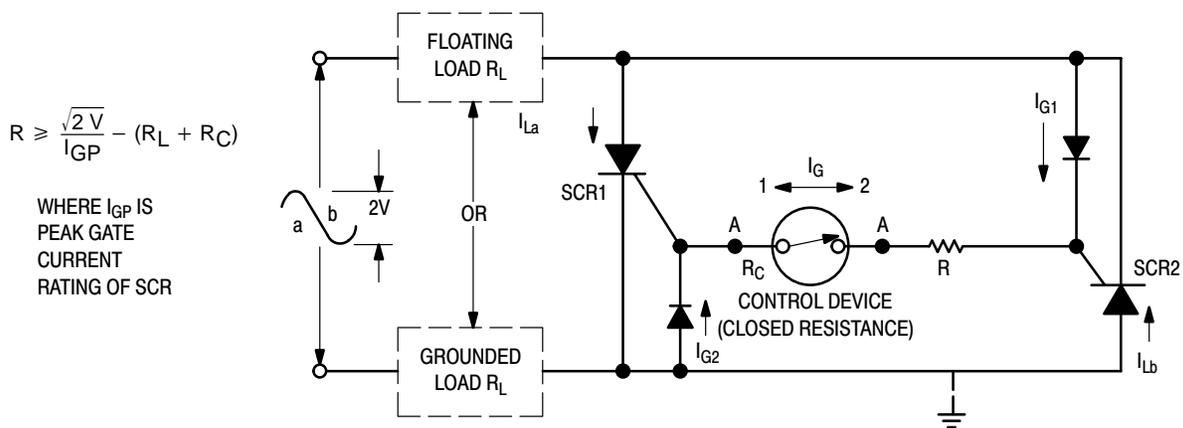
Figure 6.45. Use of Inverse Parallel SCRs

With inductive loads you no longer need to worry about commutating dv/dt, either. SCRs only need to withstand static dv/dt, for which they are typically rated an order of magnitude greater than TRIACs are for commutating dv/dt.

Better reliability can be achieved by replacing the reed relay with a low current TRIAC to drive the SCRs, although some of its limitations come with it. In the preferred circuit of Figure 6.46(b), the main requirements of the TRIAC are that it be able to block the peak system voltage and that it have a surge current rating compatible with the gate current require-ments of the SCRs. This is normally so small that a TO-92 cased device is adequate to drive the largest SCRs.

In circuits like Figure 6.45, the control devices alternately pass the gate currents I_{G1} and I_{G2} during the "a" and "b" half cycles, respectively. I_{La} and I_{Lb} are the load currents during the corresponding half cycles. Each SCR then gets the other half cycle for recovery time. Heat sinking can also be done more efficiently, since power is being dissipated in two packages, rather than all in one. The load can either be floated or grounded. the SCRs are not of the shunted-gate variety, a gate-cathode resistance should be added to shunt the leakage current at higher temperatures. The diodes act as steering diodes so the gate-cathode junctions are not avalanched. The blocking capability of the diodes need only be as high as the V_{GT} of the SCRs. A snubber can also be used if conditions dictate.

(a). Reed Relay   (b). Low-Current TRIAC   (c). Optically Coupled TRIAC Driver
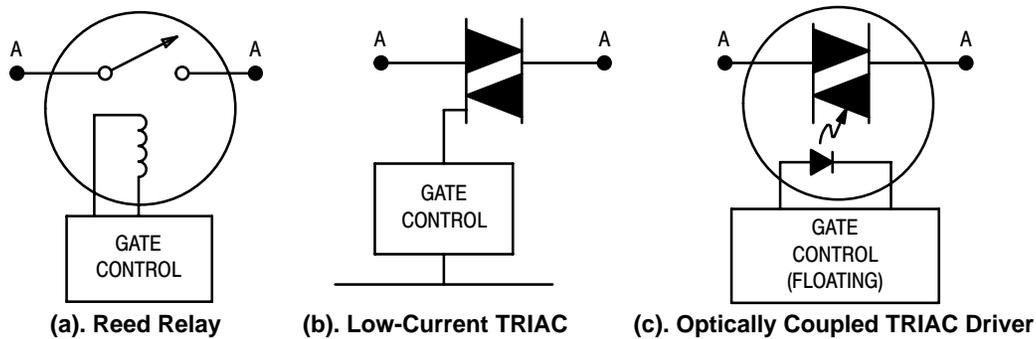
Figure 6.46. Control Devices

This circuit offers several benefits. One is a considerable increase in gain. This permits driving the TRIAC with almost any other semiconductors such as linear ICs, photosensitive devices and logic, including MOS. If necessary, it can use an optically coupled TRIAC driver to isolate (up to 7500 V isolation) delicate logic circuits from the power circuit (see Figure 6.46(c)). Table 6.6. lists suggested components. Another benefit is being able to gate the TRIAC with a supply of either polarity. Probably the most important benefit of the TRIAC/SCR combination is its ability to handle variable-phase applications — nearly impossible for non solid-state control devices.

Table 6.6. Driver TRIACs

Line Voltage	Gate Negative Or In Phase With Line Voltage	Gate Positive	Optically Coupled
120	MAC97A4	MAC97A4	MOC3030*, 3011
220	MAC97A6	MAC97A6	MOC3020, MOC3021

*Includes inhibit circuit for zero crossover firing.

INTERFACING DIGITAL CIRCUITS TO THYRISTOR CONTROLLED AC LOADS

Because they are bidirectional devices, TRIACs are the most common thyristor for controlling ac loads. A TRIAC can be triggered by either a positive or negative gate signal on either the positive or negative half-cycle of applied MT2 voltage, producing four quadrants of operation. However, the TRIAC's trigger sensitivity varies with the quadrant, with quadrants II and III (gate signal negative and MT2 either positive or negative) being the most sensitive and quadrant IV (gate positive, MT2 negative) the least sensitive.

For driving a TRIAC with IC logic, quadrants II and III are particularly desirable, not only because less gate trigger current is required, but also because IC power dissipation is reduced since the TRIAC can be triggered by an "active low" output from the IC.

There are other advantages to operating in quadrants II and III. Since the rate of rise of on-state current of a TRIAC (di/dt) is a function of how hard the TRIAC's gate is turned on, a given IC output in quadrants II and III will produce a greater di/dt capability than in the less sensitive quadrant IV. Moreover, harder gate turn-on could reduce di/dt failure. One additional advantage of quadrant II and III operation is that devices specified in all four quadrants are generally more expensive than devices specified in quadrants I, II and III, due to the additional testing involved and the resulting lower yields.

USING TRIACs

Two important thyristor parameters are gate trigger current (I_{GT}) and gate trigger voltage (V_{GT}).

I_{GT} (Gate Trigger Current) is the amount of gate trigger current required to turn the device on. I_{GT} has a negative temperature coefficient — that is, the trigger current required to turn the device on increases with decreasing temperature. If the TRIAC must operate over a wide temperature range, its I_{GT} requirement could double at the low temperature extreme from that of its 25°C rating.

It is good practice, if possible, to trigger the thyristor with three to ten times the I_{GT} rating for the device. This increases its di/dt capability and ensures adequate gate trigger current at low temperatures.

V_{GT} (Gate Trigger Voltage) is the voltage the thyristor gate needs to ensure triggering the device on. This voltage is needed to overcome the input threshold voltage of the device. To prevent thyristor triggering, gate voltage should be kept to approximately 0.4 V or less.

Like I_{GT}, V_{GT} increases with decreasing temperature.

INDUCTIVE LOAD SWITCHING

Switching of inductive loads, using TRIACs, may require special consideration in order to avoid false triggering. This false-trigger mechanism is illustrated in Figure 6.47 which shows an inductive circuit together with the accompanying waveforms.

As shown, the TRIAC is triggered on, at t1, by the positive gate current (I_{GT}). At that point, TRIAC current flows and the voltage across the TRIAC is quite low since the TRIAC resistance, during conduction, is very low.

From point t1 to t2 the applied I_{GT} keeps the TRIAC in a conductive condition, resulting in a continuous sinusoidal current flow that leads the applied voltage by 90° for this pure inductive load.

At t2, I_{GT} is turned off, but TRIAC current continues to flow until it reaches a value that is less than the sustaining current (I_H), at point A. At that point, TRIAC current is cut off and TRIAC voltage is at a maximum. Some of that voltage is fed back to the gate via the internal capacitance (from MT2 to gate) of the TRIAC.

TTL-TO-THYRISTOR INTERFACE

The subject of interfacing requires a knowledge of the output characteristics of the driving stages as well as the input requirements of the load. This section describes the driving capabilities of some of the more popular TTL circuits and matches these to the input demands of thyristors under various practical operating conditions.
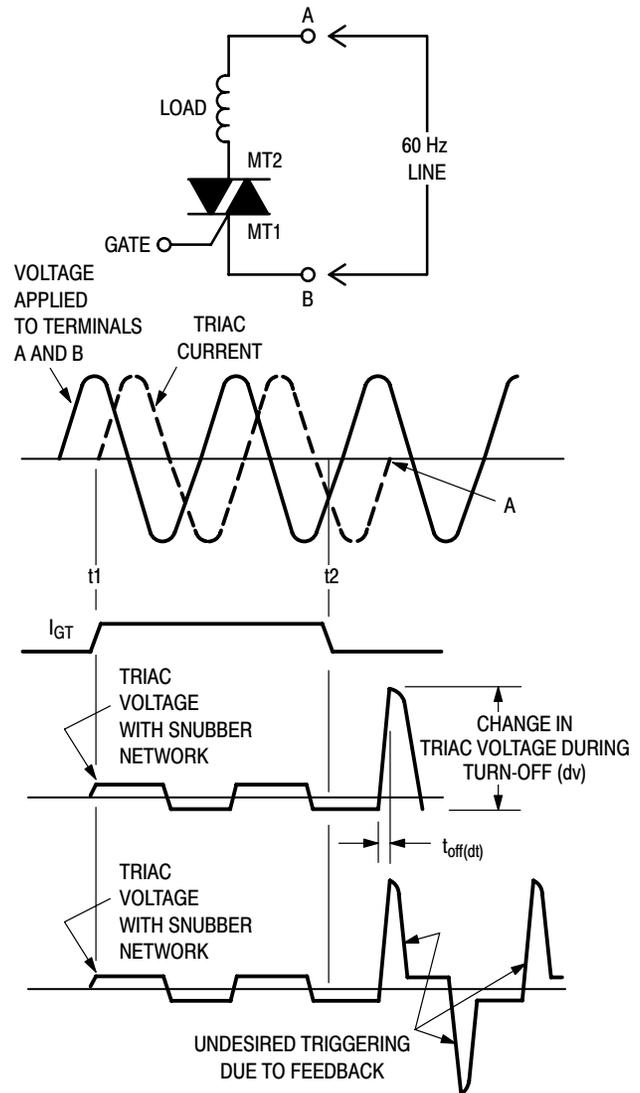
Figure 6.47. Inductive Load TRIAC Circuit and Equivalent Waveforms

TTL CIRCUITS WITH TOTEM-POLE OUTPUTS (e.g. 5400 SERIES)

The configuration of a typical totem-pole connected TTL output stage is illustrated in Figure 6.48(a). This stage is capable of "sourcing" current to a load, when the load is connected from V_{out} to ground, and of "sinking" current from the load when the latter is connected from V_{out} to V_{CC}. If the load happens to be the input circuit of a TRIAC (gate to MT_1), the TRIAC will be operating in quadrants I and IV (gate goes positive) when connected from V_{out} to ground, and of "sinking" II and III (gate goes negative) when connected from V_{out} to V_{CC}.

QUADRANT I-IV OPERATION

Considering first the gate-positive condition, Figure 6.48(b), the operation of the circuit is as follows:

When V_{in} to the TTL output stage is low (logical "zero"), transistors Q1 and Q3 of that stage are cut off, and Q2 is conducting. Therefore, Q2 sources current to the thyristor, and the thyristor would be triggered on during the $V_{in} = 0$ condition.

When V_{in} goes high (logical "one"), transistors Q1 and Q3 are on and Q2 is off. In this condition depicted by the equivalent circuit transistor Q3 is turned on and its collector voltage is, essentially, $V_{CE(sat)}$. As a result, the TRIAC is clamped off by the low internal resistance of Q3.

QUADRANT II-III OPERATION

When the TRIAC is to be operated in the more sensitive quadrants II and III (negative-gate turn-on), the circuit in Figure 6.49(a) may be employed.

With Q3 in saturation, as shown in the equivalent circuit of 6.49(b), its saturation voltage is quite small, leaving virtually the entire $-V_{EE}$ voltage available for thyristor turn-on. This could result in a TRIAC gate current that exceeds the current limit of Q3, requiring a current-limiting series resistor, ($R_{(lim)}$).

When the V_{out} level goes high, Q3 is turned off and Q2 becomes conductive. Under those conditions, the TRIAC gate voltage is below V_{GT} and the TRIAC is turned off.

DIRECT-DRIVE LIMITATIONS

With sensitive-gate TRIACs, the direct connection of a TRIAC to a TTL circuit may sometimes be practical. However, the limitations of such circuits must be recognized.

For example:

For TTL circuits, the "high" logic level is specified as 2.4 volts. In the circuit of Figure 6.48(a), transistor Q2 is capable of supplying a short-circuit output current (I_{SC}) of 20 to 55 mA (depending on the tolerances of R1 and R2, and on the h_{FE} of Q2). Although this is adequate to turn a sensitive-gate TRIAC on, the specified 2.4 volt (high) logic level can only be maintained if the sourcing current is held to a maximum of 0.4 mA — far less than the current required to turn on any thyristor. Thus, the direct connection is useful only if the driver need not activate other logic circuits in addition to a TRIAC.
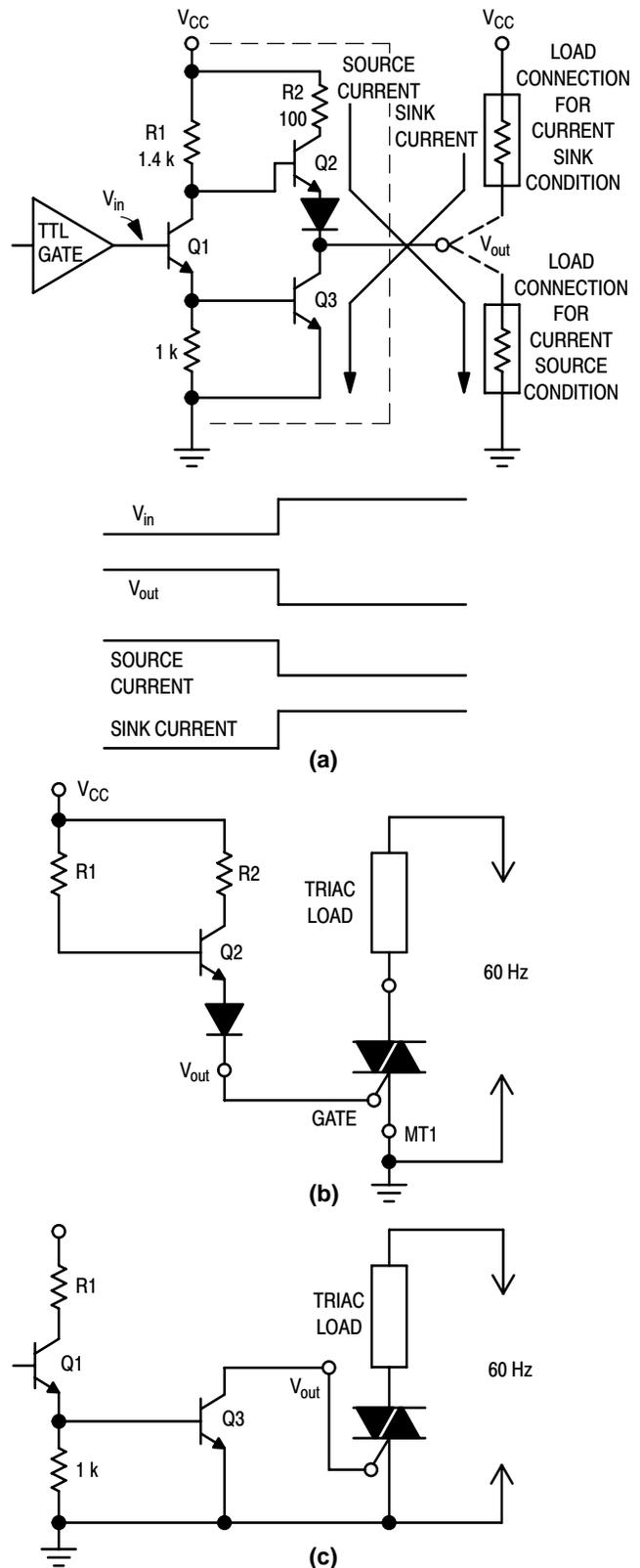
Figure 6.48. Totem-Pole Output Circuit TTL Logic, Together with Voltage and Current Waveforms, (b) Equivalent Circuit for Triggering TRIAC with a Positive Voltage — TRIAC-On Condition, (c) TRIAC-Off Condition

A similar limiting condition exists in the Logic "0" condition of the output, when the thyristor is to be clamped off. In this condition, Q3 is conducting and V_{out} equals the saturation voltage ($V_{CE(sat)}$) of Q3. TTL specifications indicate that the low logic level (logic "0") may not exceed 0.4 volts, and that the sink current must be limited to 16 mA in order not to exceed this value. A higher value of sink current would cause ($V_{CE(sat)}$) to rise, and could trigger the thyristor on.

CIRCUIT DESIGN CONSIDERATIONS

Where a 5400-type TTL circuit is used solely for controlling a TRIAC, with positive-gate turn-on (quadrants I-IV), a sensitive gate TRIAC may be directly coupled to the logic output, as in Figure 6.48. If the correct logic levels must be maintained, however, a couple of resistors must be added to the circuit, as in Figure 6.50(a). In this diagram, R1 is a pull-up which allows the circuit to source more current during a high logical output. Its value must be large enough, however, to limit the sinking current below the 16 mA maximum when V_{out} goes low so that the logical zero level of 0.4 volts is not exceeded.

Resistor R2, a voltage divider in conjunction with R1, insures V_{OH} (the "high" output voltage) to be 2.4 V or greater.

For a supply voltage of 5 V and a maximum sinking current of 16 mA

$$R_1 \geq V_{CC}/16\,\text{mA} \geq 5/0.016 \geq 312\ \Omega$$

Thus, 330 Ω, 1/4 W resistor may be used. Assuming R_1 to be 330 Ω and a thyristor gate on voltage (V_{GT}) of 1 V, the equivalent circuit of Figure 6.49(b) exists during the logical "1" output level. Since the logical "1" level must be maintaned at 2.4 volts, the voltage drop across R_2 must be 1.4 V. Therefore,

$$R_2 = 1.4/I_R = 1.4/V_{R_1/R_2} = 1.4/(2.6/3.30) \cong 175\ \Omega$$

A 180 Ω resistor may be used for R_2. If the V_{GT} is less than 1 volt, R_2 may need to be larger.

The MAC97A and 2N6071A TRIACs are compatible devices for this circuit arrangement, since they are guaranteed to be triggered on by 5 mA, whereas the current through the circuit of Figure 6.50(b) is approximately 8 mA, (V_{R_1}/R_1).

When the TRIAC is to be turned on by a negative gate voltage, as in Figure 6.49(b), the purpose of the limiting resistor $R_{(lim)}$ is to hold the current through transistor Q3 to 16 mA. With a 5 V supply, a TRIAC V_{GT} of 1 V and a maximum sink current of 16 mA

$$R_{(lim)} = (V_{CC} - V_{GT})/I_{sink} = (5-1)(0.016 \geq 250\ \Omega$$

In practice, a 270 Ω, 1/4 W resistor may be used.
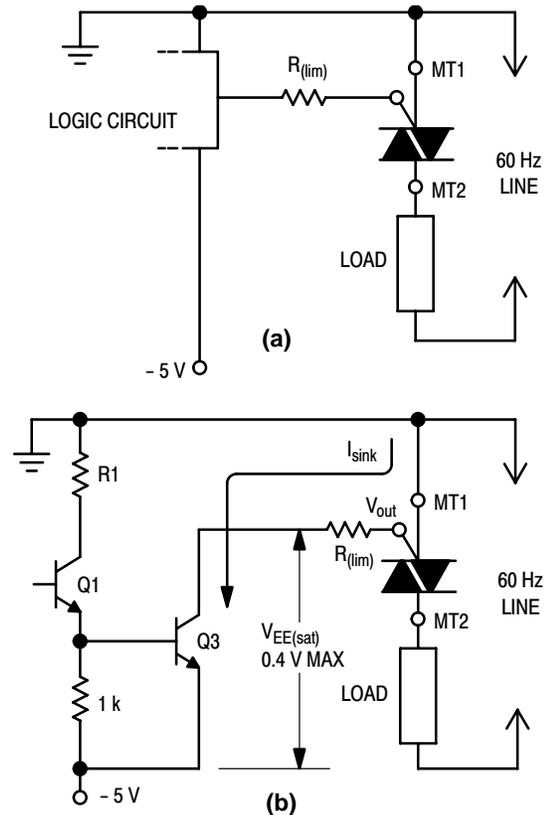
Figure 6.49. TTL Circuit for Quadrant II and III TRIAC Operation Requiring Negative V_{GT}, (b) Schematic Illustrates TRIAC Turn-On Condition, V_{out} = Logical "0"
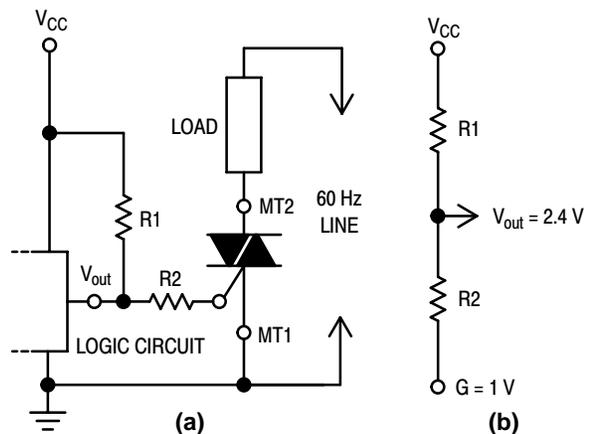
Figure 6.50. Practical Direct-Coupled TTL TRIAC Circuit, (b) Equivalent Circuit Used for Calculation of Resistor Values

OPEN COLLECTOR TTL CIRCUIT

The output section of an open-collector TTL gate is shown in Figure 6.51(a).

A typical logic gate of this kind is the 5401 type Q2-input NAND gate circuit. This logic gate also has a maximum sink current of 16 mA (V_{OL} = 0.4 V max.) because of the Q1 (sat) limitations. If this logic gate is to source any current, a pull-up-collector resistor, R_1 (6.51b) is needed. When this TTL gate is used to trigger a thyristor, R_1 should be chosen to supply the maximum trigger current available from the TTL circuit ($\approx$ 16 mA, in this case). The value of R_1 is calculated in the same way and for the same reasons as in Figure 6.50. If a logical "1" level must be maintained at the TTL output (2.4 V min.), the entire circuit of Figure 6.50 should be used.

For direct drive (logical "0") quadrants II and III triggering, the open collector, negative supplied (−5 V) TTL circuit of Figure 6.52 can be used. Resistor R_1 can have a value of 270 Ω, as in Figure 6.49. Resistor R_2 ensures that the TRIAC gate is referenced to MT1 when the TTL gate goes high (off), thus preventing unwanted turn-on. An R_2 value of about 1 k should be adequate for sensitive gate TRIACs and still draw minimal current.

(a)

(b)
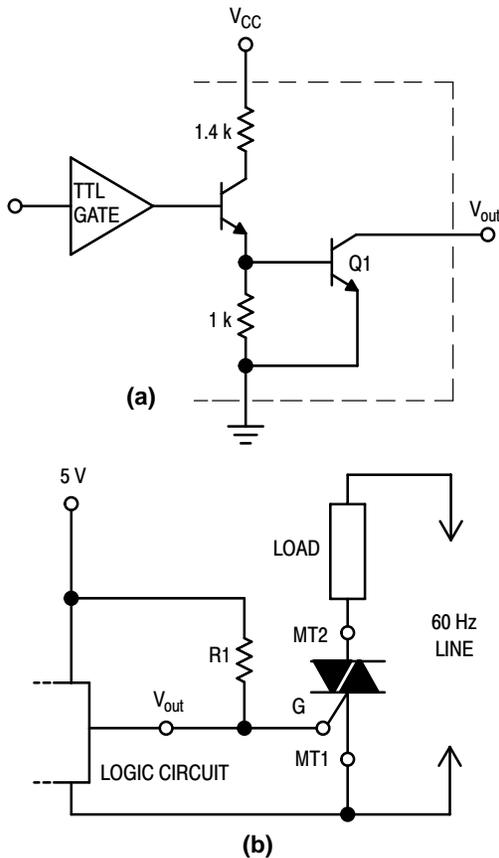
Figure 6.51. Output Section of Open-Collector TTL, (b) For Current Sourcing, A Pull-up Resistor, R1, Must Be Added

Circuits utilizing Schottky TTL are generally designed in the same way as TTL circuits, although the current source/sink capabilities may be slightly different.
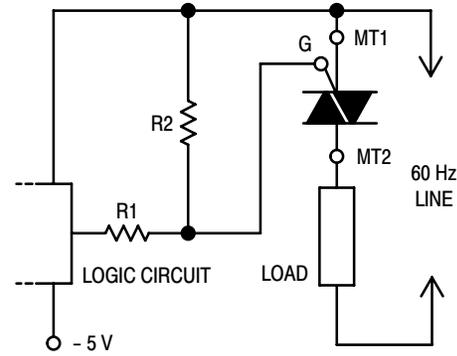
Figure 6.52. Negative-Supplied (−5 V) TTL Gate Permits TRIAC Operation in Quadrants II and III

TRIGGERING THYRISTORS FROM LOGIC GATES USING INTERFACE TRANSISTORS

For applications requiring thyristors that demand more gate current than a direct-coupled logic circuit can supply, an interface device is needed. This device can be a small-signal transistor or an opto coupler.

The transistor circuits can take several different configurations, depending on whether a series or shunt switch design is chosen, and whether gate-current sourcing (quadrants I and IV) or sinking (quadrants II and III) is selected. An example of a series switch, high output (logic 1) activation, is shown in Figure 6.53. Any logic family can be used as long as the output characteristics are known. The NPN interface transistor, Q1, is configured in the common-emitter mode — the simplest approach — with the emitter connected directly to the gate of the thyristor.
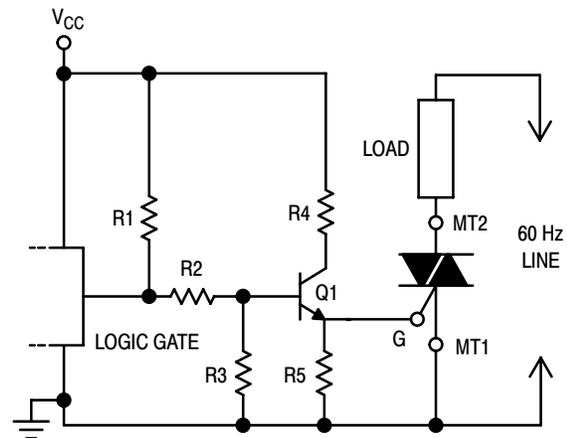
Figure 6.53. Series Switch, High Output (Logic "1")

Depending on the logic family used, resistor R_1 (pull-up resistor) and R_3 (base-emitter leakage resistor) may or may not be required. If, for example, the logic is a typical TTL totem-pole output gate that must supply 5 mA to the base of the NPN transistor and still maintain a "high" (2.4 V) logic output, then R_1 and R_2 are required. If the "high" logic level is not required, then the TTL circuit can directly source the base current, limited by resistor R_2.

To illustrate this circuit, consider the case where the selected TRIAC requires a positive-gate current of 100 mA. The interface transistor, a popular 2N4401, has a specified minimum h_{FE} (at a collector current of 150 mA) of 100. To ensure that this transistor is driven hard into saturation, under "worse case" (low temperature) conditions, a forced h_{FE} of 20 is chosen — thus, 5 mA of base current. For this example, the collector supply is chosen to be the same as the logic supply (+5 V); but for the circuit configuration, it could be a different supply, if required. The collector-resistor, R_4, is simply

$$R_4 = (V_{CC} - V_{CE(sat)} - V_{GT(typ)})/I_{GT}$$
$$= (5 - 1 - 0.9)/100 \, mA = 40 \, \Omega$$

A 39 ohm, 1 W resistor is then chosen, since its actual dissipation is about 0.4 W.

If the "logic 1" output level is not important, then the base limiting resistor R_2 is required, and the pull-up resistor R_1 is not. Since the collector resistor of the TTL upper totem-pole transistor, Q2, is about 100 Ω, this resistor plus R_2 should limit the base current to 5 mA.

Thus R_2 calculates to

$$R_2 = [(V_{CC} - V_{BE} - V_{GT})/5 \, mA] - 100 \, \Omega$$
$$= [(5 - 0.7 - 0.9)/0.005] \, 100 \, \Omega$$
$$\approx 560 \, \Omega \text{ (specified)}$$

When the TTL output is low, the lower transistor of the totem-pole, Q3, is a clamp, through the 560 Ω resistor, across the 2N4401; and, since the 560 Ω resistor is relatively low, no leakage-current shunting resistor, R_3, is required.

In a similar manner, if the TTL output must remain at "logic 1" level, the resistor R_1 can be calculated as described earlier (R_3 may or may not be required).

For low-logic activation (logic "0"), the circuit of Figure 6.54 can be used. In this example, the PNP-interface transistor 2N4403, when turned on, will supply positive-gate current to the thyristor. To ensure that the high logic level will keep the thyristor off, the logic gate and the transistor emitter must be supplied with the same power supply. The base resistors, as in the previous example, are dictated by the output characteristics of the logic family used. Thus if a TTL gate circuit is used, it must be able to sink the base current of the PNP transistor ($I_{OL(MAX)} = 16$ mA).

When thyristor operation in quadrants II and III is desired, the circuits of Figures 6.55 and 6.56 can be used; Figure 6.55 is for high logic output activation and Figure 6.56 is for low. Both circuits are similar to those on Figures 6.53 and 6.54, but with the transistor polarity and power supplies reversed.
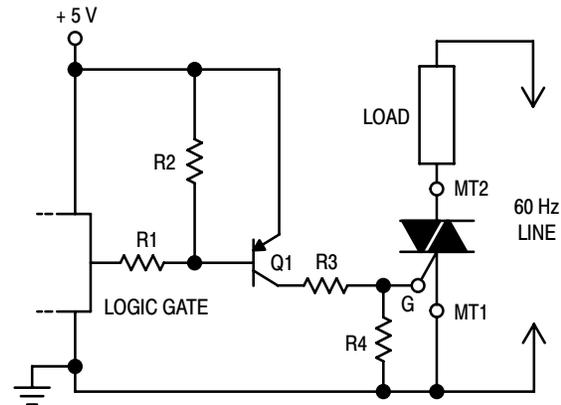
Figure 6.54. Low-Logic Activation with Interface Transistor
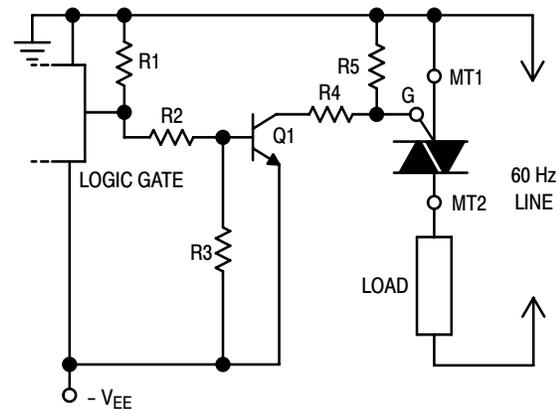
Figure 6.55. High-Logic Output Activation

Figure 6.55 sinks current from the thyristor gate through a switched NPN transistor whose emitter is referenced to a negative supply. The logic circuit must also be referenced to this negative supply to ensure that transistor Q1 is turned off when required; thus, for TTL gates, V_{EE} would be −5 V.

In Figure 6.56, the logic-high bus, which is now ground, is the common ground for both the logic, and the thyristor and the load. As in the first example (Figure 6.53), the negative supply for the logic circuit ($-V_{EE}$) and the collector supply for the PNP transistor need not be the same supply. If, for power-supply current limitations, the collector supply is chosen to be another supply ($-V_{CC}$), it must be within the V_{CEO} ratings of the PNP transistor. Also, the power dissipation of collector resistor, R3, is a function of $-V_{CC}$ — the lower $-V_{CC}$, the lower the power rating.
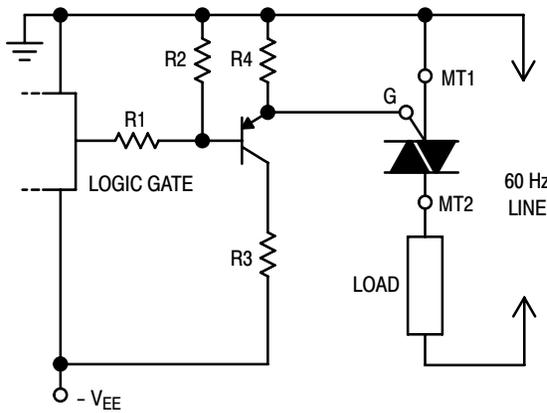
Figure 6.56. Low-Logic Output Activation
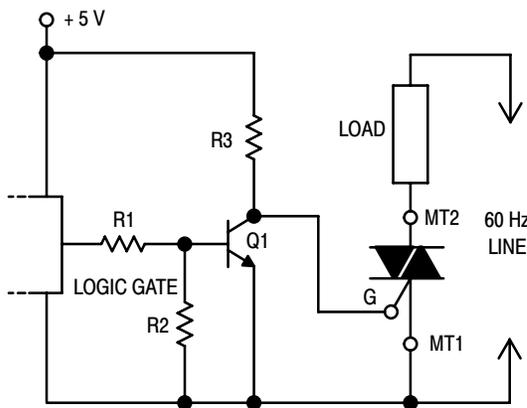
Figure 6.57. Shunt-Interface Circuit (High-Logic Output
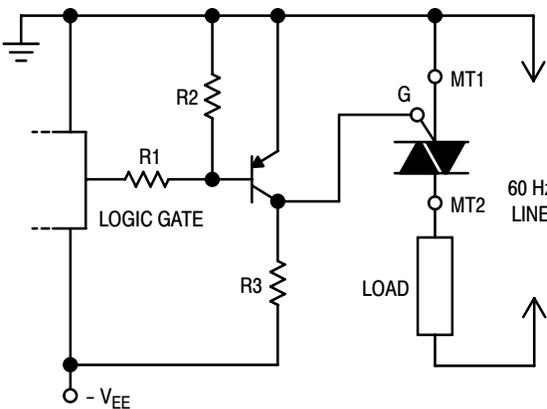
**Figure 6.58. Shunt-Interface Circuit
(Quadrants I and III Operation)**

The four examples shown use gate-series switching to activate the thyristor and load (when the interface transistor is off, the load is off). Shunt-switching can also be used if the converse is required, as shown in Figures 6.57 and 6.58. In Figure 6.57, when the logic output is high, NPN transistor, Q1, is turned on, thus clamping the gate of the thyristor off. To activate the load, the logic output goes low, turning off Q1 and allowing positive gate current, as set by resistor R3, to turn on the thyristor.

In a similar manner, quadrant's II and III operation is derived from the shunt interface circuit of Figure 6.58.

OPTICAL ISOLATORS/COUPLERS

An Optoelectronic isolator combines a light-emitting device and a photo detector in the same opaque package that provides ambient light protection. Since there is no electrical connection between input and output, and the emitter and detector cannot reverse their roles, a signal can pass through the coupler in one direction only.

Since the opto-coupler provides input circuitry protection and isolation from output-circuit conditions, ground-loop prevention, dc level shifting, and logic control of high voltage power circuitry are typical areas where opto-couplers are useful.

Figure 6.59 shows a photo-TRIAC used as a driver for a higher-power TRIAC. The photo-TRIAC is light sensitive and is turned on by a certain specified light density (H), which is a function of the LED current. With dark conditions (LED current = 0) the photo-TRIAC is not turned on, so that the only output current from the coupler is leakage current, called peak-blocking current (I_{DRM}). The coupler is bilateral and designed to switch ac signals.

The photo-TRIAC output current capability is, typically, 100 mA, continuous, or 1 A peak.
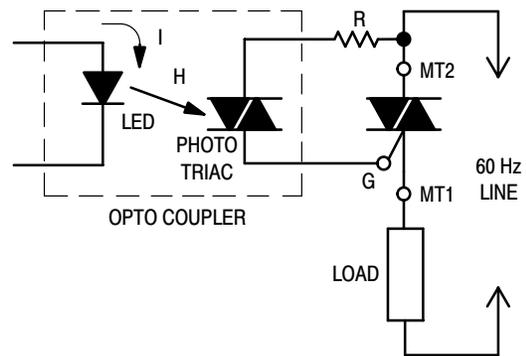
**Figure 6.59. Optically-Coupled TRIAC Driver is Used
to Drive a Higher-Power TRIAC**

Any Opto TRIAC can be used in the circuit of Figure 6.59 by using Table 6.8. The value of R is based on the photo-TRIAC's current-handling capability. For example, when the MOC3011 operates with a 120 V line voltage (approximately 175 V peak), a peak I_{GT} current of 175 V/180 ohm (approximately 1 A) flows when the line voltage is at its maximum. If less than 1 A of I_{GT} is needed, R can be increased. Circuit operation is as follows:

Table 6.8. Specifications for Typical Optically Coupled TRIAC Drivers

Device Type	Maximum Required LED Trigger Current (mA)	Peak Blocking Voltage	R(Ohms)
MOC3011	15	250	180
MOC3011	10	250	180
MOC3021	15	400	360
MOC3031	15	250	51

When an op-amp, logic gate, transistor or any other appropriate device turns on the LED, the emitted light triggers the photo-TRIAC. Since, at this time, the main TRIAC is not on, MT2-to-gate is an open circuit. The 60 Hz line can now cause a current flow via R, the photo-TRIAC, Gate-MT1 junction and load. This Gate-MT1 current triggers the main TRIAC, which then shorts and turns off the photo-TRIAC. The process repeats itself every half cycle until the LED is turned off.

Triggering the main TRIAC is thus accomplished by turning on the LED with the required LED-trigger current indicated in Table 6.7.

MICROPROCESSORS

Microprocessor systems are also capable of controlling ac power loads when interfaced with thyristors. Commonly, the output of the MPU drives a PIA (peripheral interface adaptor) which then drives the next stage. The PIA Output Port generally has a TTL compatible output with significantly less current source and sink capability than standard TTL. (MPUs and PIAs are sometimes constructed together on the same chip and called microcontrollers.)

When switching ac loads from microcomputers, it is good practice to optically isolate them from unexpected load or ac line phenomena to protect the computer system from possible damage. In addition, optical isolation will make UL recognition possible.

A typical TTL-compatible microcontroller, such as the MC3870P offers the following specifications:

$I_{OH} = 300 \ \mu A \ (V_{OH} = 2.4 \ V)$

$I_{OL} = 1.8 \ mA \ (V_{OL} = 0.4 \ V)$

$V_{CC} = 5 \ V$

Since this is not adequate for driving the optocoupler directly (10 mA for the MOC3011), an interface transistor is necessary.

The circuit of Figure 6.60 may be used for thyristor triggering from the 3870 logical "1."
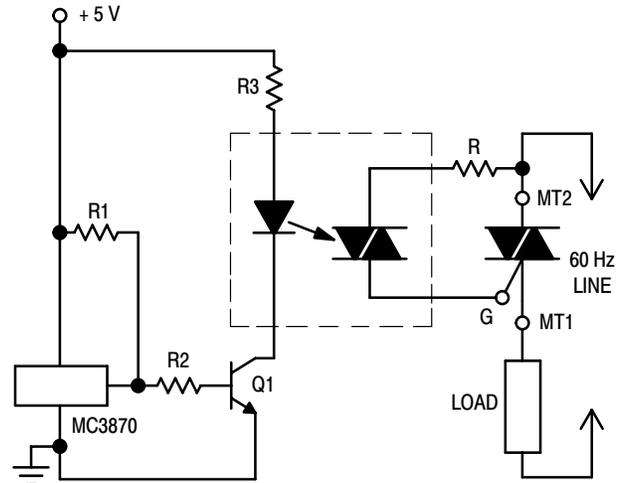
Figure 6.60. Logical "1" Activation from MC3870P Microcomputer

The interface transistor, again, can be the 2N4401. With 10 mA of collector current (for the MOC3011) and a base current of 0.75 mA, the $V_{CE(sat)}$ will be approximately 0.1 V.

R_1 can be calculated as in a previous example. Specifically:

1.8 mA (maximum I_{OL} for the 3870)

$> 5 \ V/R_1; \ R_1 \ > \ 2.77 \ k$

R_1 can be 3 k, 1/4 W

With a base current of 0.75 mA, R_1 will drop (0.75 mA) (3 k) or 2.25 V. This causes a V_{OH} of 2.75 V, which is within the logical "1" range.

$R_2 = [2.75 \ V - V_{BE(on)}]/I_B = (2.75 - 0.75)/0.75 = 2.66 \ k$

R_2 can be a 2.7 k, 1/4 W resistor.

R_3 must limit I_C to 10 mA :

$R_3 = [5 \ V - V_{CE(sat)} - V_F(diode)/10 \ mA]$

$= (5 - 0.1 - 1.2)/10 \ mA = 370 \ \Omega$

Since R_3 is relatively small, no base-emitter leakage resistor is required.

Figure 6.61 shows logical "0" activation. Resistor values are calculated in a similar way.
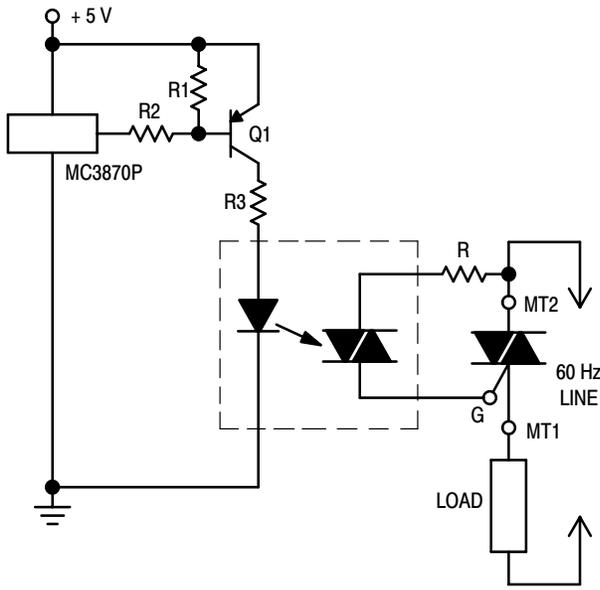
Figure 6.61. Logical "0" Activation
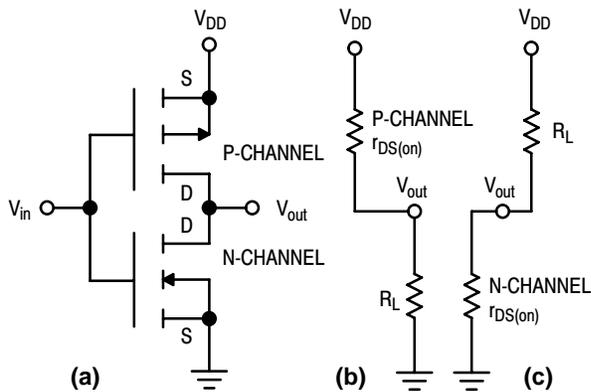
Figure 6.62. Output Section of a Typical CMOS Gate, (b) Equivalent Current-Sourcing Circuit is Activated when V_{in} goes Low, Turning the P-Channel Device Fully On, (c) Equivalent Current Sinking Circuit is Activated when the Input Goes High and Turns the N-Channel Device On

THE CMOS INTERFACE

Another popular logic family, CMOS, can also be used to drive thyristors.

As shown in Figure 6.62(a), the output stage of a typical CMOS Gate consists of a P-channel MOS device connected in series with an N-channel device (drain-to-drain), with the gates tied together and driven from a common input signal. When the input signal goes high, logical 1, the P-channel device is essentially off and conducts only leakage current (I_{DSS}), on the order of pico-amps. The N-channel unit is forward-biased and, although it has a relatively high on resistance ($r_{DS(on)}$), the drain-to-source voltage of the N-channel device (V_{DS}) is very low (essentially zero) because of the very low drain current (V_{DSS}) flowing through the device. Conversely, when the input goes low (zero), the P-channel device is turned fully on, the N-channel device is off and the output voltage will be very near V_{DD}.

When interfacing with transistors or thyristors, the CMOS Gate is current-limited mainly by its relatively high on resistance, the dc resistance between drain and source, when the device is turned on.

The equivalent circuits for sourcing and sinking current into an external load is shown in Figures 6.62(b) and 6.62(c). Normally, when interfacing CMOS to CMOS, the logic outputs will be very near their absolute maximum states (V_{DD} or 0 V) because of the extremely small load currents. With other types of loads (e.g. TRIACs), the current, and the resulting output voltage, is dictated by the simple voltage divider of $r_{DS(on)}$ and the load resistor R_L, where $r_{DS(on)}$ is the total series and/or parallel resistance of the devices comprising the NOR and NAND function.

Interfacing CMOS gates with thyristors requires a knowledge of the on resistance of the gate in the source and sink conditions. The on-resistance of CMOS devices is not normally specified on data sheets.

It can easily be calculated, however, from the output drive currents, which are specified. The drive (source/sink) currents of typical CMOS gates at various supply voltages are shown in Table 6.9. From this information, the on resistance for worst case design is calculated as follows:

For the source condition

$$r_{DS(on)(MAX)} = (V_{DD} - V_{OH})/I_{OH(MIN)}$$

Similarly, for the sink current condition

$$r_{DS(on)(MAX)} = V_{OL}/I_{OL(MIN)}$$

Values of $r_{DS(on)}$ for the various condition shown in Table 6.9 are tabulated in Table 6.10.

Specified source/sink currents to maintain logical "1" and logical "0" levels for various power-supply (V_{DD}) voltages. The I_{OH} and I_{OL} values are used to calculate the "on" resistance of the CMOS output.

Table 6.9. CMOS Characteristics

Output Drive Current	CMOS AL Series mA, dc		CMOSCL/CP Series mA, dc	
	Min	Typ	Min	Typ
$I_{(source)} - I_{OH}$ V_{DD} = 5 V; V_{OH} = 2.5 V V_{DD} = 10 V; V_{OH} = 9.5 V V_{DD} = 15 V; V_{OH} = 13.5 V	– 0.5 – 0.5	– 1.7 – 0.9 – 3.5	– 0.2 – 0.2	– 1.7 – 0.9 – 3.5
$I_{(sink)} - I_{OL}$ V_{DD} = 5 V; V_{OL} = 0.4 V V_{DD} = 10 V; V_{OL} = 0.5 V V_{DD} = 15 V; V_{OL} = 1.5 V	0.4 0.9	7.8 2 7.8	0.2 0.5	7.8 2 7.8

Table 6.10. Calculated CMOS On Resistance Values For Current Sourcing and Sinking at Various V_{DD} Options

Operating Conditions	Output Resistance, $r_{DS(on)}$ Ohms	
	Typical	Maximum
Source Condition V_{DD} = 5 V 10 V 15 V	1.7 k 500 430	12.5 k 2.5 k —
Sink Condition V_{DD} = 5 V 10 V 15 V	500 420 190	2 k 1 k —

It is apparent from this table that the on resistance decreases with increasing supply voltage.

Although the minimum currents are now shown on the data sheet for the 15 V case, the maximum on resistance can be no greater than the 10 V example and, therefore, can be assumed for worst case approximation to be 1 and 2.5 kohms for sink-and-source current cases, respectively.

The sourcing on resistance is greater than the sinking case because the difference in carrier mobilities of the two channel types.

Since $r_{DS(on)}$ for both source and sink conditions varies with supply voltage (V_{DD}), there are certain drive limitations. The relative high $r_{DS(on)}$ of the P-channel transistor could possibly limit the direct thyristor drive capability; and, in a like manner, the N-channel $r_{DS(on)}$ might limit its clamping capability. With a 10 or 15 V supply, the device may be capable of supplying more than 10 mA, but should be limited to that current, with an external limiting resistor, to avoid exceeding the reliable limits of the unit metalization.

DC MOTOR CONTROL WITH THYRISTORS

In order to control the speed of a dc series field motor at different required torque levels, it is necessary to adjust the voltage applied to the motor. For any particular applied voltage the motor speed is determined solely by the torque requirements and top speed is reached under minimum torque conditions. When a series motor is used as a traction drive for vehicles, it is desirable to control the voltage to the motor to fit the various torque requirements of grades, speed and load. The common method of varying the speed of the motor is by inserting resistance in series with the motor to reduce the supplied voltage. This type of motor speed control is very inefficient due to the I^2R loss, especially under high current and torque conditions.

A much more efficient method of controlling the voltage applied to the motor is the pulse width modulation method shown in Figure 6.63. In this method, a variable width pulse of voltage is applied to the motor at the same rate to proportionally vary the average voltage applied to the motor. A diode is placed in parallel with the inductive motor path to provide a circuit for the inductive motor current and prevent abrupt motor current change. Abrupt current changes would cause high induced voltage across the switching device.

V_M = BACK EMF OF MOTOR
L_M = MOTOR INDUCTANCE
R_M = MOTOR RESISTANCE
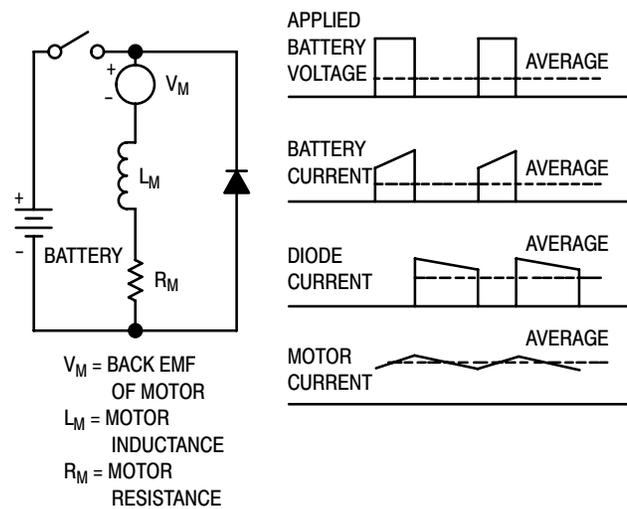
Figure 6.63. Basic Pulse Width Modulated Motor Speed Control

The circulating current through the diode decreases only in response to motor and diode loss. With reference to Figure 6.63, it can be seen that the circulating diode current causes more average current to flow through the motor than is taken from the battery. However, the power taken from the battery is approximately equal to the power delivered to the motor, indicating that energy is stored in the motor inductance at the battery voltage level and is delivered to the motor at the approximate current level when the battery is disconnected.

To provide smooth and quiet motor operation, the current variations through the motor should be kept to a minimum during the switching cycle. There are limitations on the amount of energy that can be stored in the motor inductance, which, in turn, limits the power delivered to the motor during the off time; thus the off time must be short. To operate the motor at low speeds, the on time must be approximately 10 percent of the off time and therefore, a rapid switching rate is required that is generally beyond the capabilities of mechanical switches. Practical solutions can be found by the use of semiconductor devices for fast, reliable and efficient switching operations.

SCR DC MOTOR CONTROL

SCRs offer several advantages over power transistors as semiconductor switches. They require less driver power, are less susceptible to damage by overload currents and can handle more voltage and current. Their disadvantages are that they have a higher power dissipation due to higher voltage drops and the difficulty in commutating to the off condition.

The SCR must be turned off by either interrupting the current through the anode-cathode circuit or by forcing current through the SCR in the reverse direction so that the net flow of forward current is below the holding current long enough for the SCR to recover blocking ability. Commutation of the SCR in high current motor control circuits is generally accomplished by discharging a capacitor through the SCR in the reverse direction. The value of this capacitor is determined approximately from the following equation:

$$C_c = \frac{T_q\, I_A}{V_c}$$

Where:

 C_c = value of necessary commutating capacitance
 T_q = turn-off time of the SCR
 I_A = value of anode current before commutation
 V_c = voltage of C_c before commutation

This relationship shows that to reduce the size of C_c, the capacitor should be charged to as high a voltage as possible and the SCR should be selected with as low a turn-off time as possible.

If a 20 microsecond turn-off time SCR is commutated by a capacitor charged to 36 volts, it would take over 110 μF to turn off 200 amperes in the RC commutating circuit of Figure 6.64. If a 50 cycle switching frequency is desired, the value of R_1 would be approximately 5 ohms to allow charging time with an on duty cycle of 10 percent. The value of this resistor would give approximately 260 watts dissipation in the charging circuit with 90 percent off duty cycle.

If the resonant charging commutating circuitry of Figure 6.65 is used, the capacitor is reduced to approxi-

mately 55 μF. In this circuit, SCR_3 is gated on at the same time as SCR_1 and allows the resonant charging of C_c through L_c to twice the supply voltage. SCR_3 is then turned off by the reversal of voltage in the resonant circuit before SCR_2 is gated on. It is apparent that there is very little power loss in the charge circuit depending upon the voltage drop across SCR_3 and the resistance in L_c.
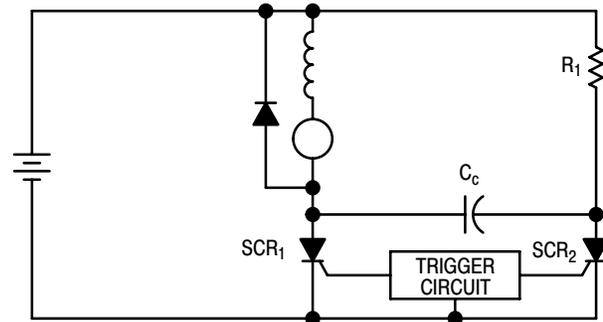
Figure 6.64. Speed Control with Resistive Charging
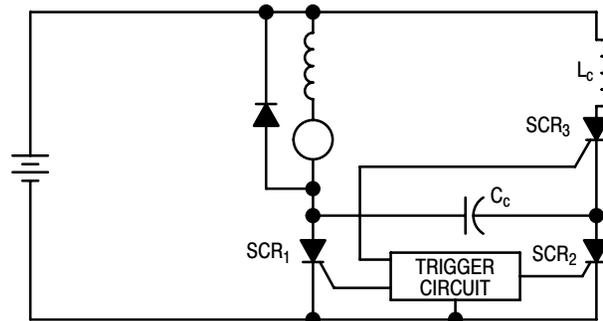
Figure 6.65. Speed Control with Inductive Charging
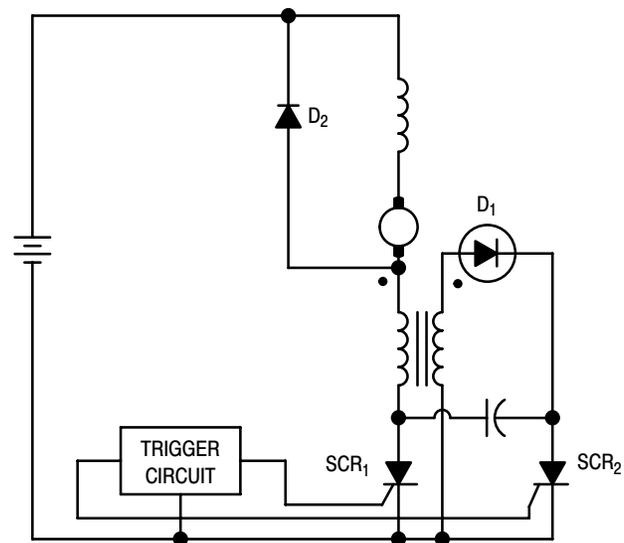
Figure 6.66. SCR Motor Control with Transformer Charging

If the commutating capacitor is to be reduced further, it is necessary to use a transformer to charge the capacitor to more than twice the supply voltage. This type of circuit is illustrated by the transformer charge circuit shown in Figure 6.66. In this circuit the capacitor can be charged to several times the supply voltage by transformer action through diode D_1 before commutating SCR_1. The disadvantage of this circuit is in the high motor current that flows through the transformer primary winding.

HEAVY DUTY MOTOR CONTROL WITH SCRs

Another advantage of SCRs is their high surge current capabilities, demonstrated in the motor drive portion of the golf cart controller shown in Figure 6.67. Germanium power transistors were used because of the low saturation voltages and resulting low static power loss. However, since switching speeds are slow and leakage currents are high, additional circuit techniques are required to ensure reliable operation:

1. The faster turn-on time of the SCR (Q9) over that of the germanium transistors shapes the turn-on load line.
2. The parallelled output transistors (Q3-Q8) require a 6 V reverse bias.
3. The driver transistor Q2 obtains reverse bias by means of diode D4.

To obtain the 6 V bias, the 36 V string of 6 V batteries are tapped, as shown in the schematic. Thus, the motor is powered from 30 V and the collector supply for Q2 is 24 V, minimizing the dissipation in colllector load resistor R1.

Total switching loss in switchmode applications is the result of the static (on-state) loss, dynamic (switching) loss and leakage current (off-state) loss. The low saturation voltage of germanium transistors produces low static loss. However, switching speeds of the germanium transistors are low and leakage currents are high. Loss due to leakage current can be reduced with off bias, and load line shaping can minimize switching loss. The turn-off switching loss was reduced with a standard snubber network (D5, C1, R2) see Figure 6.67.

Turn-on loss was uniquely and substantially reduced by using a parallel connected SCR (across the germanium transistors) the MCR265-4 (55 A rms, 550 A surge). This faster switching device diverts the initial turn-on motor load current from the germanium output transistors, reducing both system turn-on loss and transistor SOA stress.

The main point of interest is the power switching portion of the PWM motor controller. Most of the readily available PWM ICs can be used (MC3420, MC34060, TL494, SG1525A, UA78S40, etc.), as they can source at least a 10 mA, +15 V pulse for driving the following power MOSFET.
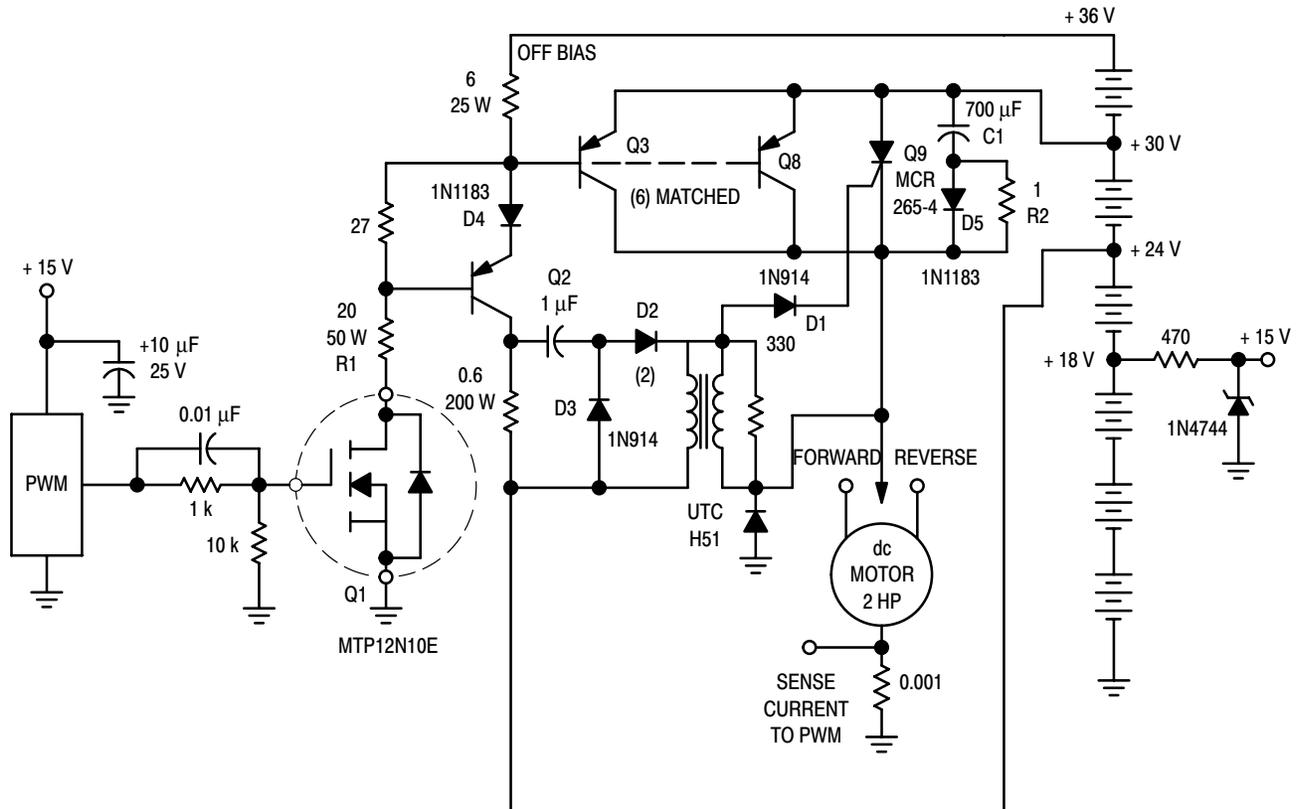
Figure 6.67. PWM DC Motor Controller Using SCR Turn-On Feature

Due to the extremely high input impedance of the power MOSFET, the PWM output can be directly connected to the FET gate, requiring no active interface circuitry. The positive going output of the PWM is power gained and inverted by the TMOS FET Q1 to supply the negative going base drive to PNP transistor Q2. Diode D1 provides off-bias to this paraphase amplifier, the negative going pulse from the emitter furnishing base drive to the six parallel connected output transistors and the positive going collector output pulse supplying the SCR gate trigger coupled through transformer T1.

Since the faster turn-on SCR is triggered on first, it will carry the high, initial turn-on motor current. Then the slower turn-on germanium transistors will conduct clamping off the SCR, and carry the full motor current. For the illustrated 2HP motor and semiconductors, a peak exponentially rising and falling SCR current pulse of 120 A lasting for about 60 μs was measured. This current is well within the rating of the SCR. Thus, the high turn-on stresses are removed from the transistors providing a much more reliable and efficient motor controller while using only a few additional components.

DIRECTION AND SPEED CONTROL FOR MOTORS

For a shunt motor, a constant voltage should be applied to the shunt field to maintain constant field flux so that the armature reaction has negligible effect. When constant voltage is applied to the shunt field, the speed is a direct function of the armature voltage and the armature current. If the field is weak, then the armature reaction may counterbalance the voltage drop due to the brushes, windings and armature resistances, with the net result of a rising speed-load characteristic.

The speed of a shunt-wound motor can be controlled with a variable resistance in series with the field or the armature. Varying the field current for small motor provides a wide range of speeds with good speed regulation. However, if the field becomes extremely weak, a rising speed-load characteristic results. This method cannot provide control below the design motor speed. Varying the resistance in series with the armature results in speeds less than the designed motor speed; however, this method yields poor speed regulation, especially at low speed settings. This method of control also increases power dissipation and reduces efficiency and the torque since the maximum armature current is reduced. Neither type of resistive speed control is very satisfactory. Thyristor drive controls, on the other hand, provide continuous control through the range of speed desired, do not have the power losses inherent in resistive circuits, and do not compromise the torque characteristics of motors.

Although a series-wound motor can be used with either dc or ac excitation, dc operation provides superior performance. A universal motor is a small series-wound motor designed to operate from either a dc or an ac supply of the same voltage. In the small motors used as universal motors, the winding inductance is not large enough to produce sufficient current through transformer action to create excessive commutation problems. Also, high-resistance brushes are used to aid commutation. The characteristics of a universal motor operated from alternating current closely approximate those obtained for a dc power source up to full load; however, above full load the ac and dc characteristics differ. For a series motor that was not designed as a universal motor, the speed-torque characteristic with ac rather than dc is not as good as that for the universal motor. At eight loads, the speed for ac operation may be greater than for dc since the effective ac field strength is smaller than that obtained on direct current. At any rate, a series motor should not be operated in a no-load condition unless precaution is are taken to limit the maximum speed.

SERIES-WOUND MOTORS

The circuit shown in Figure 6.68 can be used to control the speed and direction of rotation of a series-wound dc motor. Silicon controlled rectifiers Q1-Q4, which are connected in a bridge arrangement, are triggered in diagonal pairs. Which pair is turned on is controlled by switch S1 since it connects either coupling transformer T1 or coupling transformer T2 to a pulsing circuit. The current in the field can be reversed by selecting either SCRs Q2 and Q3 for conduction, or SCRs Q1 and Q4 for conduction. Since the armature current is always in the same direction, the field current reverses in relation to the armature current, thus reversing the direction of rotation of the motor.

A pulse circuit is used to drive the SCRs through either transformer T1 or T2. The pulse required to fire the SCR is obtained from the energy stored in capacitor C1. This capacitor charges to the breakdown voltage of zener diode D5 through potentiometer R1 and resistor R2. As the capacitor voltage exceeds the zener voltage, the zener conducts, delivering current to the gate of SCR Q5. This turns Q5 on, which discharges C1 through either T1 or T2 depending on the position of S1. This creates the desired triggering pulse. Once Q5 is on, it remains on for the duration of the half cycle. This clamps the voltage across C1 to the forward voltage drop of Q5. When the supply voltage drops to zero, Q5 turns off, permitting C1 to begin charging when the supply voltage begins to increase.
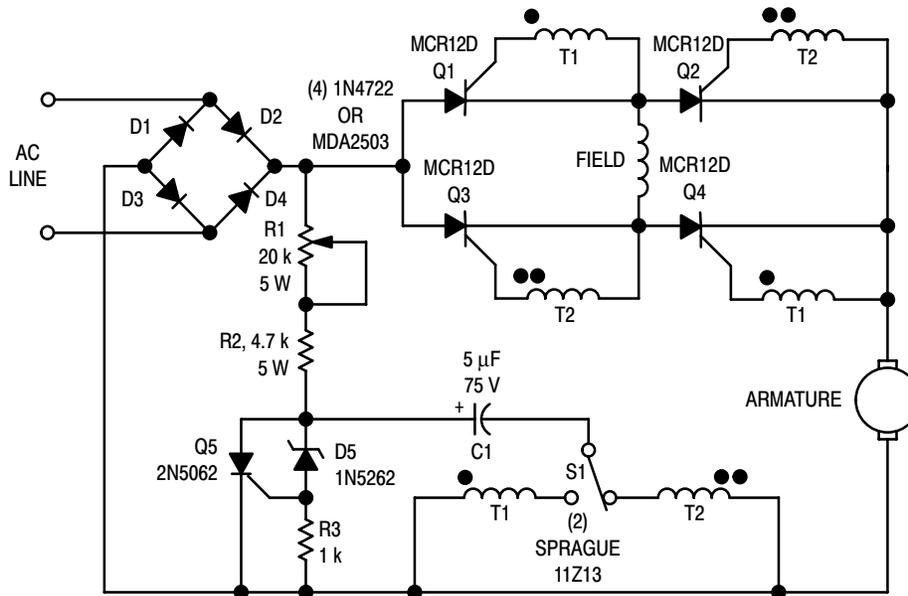
Figure 6.68. Direction and Speed Control for Series-Wound or Universal Motor
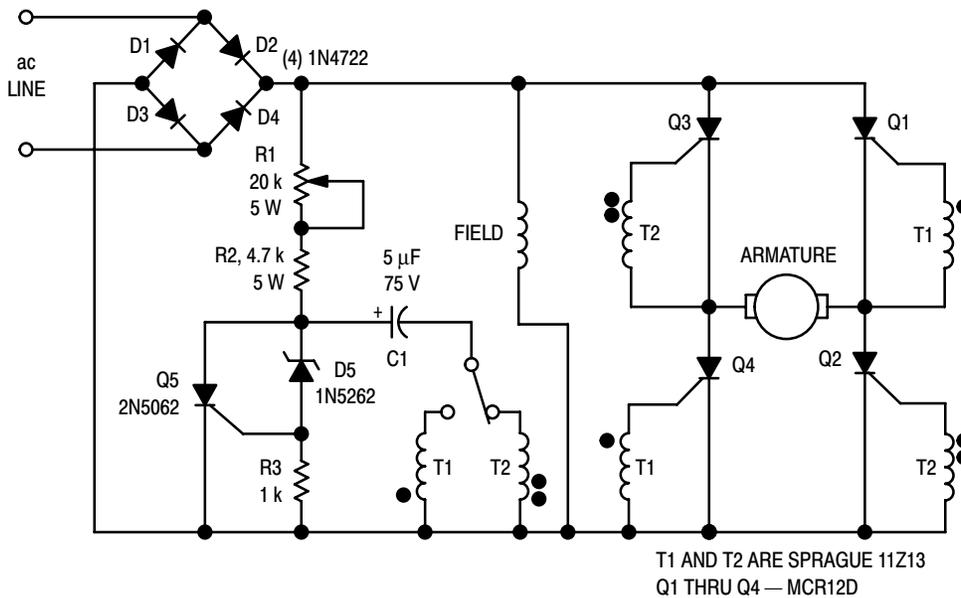
Figure 6.69. Direction and Speed Control for Shunt-Wound Motor

The speed of the motor can be controlled by potentiometer R1. The larger the resistance in the circuit, the longer required to charge C1 to the breakdown voltage of zener D5. This determines the conduction angle of either Q1 and Q4, or Q2 and Q3, thus setting the average motor voltage and thereby the speed.

SHUNT-WOUND MOTORS

If a shunt-wound motor is to be used, then the circuit in Figure 6.69 is required. This circuit operates like the one shown in Figure 6.68. The only differences are that the field is placed across the rectified supply and the armature is placed in the SCR bridge. Thus the field current is unidirectional but armature current is reversible; consequently the motor's direction of rotation is reversible. Potentiometer R1 controls the speed as explained previously.

RESULTS

Excellent results were obtained when these circuits were used to control 1/15 hp, 115 V, 5,000 r/min motors. This circuit will control larger, fractional-horsepower motors provided the motor current requirements are within the semiconductor ratings. Higher current devices will permit control of even larger motors, but the operation of the motor under worst case must not cause anode currents to exceed the ratings of the semiconductor.

PUT APPLICATIONS

PUTs are negative resistance devices and are often used in relaxation oscillator applications and as triggers for controlling thyristors. Due to their low leakage current, they are useful for high-impedance circuits such as long-duration timers and comparators.

TYPICAL CIRCUITS

The following circuits show a few of the many ways in which the PUT can be used. The circuits are not optimized even though performance data is shown.

In several of the circuit examples, the versatility of the PUT has been hidden in the design. By this it is meant that in designing the circuit, the circuit designer was able to select a particular intrinsic standoff ratio or he could select a particular RG (gate resistance) that would provide a maximum or minimum valley and peak current. This makes the PUT very versatile and very easy to design with.

LOW VOLTAGE LAMP FLASHER

The PUT operates very well at low supply voltages because of its low on-state voltage drop.

A circuit using the PUT in a low voltage application is shown in Figure 6.70 where a supply voltage of 3 volts is used. The circuit is a low voltage lamp flasher composed of a relaxation oscillator formed by Q1 and an SCR flip flop formed by Q2 and Q3.
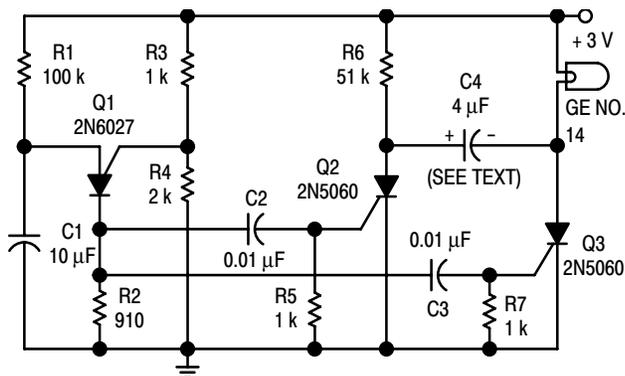
Figure 6.70. Low Voltage Lamp Flasher

With the supply voltage applied to the circuit, the timing capacitor C1 charges to the firing point of the PUT, 2 volts plus a diode drop. The output of the PUT is coupled through two 0.01 μF capacitors to the gate of Q2 and Q3. To clarify operation, assume that Q3 is on and capacitor C4 is charged plus to minus as shown in the figure. The next pulse from the PUT oscillator turns Q2 on. This places the voltage on C4 across Q3 which momentarily reverse biases Q3. This reverse voltage turns Q3 off. After discharging, C4 then charges with its polarity reversed to that shown. The next pulse from Q1 turns Q3 on and Q2 off. Note that C4 is a non-polarized capacitor.

For the component values shown, the lamp is on for about 1/2 second and off the same amount of time.
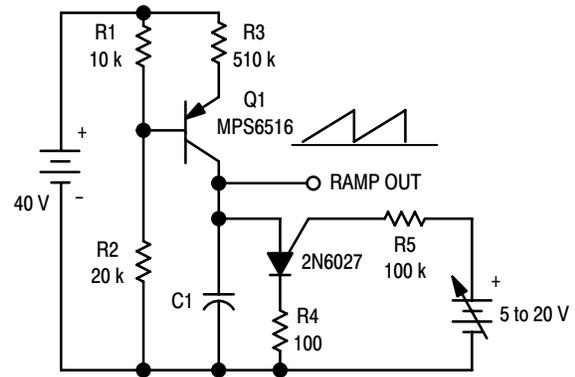
Figure 6.71. (a). Voltage Controlled Ramp Generator (VCRG)
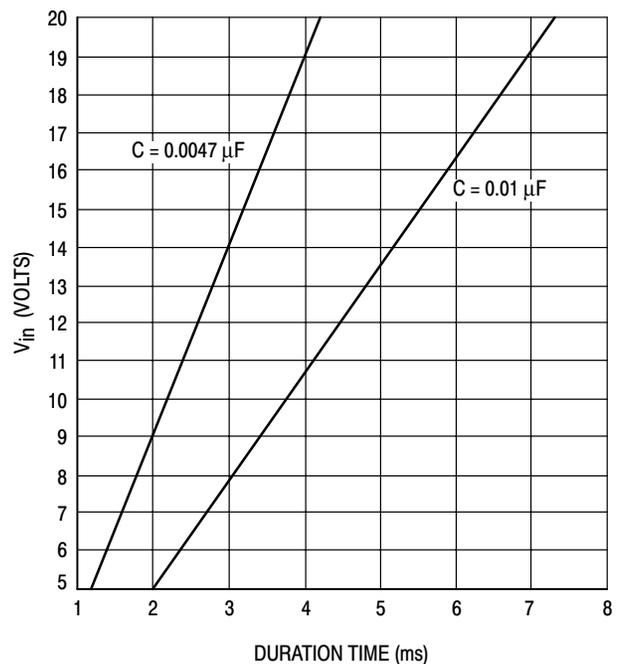
(b). Voltage versus Ramp Duration Time of VCRG

VOLTAGE CONTROLLED RAMP GENERATOR

The PUT provides a simple approach to a voltage controlled ramp generator, VCRG, as shown in Figure 6.71(a). The current source formed by Q1 in conjuction with capacitor C1 set the duration time of the ramp. As the positive dc voltage at the gate is changed, the peak point firing voltage of the PUT is changed which changes the duration time, i.e., increasing the supply voltage increases the peak point firing voltage causing the duration time to increase.

Figure 6.71(b) shows a plot of voltage-versus-ramp duration time for a 0.0047 µF and a 0.01 µF timing capacitor. The figure indicates that it is possible to have a change in frequency of 3 ms and 5.4 ms for the 0.0047 µF and the 0.01 µF capacitor respectively as the control voltage is varied from 5 to 20 volts.

LOW FREQUENCY DIVIDER

The circuit shown in Figure 6.72 is a frequency divider with the ratio of capacitors C1 and C2 determining division. With a positive pulse applied to the base of Q1, assume that C1 = C2 and that C1 and C2 are discharged. When Q1 turns off, both C1 and C2 charge to 10 volts each through R3. On the next pulse to the base of Q1, C1 is again

discharged but C2 remains charged to 10 volts. As Q1 turns off this time, C1 and C2 again charge. This time C2 charges to the peak point firing voltage of the PUT causing it to fire. This discharges capacitor C2 and allows capacitor C1 to charge to the line voltage. As soon as C2 discharges and C1 charges, the PUT turns off. The next cycle begins with another positive pulse on the base of Q1 which again discharges C1.

The input and output frequency can be approximated by the equation

$$f_{in} \approx \frac{(C1 + C2)}{C1} f_{out}$$

For a 10 kHz input frequency with an amplitude of 3 volts, Table 6.11 shows the values for C1 and C2 needed to divide by 2 to 11.

This division range can be changed by utilizing the programmable aspect of the PUT and changing the voltage on the gate by changing the ratio R6/(R6+R5). Decreasing the ratio with a given C1 and C2 decreases the division range and increasing the ratio increases the division range.

The circuit works very well and is fairly insensitive to the amplitude, pulse width, rise and fall times of the incoming pulses.
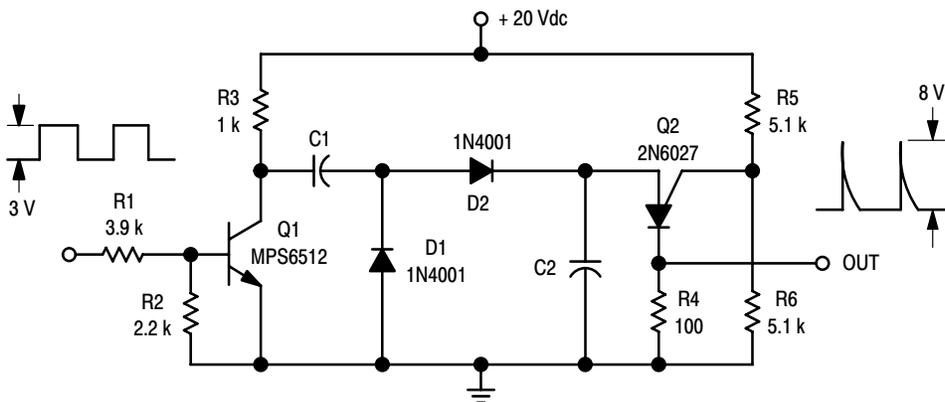
Table 6.11

C_1	C_2	Division
0.01 µF	0.01 µF	2
0.01 µF	0.02 µF	3
0.01 µF	0.03 µF	4
0.01 µF	0.04 µF	5
0.01 µF	0.05 µF	6
0.01 µF	0.06 µF	7
0.01 µF	0.07 µF	8
0.01 µF	0.08 µF	9
0.01 µF	0.09 µF	10
0.01 µF	0.1 µF	11

Figure 6.72. Low Frequency Divider

PUT LONG DURATION TIMER

A long duration timer circuit that can provide a time delay of up to 20 minutes is shown in Figure 6.73. The circuit is a standard relaxation oscillator with a FET current source in which resistor R1 is used to provide reverse bias on the gate-to-source of the JFET. This turns the JFET off and increases the charging time of C1. C1 should be a low leakage capacitor such as a mylar type.

The source resistor of the current source can be computed using the following equation:

$$V_{GS} = V_P \left(1 - \sqrt{I_O/I_{DSS}}\right)$$

$$\therefore R1 = \frac{V_{GS}}{I_O}$$

where I_O is the current out of the current source.
        V_P is the pinch off voltage,
        V_{GS} is the voltage gate-to-source and,
        I_{DSS} is the current, drain-to-source, with the gate
           shorted to the source.

The time needed to charge C1 to the peak point firing voltage of Q2 can be approximated by the following equation:

$$t = \frac{C\Delta V}{I},$$

where t is time in seconds
C is capacitance in µF,
ΔV is the change in voltage across capacitor C1, and
I is the constant current used to charge C1.

Maximum time delay of the circuit is limited by the peak point firing current, I_P, needed to fire Q2. For charging currents below I_P, there is not enough current available from the current source to fire Q2, causing the circuit to lock up. Thus PUTs are attractive for long duration timing circuits because of their low peak point current. This current becomes very small when RG (the equivalent parallel resistance of R3 and R4) is made large.

PHASE CONTROL

Figure 6.74 shows a circuit using a PUT for phase control of an SCR. The relaxation oscillator formed by Q2 provides conduction control of Q1 from 1 to 7.8 milliseconds or 21.6° to 168.5°. This constitutes control of over

For example, the 2N6028 has IP guaranteed to be less than 0.15 µA at RG = 1 M Ohm as shown in Figure 6.73.
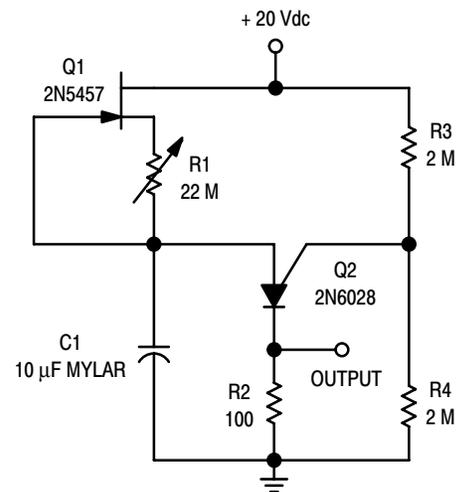
Figure 6.73. 20-Minute, Long Duration Timer

97% of the power available to the load.

Only one SCR is needed to provide phase control of both the positive and negative portion of the sine wave byputting the SCR across the bridge composed of diodes D1 through D4.
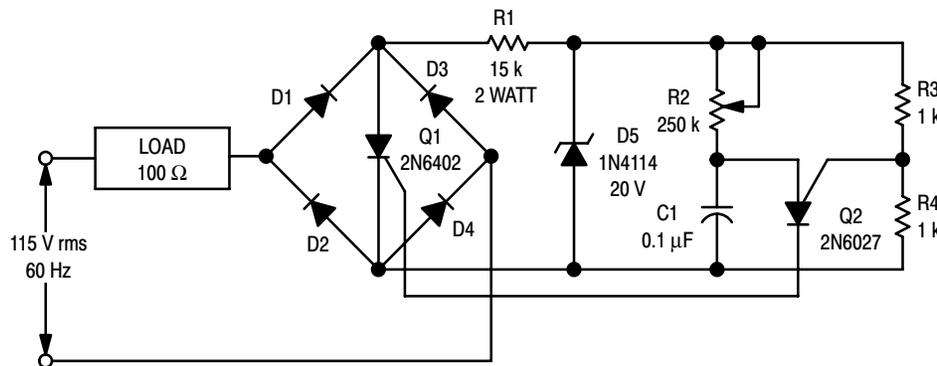
Figure 6.74. SCR Phase Control

BATTERY CHARGER USING A PUT

A short circuit proof battery charger is shown in Figure 6.75 which will provide an average charging current of about 8 amperes to a 12 volt lead acid storage battery. The charger circuit has an additional advantage in that it will not function nor will it be damaged by improperly connecting the battery to the circuit.

With 115 volts at the input, the circuit commences to function when the battery is properly attached. The battery provides the current to charge the timing capacitor C1 used in the PUT relaxation oscillator. When C1 charges to the

peak point voltage of the PUT, the PUT fires turning the SCR on, which in turn applies charging current to the battery. As the battery charges, the battery voltage increases slightly which increases the peak point voltage of the PUT. This means that C1 has to charge to a slightly higher voltage to fire the PUT. The voltage on C1 increases until the zener voltage of D1 is reached which clamps the voltage on C1 and thus prevents the PUT oscillator from oscillating and charging ceases. The maximum battery voltage is set by potentiometer R2 which sets the peak point firing voltage of the PUT.

In the circuit shown, the charging voltage can be set from 10 V to 14 V, the lower limit being set by D1 and the upper limit by T1. Lower charging voltages can be obtained by reducing the reference voltage (reducing the value of zener diode D1) and limiting the charging current (using either a lower voltage transformer, T1, or adding resistance in series with the SCR).

Resistor R4 is used to prevent the PUT from being destroyed if R2 were turned all the way up.

Figure 6.75(b) shows a plot of the charging characteristics of the battery charger.
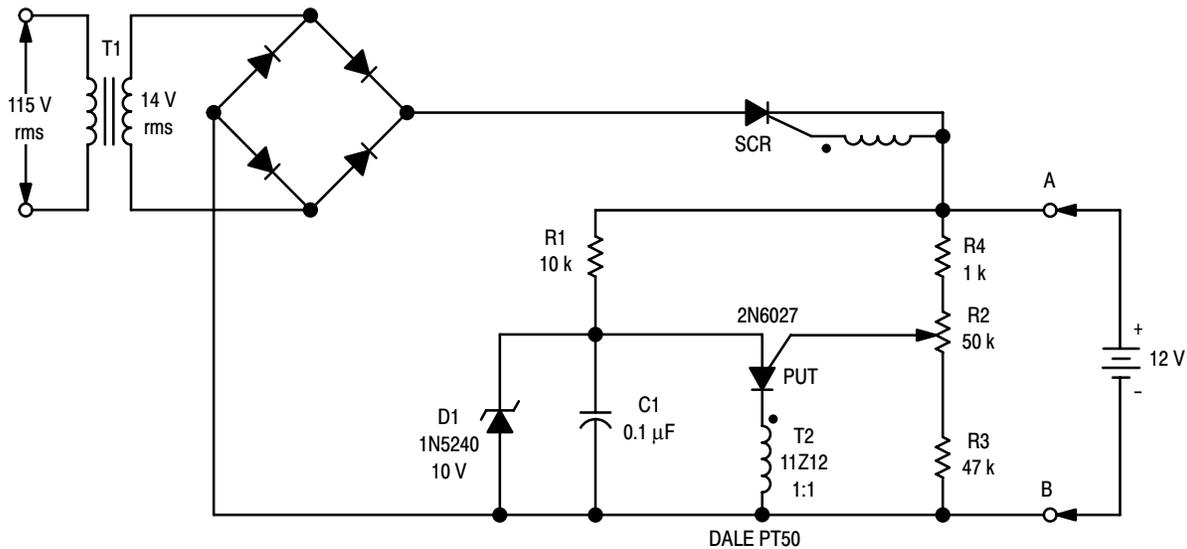
Figure 6.75. (a). 12-Volt Battery Charger
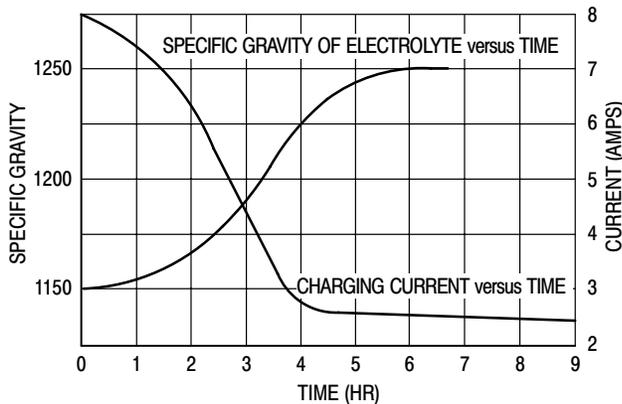
**Figure 6.75 (b) Charging Characteristics
of Battery Charger**

90 V rms VOLTAGE REGULATOR USING A PUT

The circuit of Figure 6.76 is an open loop rms voltage regulator that will provide 500 watts of power at 90 V rms with good regulation for an input voltage range of 110 – 130 V rms.

With the input voltage applied, capacitor C1 charges until the firing point of Q3 is reached causing it to fire. This turns Q5 on which allows current to flow through the load. As the input voltage increases, the voltage across R10 increases which increases the firing point of Q3. This delays the firing of Q3 because C1 now has to charge to a higher voltage before the peak-point voltage is reached. Thus the output voltage is held fairly constant by delaying the firing of Q5 as the input voltage increases. For a decrease in the input voltage, the reverse occurs.

Another means of providing compensation for increased input voltage is achieved by Q2 and the resistive divider formed by R6 and R7. As input voltage increases, the voltage at the base of Q2 increases causing Q2 to turn on harder which decreases the charging rate of C1 and further delays the firing of Q5.

To prevent the circuit from latching up at the beginning of each charging cycle, a delay network consisting of Q1 and its associated circuitry is used to prevent the current source from turning on until the trigger voltage has reached a sufficiently high level. This is achieved in the following way: Prior to the conduction of D2, the voltage on the base of Q1 is set by the voltage divider (R4 + R5)/(R1 + R3 + R4 + R5). This causes the base of Q1 to be more positive than the emitter and thus prevents Q1 from conducting until the voltage across R3 is sufficient to forward bias the base-emitter junction of Q1. This occurs when the line voltage has increased to about 15 volts.

The circuit can be operated over a different voltage range by changing resistors R6 and/or R4 which change the charging rate of C1.

Figure 6.76(b) provides a plot of output voltage and conduction angle versus input voltage for the regulator. As the figure indicates, good regulation can be obtained between the input voltage range of 110 to 130 volts.
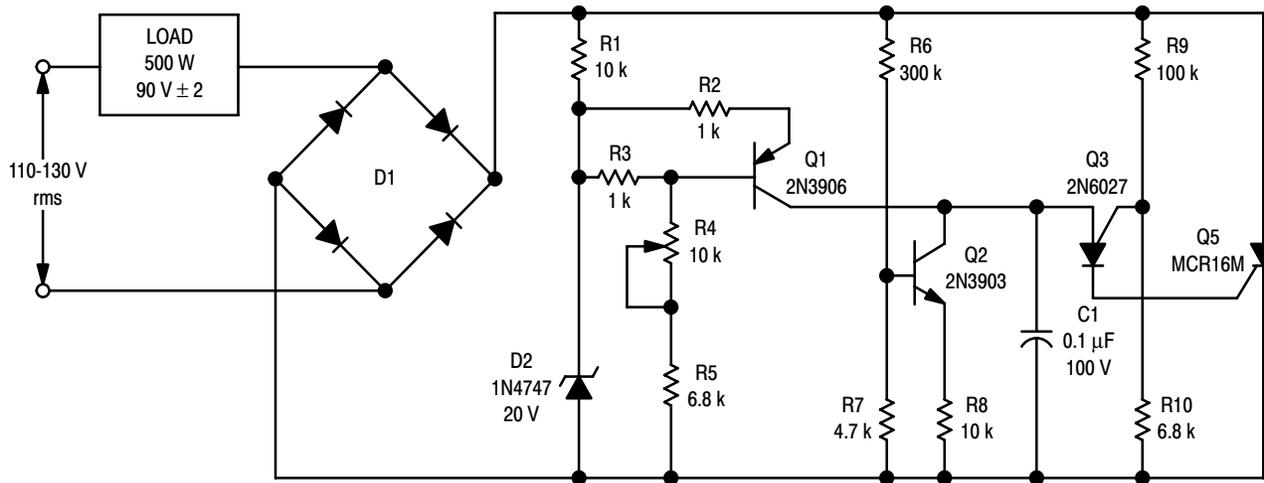
Figure 6.76. (a). rms Voltage Regulator
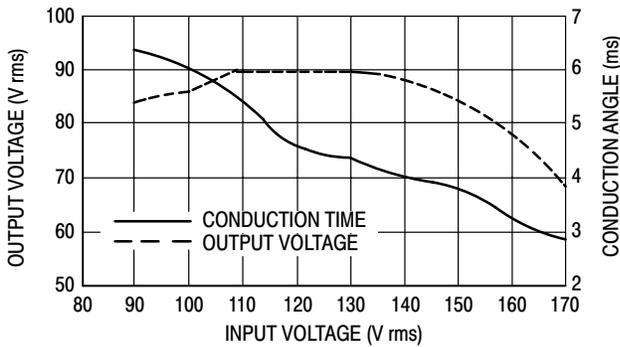
(b). Output Voltage and Conduction Angle versus Input Voltage

TRIAC ZERO-POINT SWITCH APPLICATIONS

BASIC TRIAC ZERO-POINT SWITCH

Figure 6.77 shows a manually controlled zero-point switch useful in power control for resistive loads. Operation of the circuit is as follows. On the initial part of the positive half cycle, the voltage is changing rapidly from zero causing a large current flow into capacitor C2. The current through C2 flows through R4, D3, and D4 into the gate of the TRIAC Q2 causing it to turn on very close to zero voltage. Once Q2 turns on, capacitor C3 charges to the peak of the line voltage through D5. When the line voltage passes through the peak, D5 becomes reverse-biased and C3 begins to discharge through D4 and the gate of Q2. At this time the voltage on C3 lags the line voltage. When the line voltage goes through zero there is still some charge on C3 so that when the line voltage starts negative C3 is still discharging into the gate of Q2. Thus Q2 is also turned on near zero on the negative half cycle. This operation continues for each cycle until switch S1 is closed, at which time SCR Q1 is turned on. Q1 shunts the gate current away from Q2 during each positive half cycle keeping Q2 from turning on. Q2 cannot turn on during the negative cycle because C3 cannot charge unless Q2 is on during the positive half cycle.

If S1 is initially closed during a positive half cycle, SCR Q1 turns on but circuit operation continues for the rest of the complete cycle and then turns off. If S1 is closed during a negative half cycle, Q1 does not turn on because it is reverse biased. Q1 then turns on at the beginning of the positive half cycle and Q2 turns off.

Zero-point switching when S1 is opened is ensured by the characteristic of SCR Q1. If S1 is opened during the positive half cycle, Q1 continues to conduct for the entire half cycle and TRIAC Q2 cannot turn on in the middle of the positive half cycle. Q2 does not turn on during the negative half cycle because C3 was unable to charge during the positive half cycle. Q2 starts to conduct at the first complete positive half cycle. If S1 is opened during the negative half cycle, Q2 again cannot turn on until the beginning of the positive half cycle because C3 is uncharged.

A 3-volt gate signal for SCR Q1 is obtained from D1, R1, C1, and D6.
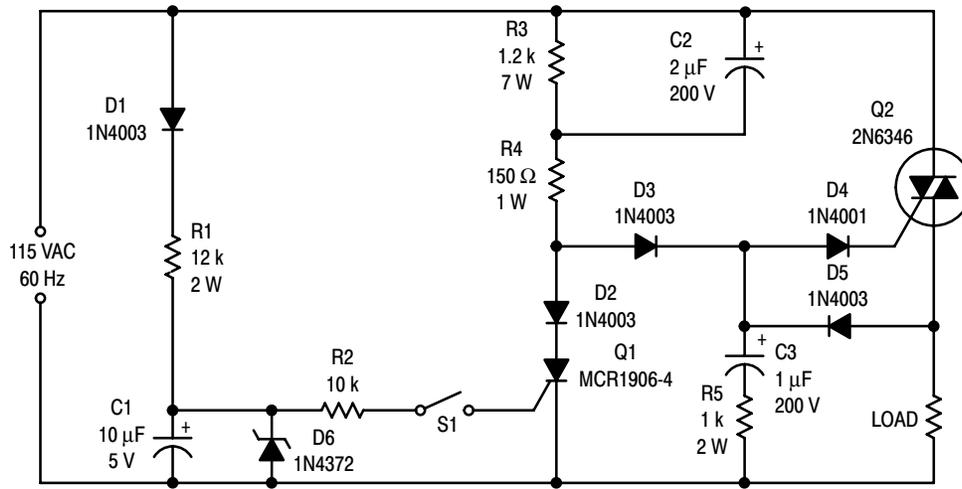
Figure 6.77. Zero-Point Switch

AN INTEGRATED CIRCUIT ZERO VOLTAGE SWITCH

A single CA3059/79 integrated circuit operating directly off the ac line provides the same function as the discrete circuit shown in Figure 6.77. Figure 6.78 shows its block diagram. The circuit operates a power triac in quadrants one and four, providing gate pulses synchronized to the zero voltage point of the ac cycle. This eliminates the RFI resulting from the control of resistive loads like heaters and flashing lamps. Table 6.12 specifies the value of the input series resistor for the operating line voltage. Figure 6.79 shows the pin connection for a typical application.
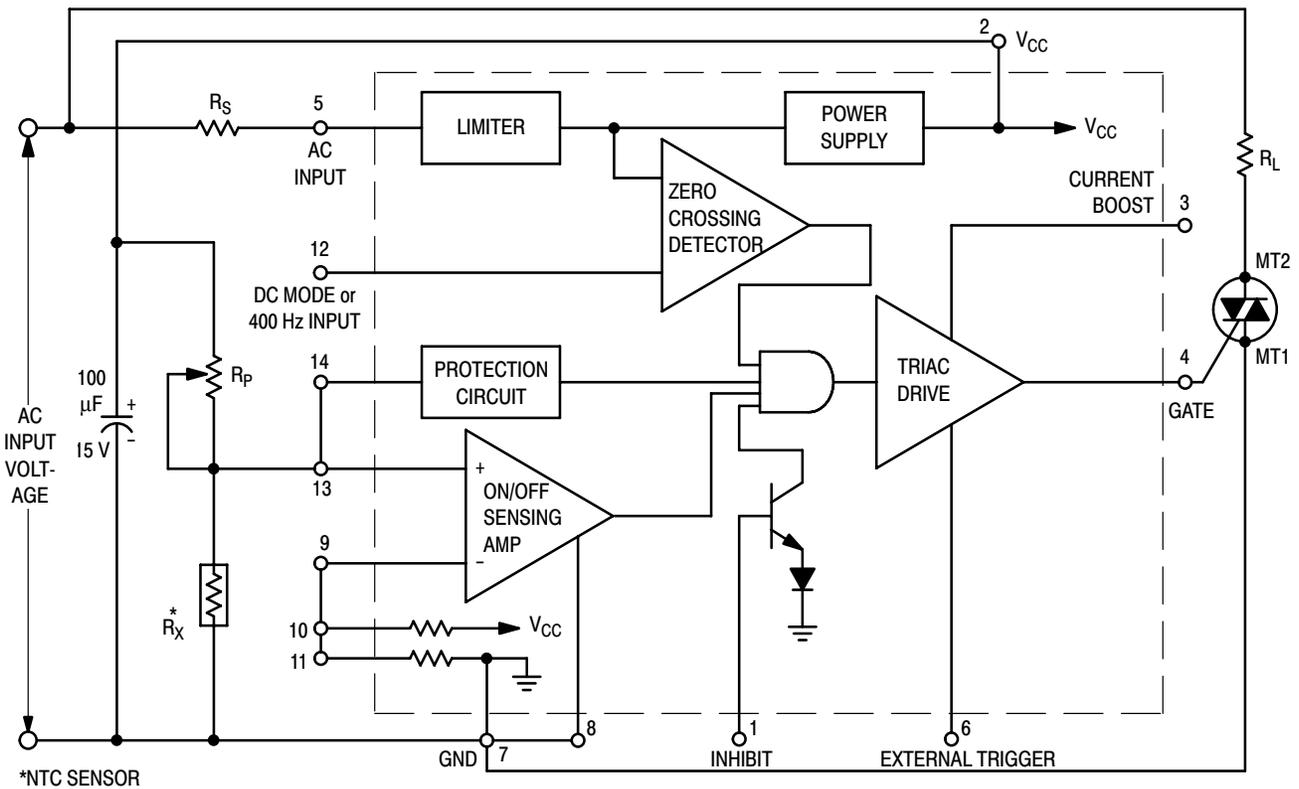
Figure 6.78. Functional Block Diagram
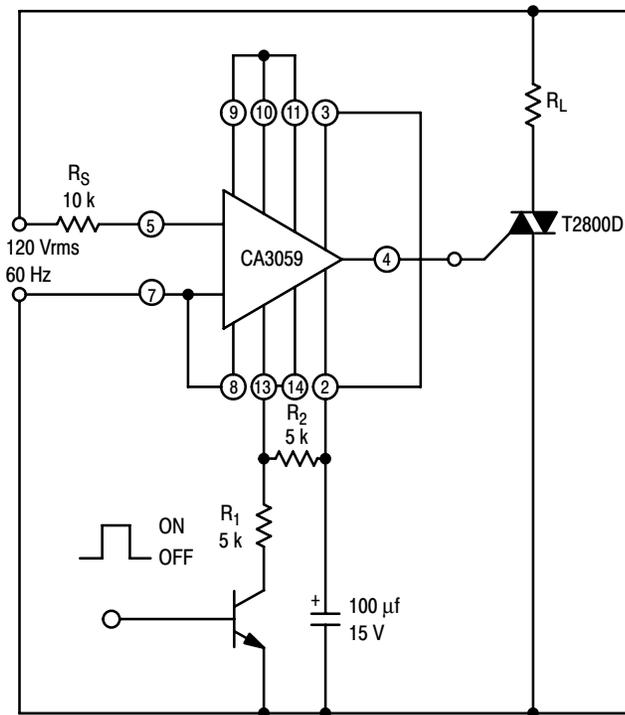
Figure 6.79. Zero Voltage Switch Using CA3059 Integrated Circuit

Table 6.12.

AC Input Voltage (50/60 Hz) vac	Input Series Resistor (R_S) kΩ	Dissipation Rating for R_S W
24	2.0	0.5
120	10	2.0
208/230	20	4.0
277	25	5.0

TEMPERATURE CONTROL WITH ZERO-POINT SWITCHING

ZERO VOLTAGE SWITCH PROPORTIONAL BAND TEMPERATURE CONTROLLER

Figure 6.80 shows the block diagram for the UAA1016B integrated circuit temperature controller. Figure 6.81 shows a typical application circuit. This device drives triacs with a zero voltage full wave technique allowing RFI free power regulation of resistive loads and adjustable burst frequency to comply with standards. It operates directly off the ac line triggers the triac in Q2 and Q3, is sensor fail-safe, and provides proportional temperature control over an adjustable band. Consult the device data sheet (DS9641) for detailed information.
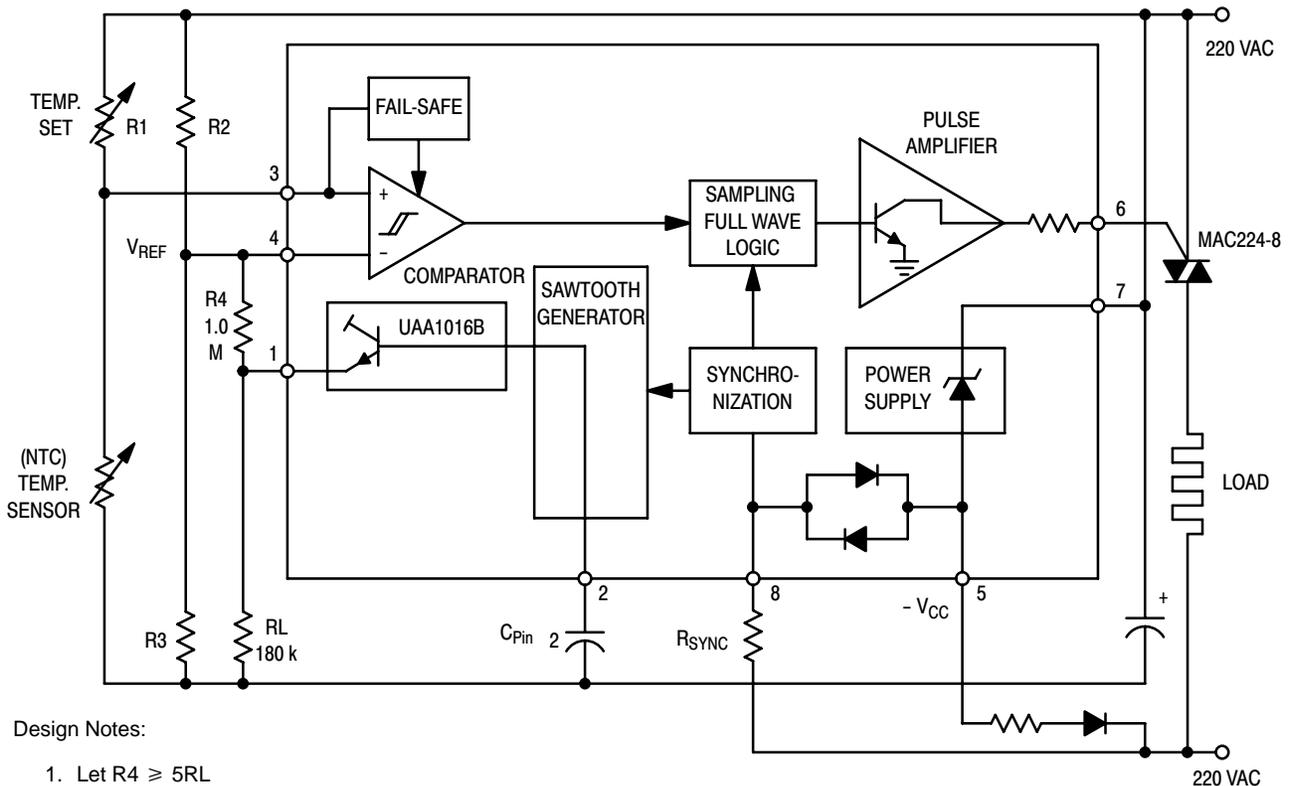
Design Notes:

1. Let R4 ≥ 5RL

2. Select $\dfrac{R2}{R3}$ Ratio for a symmetrical reference deviation centered about Pin 1 output swing, R2 will be slightly greater than R3.

3. Select R2 and R3 values for the desired reference deviation where $\Delta V_{REF} = \dfrac{\Delta V_{Pin\,1}}{\dfrac{R4}{R2 \,||\, R3} + 1}$

Figure 6.80. UA1016B Block Diagram and Pin Assignment
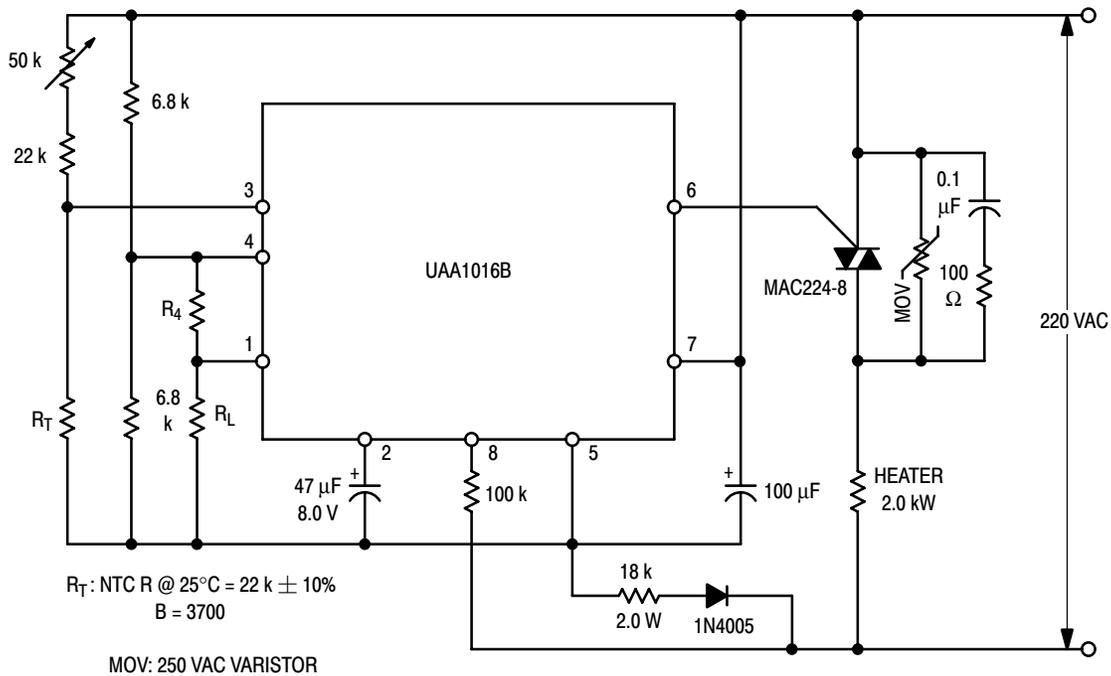
Figure 6.81. Application Circuit — Electric Radiator with Proportional Band Thermostat, Proportional Band 1°C at 25°C

TRIAC RELAY-CONTACT PROTECTION

A common problem in contact switching high current is arcing which causes erosion of the contacts. A solution to this problem is illustrated in Figure 6.82. This circuit can be used to prevent relay contact arcing for loads up to 50 amperes.

There is some delay between the time a relay coil is energized and the time the contacts close. There is also a delay between the time the coil is de-energized and the time the contacts open. For the relay used in this circuit both times are about 15 ms. The TRIAC across the relay contacts will turn on as soon as sufficient gate current is present to fire it. This occurs after switch S1 is closed but before the relay contacts close. When the contacts close, the load current passes through them, rather than through the TRIAC, even though the TRIAC is receiving gate current. If S1 should be closed during the negative half cycle of the ac line, the TRIAC will not turn on immediately but will wait until the voltage begins to go positive, at which time diode D1 conducts providing gate current through R1. The maximum time that could elapse before the TRIAC turns on is 8-1/3 ms for the 60 Hz supply. This is adequate to ensure that the TRIAC will be on before the relay contact closes. During the positive half cycle, capacitor C1 is charged through D1 and R2. This stores energy in the capacitor so that it can be used to keep

the TRIAC on after switch S1 has been opened. The time constant of R1 plus R2 and C1 is set so that sufficient gate current is present at the time of relay drop-out after the opening of S1, to assure that the TRIAC will still be on. For the relay used, this time is 15 ms. The TRIAC therefore limits the maximum voltage, across the relay contacts upon dropout to the TRIAC's voltage drop of about 1 volt. The TRIAC will conduct until its gate current falls below the threshold level, after which it will turn off when the anode current goes to zero. The TRIAC will conduct for several cycles after the relay contacts open.

This circuit not only reduces contact bounce and arcing but also reduces the physical size of the relay. Since the relay is not required to interrupt the load current, its rating can be based on two factors: the first is the rms rating of the current-carrying metal, and the second is the contact area. This means that many well-designed 5 ampere relays can be used in a 50 ampere load circuit. Because the size of the relay has been reduced, so will the noise on closing. Another advantage of this circuit is that the life of the relay will be increased since it will not be subjected to contact burning, welding, etc.

The RC circuit shown across the contact and TRIAC (R3 and C2) is to reduce dv/dt if any other switching element is used in the line.
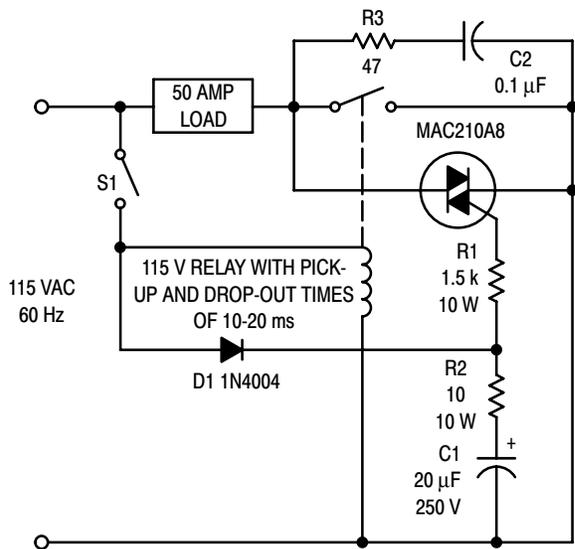
Figure 6.82. TRIAC Prevents Relay Contact Arcing

AN AUTOMATIC AC LINE VOLTAGE SELECTOR USING THE MC34161 AND A TRIAC

Line operated switching regulators run off of 120 or 240 VAC by configuring the main reservoir input capacitor filter as a full-wave doubler or full-wave bridge. This integrated circuit provides the control signals and triggering for a TRIAC to automatically provide this function.

Channel 1 senses the negative half cycles of the AC line voltage. If the line voltage is less than 150 V, the circuit will switch from bridge mode to voltage doubling mode after a preset time delay. The delay is controlled by the 100 kΩ resistor and the 10 µF capacitor. If the line voltage is greater than 150 V, the circuit will immediately return to fullwave bridge mode.
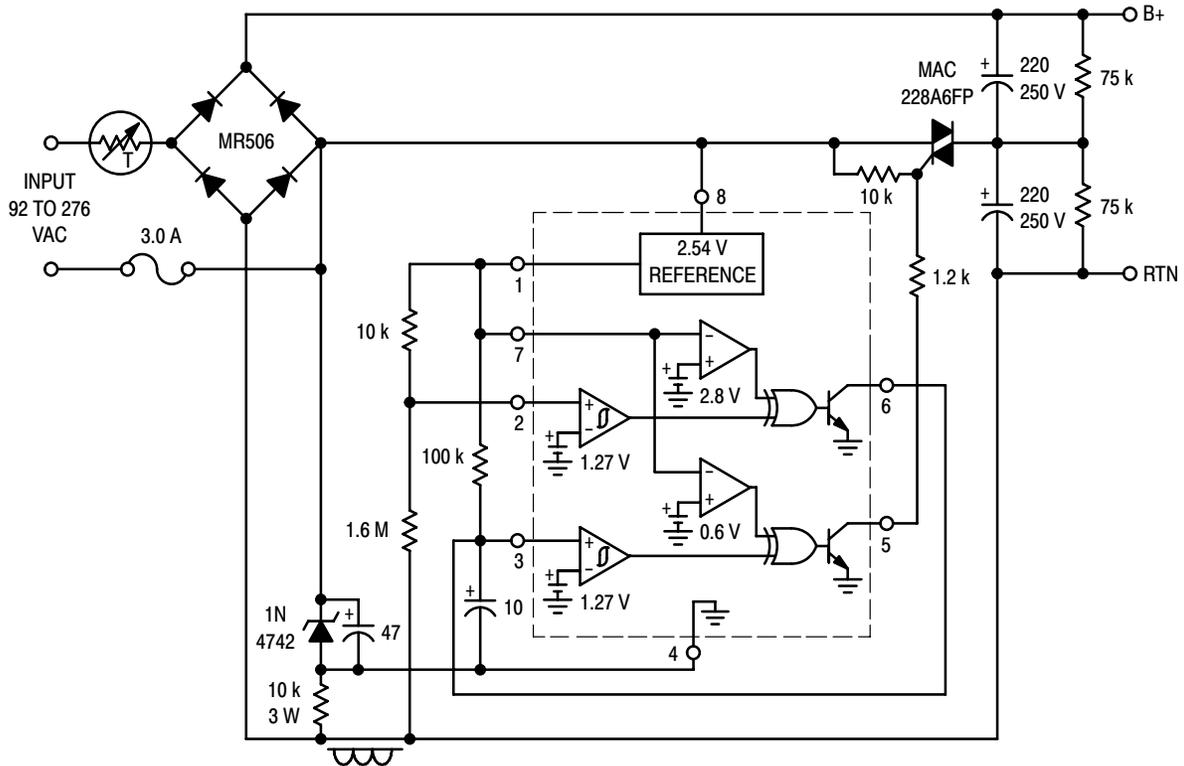
Figure 6.83. Automatic AC Line Voltage Selector

AN1045/D

Series Triacs
In AC High Voltage
Switching Circuits

By George Templeton
Thyristor Applications Engineer

ON Semiconductor

http://onsemi.com

APPLICATION NOTE

INTRODUCTION

Edited and Updated

This paper describes the series connection of triacs to create a high voltage switch suitable for operation at voltages up to 2000 Volts. They can replace electromechanical contactors or extend their current rating and lifetime. Motor starters and controllers operating at line voltages of 240 Volts or more require high-voltage switches. Transformer action and resonant snubber charging result in voltages much greater than the peak of the line. Triacs can be subjected to both commutating and static dV/dt when multiple switching devices are present in the circuit. Snubber designs to prevent static dV/dt turn-on result in higher voltages at turn-off. Variable load impedances also raise voltage requirements.

The benefits of series operation include: higher blocking voltage, reduced leakage, better thermal stability, higher dV/dt capability, reduced snubber costs, possible snubberless operation, and greater latitude in snubber design. The advantages of triacs as replacements for relays include:

- Small size and light weight
- Safety — freedom from arcing and spark initiated explosions
- Long lifespan — contact bounce and burning eliminated
- Fast operation — turn-on in microseconds and turn-off in milliseconds
- Quiet operation

Triacs can be used to replace the centrifugal switch in capacitor start motors. The blocking voltage required of the triac can be much greater than the line voltage would suggest. It must block the vector sum of the line, auxiliary winding, and start capacitor voltage. This voltage increases when triac turn-off occurs at higher rpm.

TRIGGERING

Figure 1 illustrates a series thyristor switching circuit. In this circuit, the top triac triggers in Quadrant 1 when the bottom triac triggers in Quadrant 3. When the optocoupler turns on, gate current flows until the triacs latch. At that time, the voltage between the gate terminals drops to about 0.6 Volts stopping the gate current. This process repeats each half cycle. The power rating of the gate resistor can be small because of the short duration of the gate current. Optocoupler surge or triac gate ratings determine the minimum resistance value. For example, when the maximum optocoupler I_{TSM} rating is 1 A:

$$R_g >= V_{peak}/I_{max} \qquad (1.0)$$
$$R_g = 750\,V/1\,A = 750\,Ohm$$

The triacs retrigger every half cycle as soon as the line voltage rises to the value necessary to force the trigger current. The instantaneous line voltage V is

$$V = I_{GT}\,R_g + 2\,V_{GT} + 2\,V_{TM} \qquad (1.1)$$

where V_{GT}, I_{GT} are data book specifications for the triac and V_{TM} is the on-voltage specification for the optocoupler.

The phase delay angle is

$$\theta_d = SIN^{-1}\left[\frac{V}{\sqrt{2}\;V_{LINE}}\right] \qquad (1.2)$$

Figure 6.1. Series Switch

Figure 6.2. Designing for Probable Leakage
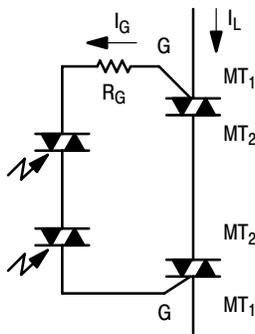
STATIC VOLTAGE SHARING

Maximum blocking voltage capability results when the triacs share voltage equally. The blocking voltage can be dc or ac. A combination of both results when the triac switches the start winding in capacitor start motors. In the simple series connection, both triacs operate with an identical leakage current which is less than that of either part operated alone at the same voltage. The voltages across the devices are the same only when their leakage resistances are identical. Dividing the voltage by the leakage current gives the leakage resistance. It can range from 200 kohm to 2000 megohm depending on device characteristics, temperature, and applied voltage.

Drawing a line corresponding to the measured series leakage on each device's characteristic curve locates its operating point. Figure 3a shows the highest and lowest leakage units from a sample of 100 units. At room temperature, a leakage of 350 nA results at 920 Volts. The lowest leakage unit blocks at the maximum specified value of 600 Volts, while the highest blocks 320 Volts. A 50 percent boost results.

Figure 3b shows the same two triacs at rated $T_J$max. The magnitude of their leakage increased by a factor of about 1000. Matching between the devices improved, allowing operation to 1100 Volts without exceeding the 600 Volt rating of either device.

Identical case temperatures are necessary to achieve good matching. Mounting the devices closely together on a common heatsink helps.

A stable blocking condition for operation of a single triac with no other components on the heatsink results when

$$\frac{dI_{MT}}{dT_J} \cdot \frac{dT_J}{dP_J} \cdot \frac{dP_J}{dI_{MT}} < 1 \qquad (2.0)$$

Thermal run-away is a regenerative process which occurs whenever the loop gain in the thermal feedback circuit reaches unity. An increase in junction temperature causes increased leakage current and higher power dissipation. Higher power causes higher junction temperature which in turn leads to greater leakage. If the rate of heat release at the junction exceeds the rate of removal as temperature increases, this process repeats until the leakage current is sufficient to trigger the thyristor on.
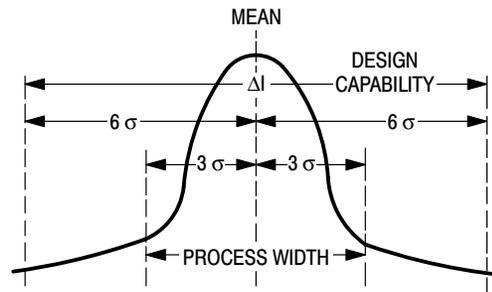
DC blocking simplifies analysis. A design providing stable dc operation guarantees ac performance. AC operation allows smaller heatsinks.

The last term in the stability equation is the applied voltage when the load resistance is low and the leakage causes negligible voltage drop across it. The second term is the thermal resistance from junction to ambient. The first term describes the behavior of leakage at the operating conditions. For example, if leakage doubles every 10°C, a triac operating with 2 mA of leakage at 800 Vdc with a 6°C/W thermal resistance is stable because

$$\frac{2\ mA}{10°C} \cdot \frac{6°C}{W} \cdot 800\ V \ = \ 0.96$$

Operating two triacs in series improves thermal stability. When two devices have matched leakages, each device sees half the voltage and current or 1/4 of the power in a single triac. The total leakage dissipation will approach half that of a single device operated at the same voltage. The additional voltage margin resulting from the higher total blocking voltage reduces the chance that either device will operate near its breakdown voltage where the leakage current increases rapidly with small increments in voltage. Higher voltage devices have lower leakage currents when operated near breakdown. Consequently, the highest breakover voltage unit in the pair will carry the greatest proportion of the burden. If the leakage current is large enough to cause significant changes in junction temperature, $(\Delta T_J = \phi_{JC}\ P_D)$, the effect will tend to balance the voltage division between the two by lowering the leakage resistance of the hotter unit. If the leakage mismatch between the two is large, nearly all the voltage will drop across one device. As a result there will be little benefit connecting two in series.

Series blocking voltage depends on leakage matching. Blocking stability depends on predictable changes in leakage with temperature. Leakage has three components.
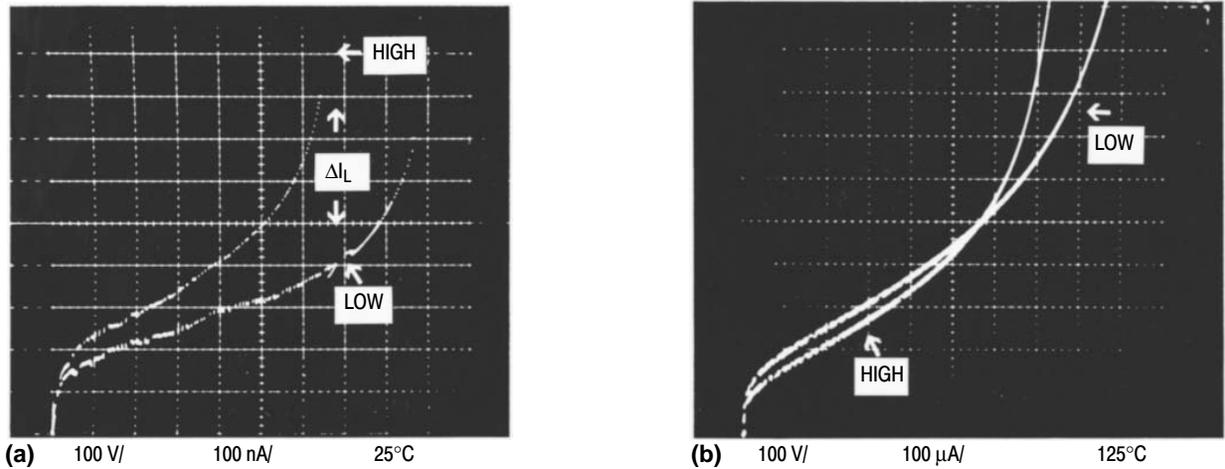
Figure 6.3. Leakage Matching versus Temperature

Surface Leakage

Passivation technique, junction design, and cleanliness determine the size of this component. It tends to be small and not very dependent on temperature.

Diffusion Leakage

Measurements with 1 volt reverse bias show that this component is less than 10 percent of the total leakage for allowed junction temperatures. It follows an equation of the form:

$$I \propto e^{-(qv/kT)} \qquad (2.1)$$

and doubles about every 10°C. Its value can be estimated by extrapolating backward from high temperature data points.

Depletion Layer Charge Generation

This component is a result of carriers liberated from within the blocking junction depletion layer. It grows with the square root of the applied voltage. The slope of the leakage versus applied voltage is the mechanism allowing for series operation with less than perfect leakage matching. Predictable diffusion processes determine this leakage. At temperatures between 70 and 150°C it is given by:

$$i \propto e^{-\frac{E}{kT}} \qquad (2.2)$$

where E = 1.1 eV, k = 8.62E − 5 eV/k, T = degrees Kelvin, and k = 8.62 x 10^{-5} eV/k.

It is useful to calculate the percentage change in leakage current with temperature:

$$A = \frac{1}{i}\frac{di}{dT_J} = \frac{E}{kT^2} = 0.08 = \frac{8\%}{°C}$$

The coefficient A was evaluated on 3 different die size triacs by curve fitting to leakage measurements every 10°

from 70 to 150°C. Actual values measured 0.064 at 125° and 0.057 at 150°.

Deviations from this behavior will result at voltages and temperatures where leakage magnitude, current gain, and avalanche multiplication aid unwanted turn-on. Sensitive gate triacs are not recommended for this reason.

DERATING AND LEAKAGE MATCHING

Operation near breakdown increases leakage mismatch because of the effects of avalanche multiplication. For series operation, devices should be operated at least 100 Volts below their rating.
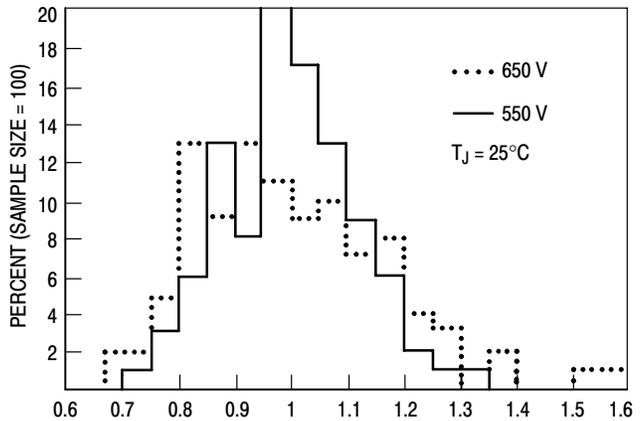
Figure 6.4. Normalized Leakage (Mean = 1.0)

Figure 4 shows the leakage histogram for a triac sample operated at two different voltages. The skewedness in the high-voltage distribution is a consequence of some of the sample operating near breakdown.

HEATSINK SELECTION

Solving equations (2.0) and (2.3) for the thermal resistance required to prevent runaway gives:

$$\theta_{JA} < \frac{1}{A \cdot V \cdot i} \qquad (3.0)$$

where θ_{JA} is thermal resistance, junction to ambient, in °C/W, A = 0.08 at T_J = 125°C, V = rated V_{DRM}, and i = rated I_{DRM}.

θ_{JA} must be low enough to remove the heat resulting from conduction losses and insure blocking stability. The latter can be the limiting factor when circuit voltages are high. For example, consider a triac operated at 8 amps (rms) and 8 Watts. The allowed case temperature rise at 25° ambient is 85°C giving a required θ_{CA} (thermal resistance, case to ambient) of 10.6°C/W. Allowing 1°C/W for θ_{CHS} (thermal resistance, case to heatsink) leaves 9.6°C/W for θ_{SA} (thermal resistance, heatsink to ambient). However, thermal stability at 600 V and 2 mA I_{DRM} requires θ_{JA} = 10.4°C/W. A heatsink with θ_{SA} less than 7.4°C/W is needed, given a junction to case thermal resistance of 2°C/W.

The operation of devices in series does not change the coefficient A. When matching and thermal tracking is perfect, both devices block half the voltage. The leakage current and power divide by half and the allowed θ_{JA} for blocking stability increases by 4.

Low duty cycles allow the reduction of the heatsink size. The thermal capacitance of the heatsink keeps the junction temperature within specification. The package time constant ($C_{pkg} R_{\theta JA}$) is long in comparison with the thermal response time of the die, causing the instantaneous T_J to rise above the case as it would were the semiconductor mounted on an infinite heatsink. Heatsink design requires estimation of the peak case temperature and the use of the thermal derating curves on the data sheet. The simplest model applies to a very small heatsink which could be the semicondutor package itself. When θ_{SA} is large in comparison with θ_{CHS}, it is sufficient to lump both the package and heatsink capacitances together and treat them as a single quantity. The models provide good results when the heatsink is small and the thermal paths are short.

Model C, Figure 5 is a useful simplification for low duty cycle applications. Increasing heatsink mass adds thermal capacitance and reduces peak junction temperature. Heatsink thermal resistance is proportional to surface area and determines the average temperature.

$$\theta_{SA} = 32.6\, A^{(-0.47)} \qquad (3.1)$$

where A = total surface area in square inches, θ_{SA} = thermal resistance sink to ambient in °C/W.

Analysis of heatsink thermal response to a train of periodic pulses can be treated using the methods in ON Semiconductor application note AN569 and Figure 6. For example:
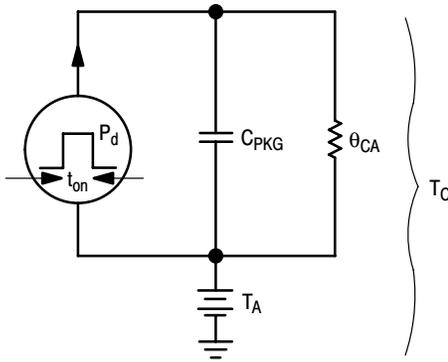
(a.) Standard Thermal Analogue For a Thyristor in Free Air

(b.) Equivalent Circuit For (a)

In Circuit (B):

The steady state case temperature is given by

(5.0) $\qquad T_{CSS} = P_d \theta_{CA} + T_A$ in $^\circ$C

where P_d = Applied average power, watts

$\qquad \theta_{CA}$ = Case to ambient thermal resistance, $^\circ$C/W

$\qquad T_A$ = ambient temperature, $^\circ$C

The package rises toward the steady state temperature exponentially with time constant

(5.1) $\qquad \tau = \theta_{CA} C_{PKG}$, seconds

where C_{pkg} = HM, Joules/$^\circ$C

$\qquad$ H = Specific heat, calories/(gm • $^\circ$C)

$\qquad$ M = Mass in grams

and $\quad$ 1 Calorie = 4.184 Joule

$\qquad$ 1 Joule = 1 Watt • Sec

The case temperature rise above ambient at the end of power pulse is:

(5.2) $\qquad \Delta T_{C_{pk}} = \Delta T_{CSS}(1 - e^{-t_{on}/\tau})$

where $\Delta T_{C_{pk}} = T_{C_{pk}} - T_A$

$\Delta T_{CSS} = T_{CSS} - T_A$

To account for thermal capacity, a time dependent factor r(t) is applied to the steady state case-to-ambient thermal resistance. The package thermal resistance, at a given on-time, is called transient thermal resistance and is given by:

$\qquad R_{\theta CA}$ (ton) = r(ton) θ_{CA}

where r(t$_{on}$) = Unitless transient thermal impedance coefficient.
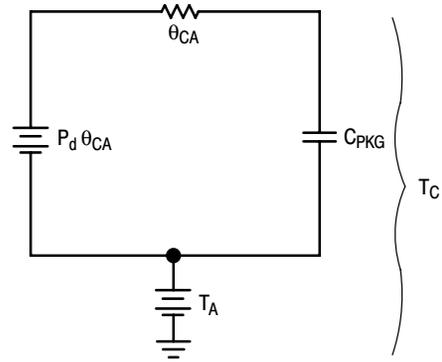
In terms of measurable temperatures:

(5.3) $\qquad r(t_{on}) = \dfrac{\Delta T_{C_{pk}}}{\Delta T_{CSS}}$

In model (b.) this is

(5.4) $\qquad r(t_{on}) = (1 - e^{-t_{on}/\tau})$

Solving 5-4 for the package capacitance gives

(5.5) $\qquad C_{PKG} = \dfrac{-t_{on}}{(\theta_{CA} \ln (1 - r(t_{on}))}$

Use simplified model C when

$t_{on} << \tau$

$\Delta T_{C_{pk}} << \Delta T_{CSS}$
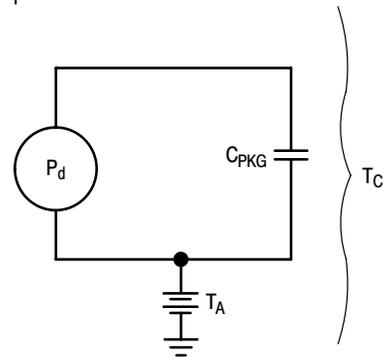
(c.) Simplified Model

(5.6) $T_C = \dfrac{P_d t_{on}}{C_{PKG}} + T_A$

Figure 6.5. Transient Thermal Response For a Single Power Pulse

Assume the case temperature changes by 40°C for a single power pulse of 66.67 W and 3 s duration. Then from equation (5.6):

$$C_{pkg} = \frac{(66.7 \text{ Watts}) (3 \text{ seconds})}{40°C} = \frac{5 \text{ Joules}}{°C}$$

The heatsink thermal resistance can be determined by applying dc power, measuring the final case temperature, and using equation (5.0).

$$\frac{T_C - T_A}{P_D} = \frac{175\text{-}25}{5} = 30°C/W$$

The application requires a 3 s on-time and 180 s period at 66.7 W. Then

$$P_{avg} = (66.7 \text{ W}) (3/180) = 1.111 \text{ W}$$

$$\Delta T_C (N + 1) = [P_{AVG} + (P_d - P_{AVG}) \, r(t_{on} + t_p) + P_d \, r(t_{on}) - P_d \, r(t_p)]\theta_{CA}$$

Where $\Delta T_C (N + 1)$ = maximum rise above ambient
P_d = applied average power within a pulse
P_{AVG} = average power within a period
$r(t_{on} + t_p)$ = time dependent factor for sum of t_{on} and t_p
$r(t_{on})$ = time dependent factor for t_{on}
$r(t_p)$ = time dependent factor for t_p
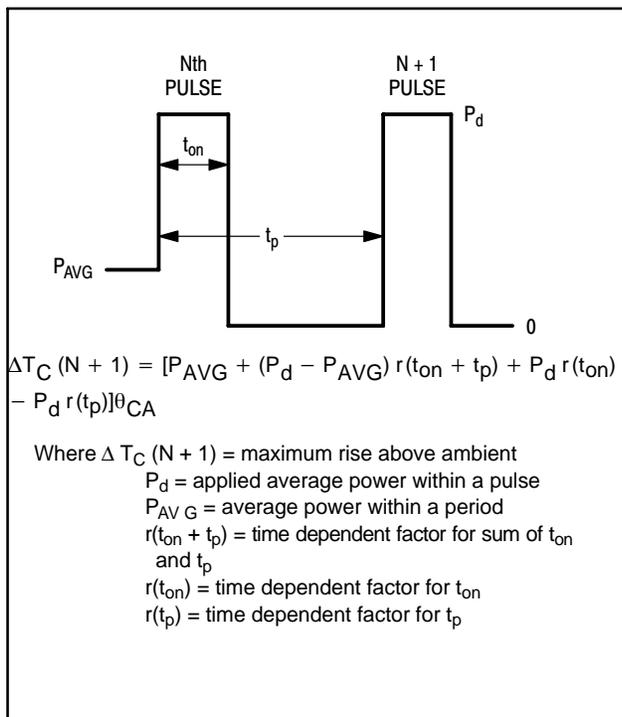
Figure 6.6. Steady State Peak Case Temperature Rise

Using equation (5.3), the theoretical steady state case temperature rise is:

$$T_{CSS} - T_A = (66.7 \text{ W}) (30°C/W) = 2000°C$$

and

$$R(t_{on}) = R (3 \text{ s}) = (40°C \text{ measured rise})/2000 = 0.02$$

From equation (5.4) and (5.1):

$$R (T_p) = (1 - e^{-180/150}) = .6988$$

$$R (t_{on} + T_p) = (1 - 1^{-183/150}) = .7047$$

Then from Figure 6:
delta T_C = (1.111 + 46.225 + 1.333 − 46.61) 30 = 61.8°C
If the ambient temperature is 25°C, T_C = 87°C.

COMPENSATING FOR MAXIMUM SPECIFIED LEAKAGE

Identical value parallel resistors around each triac will prevent breakdown resulting from mismatched leakages. Figure 7 derives the method for selecting the maximum allowed resistor size. A worst case design assumes that the series pair will operate at maximum T_J and that one of the triacs leaks at the full specified value while the other has no leakage at all. A conservative design results when the tolerances in the shunt resistors place the highest possible resistor across the low leakage unit and the lowest possible resistor around the high leakage unit.

This method does not necessarily provide equal voltage balancing. It prevents triac breakover. Perfect voltage sharing requires expensive high-wattage resistors to provide large bleeder currents.

$$V_1 = \frac{V_S R_1}{R_1 + R_2} + \frac{\Delta I_L R_1 R_2}{R_1 + R_2}$$

Let $R_1 = R (1 + p)$ and $R_2 = R (1 - p)$ where
  R = Nominal resistor value
  p = 0.05 for 5% tolerance, etc.

$$R \le \frac{2 \, V_{DRM} - V_S (1 + p)}{\Delta I_L (1 - p^2)}$$

Worst case becomes:

and $I_{DRM} (T_1) = 0$; $I_{DRM} (T_2)$ = Spec. max. value
  ΔI_L = Spec. Max. Value
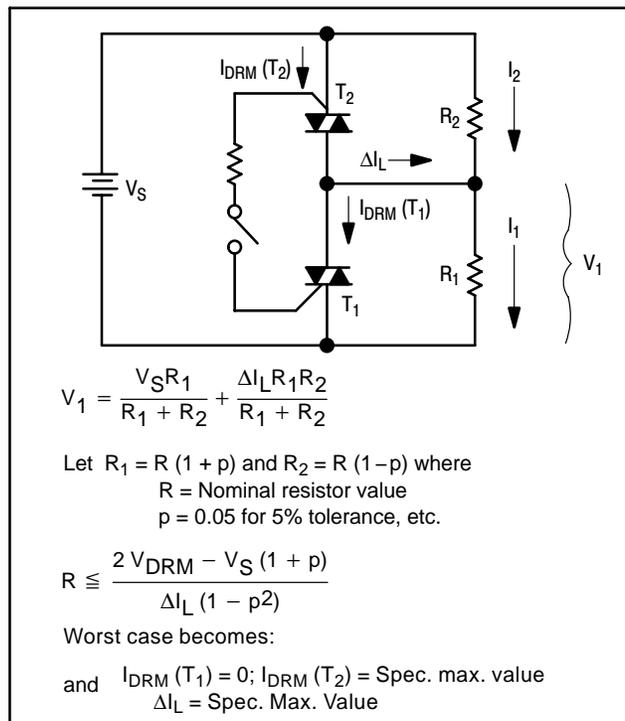
Figure 6.7. Maximum Allowed Resistor for Static Voltage Sharing

COMPENSATION FOR PROBABLE LEAKAGE

Real triacs have a leakage current greater than zero and less than the specified value. Knowledge of the leakage distribution can be used to reduce resistor power requirements. The first step is to statistically characterize the product at maximum temperature. Careful control of the temperature is critical because leakage depends strongly on it.

The process width is the leakage span at plus or minus 3 standard deviations (sigma) from the mean. To minimize the probability of out of spec parts, use a design capability index (Cp) of 2.0.

$$C_p = (design\ \Delta I)/(process\ width) \qquad (4.0)$$
$$Cp = (12\ sigma)/(6\ sigma)$$

Figure 2 and Figure 7 describe this. Substituting delta I_L at 6 sigma in Figure 7 gives the resistor value. The required power drops by about 4.

Theoretically there would be no more than 3.4 triacs per million exceeding the design tolerance even if the mean value of the leakage shifted by plus or minus 1.5 sigma.

SELECTING RESISTORS

Small resistors have low voltage ratings which can impose a lower constraint on maximum voltage than the triac. A common voltage rating for carbon resistors is:

Rated Power (W)	Maximum Voltage (V)
1/4 Watt	250 Volts
1/2	350
1	500
2	750

Series resistors are used for higher voltage.

Let $V_{DRM} = E \dfrac{R_{max}}{R_{max} + R_{min}}$

$E = V_{DRM} \left(1 + \dfrac{I_{min}}{I_{max}} \right)$

$R_{max} = \dfrac{V_{DRM}}{I_{min}} \qquad R_{min} = \dfrac{V_{DRM}}{I_{max}} \qquad (8.0)$

(a) Equivalent Circuit   **(b) Model**
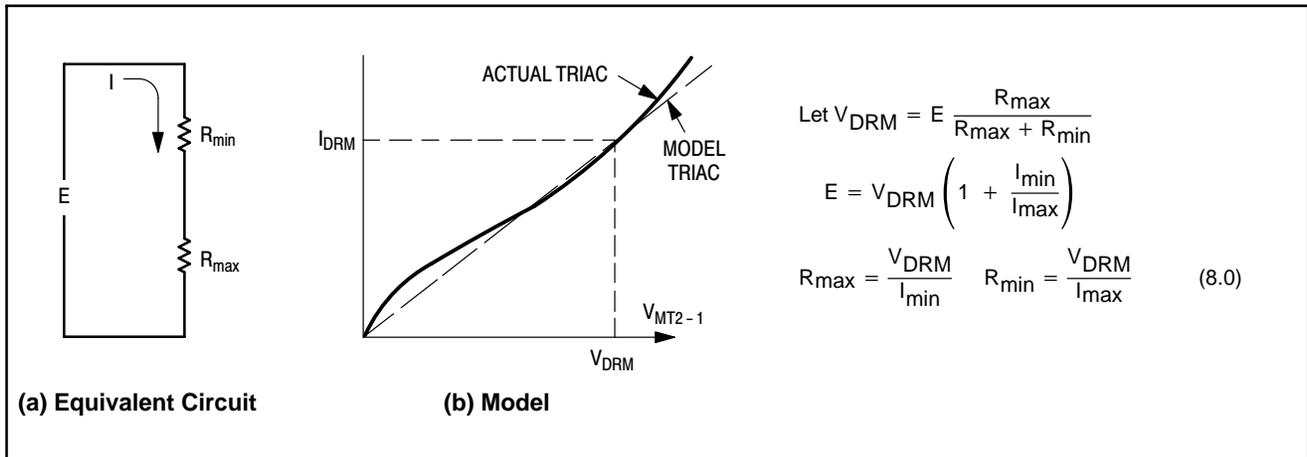
Figure 6.8. Maximum Voltage Sharing Without Shunt Resistor

OPERATION WITHOUT RESISTORS

Figure 8 derives the method for calculating maximum operating voltage. The voltage boost depends on the values of I_{min} and I_{max}. For example :

$$\left(1 + \frac{131\ \mu A}{683\ \mu A} \right) = 1.19$$

A 19 percent voltage boost is possible with the 6 sigma design. Testing to the measured maximum and minimum of the sample allows the boost to approach the values given in Table 1.

$$(1 + 0.835/1.228) = 1.68$$

Table 1. Normalized leakage and voltage boost factor.
(Mean = 1.0)

Voltage (V)	550	650	550	550	550	550	550
T_J (°C)	25	25	100	125	125	150	150
R_{shunt}	—	—	—	—	1.5M	1.5M	510K
Sample Size	100	100	16	16	16	16	16
Maximum	1.315	1.591	1.187	1.228	1.123	1.346	1.186
Minimum	0.729	0.681	0.840	0.835	0.920	0.820	0.877
Sigma	0.116	0.172	0.106	0.113	0.055	0.132	0.084
Sample Boost	1.55	1.43	1.71	1.68	1.82	1.61	1.74
6 Sigma Boost	1.18	1.00	1.22	1.19	1.50	1.12	1.33

COMPENSATING FOR SURFACE LEAKAGE

A small low power shunt resistance will provide nearly perfect low temperature voltage sharing and will improve high temperature performance. It defines the minimum leakage current of the parallel triac-resistor combination. The design method in Figure 8 can be used by adding the resistor current to the measured maximum and minimum leakage currents of the triac sample. This is described in Table 1.

SERIES $\left(\dfrac{dV}{dt}\right)_S$

The series connection will provide twice the $\left(\dfrac{dV}{dt}\right)_S$ capability of the lowest device in the pair (Figure 9).

Dynamic matching without a snubber network depends on equality of the thyristor self capacitance. There is little variation in junction capacitance. Device gain variations introduce most of the spread in triac performance.

The blocking junction capacitance of a thyristor is a declining function of dc bias voltage. Mismatch in static blocking voltage will contribute to unequal capacitances. However, this effect is small at voltages beyond a few volts. The attachment of a heatsink at the high-impedance node formed by connection of the triac main-terminals can also contribute to imbalance by introducing stray capacitance to ground. This can be made insignificant by adding small capacitors in parallel with the triacs. Snubbers will serve the same purpose.
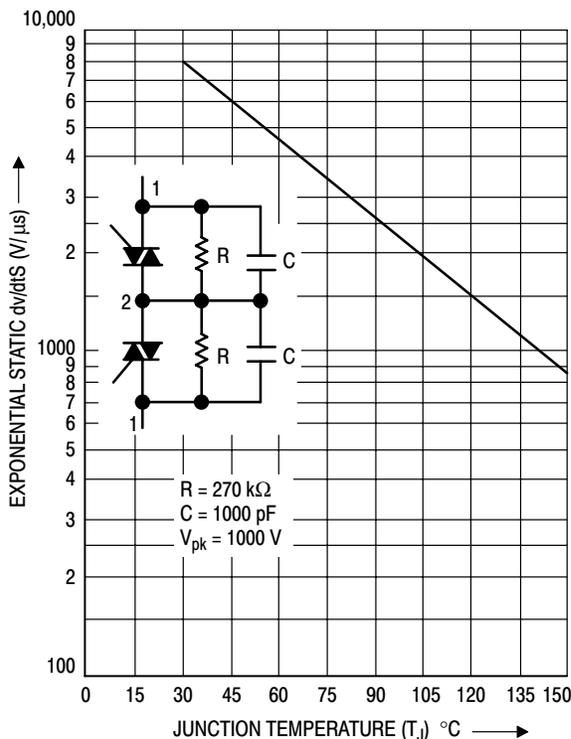
Figure 6.9. Exponential Static dV/dt, Series MAC15-8 Triacs

Triacs can tolerate very high rates of voltage rise when the peak voltage magnitude is below the threshold needed to trigger the device on. This behavior is a consequence of the voltage divider action between the device collector and gate-cathode junction capacitances. If the rise-time is made short in comparison with minority carrier lifetime, voltage and displaced charge determine whether the device triggers on or not. Series operation will extend the range of voltage and load conditions where a static $\dfrac{dV}{dt}$ snubber is not needed.

Figure 10 graphs the results of measurements on two series connected triacs operated without snubbers. The series connection doubled the allowed step voltage. However, this voltage remained far below the combined 1200 V breakover voltage of the pair.
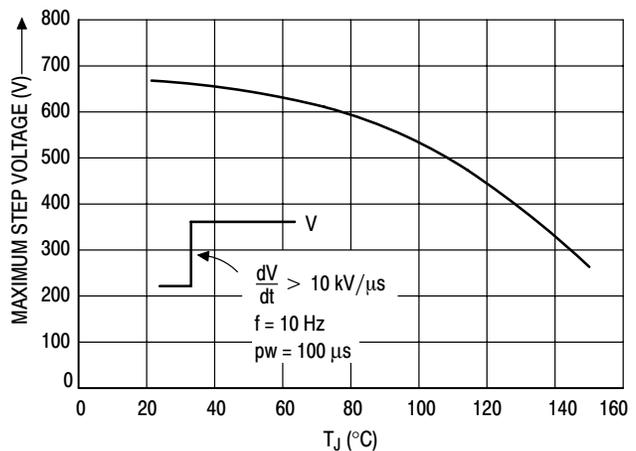
Figure 6.10. Step Blocking Voltage V_S T_J (Unsnubbed Series Triacs)

Exponential $\left(\dfrac{dV}{dt}\right)_S$ tests performed at 1000 V and less than 2 kV/μs showed that turn-on of the series pair can occur because of breakdown or $\dfrac{dV}{dt}$. The former was the limiting factor at junction temperatures below 100°C. Performance improved with temperature because device gain aided voltage sharing. The triac with the highest current gain in the pair is most likely to turn-on. However, this device has the largest effective capacitance. Consequently it is exposed to less voltage and $\dfrac{dV}{dt}$. At higher temperatures, rate effects dominated over voltage magnitudes, and the capability of the series pair fell. $\dfrac{dV}{dt}$ performance of the series devices was always better than that of a single triac alone.

TURNOFF

Process tolerances cause small variations in triac turn-off time. Series operation will allow most of the reapplied blocking voltage to appear across the faster triac when a dynamic voltage sharing network is not used.

Figure 11 describes the circuit used to investigate this behavior. It is a capacitor discharge circuit with the load series resonant at 60 Hz. This method of testing is desirable because of the reduced burn and shock hazard resulting from the limited energy storage in the load capacitor.

The triacs were mounted on a temperature controlled hotplate. The single pulse non-repetitive test aids junction temperature control and allows the use of lower power rated components in the snubber and load circuit.

(a) Triac Gate Circuit

S_1 = GORDES MR988 REED WOUND
WITH 1 LAYER AWG #18
L_L = 320 MHY
C_L = 24 μFD, NON-POLAR

REVERSE S_4 AND V_{CC} TO
CHECK OPPOSITE POLARITY.

(b) Optocoupler Gate Circuit

(c) Load Circuit

Figure 6.11. $\left(\dfrac{dV}{dt}\right)_c$ **Test Circuit**

Snubberless turn-off at 1200 V and 320 milli-henry resulted in 800 V peak and 100 V/μs. Although this test exceeded the ratings of the triacs, they turned off successfully.

Snubberless operation is allowable when:

1. The total transient voltage across both triacs does not exceed the rating for a single device. This voltage depends on the load phase angle, self capacitance of the load and triac, damping constant, and natural resonance of the circuit.

2. The total $\left(\dfrac{dV}{dt}\right)_c$ across the series combination does not exceed the capability of a single device.

Maximum turn-off voltage capability and tolerance for variable loads requires the use of a snubber network to provide equal dynamic voltage sharing. Figure 12 and Figure 13 derives the minimum size snubber capacitor allowed. It is determined by the recovery charge of the triac. Measurements in fast current crossing applications

suggest that the reverse recovery charge is less than 2 micro-coulombs. Recovery currents cannot be much greater than I_H or I_{GT}, or the triac would never turn-off. Recovery can be forward, reverse, or near zero current depending on conditions.

Snubber design for the series switch has the following objectives:

- Controlling the voltage peak. Resonant charging will magnify the turn-off voltage.
- Controlling the voltage rate. Peak voltage trades with voltage rate.
- Equalizing the voltage across the series devices by providing for imbalance in turn-off charge.

Designs that satisfy the first two objectives will usually provide capacitor values above the minimum size. Select the snubber for a satisfactory compromise between voltage and $\dfrac{dV}{dt}$. Then check the capacitor to insure that it is sufficiently large.

Worst case:

$$C_2 = C(1 + p); \quad C_1 = C(1 - p); \quad Q_1 = 0; \quad Q_2 = \Delta Q$$

where C = Nominal value of capacitor
and p = 0.1 for 10% tolerance, etc.
ΔQ = Reverse recovery charge

Note that T_1 has no charge while T_2 carries full recovery charge.

For the model shown above,

$$V_S = \frac{Q_1}{C_1} + \frac{Q_2}{C_2} = \frac{Q_1}{C(1 - p)} + \frac{Q_1 - \Delta Q}{C(1 + p)}$$

$$C \geqq \frac{\Delta Q}{2 \, V_{DRM} - V_S(1 + p)}$$

Figure 6.12. Minimum Capacitor Size for Dynamic Voltage Sharing

Snubber designs for static, commutating, and combined $\frac{dV}{dt}$ stress are shown in Table 2. Circuits switching the line or a charged capacitor across a blocking triac require the addition of a series snubber inductor. The snubber must be designed for maximum $\frac{dV}{dt}$ with the minimum circuit inductance. This contraint increases the required triac blocking voltage.

Table 2. Snubber Designs

Type	$\left(\frac{dV}{dt}\right)_C$	$\left(\frac{dV}{dt}\right)_S$	Both
L (mh)	320	0.4	320
R_L Ohm	8	0	8
R_s Ohm	1820	48	48
C_s (μf)	0.5	0.5	0.5
Damping Ratio	1.14	0.85	.035
V_{step} (V)	1200	1200	750
V_{pk} (V)	1332	1400	1423
t_{pk} (μs)	768	29.8	1230
$\frac{dV}{dt}$ (V/μs)	4.6	103	1.3

Note: Divide R_s and $\frac{dV}{dt}$ by 2, multiply C_s by 2 for each triac.

$\frac{dI}{dt}$ CAPABILITY

The hazard of thyristor damage by $\frac{dI}{dt}$ overstress is greater when circuit operating voltages are high because $\frac{dI}{dt}$ is proportional to voltage. Damage by short duration transients is possible even though the pulse is undetectable when observed with non-storage oscilloscopes. This type of damage can be consequence of snubber design, transients, or parasitic capacitances.

A thyristor can be triggered on by gate current, exceeding its breakdown voltage, or by exceeding its $\left(\frac{dV}{dt}\right)_S$ capability. In the latter case, a trigger current is generated by charging of the internal depletion layer capacitance in the device. This effect aids turn-on current spreading, although damage can still occur if the rate of follow on $\frac{dI}{dt}$ is high. Repetitive operation off the ac line at voltages above breakdown is a worst case condition. Quadrant 3 has a slightly slower gated turn-on time, increasing the chance of damage in this direction. Higher operating voltages raise power density and local heating, increasing the possibility of die damage due to hot-spots and thermal run-away.
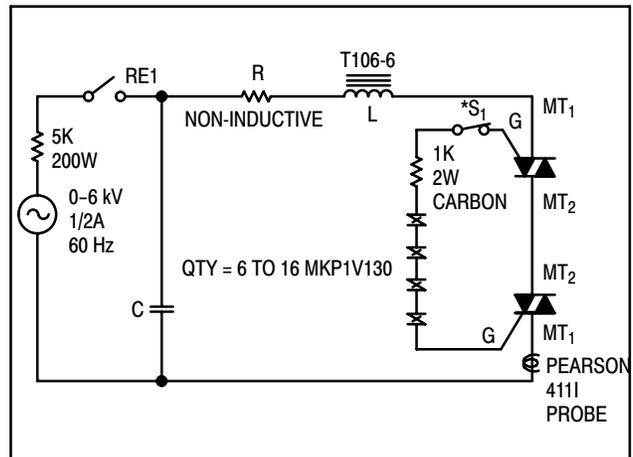
Vci V	C μFD	L μHY	R Ω	dI/dt A/μs	Rejects Tested
1000	4.06	3.4	5.7	100	0/100
1900*	1.05	7.9	5.7	179	0/195
1500	0.002	0.3	10	3000	3/10

* Open S_1 to test breakover dI/dt

Figure 6.13. dI/dt Test Circuit

Ideally, turn-on speed mismatch should not be allowed to force the slower thyristor into breakdown. An RC snubber across each thyristor prevents this. In the worst case, one device turns on instantly while the other switches at the slowest possible turn-on time. The rate of voltage rise at the slower device is roughly $\dfrac{dV}{dt} = \dfrac{V_I R_s}{2L}$, where V_I is the maximum voltage across L. This rate should not allow the voltage to exceed V_{DRM} in less than T_{gt} to prevent breakover. But what if the thyristors are operated without a snubber, or if avalanche occurs because of a transient overvoltage condition?

The circuit in Figure 13 was constructed to investigate this behavior. The capacitor, resistor, and inductor create a pulse forming network to shape the current wave. The initial voltage on the capacitor was set by a series string of sidac bidirectional breakover devices.

Test results showed that operation of the triac switch was safe as long as the rate of current rise was below 200 A/μs. This was true even when the devices turned on because of breakover. However, a 0.002 μf capacitor with no series limiting impedance was sufficient to cause damage in the Q3 firing polarity.

Circuit malfunctions because of breakover will be temporary if the triac is not damaged. Test results suggest that there will be no damage when the series inductance is sufficient to hold dI/dt to acceptable values. Highly energetic transients such as those resulting from lightning strikes can cause damage to the thyristor by I^2t surge overstress. Device survival requires the use of voltage limiting devices in the circuit and $\dfrac{dV}{dt}$ limiting snubbers to prevent unwanted turn-on. Alternatively, a large triac capable of surviving the surge can be used.

ΔQ for turn-off at I_H

$$\Delta Q = \int_{t_1}^{t_2} I_{pk}\, \mathrm{SIN}\omega t\, dt = \frac{I_{pk}}{\omega}(\cos \omega t_1 - \cos \omega t_2)$$

$$I_{H1} = I_{pk}\, \mathrm{Sin}\omega t_1$$

thus $t_1 = \dfrac{1}{\omega}\, \mathrm{Sin}^{-1}\dfrac{I_{H1}}{I_{pk}}$

Worst case : $I_{H2} = 0;\ \phi_2 = \omega t_2 = \pi$

$$\Delta Q = \frac{I_{pk}}{\omega}(1 + \cos[\mathrm{SIN}^{-1}\frac{I_{H1}}{I_{pk}}])$$

$$\Delta Q = \frac{I_{pk}}{\omega}\left[1 + \sqrt{I - \left(\frac{I_{H1}}{I_{pk}}\right)^2}\right]$$
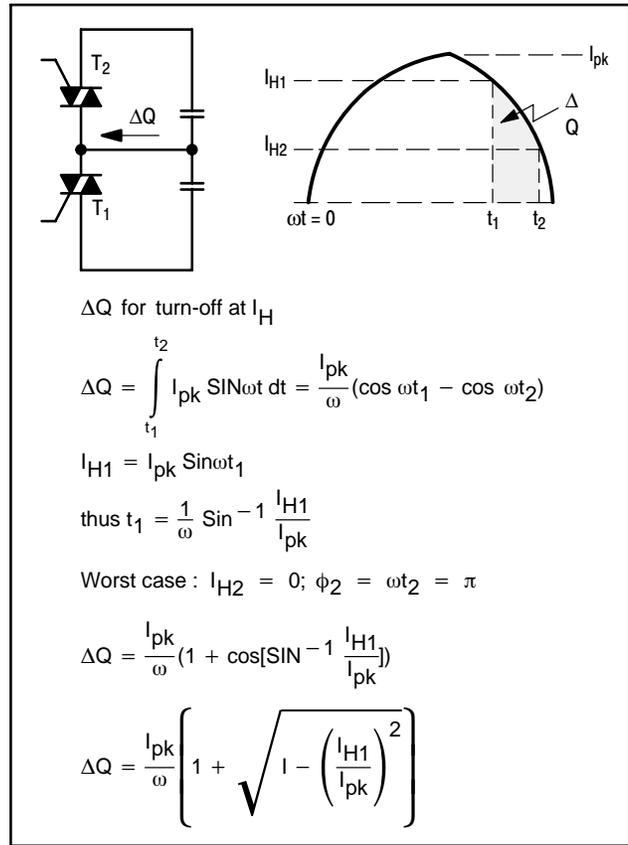
Figure 6.14. Forward Recovery Charge for Turn-Off at I_H

AN1048/D

RC Snubber Networks For Thyristor Power Control and Transient Suppression

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APPLICATION NOTE

INTRODUCTION

Edited and Updated

RC networks are used to control voltage transients that could falsely turn-on a thyristor. These networks are called snubbers.

The simple snubber consists of a series resistor and capacitor placed around the thyristor. These components along with the load inductance form a series CRL circuit. Snubber theory follows from the solution of the circuit's differential equation.

Many RC combinations are capable of providing acceptable performance. However, improperly used snubbers can cause unreliable circuit operation and damage to the semiconductor device.

Both turn-on and turn-off protection may be necessary for reliability. Sometimes the thyristor must function with a range of load values. The type of thyristors used, circuit configuration, and load characteristics are influential.

Snubber design involves compromises. They include cost, voltage rate, peak voltage, and turn-on stress. Practical solutions depend on device and circuit physics.

STATIC $\dfrac{dV}{dt}$

WHAT IS STATIC $\dfrac{dV}{dt}$?

Static $\dfrac{dV}{dt}$ is a measure of the ability of a thyristor to retain a blocking state under the influence of a voltage transient.

$\left(\dfrac{dV}{dt}\right)_S$ DEVICE PHYSICS

Static $\dfrac{dV}{dt}$ turn-on is a consequence of the Miller effect and regeneration (Figure 1). A change in voltage across the junction capacitance induces a current through it. This current is proportional to the rate of voltage change $\left(\dfrac{dV}{dt}\right)$. It triggers the device on when it becomes large enough to raise the sum of the NPN and PNP transistor alphas to unity.
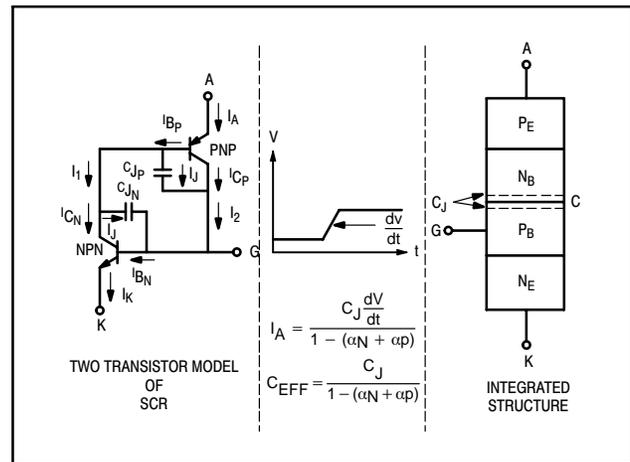
Figure 6.1. $\left(\dfrac{dV}{dt}\right)_S$ **Model**

CONDITIONS INFLUENCING $\left(\dfrac{dV}{dt}\right)_S$

Transients occurring at line crossing or when there is no initial voltage across the thyristor are worst case. The collector junction capacitance is greatest then because the depletion layer widens at higher voltage.

Small transients are incapable of charging the self-capacitance of the gate layer to its forward biased threshold voltage (Figure 2). Capacitance voltage divider action between the collector and gate-cathode junctions and built-in resistors that shunt current away from the cathode emitter are responsible for this effect.
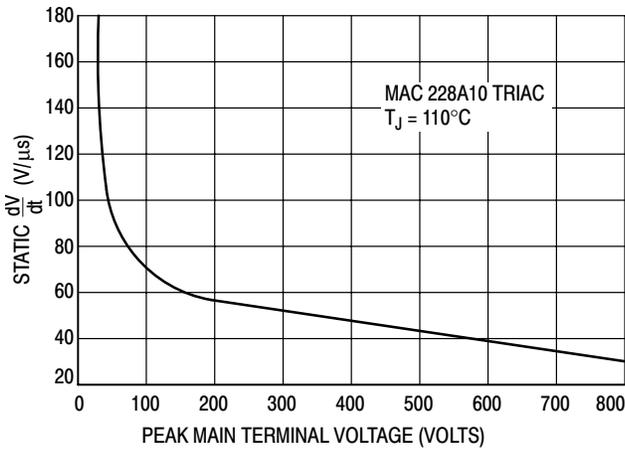
Figure 6.2. Exponential $\left(\dfrac{dV}{dt}\right)_S$ versus Peak Voltage

Static $\dfrac{dV}{dt}$ does not depend strongly on voltage for operation below the maximum voltage and temperature rating. Avalanche multiplication will increase leakage current and reduce $\dfrac{dV}{dt}$ capability if a transient is within roughly 50 volts of the actual device breakover voltage.

A higher rated voltage device guarantees increased $\dfrac{dV}{dt}$ at lower voltage. This is a consequence of the exponential rating method where a 400 V device rated at 50 V/µs has a higher $\dfrac{dV}{dt}$ to 200 V than a 200 V device with an identical rating. However, the same diffusion recipe usually applies for all voltages. So actual capabilities of the product are not much different.

Heat increases current gain and leakage, lowering $\left(\dfrac{dV}{dt}\right)_S$, the gate trigger voltage and noise immunity (Figure 3).
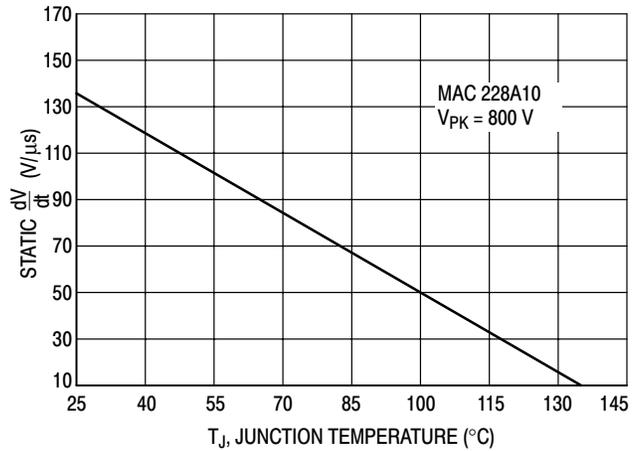
Figure 6.3. Exponential $\left(\dfrac{dV}{dt}\right)_S$ versus Temperature

$\left(\dfrac{dV}{dt}\right)_S$ FAILURE MODE

Occasional unwanted turn-on by a transient may be acceptable in a heater circuit but isn't in a fire prevention sprinkler system or for the control of a large motor. Turn-on is destructive when the follow-on current amplitude or rate is excessive. If the thyristor shorts the power line or a charged capacitor, it will be damaged.

Static $\dfrac{dV}{dt}$ turn-on is non-destructive when series impedance limits the surge. The thyristor turns off after a half-cycle of conduction. High $\dfrac{dV}{dt}$ aids current spreading in the thyristor, improving its ability to withstand $\dfrac{dI}{dt}$. Breakdown turn-on does not have this benefit and should be prevented.
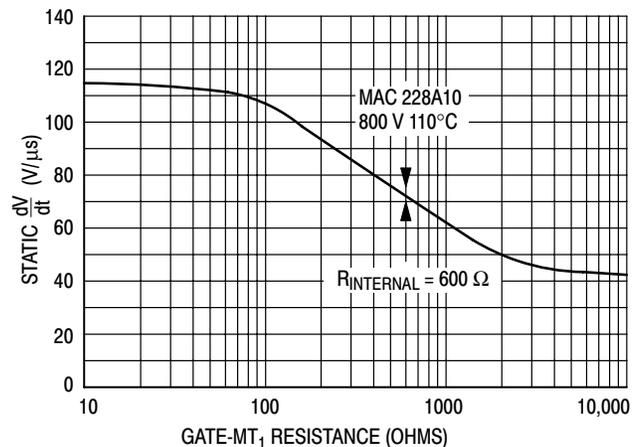
Figure 6.4. Exponential $\left(\dfrac{dV}{dt}\right)_S$ versus Gate to MT$_1$ Resistance

IMPROVING $\left(\dfrac{dV}{dt}\right)_S$

Static $\dfrac{dV}{dt}$ can be improved by adding an external resistor from the gate to MT1 (Figure 4). The resistor provides a path for leakage and $\dfrac{dV}{dt}$ induced currents that originate in the drive circuit or the thyristor itself.

Non-sensitive devices (Figure 5) have internal shorting resistors dispersed throughout the chip's cathode area. This design feature improves noise immunity and high temperature blocking stability at the expense of increased trigger and holding current. External resistors are optional for non-sensitive SCRs and TRIACs. They should be comparable in size to the internal shorting resistance of the device (20 to 100 ohms) to provide maximum improvement. The internal resistance of the thyristor should be measured with an ohm-meter that does not forward bias a diode junction.
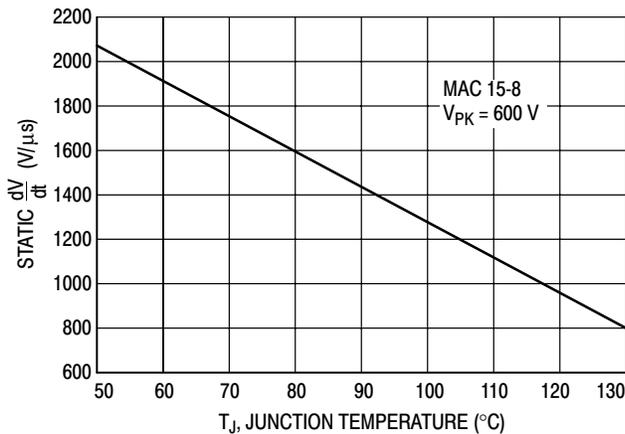
Figure 6.5. Exponential $\left(\dfrac{dV}{dt}\right)_S$ versus Junction Temperature

Sensitive gate TRIACs run 100 to 1000 ohms. With an external resistor, their $\dfrac{dV}{dt}$ capability remains inferior to non-sensitive devices because lateral resistance within the gate layer reduces its benefit.

Sensitive gate SCRs ($I_{GT} < 200\ \mu A$) have no built-in resistor. They should be used with an external resistor. The recommended value of the resistor is 1000 ohms. Higher values reduce maximum operating temperature and $\left(\dfrac{dV}{dt}\right)_S$ (Figure 6). The capability of these parts varies by more than 100 to 1 depending on gate-cathode termination.
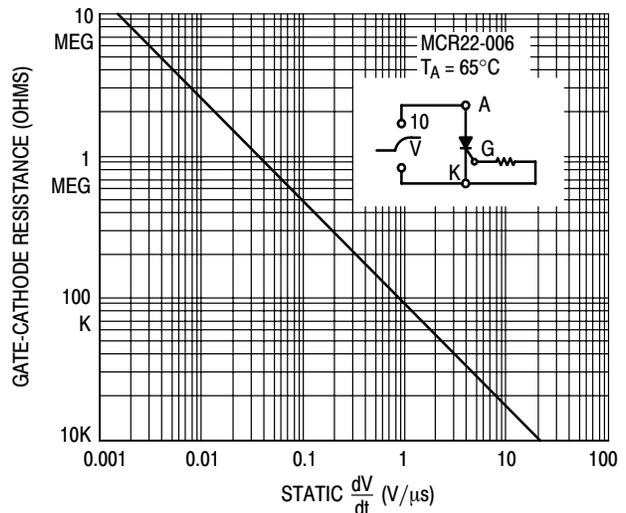
Figure 6.6. Exponential $\left(\dfrac{dV}{dt}\right)_S$ versus Gate-Cathode Resistance

A gate-cathode capacitor (Figure 7) provides a shunt path for transient currents in the same manner as the resistor. It also filters noise currents from the drive circuit and enhances the built-in gate-cathode capacitance voltage divider effect. The gate drive circuit needs to be able to charge the capacitor without excessive delay, but it does not need to supply continuous current as it would for a resistor that increases $\dfrac{dV}{dt}$ the same amount. However, the capacitor does not enhance static thermal stability.
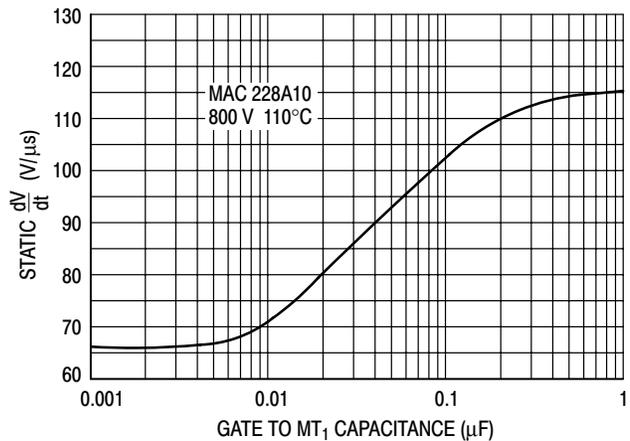
Figure 6.7. Exponential $\left(\dfrac{dV}{dt}\right)_S$ versus Gate to MT$_1$ Capacitance

The maximum $\left(\dfrac{dV}{dt}\right)_S$ improvement occurs with a short. Actual improvement stops before this because of spreading resistance in the thyristor. An external capacitor of about 0.1 μF allows the maximum enhancement at a higher value of R_{GK}.

One should keep the thyristor cool for the highest $\left(\dfrac{dV}{dt}\right)_s$. Also devices should be tested in the application circuit at the highest possible temperature using thyristors with the lowest measured trigger current.

TRIAC COMMUTATING $\dfrac{dV}{dt}$

WHAT IS COMMUTATING $\dfrac{dV}{dt}$?

The commutating $\dfrac{dV}{dt}$ rating applies when a TRIAC has been conducting and attempts to turn-off with an inductive load. The current and voltage are out of phase (Figure 8). The TRIAC attempts to turn-off as the current drops below the holding value. Now the line voltage is high and in the opposite polarity to the direction of conduction. Successful turn-off requires the voltage across the TRIAC to rise to the instantaneous line voltage at a rate slow enough to prevent retriggering of the device.
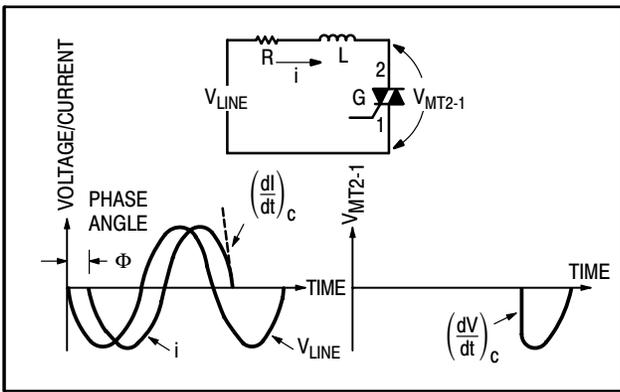
Figure 6.8. TRIAC Inductive Load Turn-Off $\left(\dfrac{dV}{dt}\right)_c$

$\left(\dfrac{dV}{dt}\right)_c$ DEVICE PHYSICS

A TRIAC functions like two SCRs connected in inverse-parallel. So, a transient of either polarity turns it on.

There is charge within the crystal's volume because of prior conduction (Figure 9). The charge at the boundaries of the collector junction depletion layer responsible for $\left(\dfrac{dV}{dt}\right)_s$ is also present. TRIACs have lower $\left(\dfrac{dV}{dt}\right)_c$ than $\left(\dfrac{dV}{dt}\right)_s$ because of this additional charge.

The volume charge storage within the TRIAC depends on the peak current before turn-off and its rate of zero crossing $\left(\dfrac{dI}{dt}\right)_c$. In the classic circuit, the load impedance and line frequency determine $\left(\dfrac{dI}{dt}\right)_c$. The rate of crossing for sinusoidal currents is given by the slope of the secant line between the 50% and 0% levels as:

$$\left(\frac{dI}{dt}\right)_c = \frac{6\,f\,I_{TM}}{1000}\ A/ms$$

where f = line frequency and I_{TM} = maximum on-state current in the TRIAC.

Turn-off depends on both the Miller effect displacement current generated by $\dfrac{dV}{dt}$ across the collector capacitance and the currents resulting from internal charge storage within the volume of the device (Figure 10). If the reverse recovery current resulting from both these components is high, the lateral IR drop within the TRIAC base layer will forward bias the emitter and turn the TRIAC on. Commutating $\dfrac{dV}{dt}$ capability is lower when turning off from the positive direction of current conduction because of device geometry. The gate is on the top of the die and obstructs current flow.

Recombination takes place throughout the conduction period and along the back side of the current wave as it declines to zero. Turn-off capability depends on its shape. If the current amplitude is small and its zero crossing $\left(\dfrac{dI}{dt}\right)_c$ is low, there is little volume charge storage and turn-off becomes limited by $\left(\dfrac{dV}{dt}\right)_s$. At moderate current amplitudes, the volume charge begins to influence turn-off, requiring a larger snubber. When the current is large or has rapid zero crossing, $\left(\dfrac{dV}{dt}\right)_c$ has little influence. Commutating $\dfrac{dI}{dt}$ and delay time to voltage reapplication determine whether turn-off will be successful or not (Figures 11, 12).
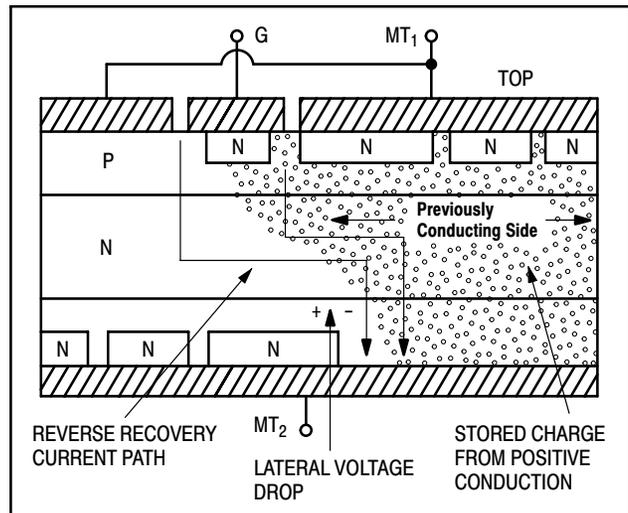
Figure 6.9. TRIAC Structure and Current Flow at Commutation
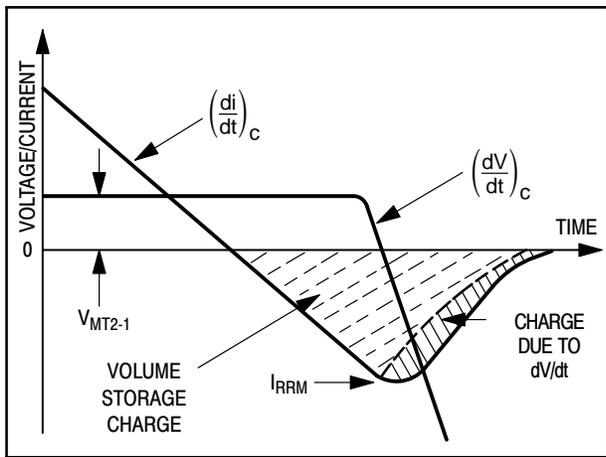
**Figure 6.10. TRIAC Current and Voltage
at Commutation**
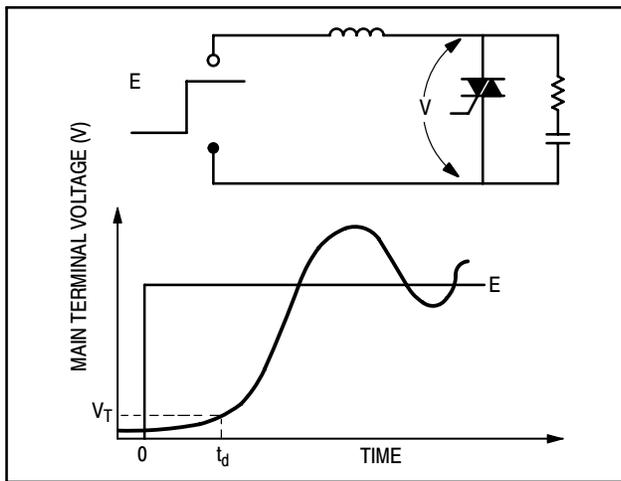
Figure 6.11. Snubber Delay Time
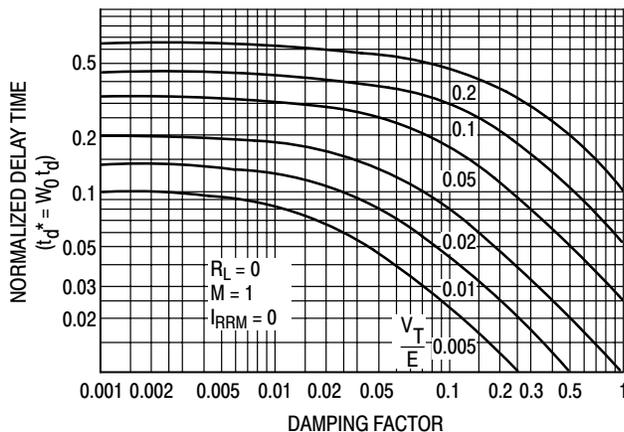
Figure 6.12. Delay Time To Normalized Voltage

CONDITIONS INFLUENCING $\left(\dfrac{dV}{dt}\right)_c$

Commutating $\dfrac{dV}{dt}$ depends on charge storage and recovery dynamics in addition to the variables influencing static $\dfrac{dV}{dt}$. High temperatures increase minority carrier life-time and the size of recovery currents, making turn-off more difficult. Loads that slow the rate of current zero-crossing aid turn-off. Those with harmonic content hinder turn-off.

Circuit Examples

Figure 13 shows a TRIAC controlling an inductive load in a bridge. The inductive load has a time constant longer than the line period. This causes the load current to remain constant and the TRIAC current to switch rapidly as the line voltage reverses. This application is notorious for causing TRIAC turn-off difficulty because of high $\left(\dfrac{dI}{dt}\right)_c$.
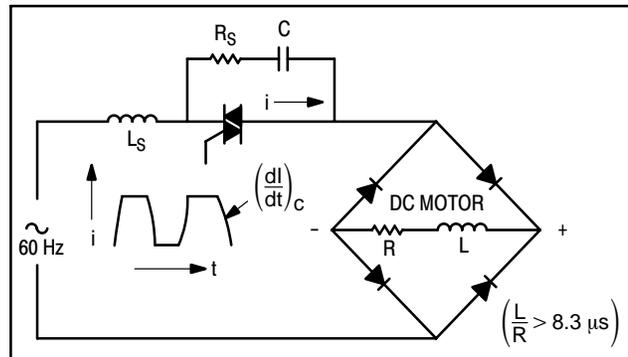
Figure 6.13. Phase Controlling a Motor in a Bridge

High currents lead to high junction temperatures and rates of current crossing. Motors can have 5 to 6 times the normal current amplitude at start-up. This increases both junction temperature and the rate of current crossing, leading to turn-off problems.

The line frequency causes high rates of current crossing in 400 Hz applications. Resonant transformer circuits are doubly periodic and have current harmonics at both the primary and secondary resonance. Non-sinusoidal currents can lead to turn-off difficulty even if the current amplitude is low before zero-crossing.

$\left(\dfrac{dV}{dt}\right)_c$ FAILURE MODE

$\left(\dfrac{dV}{dt}\right)_c$ failure causes a loss of phase control. Temporary turn-on or total turn-off failure is possible. This can be destructive if the TRIAC conducts asymmetrically causing a dc current component and magnetic saturation. The winding resistance limits the current. Failure results because of excessive surge current and junction temperature.

IMPROVING $\left(\dfrac{dV}{dt}\right)_c$

The same steps that improve $\left(\dfrac{dV}{dt}\right)_S$ aid $\left(\dfrac{dV}{dt}\right)_c$ except when stored charge dominates turn-off. Steps that reduce the stored charge or soften the commutation are necessary then.

Larger TRIACs have better turn-off capability than smaller ones with a given load. The current density is lower in the larger device allowing recombination to claim a greater proportion of the internal charge. Also junction temperatures are lower.

TRIACs with high gate trigger currents have greater turn-off ability because of lower spreading resistance in the gate layer, reduced Miller effect, or shorter lifetime.

The rate of current crossing can be adjusted by adding a commutation softening inductor in series with the load. Small high permeability "square loop" inductors saturate causing no significant disturbance to the load current. The inductor resets as the current crosses zero introducing a large inductance into the snubber circuit at that time. This slows the current crossing and delays the reapplication of blocking voltage aiding turn-off.

The commutation inductor is a circuit element that introduces time delay, as opposed to inductance, into the circuit. It will have little influence on observed $\dfrac{dV}{dt}$ at the device. The following example illustrates the improvement resulting from the addition of an inductor constructed by winding 33 turns of number 18 wire on a tape wound core (52000-1A). This core is very small having an outside diameter of 3/4 inch and a thickness of 1/8 inch. The delay time can be calculated from:

$$t_S = \frac{(N\,A\,B\,10^{-8})}{E} \text{ where:}$$

t_s = time delay to saturation in seconds.
B = saturating flux density in Gauss
A = effective core cross sectional area in cm^2
N = number of turns.

For the described inductor:

$$t_S = (33 \text{ turns}) \, (0.076 \text{ cm}^2) \, (28000 \text{ Gauss})$$
$$(1 \times 10^{-8}) \; / \; (175 \text{ V}) = 4.0 \; \mu s.$$

The saturation current of the inductor does not need to be much larger than the TRIAC trigger current. Turn-off failure will result before recovery currents become greater than this value. This criterion allows sizing the inductor with the following equation:

$$I_S = \frac{H_S\,M_L}{0.4\,\pi\,N} \text{ where :}$$

H_s = MMF to saturate = 0.5 Oersted
ML = mean magnetic path length = 4.99 cm.

$$I_S = \frac{(.5)\,(4.99)}{.4\,\pi\,33} = 60 \text{ mA.}$$

SNUBBER PHYSICS

UNDAMPED NATURAL RESONANCE

$$\omega_0 = \frac{1}{\sqrt{LC}} \text{ Radians/second}$$

Resonance determines $\dfrac{dV}{dt}$ and boosts the peak capacitor voltage when the snubber resistor is small. C and L are related to one another by $\omega_0{}^2$. $\dfrac{dV}{dt}$ scales linearly with ω_0 when the damping factor is held constant. A ten to one reduction in $\dfrac{dV}{dt}$ requires a 100 to 1 increase in either component.

DAMPING FACTOR

$$\rho = \frac{R}{2}\sqrt{\frac{C}{L}}$$

The damping factor is proportional to the ratio of the circuit loss and its surge impedance. It determines the trade off between $\dfrac{dV}{dt}$ and peak voltage. Damping factors between 0.01 and 1.0 are recommended.

The Snubber Resistor

Damping and $\dfrac{dV}{dt}$

When $\rho\,<\,0.5$, the snubber resistor is small, and $\dfrac{dV}{dt}$ depends mostly on resonance. There is little improvement in $\dfrac{dV}{dt}$ for damping factors less than 0.3, but peak voltage and snubber discharge current increase. The voltage wave has a 1-COS (θ) shape with overshoot and ringing. Maximum $\dfrac{dV}{dt}$ occurs at a time later than t = 0. There is a time delay before the voltage rise, and the peak voltage almost doubles.

When $\rho\,>\,0.5$, the voltage wave is nearly exponential in shape. The maximum instantaneous $\dfrac{dV}{dt}$ occurs at t = 0. There is little time delay and moderate voltage overshoot.

When $\rho\,>\,1.0$, the snubber resistor is large and $\dfrac{dV}{dt}$ depends mostly on its value. There is some overshoot even through the circuit is overdamped.

High load inductance requires large snubber resistors and small snubber capacitors. Low inductances imply small resistors and large capacitors.

Damping and Transient Voltages

Figure 14 shows a series inductor and filter capacitor connected across the ac main line. The peak to peak voltage of a transient disturbance increases by nearly four times. Also the duration of the disturbance spreads because of ringing, increasing the chance of malfunction or damage to the voltage sensitive circuit. Closing a switch causes this behavior. The problem can be reduced by adding a damping resistor in series with the capacitor.
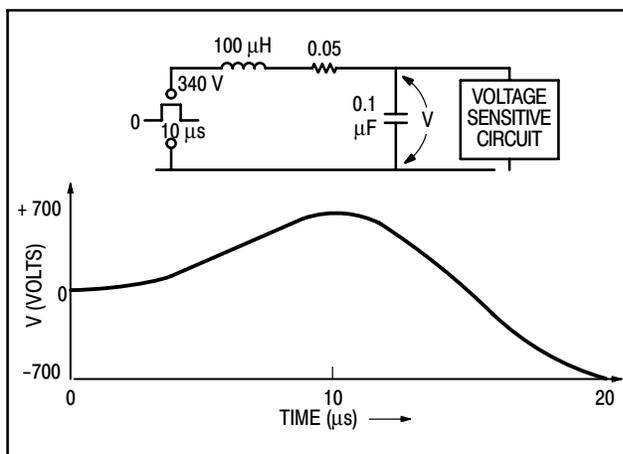
Figure 6.14. Undamped LC Filter Magnifies and Lengthens a Transient

$\frac{dI}{dt}$

Non-Inductive Resistor

The snubber resistor limits the capacitor discharge current and reduces $\frac{dI}{dt}$ stress. High $\frac{dI}{dt}$ destroys the thyristor even though the pulse duration is very short.

The rate of current rise is directly proportional to circuit voltage and inversely proportional to series inductance. The snubber is often the major offender because of its low inductance and close proximity to the thyristor.

With no transient suppressor, breakdown of the thyristor sets the maximum voltage on the capacitor. It is possible to exceed the highest rated voltage in the device series because high voltage devices are often used to supply low voltage specifications.

The minimum value of the snubber resistor depends on the type of thyristor, triggering quadrants, gate current amplitude, voltage, repetitive or non-repetitive operation, and required life expectancy. There is no simple way to predict the rate of current rise because it depends on turn-on speed of the thyristor, circuit layout, type and size of snubber capacitor, and inductance in the snubber resistor. The equations in Appendix D describe the circuit. However, the values required for the model are not easily obtained except by testing. Therefore, reliability should be verified in the actual application circuit.

Table 1 shows suggested minimum resistor values estimated (Appendix A) by testing a 20 piece sample from the four different TRIAC die sizes.

Table 1. Minimum Non-inductive Snubber Resistor for Four Quadrant Triggering.

TRIAC Type	Peak V_C Volts	R_s Ohms	$\frac{dI}{dt}$ A/μs
Non-Sensitive Gate (I_{GT} > 10 mA) 8 to 40 A$_{(RMS)}$	200	3.3	170
	300	6.8	250
	400	11	308
	600	39	400
	800	51	400

Reducing $\frac{dI}{dt}$

TRIAC $\frac{dI}{dt}$ can be improved by avoiding quadrant 4 triggering. Most optocoupler circuits operate the TRIAC in quadrants 1 and 3. Integrated circuit drivers use quadrants 2 and 3. Zero crossing trigger devices are helpful because they prohibit triggering when the voltage is high.

Driving the gate with a high amplitude fast rise pulse increases $\frac{dI}{dt}$ capability. The gate ratings section defines the maximum allowed current.

Inductance in series with the snubber capacitor reduces $\frac{dI}{dt}$. It should not be more than five percent of the load inductance to prevent degradation of the snubber's $\frac{dV}{dt}$ suppression capability. Wirewound snubber resistors sometimes serve this purpose. Alternatively, a separate inductor can be added in series with the snubber capacitor. It can be small because it does not need to carry the load current. For example, 18 turns of AWG No. 20 wire on a T50-3 (1/2 inch) powdered iron core creates a non-saturating 6.0 μH inductor.

A 10 ohm, 0.33 μF snubber charged to 650 volts resulted in a 1000 A/μs $\frac{dI}{dt}$. Replacement of the non-inductive snubber resistor with a 20 watt wirewound unit lowered the rate of rise to a non-destructive 170 A/μs at 800 V. The inductor gave an 80 A/μs rise at 800 V with the non-inductive resistor.

The Snubber Capacitor

A damping factor of 0.3 minimizes the size of the snubber capacitor for a given value of $\frac{dV}{dt}$. This reduces the cost and physical dimensions of the capacitor. However, it raises voltage causing a counter balancing cost increase.

Snubber operation relies on the charging of the snubber capacitor. Turn-off snubbers need a minimum conduction angle long enough to discharge the capacitor. It should be at least several time constants ($R_S C_S$).

STORED ENERGY

Inductive Switching Transients

$E = \frac{1}{2} L I_0{}^2$ Watt-seconds or Joules

$I_0 =$ current in Amperes flowing in the inductor at t = 0.

Resonant charging cannot boost the supply voltage at turn-off by more than 2. If there is an initial current flowing in the load inductance at turn-off, much higher voltages are possible. Energy storage is negligible when a TRIAC turns off because of its low holding or recovery current.

The presence of an additional switch such as a relay, thermostat or breaker allows the interruption of load current and the generation of high spike voltages at switch opening. The energy in the inductance transfers into the circuit capacitance and determines the peak voltage (Figure 15).

$$\frac{dV}{dt} = \frac{I}{C} \quad V_{PK} = I \sqrt{\frac{L}{C}}$$

(a.) Protected Circuit   **(b.) Unprotected Circuit**
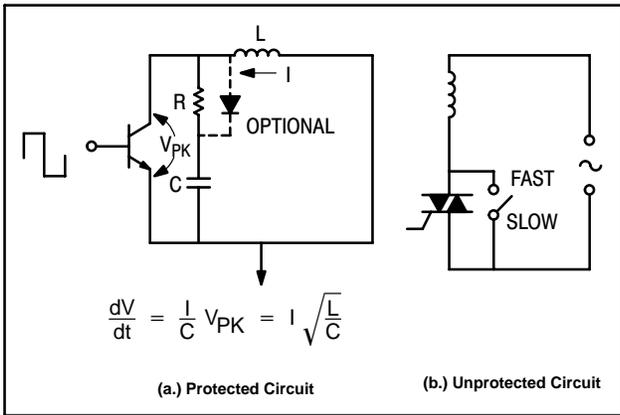
Figure 6.15. Interrupting Inductive Load Current

Capacitor Discharge

The energy stored in the snubber capacitor $\left(E_C = \frac{1}{2} C V^2 \right)$ transfers to the snubber resistor and thyristor every time it turns on. The power loss is proportional to frequency ($P_{AV} = 120\ E_c$ @ 60 Hz).

CURRENT DIVERSION

The current flowing in the load inductor cannot change instantly. This current diverts through the snubber resistor causing a spike of theoretically infinite $\frac{dV}{dt}$ with magnitude equal to (I_{RRM} R) or (I_H R).

LOAD PHASE ANGLE

Highly inductive loads cause increased voltage and $\left(\frac{dV}{dt} \right)_C$ at turn-off. However, they help to protect the thyristor from transients and $\left(\frac{dV}{dt} \right)_S$. The load serves as the

snubber inductor and limits the rate of inrush current if the device does turn on. Resistance in the load lowers $\frac{dV}{dt}$ and V_{PK} (Figure 16).

$$\left(M = \text{RESISTIVE DIVISION RATIO} = \frac{R_S}{R_L + R_S} \right)$$

$$I_{RRM} = 0$$
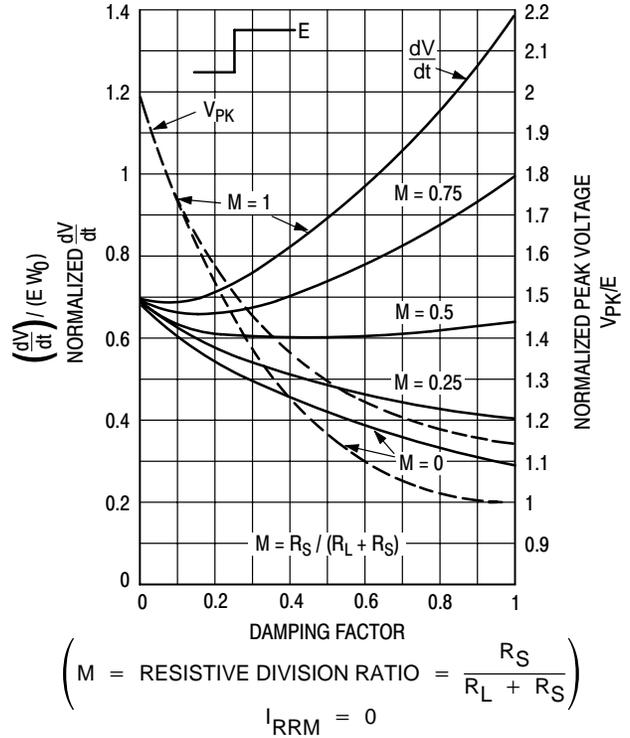
Figure 6.16. 0 To 63% $\frac{dV}{dt}$

CHARACTERISTIC VOLTAGE WAVES

Damping factor and reverse recovery current determine the shape of the voltage wave. It is not exponential when the snubber damping factor is less than 0.5 (Figure 17) or when significant recovery currents are present.
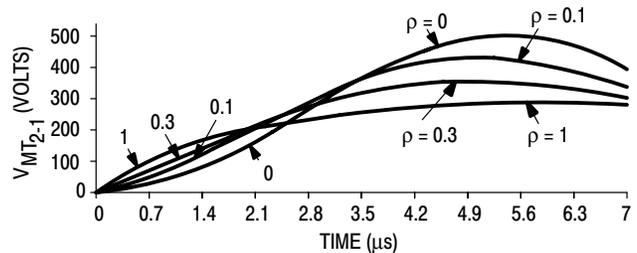
$$\left[0\text{–}63\% \left(\frac{dV}{dt} \right)_S = 100\ V/\mu s,\ E = 250\ V, \atop R_L = 0,\ I_{RRM} = 0 \right]$$

Figure 6.17. Voltage Waves For Different Damping Factors

$$(R_L = 0, \ M = 1, \ I_{RRM} = 0)$$

$$\text{NORMALIZED} \ \frac{dV}{dt} = \frac{dV/dt}{E \ \omega_0} \quad \text{NORMALIZED} \ V_{PK} = \frac{V_{PK}}{E}$$
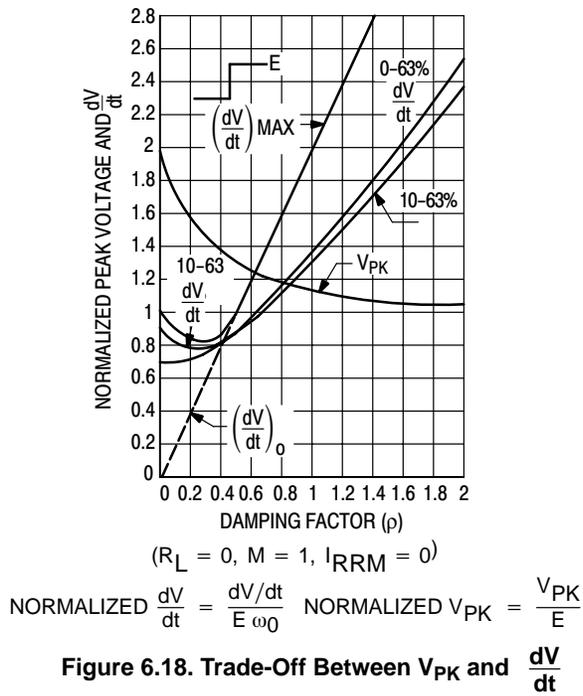
Figure 6.18. Trade-Off Between V_{PK} and $\dfrac{dV}{dt}$

A variety of wave parameters (Figure 18) describe $\frac{dV}{dt}$ Some are easy to solve for and assist understanding. These include the initial $\frac{dV}{dt}$, the maximum instantaneous $\frac{dV}{dt}$, and the average $\frac{dV}{dt}$ to the peak reapplied voltage. The 0 to 63% $\left(\frac{dV}{dt}\right)_S$ and 10 to 63% $\left(\frac{dV}{dt}\right)_C$ definitions on device data sheets are easy to measure but difficult to compute.

NON-IDEAL BEHAVIORS
CORE LOSSES

The magnetic core materials in typical 60 Hz loads introduce losses at the snubber natural frequency. They appear as a resistance in series with the load inductance and winding dc resistance (Figure 19). This causes actual $\frac{dV}{dt}$ to be less than the theoretical value.

L DEPENDS ON CURRENT AMPLITUDE, CORE SATURATION

R INCLUDES CORE LOSS, WINDING R. INCREASES WITH FREQUENCY

C WINDING CAPACITANCE. DEPENDS ON INSULATION, WIRE SIZE, GEOMETRY
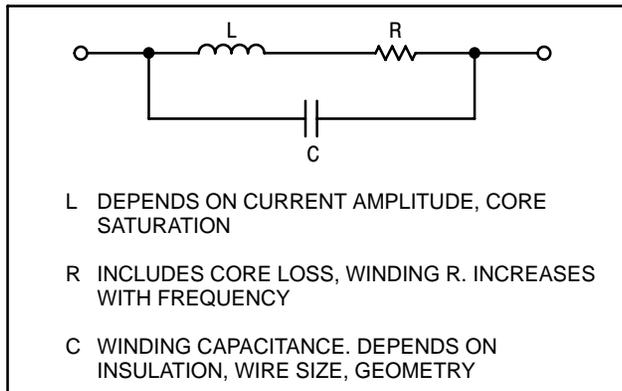
Figure 6.19. Inductor Model

COMPLEX LOADS

Many real-world inductances are non-linear. Their core materials are not gapped causing inductance to vary with current amplitude. Small signal measurements poorly characterize them. For modeling purposes, it is best to measure them in the actual application.

Complex load circuits should be checked for transient voltages and currents at turn-on and off. With a capacitive load, turn-on at peak input voltage causes the maximum surge current. Motor starting current runs 4 to 6 times the steady state value. Generator action can boost voltages above the line value. Incandescent lamps have cold start currents 10 to 20 times the steady state value. Transformers generate voltage spikes when they are energized. Power factor correction circuits and switching devices create complex loads. In most cases, the simple CRL model allows an approximate snubber design. However, there is no substitute for testing and measuring the worst case load conditions.

SURGE CURRENTS IN INDUCTIVE CIRCUITS

Inductive loads with long L/R time constants cause asymmetric multi-cycle surges at start up (Figure 20). Triggering at zero voltage crossing is the worst case condition. The surge can be eliminated by triggering at the zero current crossing angle.
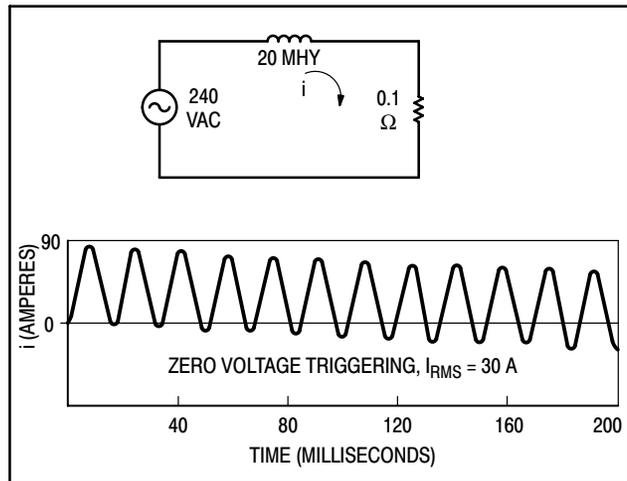
Figure 6.20. Start-Up Surge For Inductive Circuit

Core remanence and saturation cause surge currents. They depend on trigger angle, line impedance, core characteristics, and direction of the residual magnetization. For example, a 2.8 kVA 120 V 1:1 transformer with a 1.0 ampere load produced 160 ampere currents at start-up. Soft starting the circuit at a small conduction angle reduces this current.

Transformer cores are usually not gapped and saturate easily. A small asymmetry in the conduction angle causes magnetic saturation and multi-cycle current surges.

Steps to achieve reliable operation include:

1. Supply sufficient trigger current amplitude. TRIACs have different trigger currents depending on their quadrant of operation. Marginal gate current or optocoupler LED current causes halfwave operation.

2. Supply sufficient gate current duration to achieve latching. Inductive loads slow down the main terminal current rise. The gate current must remain above the specified I_{GT} until the main terminal current exceeds the latching value. Both a resistive bleeder around the load and the snubber discharge current help latching.

3. Use a snubber to prevent TRIAC $\left(\dfrac{dV}{dt}\right)_C$ failure.

4. Minimize designed-in trigger asymmetry. Triggering must be correct every half-cycle including the first. Use a storage scope to investigate circuit behavior during the first few cycles of turn-on. Alternatively, get the gate circuit up and running before energizing the load.

5. Derive the trigger synchronization from the line instead of the TRIAC main terminal voltage. This avoids regenerative interaction between the core hysteresis and the triggering angle preventing trigger runaway, halfwave operation, and core saturation.

6. Avoid high surge currents at start-up. Use a current probe to determine surge amplitude. Use a soft start circuit to reduce inrush current.

DISTRIBUTED WINDING CAPACITANCE

There are small capacitances between the turns and layers of a coil. Lumped together, they model as a single shunt capacitance. The load inductor behaves like a capacitor at frequencies above its self-resonance. It becomes ineffective in controlling $\dfrac{dV}{dt}$ and V_{PK} when a fast transient such as that resulting from the closing of a switch occurs. This problem can be solved by adding a small snubber across the line.

SELF-CAPACITANCE

A thyristor has self-capacitance which limits $\dfrac{dV}{dt}$ when the load inductance is large. Large load inductances, high power factors, and low voltages may allow snubberless operation.

SNUBBER EXAMPLES

WITHOUT INDUCTANCE

Power TRIAC Example

Figure 21 shows a transient voltage applied to a TRIAC controlling a resistive load. Theoretically there will be an instantaneous step of voltage across the TRIAC. The only elements slowing this rate are the inductance of the wiring and the self-capacitance of the thyristor. There is an exponential capacitor charging component added along with a decaying component because of the IR drop in the snubber resistor. The non-inductive snubber circuit is useful when the load resistance is much larger than the snubber resistor.

$$e_{(t\,=\,o+)} = E\left[\left(\frac{R_S}{R_S + R_L}\right)e^{-t/\tau} + (1 - e^{-t/\tau})\right]$$
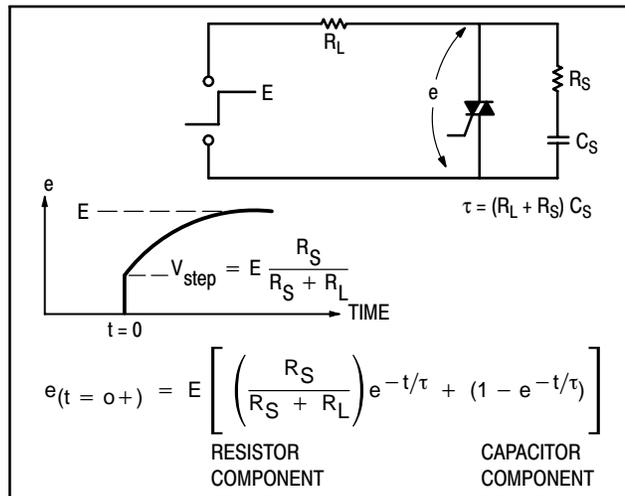
Figure 6.21. Non-Inductive Snubber Circuit

Opto-TRIAC Examples

Single Snubber, Time Constant Design

Figure 22 illustrates the use of the RC time constant design method. The optocoupler sees only the voltage across the snubber capacitor. The resistor R1 supplies the trigger current of the power TRIAC. A worst case design procedure assumes that the voltage across the power TRIAC changes instantly. The capacitor voltage rises to 63% of the maximum in one time constant. Then:

$$R_1 C_S = \tau = \frac{0.63\,E}{\left(\dfrac{dV}{dt}\right)_S} \quad \text{where } \left(\frac{dV}{dt}\right)_S \text{ is the rated static } \frac{dV}{dt}$$

for the optocoupler.

Figure 6.22. Single Snubber For Sensitive Gate TRIAC and Phase Controllable Optocoupler (ρ = 0.67)
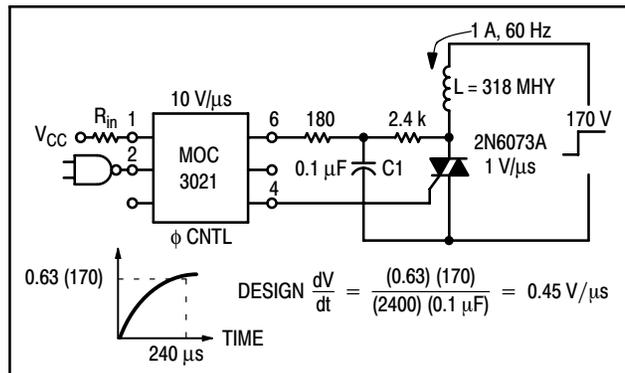
$\dfrac{dV}{dt}$ (V/µs)	
Power TRIAC	**Optocoupler**
0.99	0.35

The optocoupler conducts current only long enough to trigger the power device. When it turns on, the voltage between MT2 and the gate drops below the forward threshold voltage of the opto-TRIAC causing turn-off. The optocoupler sees $\left(\dfrac{dV}{dt}\right)_s$ when the power TRIAC turns off later in the conduction cycle at zero current crossing. Therefore, it is not necessary to design for the lower optocoupler $\left(\dfrac{dV}{dt}\right)_c$ rating. In this example, a single snubber designed for the optocoupler protects both devices.
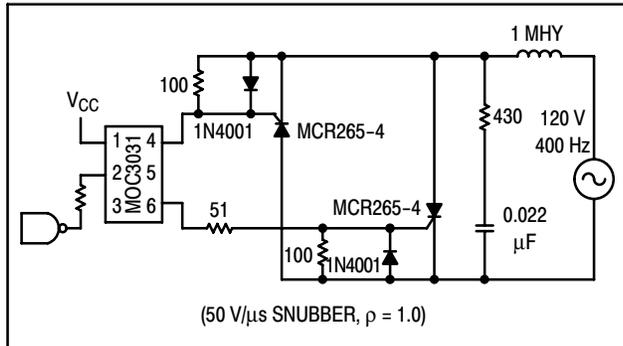
Figure 6.23. Anti-Parallel SCR Driver

Optocouplers with SCRs

Anti-parallel SCR circuits result in the same $\dfrac{dV}{dt}$ across the optocoupler and SCR (Figure 23). Phase controllable opto-couplers require the SCRs to be snubbed to their lower $\dfrac{dV}{dt}$ rating. Anti-parallel SCR circuits are free from the charge storage behaviors that reduce the turn-off capability of TRIACs. Each SCR conducts for a half-cycle and has the next half cycle of the ac line in which to recover. The turn-off $\dfrac{dV}{dt}$ of the conducting SCR becomes a static forward blocking $\dfrac{dV}{dt}$ for the other device. Use the SCR data sheet $\left(\dfrac{dV}{dt}\right)_s$ rating in the snubber design.

A SCR used inside a rectifier bridge to control an ac load will not have a half cycle in which to recover. The available time decreases with increasing line voltage. This makes the circuit less attractive. Inductive transients can be suppressed by a snubber at the input to the bridge or across the SCR. However, the time limitation still applies.

OPTO $\left(\dfrac{dV}{dt}\right)_C$

Zero-crossing optocouplers can be used to switch inductive loads at currents less than 100 mA (Figure 24).

However a power TRIAC along with the optocoupler should be used for higher load currents.

$(R_S = 100\ \Omega,\ V_{RMS} = 220\ V,\ \text{POWER FACTOR} = 0.5)$
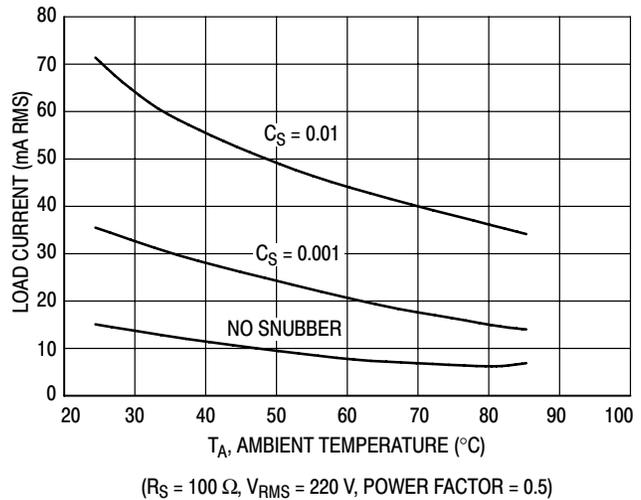
Figure 6.24. MOC3062 Inductive Load Current versus T_A

A phase controllable optocoupler is recommended with a power device. When the load current is small, a MAC97A TRIAC is suitable.

Unusual circuit conditions sometimes lead to unwanted operation of an optocoupler in $\left(\dfrac{dV}{dt}\right)_c$ mode. Very large currents in the power device cause increased voltages between MT2 and the gate that hold the optocoupler on. Use of a larger TRIAC or other measures that limit inrush current solve this problem.

Very short conduction times leave residual charge in the optocoupler. A minimum conduction angle allows recovery before voltage reapplication.

THE SNUBBER WITH INDUCTANCE

Consider an overdamped snubber using a large capacitor whose voltage changes insignificantly during the time under consideration. The circuit reduces to an equivalent L/R series charging circuit.

The current through the snubber resistor is:

$$i = \frac{V}{R\tau}\left(1 - e^{-\frac{t}{\tau}}\right),$$

and the voltage across the TRIAC is:

$$e = i\,R_S.$$

The voltage wave across the TRIAC has an exponential rise with maximum rate at t = 0. Taking its derivative gives its value as:

$$\left(\frac{dV}{dt}\right)_0 = \frac{V\,R_S}{L}.$$

Highly overdamped snubber circuits are not practical designs. The example illustrates several properties:

1. The initial voltage appears completely across the circuit inductance. Thus, it determines the rate of change of current through the snubber resistor and the initial $\frac{dV}{dt}$. This result does not change when there is resistance in the load and holds true for all damping factors.

2. The snubber works because the inductor controls the rate of current change through the resistor and the rate of capacitor charging. Snubber design cannot ignore the inductance. This approach suggests that the snubber capacitance is not important but that is only true for this hypothetical condition. The snubber resistor shunts the thyristor causing unacceptable leakage when the capacitor is not present. If the power loss is tolerable, $\frac{dV}{dt}$ can be controlled without the capacitor. An example is the soft-start circuit used to limit inrush current in switching power supplies (Figure 25).
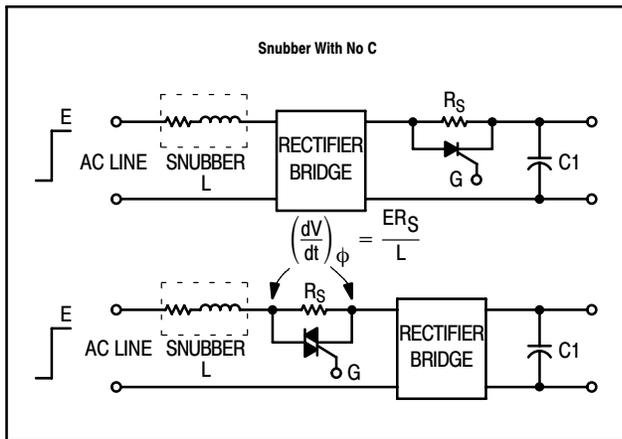
Figure 6.25. Surge Current Limiting For a Switching Power Supply

TRIAC DESIGN PROCEDURE $\left(\frac{dV}{dt}\right)_c$

1. Refer to Figure 18 and select a particular damping factor (ρ) giving a suitable trade-off between V_{PK} and $\frac{dV}{dt}$. Determine the normalized $\frac{dV}{dt}$ corresponding to the chosen damping factor.

The voltage E depends on the load phase angle:

$$E = \sqrt{2}\ V_{RMS}\ \text{Sin}\ (\phi) \text{ where } \phi = \tan^{-1}\left(\frac{X_L}{R_L}\right) \text{ where}$$

ϕ = measured phase angle between line V and load I
R_L = measured dc resistance of the load.
Then

$$Z = \frac{V_{RMS}}{I_{RMS}} \sqrt{R_L{}^2 + X_L{}^2} \quad X_L = \sqrt{Z^2 - R_L{}^2} \text{ and}$$

$$L = \frac{X_L}{2\,\pi\,f_{Line}}.$$

If only the load current is known, assume a pure inductance. This gives a conservative design. Then:

$$L = \frac{V_{RMS}}{2\,\pi\,f_{Line}\,I_{RMS}} \text{ where } E = \sqrt{2}\ V_{RMS}.$$

For example:

$$E = \sqrt{2}\ 120 = 170\ V;\ L = \frac{120}{(8\ A)\ (377\ rps)} = 39.8\ mH.$$

Read from the graph at $\rho = 0.6$, $V_{PK} = (1.25)\ 170 = 213$ V. Use 400 V TRIAC. Read $\frac{dV}{dt}_{(\rho\,=\,0.6)} = 1.0$.

2. Apply the resonance criterion:

$$\omega_0 = \left(\text{spec}\ \frac{dV}{dt}\right) / \left(\frac{dV}{dt_{(P)}}\ E\right).$$

$$\omega_0 = \frac{5 \times 10^6\ V/S}{(1)\ (170\ V)} = 29.4 \times 10^3\ rps.$$

$$C = \frac{1}{\omega_0{}^2\ L} = 0.029\ \mu F$$

3. Apply the damping criterion:

$$R_S = 2\rho\ \sqrt{\frac{L}{C}} = 2\,(0.6)\ \sqrt{\frac{39.8 \times 10^{-3}}{0.029 \times 10^{-6}}} = 1400\,\text{ohms}.$$

$\left(\frac{dV}{dt}\right)_c$ SAFE AREA CURVE

Figure 26 shows a MAC15 TRIAC turn-off safe operating area curve. Turn-off occurs without problem under the curve. The region is bounded by static $\frac{dV}{dt}$ at low values of $\left(\frac{dI}{dt}\right)_c$ and delay time at high currents. Reduction of the peak current permits operation at higher line frequency. This TRIAC operated at f = 400 Hz, $T_J = 125°C$, and $I_{TM} = 6.0$ amperes using a 30 ohm and 0.068 μF snubber. Low damping factors extend operation to higher $\left(\frac{dI}{dt}\right)_c$, but capacitor sizes increase. The addition of a small, saturable commutation inductor extends the allowed current rate by introducing recovery delay time.

$$\left(\frac{dI}{dt}\right)_C = 6\,f\,ITM \times 10^{-3}\,\text{A/ms}$$

WITH COMMUTATION L

$$\left(\begin{array}{l}\text{MAC 16-8, COMMUTATIONAL L} = 33\ \text{TURNS \#18,}\\ \text{52000-1A TAPE WOUND CORE 3/4 INCH OD}\end{array}\right)$$
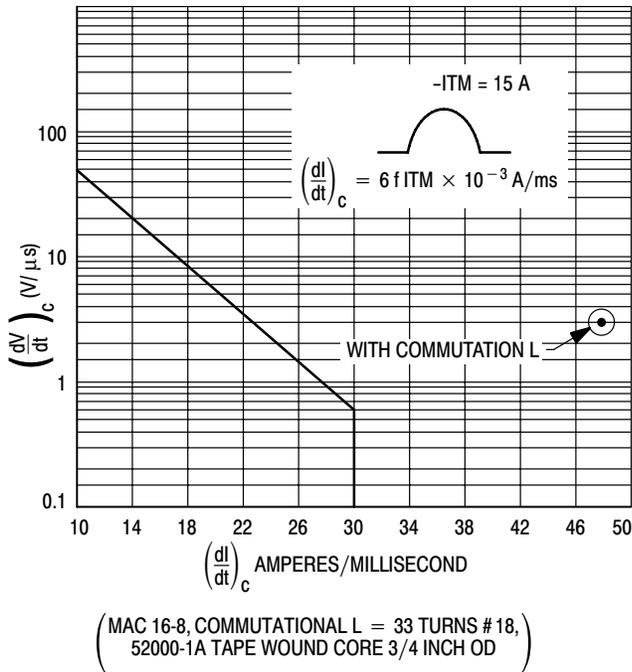
Figure 6.26. $\left(\dfrac{dV}{dt}\right)_C$ versus $\left(\dfrac{dI}{dt}\right)_C$ $T_J = 125°C$

STATIC $\dfrac{dV}{dt}$ DESIGN

There is usually some inductance in the ac main and power wiring. The inductance may be more than 100 µH if there is a transformer in the circuit or nearly zero when a shunt power factor correction capacitor is present. Usually the line inductance is roughly several µH. The minimum inductance must be known or defined by adding a series inductor to insure reliable operation (Figure 27).
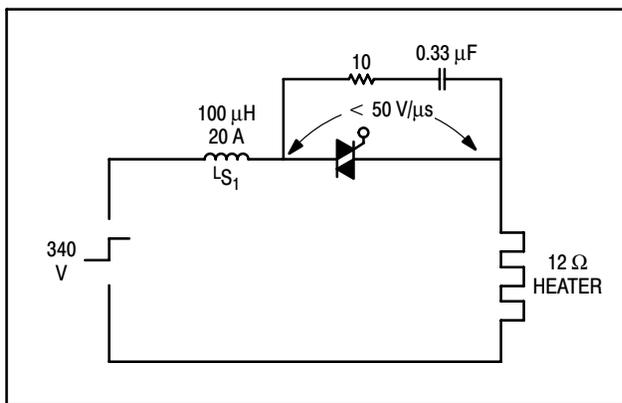
Figure 6.27. Snubbing For a Resistive Load

One hundred µH is a suggested value for starting the design. Plug the assumed inductance into the equation for C. Larger values of inductance result in higher snubber resistance and reduced $\dfrac{dI}{dt}$. For example:

Given E = 240 $\sqrt{2}$ = 340 V.

Pick ρ = 0.3.

Then from Figure 18, V_{PK} = 1.42 (340) = 483 V.
Thus, it will be necessary to use a 600 V device. Using the previously stated formulas for ω_0, C and R we find:

$$\omega_0 = \frac{50 \times 10^6\,\text{V/S}}{(0.73)\,(340\,\text{V})} = 201450\ \text{rps}$$

$$C = \frac{1}{(201450)^2\,(100 \times 10^{-6})} = 0.2464\ \mu F$$

$$R = 2\,(0.3)\ \sqrt{\frac{100 \times 10^{-6}}{0.2464 \times 10^{-6}}} = 12\ \text{ohms}$$

VARIABLE LOADS

The snubber should be designed for the smallest load inductance because $\dfrac{dV}{dt}$ will then be highest because of its dependence on ω_0. This requires a higher voltage device for operation with the largest inductance because of the corresponding low damping factor.

Figure 28 describes $\dfrac{dV}{dt}$ for an 8.0 ampere load at various power factors. The minimum inductance is a component added to prevent static $\dfrac{dV}{dt}$ firing with a resistive load.

$$\left(\frac{dV}{dt}\right)_S = 100\ \text{V/}\mu s \qquad \left(\frac{dV}{dt}\right)_C = 5\ \text{V/}\mu s$$
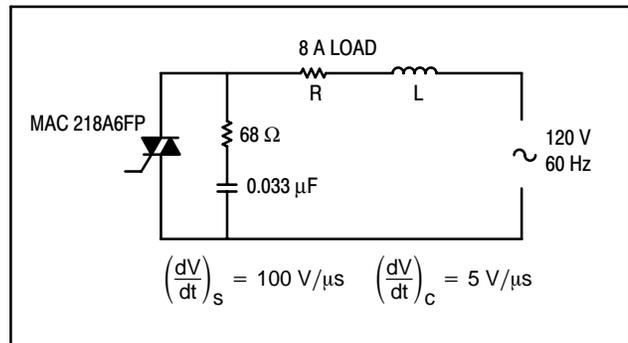
ρ	R	L	V_{step}	V_{PK}	$\dfrac{dv}{dt}$
	Ω	MHY	V	V	V/µs
0.75	15	0.1	170	191	86
0.03	0	39.8	170	325	4.0
0.04	10.6	28.1	120	225	3.3
0.06	13.5	17.3	74	136	2.6

Figure 6.28. Snubber For a Variable Load

EXAMPLES OF SNUBBER DESIGNS

Table 2 describes snubber RC values for $\left(\frac{dV}{dt}\right)_S$. Figures 31 and 32 show possible R and C values for a 5.0 V/μs $\left(\frac{dV}{dt}\right)_C$ assuming a pure inductive load.

Table 2. Static $\dfrac{dV}{dt}$ Designs
(E = 340 V, V_{peak} = 500 V, ρ = 0.3)

L μH	5.0 V/μs		50 V/μs		100 V/μs	
	C μF	R Ohm	C μF	R Ohm	C μF	R Ohm
47					0.15	10
100			0.33	10	0.1	20
220			0.15	22	0.033	47
500			0.068	51	0.015	110
1000	3.0	11	0.033	100		

TRANSIENT AND NOISE SUPPRESSION

Transients arise internally from normal circuit operation or externally from the environment. The latter is particularly frustrating because the transient characteristics are undefined. A statistical description applies. Greater or smaller stresses are possible. Long duration high voltage transients are much less probable than those of lower amplitude and higher frequency. Environments with infrequent lightning and load switching see transient voltages below 3.0 kV.
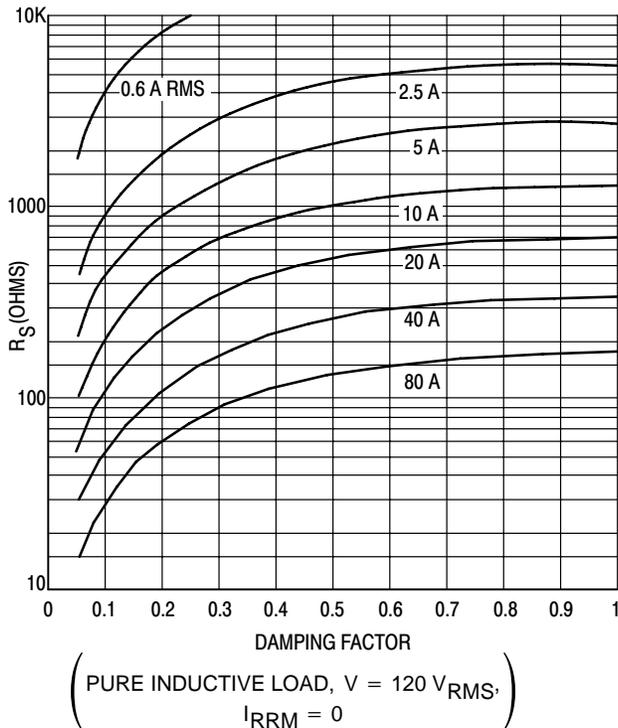
Figure 6.29. Snubber Resistor For $\left(\dfrac{dV}{dt}\right)_C$ = 5.0 V/μs

$\left(\begin{array}{c}\text{PURE INDUCTIVE LOAD, V = 120 }V_{RMS},\\ I_{RRM} = 0\end{array}\right)$

$\left(\begin{array}{c}\text{PURE INDUCTIVE LOAD, V = 120 }V_{RMS},\\ I_{RRM} = 0\end{array}\right)$
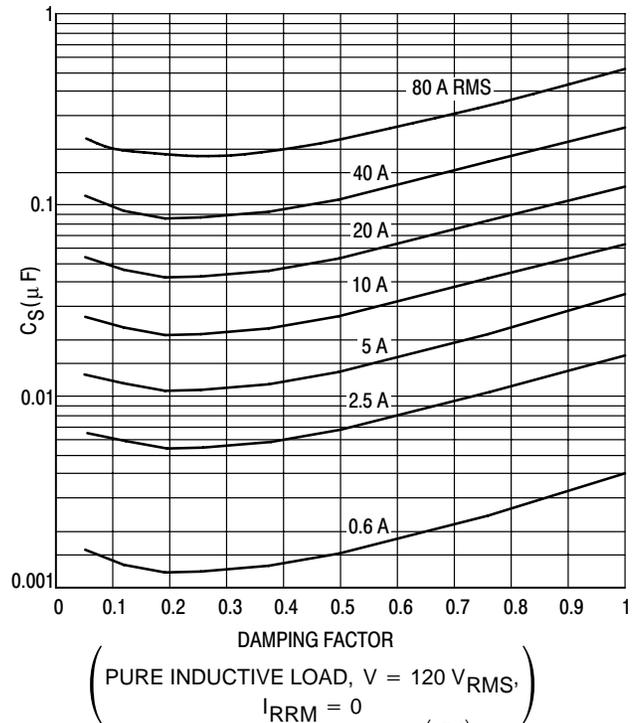
Figure 6.30. Snubber Capacitor For $\left(\dfrac{dV}{dt}\right)_C$ = 5.0 V/μs

The natural frequencies and impedances of indoor ac wiring result in damped oscillatory surges with typical frequencies ranging from 30 kHz to 1.5 MHz. Surge amplitude depends on both the wiring and the source of surge energy. Disturbances tend to die out at locations far away from the source. Spark-over (6.0 kV in indoor ac wiring) sets the maximum voltage when transient suppressors are not present. Transients closer to the service entrance or in heavy wiring have higher amplitudes, longer durations, and more damping because of the lower inductance at those locations.

The simple CRL snubber is a low pass filter attenuating frequencies above its natural resonance. A steady state sinusoidal input voltage results in a sine wave output at the same frequency. With no snubber resistor, the rate of roll off approaches 12 dB per octave. The corner frequency is at the snubber's natural resonance. If the damping factor is low, the response peaks at this frequency. The snubber resistor degrades filter characteristics introducing an up-turn at ω = 1 / (RC). The roll-off approaches 6.0 dB/octave at frequencies above this. Inductance in the snubber resistor further reduces the roll-off rate.

Figure 32 describes the frequency response of the circuit in Figure 27. Figure 31 gives the theoretical response to a 3.0 kV 100 kHz ring-wave. The snubber reduces the peak voltage across the thyristor. However, the fast rise input causes a high $\frac{dV}{dt}$ step when series inductance is added to the snubber resistor. Limiting the input voltage with a transient suppressor reduces the step.
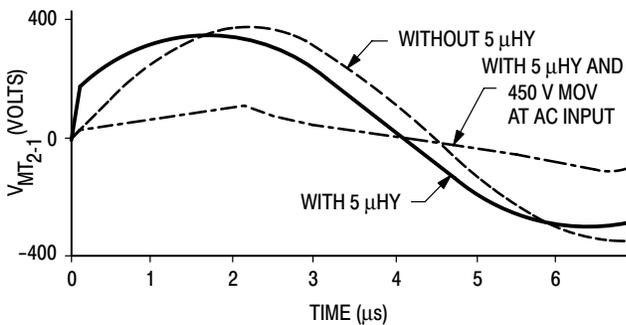
Figure 6.31. Theoretical Response of Figure 33 Circuit to 3.0 kV IEEE 587 Ring Wave (R_{SC} = 27.5 Ω)
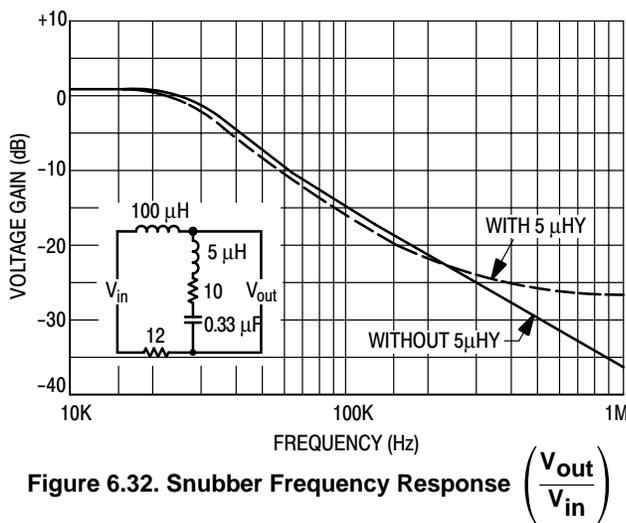
Figure 6.32. Snubber Frequency Response $\left(\dfrac{V_{out}}{V_{in}}\right)$

The noise induced into a circuit is proportional to $\dfrac{dV}{dt}$ when coupling is by stray capacitance, and $\dfrac{dI}{dt}$ when the coupling is by mutual inductance. Best suppression requires the use of a voltage limiting device along with a rate limiting CRL snubber.

The thyristor is best protected by preventing turn-on from $\dfrac{dV}{dt}$ or breakover. The circuit should be designed for what can happen instead of what normally occurs.

In Figure 30, a MOV connected across the line protects many parallel circuit branches and their loads. The MOV defines the maximum input voltage and $\dfrac{dI}{dt}$ through the load. With the snubber, it sets the maximum $\dfrac{dV}{dt}$ and peak voltage across the thyristor. The MOV must be large because there is little surge limiting impedance to prevent its burn-out.

In Figure 32, there is a separate suppressor across each thyristor. The load impedance limits the surge energy delivered from the line. This allows the use of a smaller device but omits load protection. This arrangement protects each thyristor when its load is a possible transient source.
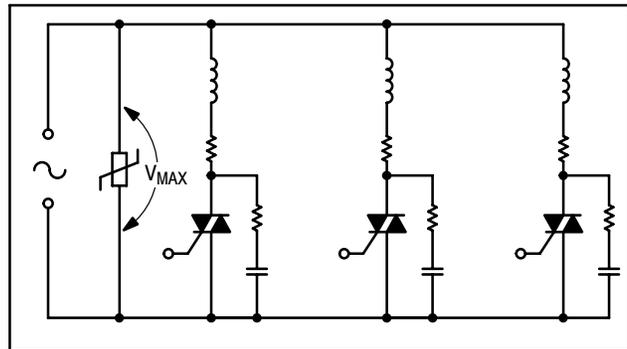
Figure 6.33. Limiting Line Voltage
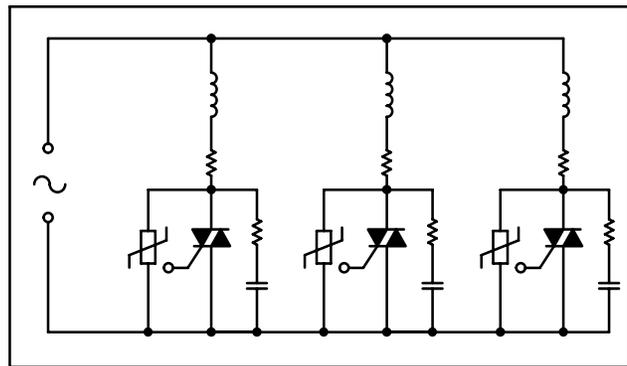
Figure 6.34. Limiting Thyristor Voltage

It is desirable to place the suppression device directly across the source of transient energy to prevent the induction of energy into other circuits. However, there is no protection for energy injected between the load and its controlling thyristor. Placing the suppressor directly across each thyristor positively limits maximum voltage and snubber discharge $\dfrac{dI}{dt}$.

EXAMPLES OF SNUBBER APPLICATIONS

In Figure 35, TRIACs switch a 3 phase motor on and off and reverse its rotation. Each TRIAC pair functions as a SPDT switch. The turn-on of one TRIAC applies the differential voltage between line phases across the blocking device without the benefit of the motor impedance to constrain the rate of voltage rise. The inductors are added to prevent static $\dfrac{dV}{dt}$ firing and a line-to-line short.

Figure 6.35. 3 Phase Reversing Motor

Figure 36 shows a split phase capacitor-run motor with reversing accomplished by switching the capacitor in series with one or the other winding. The forward and reverse TRIACs function as a SPDT switch. Reversing the motor applies the voltage on the capacitor abruptly across the blocking thyristor. Again, the inductor L is added to prevent $\left(\dfrac{dV}{dt}\right)_S$ firing of the blocking TRIAC. If turn-on occurs, the forward and reverse TRIACs short the capacitors (C_S) resulting in damage to them. It is wise to add the resistor R_S to limit the discharge current.
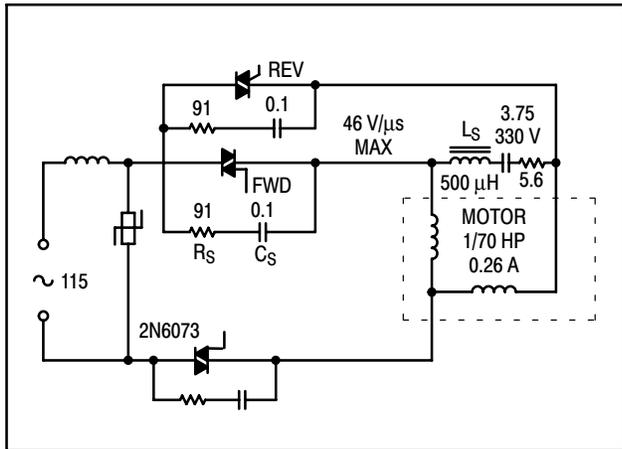
Figure 6.36. Split Phase Reversing Motor

Figure 37 shows a "tap changer." This circuit allows the operation of switching power supplies from a 120 or 240 vac line. When the TRIAC is on, the circuit functions as a conventional voltage doubler with diodes D1 and D2 conducting on alternate half-cycles. In this mode of operation, inrush current and $\dfrac{dI}{dt}$ are hazards to TRIAC reliability. Series impedance is necessary to prevent damage to the TRIAC.

The TRIAC is off when the circuit is not doubling. In this state, the TRIAC sees the difference between the line voltage and the voltage at the intersection of C1 and C2. Transients on the line cause $\left(\dfrac{dV}{dt}\right)_S$ firing of the TRIAC. High inrush current, $\dfrac{dI}{dt}$, and overvoltage damage to the filter capacitor are possibilities. Prevention requires the addition of a RC snubber across the TRIAC and an inductor in series with the line.

THYRISTOR TYPES

Sensitive gate thyristors are easy to turn-on because of their low trigger current requirements. However, they have less $\dfrac{dV}{dt}$ capability than similar non-sensitive devices. A non-sensitive thyristor should be used for high $\dfrac{dV}{dt}$.

TRIAC commutating $\dfrac{dV}{dt}$ ratings are 5 to 20 times less than static $\dfrac{dV}{dt}$ ratings.
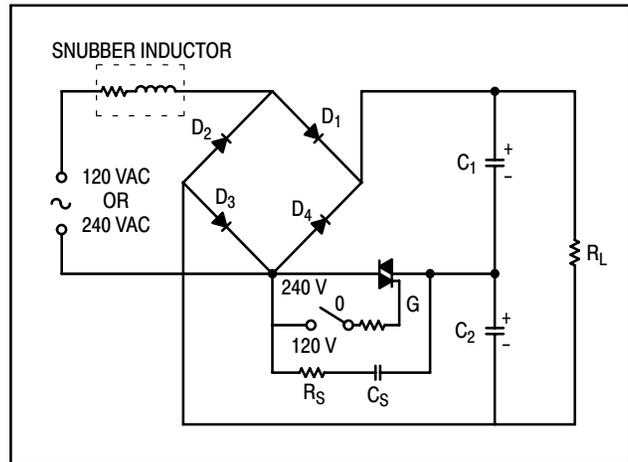
Figure 6.37. Tap Changer For Dual Voltage Switching Power Supply

Phase controllable optocouplers have lower $\dfrac{dV}{dt}$ ratings than zero crossing optocouplers and power TRIACs. These should be used when a dc voltage component is present, or to prevent turn-on delay.

Zero crossing optocouplers have more $\dfrac{dV}{dt}$ capability than power thyristors; and they should be used in place of phase controllable devices in static switching applications.

APPENDIX A
MEASURING $\left(\dfrac{dV}{dt}\right)_S$

Figure 38 shows a test circuit for measuring the static $\dfrac{dV}{dt}$ of power thyristors. A 1000 volt FET switch insures that the voltage across the device under test (D.U.T.) rises rapidly from zero. A differential preamp allows the use of a N-channel device while keeping the storage scope chassis at ground for safety purposes. The rate of voltage rise is adjusted by a variable RC time constant. The charging resistance is low to avoid waveform distortion because of the thyristor's self-capacitance but is large enough to prevent damage to the D.U.T. from turn-on $\dfrac{dI}{dt}$. Mounting the miniature range switches, capacitors, and G-K network close to the device under test reduces stray inductance and allows testing at more than 10 kV/μs.
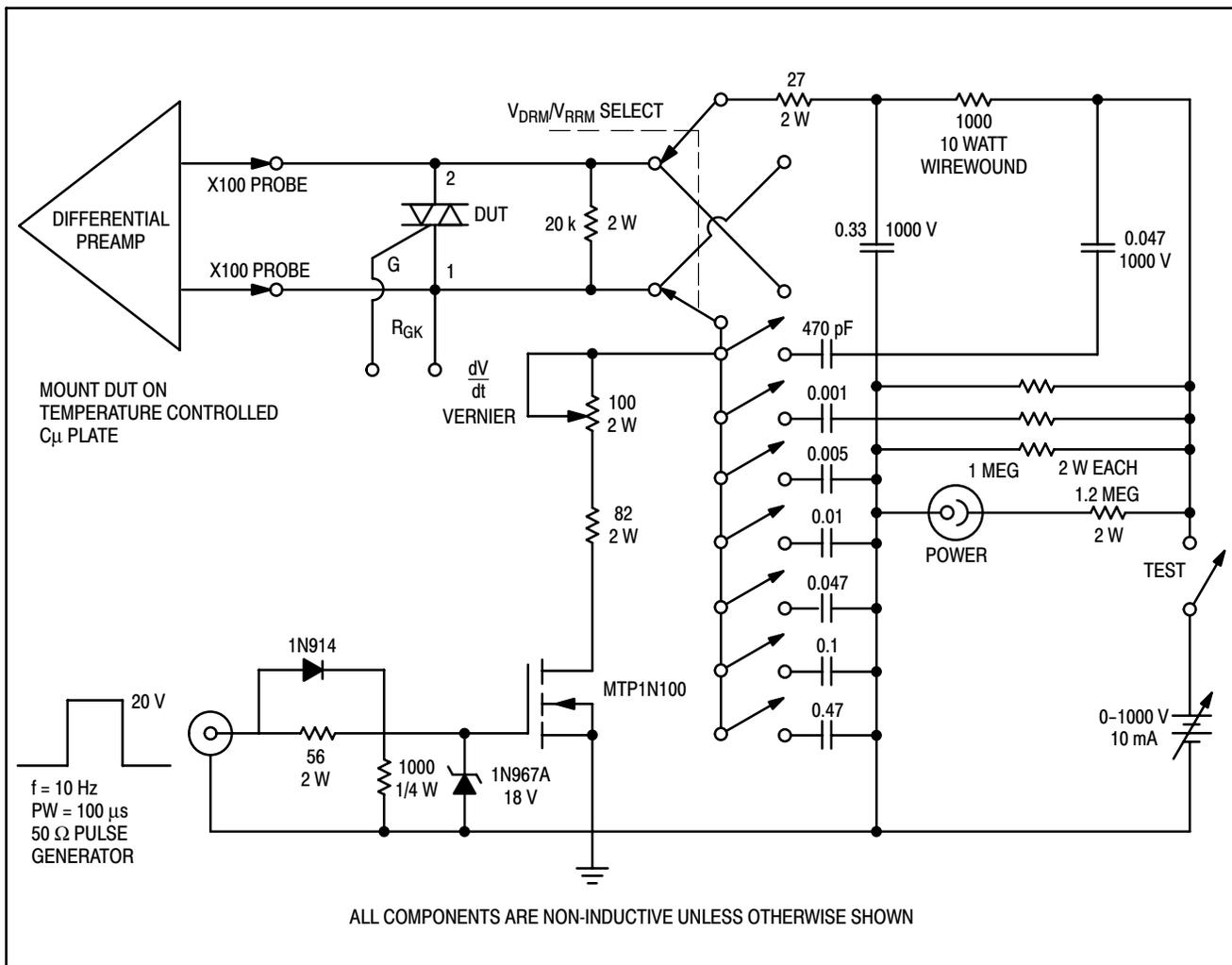
Figure 6.38. Circuit For Static $\dfrac{dV}{dt}$ Measurement of Power Thyristors

APPENDIX B
MEASURING $\left(\dfrac{dV}{dt}\right)_C$

A test fixture to measure commutating $\dfrac{dV}{dt}$ is shown in Figure 39. It is a capacitor discharge circuit with the load series resonant. The single pulse test aids temperature control and allows the use of lower power components. The limited energy in the load capacitor reduces burn and shock hazards. The conventional load and snubber circuit provides recovery and damping behaviors like those in the application.

The voltage across the load capacitor triggers the D.U.T. It terminates the gate current when the load capacitor voltage crosses zero and the TRIAC current is at its peak.

Each V_{DRM}, I_{TM} combination requires different components. Calculate their values using the equations given in Figure 39.

Commercial chokes simplify the construction of the necessary inductors. Their inductance should be adjusted by increasing the air gap in the core. Removal of the magnetic pole piece reduces inductance by 4 to 6 but extends the current without saturation.

The load capacitor consists of a parallel bank of 1500 Vdc non-polar units, with individual bleeders mounted at each capacitor for safety purposes.

An optional adjustable voltage clamp prevents TRIAC breakdown.

To measure $\left(\dfrac{dV}{dt}\right)_C$, synchronize the storage scope on the current waveform and verify the proper current amplitude and period. Increase the initial voltage on the capacitor to compensate for losses within the coil if necessary. Adjust the snubber until the device fails to turn off after the first half-cycle. Inspect the rate of voltage rise at the fastest passing condition.
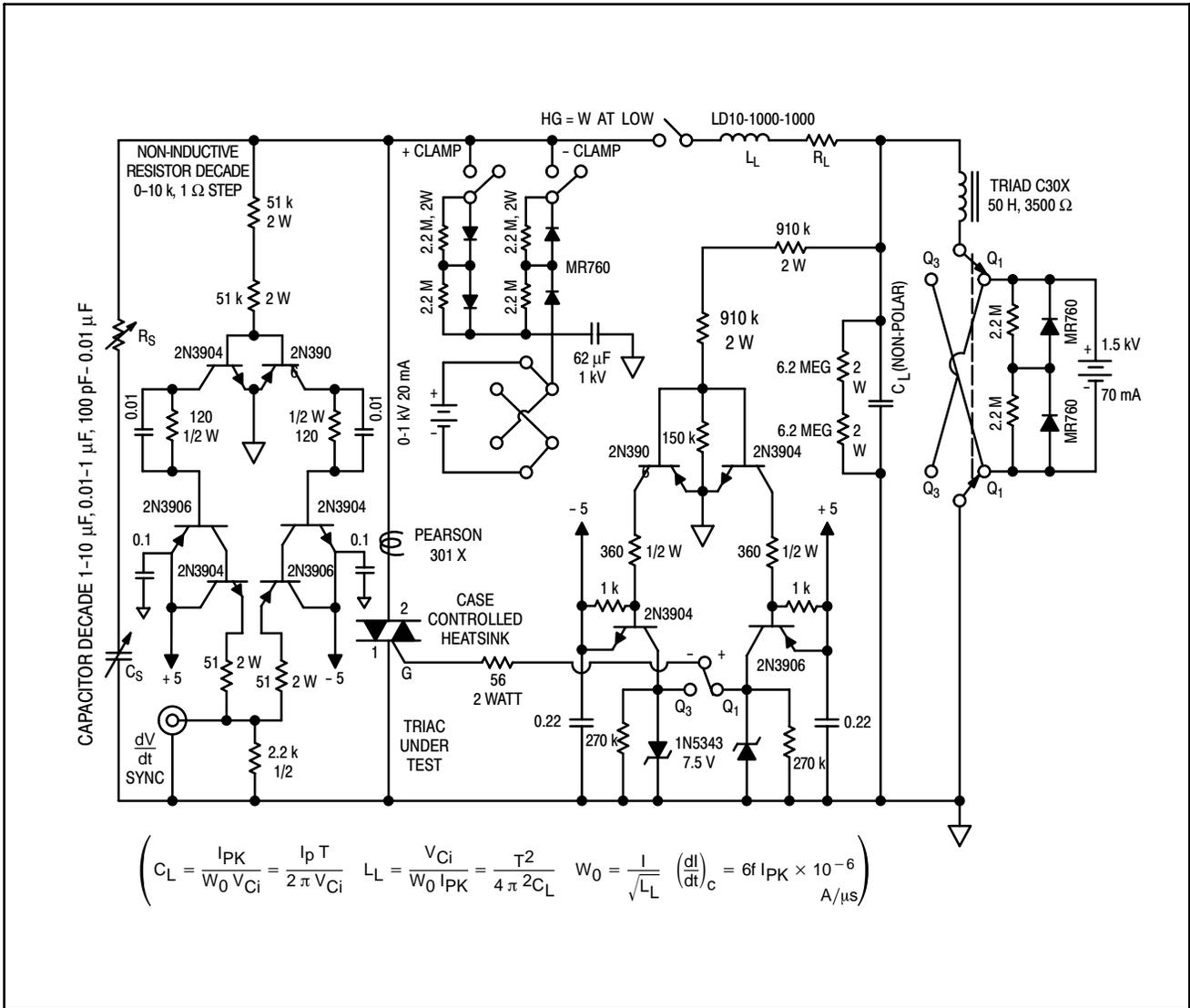
Figure 6.39. $\left(\dfrac{dV}{dt}\right)_c$ **Test Circuit For Power TRIACs**

APPENDIX C
$\frac{dV}{dt}$ DERIVATIONS

DEFINITIONS

1.0 $R_T = R_L + R_S$ = Total Resistance

1.1 $M = \dfrac{R_S}{R_T}$ = Snubber Divider Ratio

1.2 $\omega_0 = \dfrac{1}{\sqrt{L\,C_S}}$ = Undamped Natural Frequency

  ω = Damped Natural Frequency

1.3 $\alpha = \dfrac{R_T}{2\,L}$ = Wave Decrement Factor

1.4 $\chi^2 = \dfrac{1/2\,LI^2}{1/2\,CV^2} = \dfrac{\text{Initial Energy In Inductor}}{\text{Final Energy In Capacitor}}$

1.5 $\chi = \dfrac{I}{E}\sqrt{\dfrac{L}{C}}$ = Initial Current Factor

1.6 $\rho = \dfrac{R_T}{2}\sqrt{\dfrac{C}{L}} = \dfrac{\alpha}{\omega_0}$ = Damping Factor

1.7 $V_{0_L} = E - R_S\,I$ = Initial Voltage drop at t = 0 across the load

1.8 $\xi = \dfrac{I}{C_S} - \dfrac{E\,R_L}{L}$

  $\left(\dfrac{dV}{dt}\right)_0$ = Initial instantaneous $\dfrac{dV}{dt}$ at t = 0, ignoring any initial instantaneous voltage step at t = 0 because of I_{RRM}

1.9 $\left(\dfrac{dV}{dt}\right)_0 = V_{OL}\dfrac{R_T}{L} + \xi$. For all damping conditions

2.0 When I = 0, $\left(\dfrac{dV}{dt}\right)_0 = \dfrac{E\,R_S}{L}$

  $\left(\dfrac{dV}{dt}\right)_{max}$ = Maximum instantaneous $\dfrac{dV}{dt}$

  t_{max} = Time of maximum instantaneous $\dfrac{dV}{dt}$

  t_{peak} = Time of maximum instantaneous peak voltage across thyristor

  Average $\dfrac{dV}{dt} = V_{PK}/t_{PK}$ = Slope of the secant line from t = 0 through V_{PK}

  V_{PK} = Maximum instantaneous voltage across the thyristor.

CONSTANTS (depending on the damping factor):

2.1 No Damping ($\rho = 0$)
  $\omega = \omega_0$
  $R_T = \alpha = \rho = 0$

2.2 Underdamped ($0 < \rho < 1$)
  $\omega = \sqrt{\omega_0{}^2 - \alpha^2} = \omega_0\sqrt{1 - \rho^2}$

2.3 Critical Damped ($\rho = 1$)
  $\alpha = \omega_0,\ \ \omega = 0,\ \ R = 2\sqrt{\dfrac{L}{C}},\ \ C = \dfrac{2}{\alpha\,R_T}$

2.4 Overdamped ($\rho > 1$)
  $\omega = \sqrt{\alpha^2 - \omega_0{}^2} = \omega_0\sqrt{\rho^2 - 1}$

Laplace transforms for the current and voltage in Figure 40 are:

3.0 $i_{(S)} = \dfrac{E/L + SI}{S^2 + S\,\dfrac{R_T}{L} + \dfrac{1}{LC}}$; $e = \dfrac{E}{S} - \dfrac{S\,V_{0_L} - \xi}{S^2 + \dfrac{R_T}{L}\,S + \dfrac{1}{LC}}$
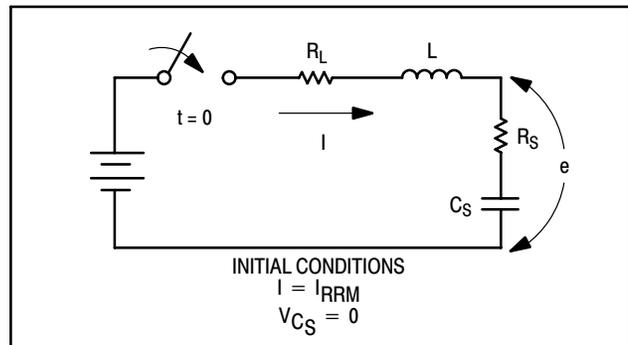
Figure 6.40. Equivalent Circuit for Load and Snubber

The inverse laplace transform for each of the conditions gives:

UNDERDAMPED (Typical Snubber Design)

4.0 $e = E - V_{0_L}\left[\text{Cos}\,(\omega t) - \dfrac{\alpha}{\omega}\sin\,(\omega t)\right]e^{-\alpha t} + \dfrac{\xi}{\omega}\sin\,(\omega t)\,e^{-\alpha t}$

4.1 $\dfrac{de}{dt} = V_{0_L}\left[2\alpha\,\text{Cos}\,(\omega t) + \dfrac{(\omega^2 - \alpha^2)}{\omega}\sin\,(\omega t)\right]e^{-\alpha t} + \xi\left[\text{Cos}\,(\omega t) - \dfrac{\alpha}{\omega}\sin\,(\omega t)\right]e^{-\alpha t}$

4.2 $t_{PK} = \dfrac{1}{\omega}\tan^{-1}\left[-\dfrac{2\alpha\,V_{0_L} + \xi}{V_{0_L}\left(\dfrac{\omega^2 - \alpha^2}{\omega}\right) - \dfrac{\xi\alpha}{\omega}}\right]$

  When M = 0, $R_S = 0, I = 0 : \omega\,t_{PK} = \pi$

4.3 $V_{PK} = E + \dfrac{\alpha}{\omega_0} - \alpha\, t_{PK} \sqrt{\omega_0{}^2\, V_{0L}{}^2 + 2\alpha\xi\, V_{0L} + \xi^2}$

  When $I = 0, R_L = 0, M = 1$:

4.4 $\dfrac{V_{PK}}{E} = (1 + e^{-\alpha\, t_{PK}})$

  Average $\dfrac{dV}{dt} = \dfrac{V_{PK}}{t_{PK}}$

4.5 $t_{max} = \dfrac{1}{\omega}ATN\left[\dfrac{\omega\,(2\alpha\xi - V_{0L}\,(\omega^2 - 3\alpha^2))}{V_{0L}(\alpha^3 - 3\alpha\omega^2) + \xi(\alpha^2 - \omega^2)}\right]$

4.6 $\left(\dfrac{dV}{dt}\right)_{max} = \sqrt{V_{0L}{}^2\,\omega_0{}^2 + 2\alpha\xi\, V_{0L} + \xi^2}\ e^{-\alpha t_{max}}$

NO DAMPING

5.0 $e = E\,(1 - Cos\,(\omega_0 t)) + \dfrac{I}{C\,\omega_0}\,\sin\,(\omega_0 t)$

5.1 $\dfrac{de}{dt} = E\,\omega_0\,\sin\,(\omega_0 t) + \dfrac{I}{C}\,Cos\,(\omega_0 t)$

5.2 $\left(\dfrac{dV}{dt}\right)_0 = \dfrac{I}{C} = 0$ when $I = 0$

5.3 $t_{PK} = \dfrac{\pi - \tan^{-1}\left(\dfrac{I}{CE\,\omega_0}\right)}{\omega_0}$

5.4 $V_{PK} = E + \sqrt{E^2 + \dfrac{I^2}{\omega_0{}^2 C^2}}$

5.5 $\left(\dfrac{dV}{dt}\right)_{AVG} = \dfrac{V_{PK}}{t_{PK}}$

5.6 $t_{max} = \dfrac{1}{\omega_0}\left[\tan^{-1}\left(\dfrac{\omega_0\,EC}{I}\right)\right] = \dfrac{1}{\omega_0}\dfrac{\pi}{2}$ when $I = 0$

5.7 $\left(\dfrac{dV}{dt}\right)_{max} = \dfrac{I}{C}\sqrt{E^2\omega_0{}^2\,C^2 + I^2} = \omega_0 E$ when $I = 0$

CRITICAL DAMPING

6.0 $e = E - V_{0L}(1 - \alpha t)e^{-\alpha t} + \xi t e^{-\alpha t}$

6.1 $\dfrac{de}{dt} = \left[\alpha\, V_{0L}\,(2 - \alpha t) + \xi(1 - \alpha t)\right]e^{-\alpha t}$

6.2 $t_{PK} = \dfrac{2 + \dfrac{\xi}{2\,V_{0L}}}{\alpha + \dfrac{\xi}{V_{0L}}}$

6.3 $V_{PK} = E - \left[V_{0L}\,(1 - \alpha\, t_{PK}) - \xi\, t_{PK}\right]e^{-\alpha\, t_{PK}}$

6.4 Average $\dfrac{dV}{dt} = \dfrac{V_{PK}}{t_{PK}}$

  When $I = 0, R_S = 0, M = 0$

  e(t) rises asymptotically to E. t_{PK} and average $\dfrac{dV}{dt}$
  do not exist.

6.5 $t_{max} = \dfrac{3\alpha V_{0L} + 2\xi}{\alpha^2 V_{0L} + \alpha\xi}$

  When $I = 0,\ t_{max} = 0$

  For $\dfrac{R_S}{R_T} \gtrsim 3/4$,

  then $\dfrac{dV}{dt}_{max} = \left(\dfrac{dV}{dt}\right)_0$

6.6 $\left(\dfrac{dV}{dt}\right)_{max}$
  $= \left[\alpha\, V_{0L}\,(2 - \alpha\, t_{max}) + \xi\,(1 - \alpha\, t_{max})\right]e^{-\alpha\, t_{max}}$

APPENDIX D

SNUBBER DISCHARGE $\dfrac{dI}{dt}$ DERIVATIONS

OVERDAMPED

1.0 $i = \dfrac{V_{CS}}{\omega\,L_S}\,\alpha^{-\alpha t}\sinh\,(\omega t)$

1.1 $i_{PK} = V_{CS}\sqrt{\dfrac{C_S}{L_S}}\ e^{-\alpha\, t_{PK}}$

1.2 $t_{PK} = \dfrac{1}{\omega}\tanh^{-1}\left[\dfrac{\omega}{\alpha}\right]$

CRITICAL DAMPED

2.0 $i = \dfrac{V_{CS}}{L_S}\,t e^{-\alpha t}$

2.1 $i_{PK} = 0.736\dfrac{V_{CS}}{R_S}$

2.2 $t_{PK} = \dfrac{1}{\alpha}$

UNDERDAMPED

3.0 $\quad i = \dfrac{V_{CS}}{\omega\,L_S}\,e^{-\alpha t}\,\sin(\omega t)$

3.1 $\quad i_{PK} = V_{CS}\sqrt{\dfrac{C_S}{L_S}}\,e^{-\alpha\,t_{PK}}$

3.2 $\quad t_{PK} = \dfrac{1}{\omega}\tan^{-1}\left(\dfrac{\omega}{\alpha}\right)$

NO DAMPING

4.0 $\quad i = \dfrac{V_{CS}}{\omega\,L_S}\,\sin(\omega t)$

4.1 $\quad i_{PK} = V_{CS}\sqrt{\dfrac{C_S}{L_S}}$

4.2 $\quad t_{PK} = \dfrac{\pi}{2\,\omega}$
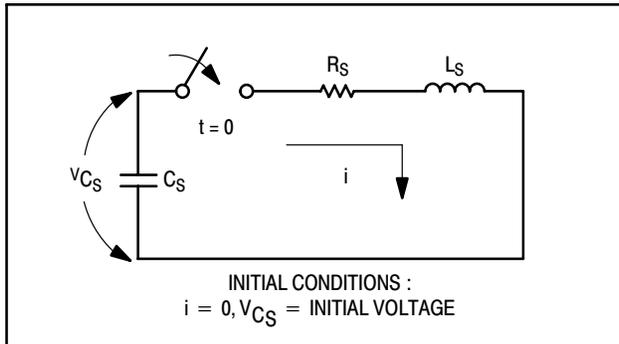
Figure 6.41. Equivalent Circuit for Snubber Discharge

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AND8005/D

Automatic AC Line Voltage Selector

ON Semiconductor

Prepared by: Alfredo Ochoa, Alex Lara & Gabriel Gonzalez
Thyristors Applications Engineers

APPLICATION NOTE

INTRODUCTION

In some cases, appliances and equipment are able to operate when supplied by two different levels of AC line voltage to their main terminals (120V or 240V). This is why, it is very common that appliances and equipment have mechanical selectors or switches as an option for selecting the level of voltage needed. Nevertheless, it is also very common that these types of equipment can suffer extensive damage caused for not putting the selector in the right position. To prevent these kind of problems, thyristors can be used as a solution for making automatic voltage selectors in order to avoid possibilities of equipment damage due to over or low voltages AC line supplied to them. Thyristors can take many forms, but they have certain things in common. All of them are solid state switches, which act as open circuits capable of withstanding the rated voltage until triggered. When they are triggered, thyristors become low impedance current paths and remain in that condition (i.e. conduction) until the current either stops or drops below a minimum value called the holding level. A useful application of triacs is a direct replacement for mechanical selectors, relays or switches. In this application, the triac furnishes on−off control and the power regulating ability of the triac is not utilized. The control circuitry for these applications is usually very simple and these circuits are useful in applications where simplicity and reliability are important. In addition, as is

well known, there is no arcing with the triac, which can also be very important in some applications.

The main disadvantages of the mechanical switches or selectors appear when they are driving high current levels that can cause arcing and sparks on their contacts each time they are activated or de−activated. Because of these kind of effects the contacts of the switches get very significantly damaged causing problems in the functionality of the equipment or appliances.

DEFINITIONS

Control Transformers. This transformer consists of two or more windings coupled by a common or mutual magnetic field. One of these windings, the primary, is connected to an alternating voltage source. An alternating flux will be produced whose amplitude will depend on the primary voltage and number of turns. The mutual flux will link the other winding, the secondary, in which it will induce a voltage whose value will depend on the number of secondary turns. When the numbers of primary and secondary turns are properly proportioned, almost any desired voltage ratio or ratio of transformation can be obtained. This transformer is also widely used in low power electronic and control circuits. There it performs such functions as matching the source impedance and its load for maximum power transfer, isolating one circuit from another, or isolating direct current while maintaining AC continuity between two circuits.

The following schematic diagram shows an automatic voltage selector for AC voltage supply of 110V/220V and load of 10 Amp rms max. Loads can be equipment or any kind of appliances:
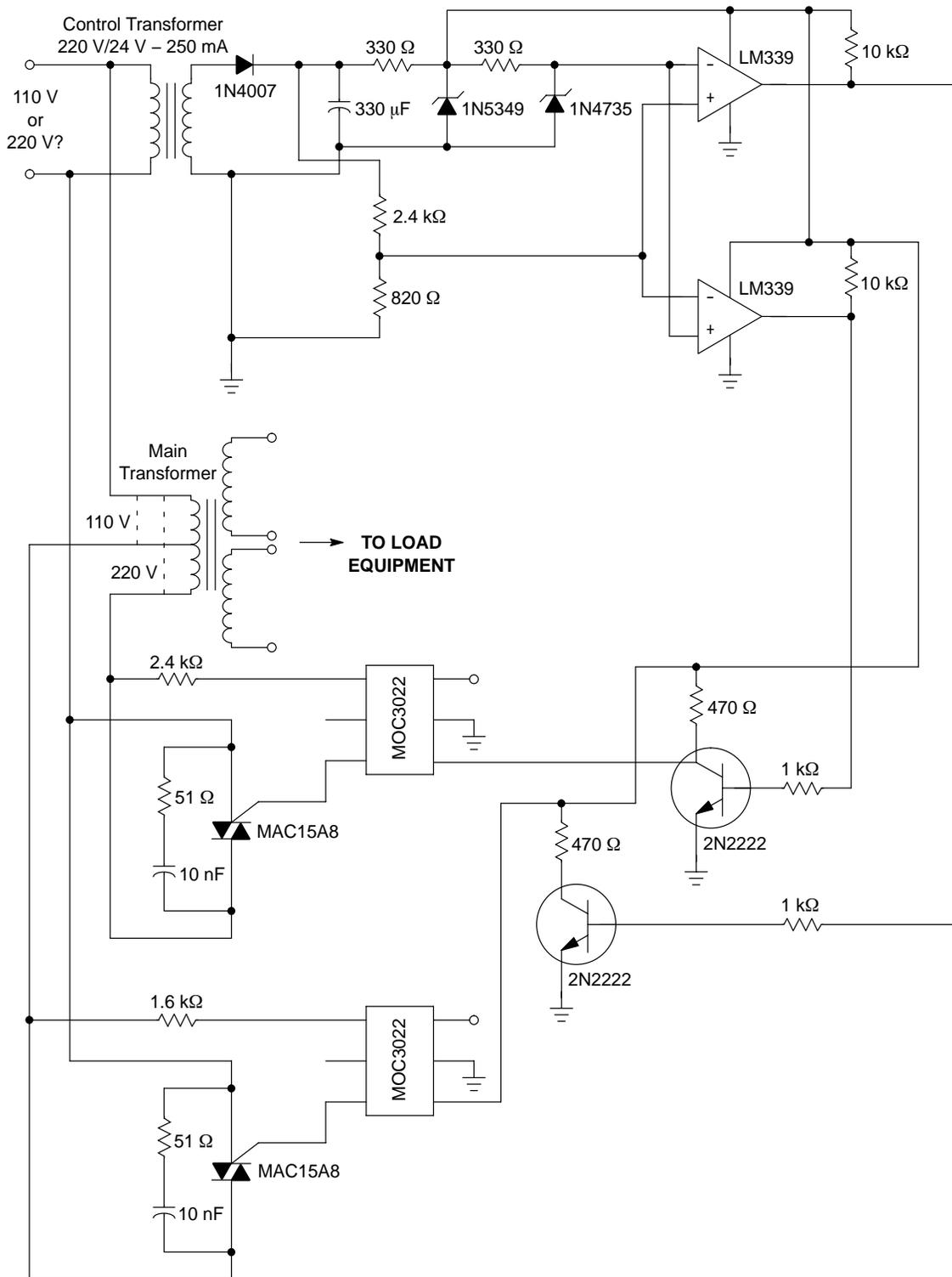
When the main terminals of the equipment are connected to the AC line voltage, one of the comparators (LM339) keeps its output at low level and the other one at high level because of the voltage references connected to their inverter and non−inverter input pins. Therefore, one of the transistors (2N2222) is activated allowing current through the LED of the optocoupler, and which triggers one of the triacs (MAC15A8) that then provides the right level of AC line voltage to the main transformer of the equipment by connecting one of the primary windings through the triac triggered.

The operational range, in the previous circuit, in the low AC line voltage condition (110V) is from 100 Vrms to 150 Vrms. This means, the triac that is driving the winding of the main transformer for 110V would keep itself triggered whenever the input voltage in the control transformer is within 100 and 150 Vrms. The operation range in high AC line voltage condition (220V) is from 180 Vrms to 250 Vrms, therefore, the triac that is driving the winding of the main transformer for 220V would keep itself triggered whenever the voltage in the control transformer is within 180 and 250 Vrms. Another very important item to take into consideration is the operational range of environmental temperature which is from 0°C to 65°C. If the circuit is working outside of these temperature limits, it very probably will experience unreliable functionality.

In conclusion, this automatic voltage selector provides a very important protection for any kind of voltage sensitive equipment or appliances against the wrong levels of AC line input voltages. It eliminates the possibility of any damage in the circuitry of the equipment caused by connecting low or high voltage to the main terminals. In addition, the total price of the electronic circuitry is inexpensive when compared to the cost of the equipment if it suffers any damage.

AND8006/D

Electronic Starter for Flourescent Lamps

Prepared by: **Alfredo Ochoa, Alex Lara & Gabriel Gonzalez**
Thyristors Applications Engineers

APPLICATION NOTE

INTRODUCTION

In lighting applications for fluorescent lamps the choice of the starter switch to be used is always very important for the designers: the cost, reliability, ruggedness, and ease to be driven must always be kept in mind. This is especially important in lighting circuits where the designer has to optimize the operating life of the fluorescent lamps by using the right starter switch.

In the large family of electronic switches, the thyristor must be considered as a low cost and powerful device for lighting applications. Thyristors can take many forms, but they have certain features in common. All of them are solid state switches that act as open circuits capable of withstanding the rated voltage until triggered. When they are triggered, thyristors become low impedance current paths and remain in that condition (i.e. conduction) until the current either stops or drops below a minimum value called the holding level. Once a thyristor has been triggered, the trigger current can be removed without turning off the device.

Silicon controlled rectifiers (SCRs) and triacs are both members of the thyristor family. SCRs are unidirectional devices while triacs are bi–directional. A SCR is designed to switch load current in one direction, while a triac is designed to conduct load currents in either direction.

Structurally, all thyristors consist of several alternating layers of opposite P and N silicon, with the exact structure varying with the particular kind of device. The load is applied across the multiple junctions and the trigger current is injected at one of them. The trigger current allows the load current to flow through the device setting up a regenerative action which keeps the current flowing even after the trigger is removed.

These characteristics make thyristors extremely useful in control applications. Compared to a mechanical switch, a thyristor has a very long service life and very fast turn on and turn off times. Because of their fast reaction times, regenerative action, and low resistance, once triggered, thyristors are useful as power controllers and transient over voltage protectors, as well as simply turning devices on and off. Thyristors are used to control motors, incandescent and fluorescent lamps, and many other kinds of equipment.

Although thyristors of all sorts are generally rugged, there are several points to keep in mind when designing circuits using them. One of the most important parameters to respect is the devices' rated limits on rate of change of voltage and current (dV/dt and di/dt). If these are exceeded, the thyristor may be damaged or destroyed.

DEFINITIONS

Ambient Sound Levels. Background noise generated by ballast and other equipment operating in a building.

Arc. Intense luminous discharge formed by the passage of electric current across a space between electrodes.

Ballast. An electrical device used in fluorescent and high intensity discharge (HID) fixtures. It furnishes the necessary starting and operating current to the lamp for proper performance.

Electrode. Metal filament that emits electrons in a fluorescent lamp.

Fluorescent lamp. Gas filled lamp in which light is produced by the interaction of an arc with phosphorus lining the lamp's glass tube.

Fluorescent light circuit. Path over which electric current flows to operate fluorescent lamps. Three major types of fluorescent lighting circuits are in use today, preheat, instant start (slimline) and rapid start.

Instant start (slimline). A class of fluorescent. Ballast provides a high starting voltage surge to quickly light the lamp. All instant start lamps have a single pin base and can be used only with instant ballast.

Rapid Start Lamps. Fluorescent lamps that glow immediately when turned on and reach full brightness in about 2 seconds.

Preheat Lamp. A fluorescent lamp in which the filament must be heated before the arc is created.

This application note is designed for Preheat Start Lamp circuit. The description of the functionality of this Lamp is described below:

HOW THE LAMP WORKS (Using the conventional glow−tube starter)
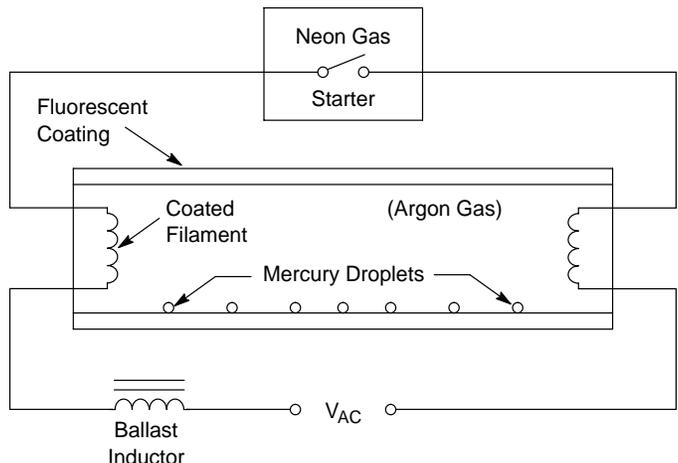
The above Figure illustrates a fluorescent lamp with the conventional glow−tube starter. The glow−tube starter consists of a bimetallic switch placed in series with the tube filament which closes to energize the filaments and then opens to interrupt the current flowing through the ballast inductor, thereby, generating the high voltage pulse necessary for starting. The mechanical glow−tube starter is the circuit component most likely to cause unreliable starting.

The principle disadvantage of the conventional glow−tube starter is that it has to open several times in the filament circuit to interrupt the current flowing through the ballast inductor in order to generate the high voltage necessary for turning−on the fluorescent lamp. However, those interactions decrease the life of the lamp considerably. Besides, the lamp turns−on in around 3 seconds when it is using the conventional glow−tube starter and it also causes degradation to the lamp.

On the other hand, the following schematic diagrams show the electronic circuitry which substitutes the conventional glow−tube starter for fluorescent lamps applications of 20 Watts and 40 Watts using a diode, SCR, and a TVS or zener clipper(s):

Fluorescent Lamp of 20 Watts
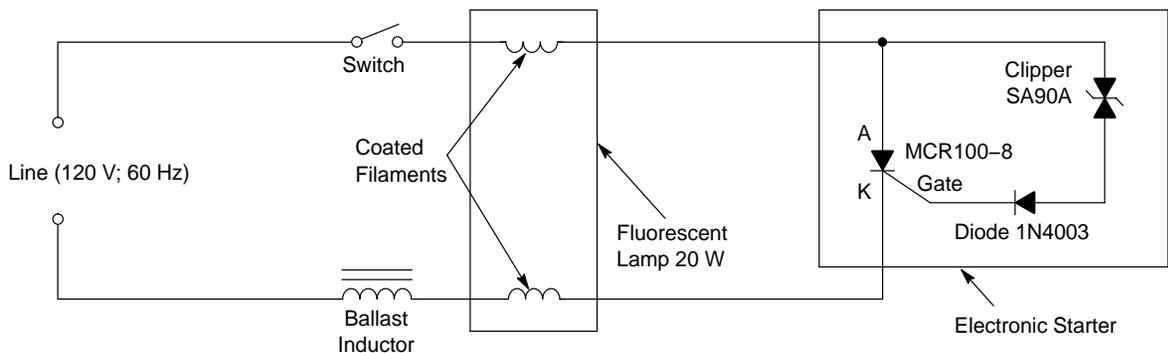
Fluorescent Lamp of 40 Watts
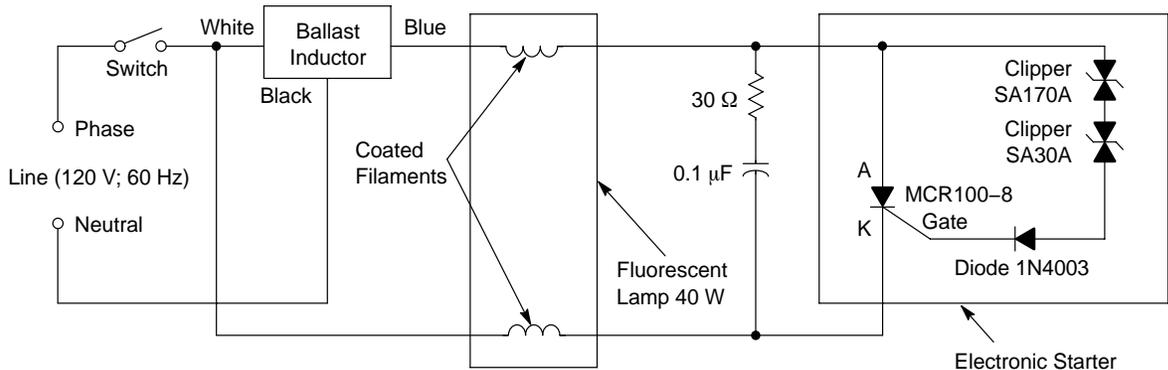
The main reason why the previous circuits are different is due to the high voltage must be generated for each kind of lamp. This means, the inductor ballast for fluorescent lamps of 40 Watts provides higher voltage than the inductor ballast for lamps of 20 Watts, that is why, the electronic circuits have to be different. As an observation, even the conventional glow–tube starters have to be selected according the power of the lamp, it means, there is not a general glow–tube starter who can operate for all kinds of fluorescent lamps.

The following plots show the voltage and current waveform in the electronic starter circuitry when the fluorescent lamps is turned–on:

Fluorescent Lamp of 20 Watts:
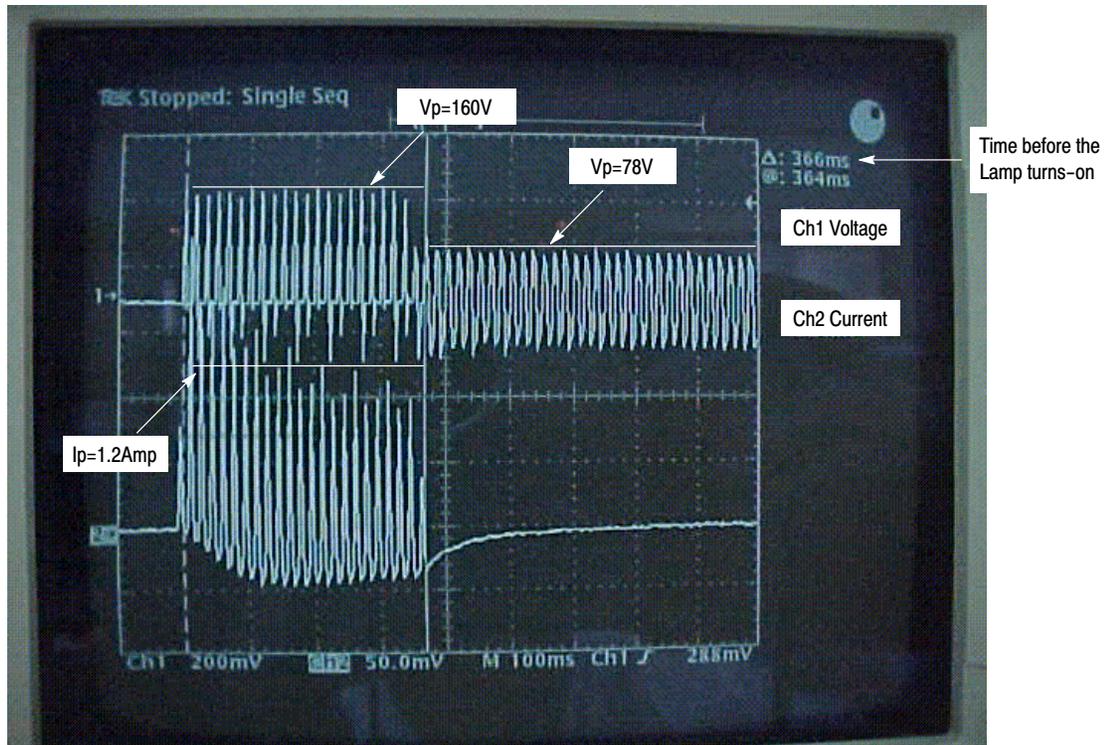
When the switch is turned–on, the voltage across the Clipper (SA90A) is the same as the voltage of the AC Line (Vpeak=160V), and since the Clipper allows current–flow through itself only once its VBR is reached (100V peak), the SCR (MCR100–8) turns–on and closes the circuit to energize the filaments of the fluorescent lamp. At this time, the current across the circuit is around 1.2A peak, and once the lamp has got enough heat, it decreases its dynamic resistance and permits current–flow through itself which causes the voltage across the Clipper to decrease to around 78 Vpeak. This effect makes the clipper turn off, since the voltage is less than the VBR of the device (SA90A), and because the clipper turns off, the SCR also turns–off, and opens the circuit to interrupt the current flowing through the ballast inductor, thereby, generating the high voltage pulse necessary for starting the lamp. The time that the fluorescent lamp will take before to turn–on is around 400 msecs by using the electronic starter. It is a faster starter then when the lamp is using the conventional glow–tube starter.

Fluorescent Lamp of 40 Watts:
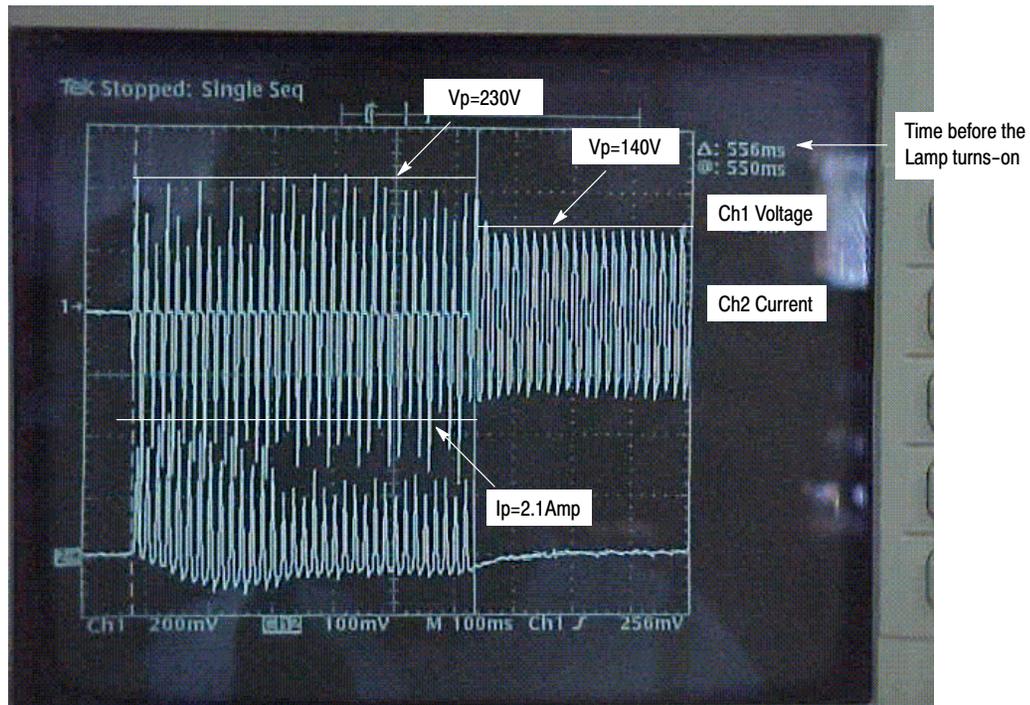
The operation of the electronic starter circuit of 40 watts is similar than for 20 watts, the only difference between them is that the Inductor Ballast of 40 watts generates higher voltage than the inductor ballast of 20 watts. That is why the schematic circuit for lamps of 40 watts has two clippers and one snubber inside its control circuit. Besides, the current flowing through this circuit is around 2.1A peak and it appears around 550 msecs (which is the time that the lamp takes before it turn itself on), longer than in the electronic starter circuit of 20 watts.

In conclusion the electronic starter circuits (for 20 and 40 watts) are more reliable than the conventional glow–tube

starters since the lamps turn–on faster and more efficiently increasing their life–time considerably. Besides, the total price of the electronic devices is comparable with the current starters (glow–tube).

In summary, it is also important to mention that the range of the AC voltage supply to the electronic starter circuits must be from 115Vrms to 130Vrms for operating correctly. If it is not within this voltage range the circuits may not be able to operate in the correct way causing unreliable starting of the lamp. Also, extreme environmental temperatures could effect the right functionality of the electronic starters but it is a fact that they can operate between 15°C to 40°C.

AND8007/D

Momentary Solid State Switch for Split Phase Motors

ON Semiconductor

APPLICATION NOTE

Prepared by: Alfredo Ochoa, Alex Lara & Gabriel Gonzalez
Thyristors Applications Engineers

INTRODUCTION

In control applications for motors the choice of the solid state switch to be used is always very important for the designers: the cost, reliability, ruggedness, and ease to be driven must always be kept in mind. This is especially important in motor control circuits where the designer has to optimize the circuitry for controlling the motors in the correct and efficient way.

In the large family of electronic switches, the thyristor must be considered as a low cost and powerful device for motor applications. Thyristors can take many forms, but they have certain features in common. All of them are solid state switches which act as open circuits capable of withstanding the rated voltage until triggered. When they are triggered, thyristors become low impedance current paths and remain in that condition (i.e. conduction) until the current either stops or drops below a minimum value called the holding level. Once a thyristor has been triggered, the trigger current can be removed without turning off the device.

Because Thyristors are reliable solid state switches, they have many applications, especially as controls. A useful application of triac is as a direct replacement for an AC mechanical relay. In this application, the triac furnishes on−off control and the power regulating ability of the triac is utilized. The control circuitry for this application is usually very simple, consisting of a source for the gate signal and some type of small current switch, either mechanical or electrical. The gate signal can be obtained from a separate source or directly from the line voltage at terminal MT2 of the triac.

One of the most common uses for thyristors is to control AC loads such as electric motors. This can be done either by controlling the part of each AC cycle when the circuit conducts current (Phase control) or by controlling the number or cycles per time period when current is conducted (cycle control). In addition, thyristors can serve as the basis of relaxation oscillators for timers and other applications.

DEFINITIONS

Split−Phase Motor. Split−Phase motors have two stator windings, a main winding and an auxiliary winding, with their axes displaced 90 electrical degrees in space. The auxiliary winding has a higher resistance−to−reactance ratio than the main winding, so that the two currents are out of phase. The stator field thus first reaches a maximum about the axis of one winding and then somewhat later in time (about 80 to 85 electrical degrees) reaches a maximum about the axis of the winding 90 electrical degrees away in space. The result is a rotating stator field which causes the motor to start. At about 75 percent of synchronous speed, the auxiliary winding is cut out by a centrifugal switch.

The below figure shows an schematic representation of a split−phase motor:
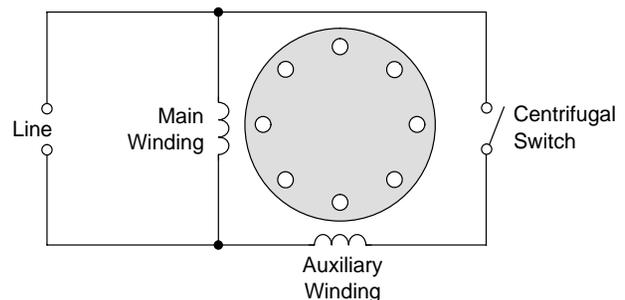
When the line voltage is applied, the current flows through both windings and the result is a rotating stator field which causes the motor to start. At about 75 percent of synchronous speed, the auxiliary winding is cut out by a centrifugal switch.

The following figure shows a conventional schematic diagram using a relay for controlling a split–phase fractional horsepower motor (the compressor of a refrigerator for example):
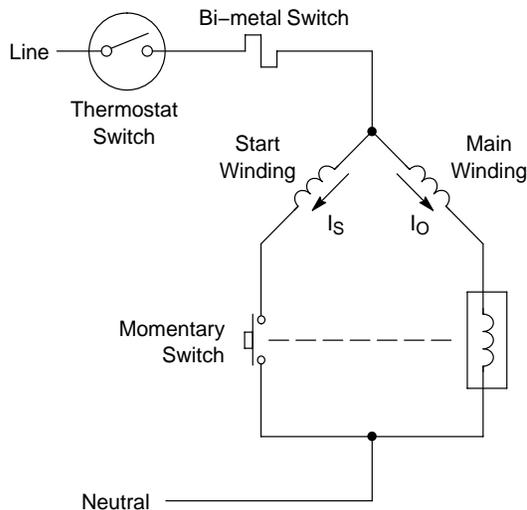
In the previous figure the thermostat–switch is controlling the working–cycle of the compressor and it is dependent on the set point of environment temperature which has to be selected according to the temperature needed. The bi–metal switch protects the compressor against overload and the relay controls the momentary switch which cuts out the starter winding once the motor has reached about 75 percent of the synchronous speed (after around 300 msecs).

The below plot shows the current flowing through the compressor (1 Phase, 115Vac, 60Hz, 4.1Arms) when it starts to operate under normal conditions:
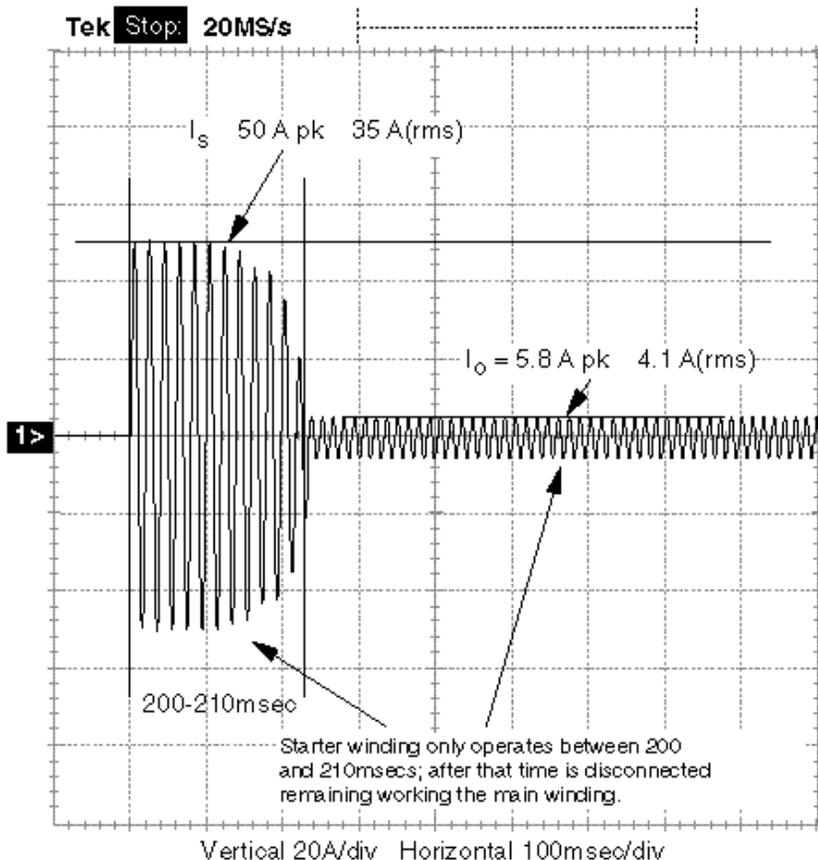
This plot shows the total current flowing through the compressor when it starts to operate and the time in which the current reaches the maximum value (Is) due to the start of the motor. After this time (210 msecs) the start winding is cut out by the momentary switch and then the current decreases to reach the nominal current of the compressor (Io=4.1 Arms).

The following schematic diagrams show the way triacs can substitute for the relay and how they can be triggered by using different control options:

Non−sensitive Gate TRIAC
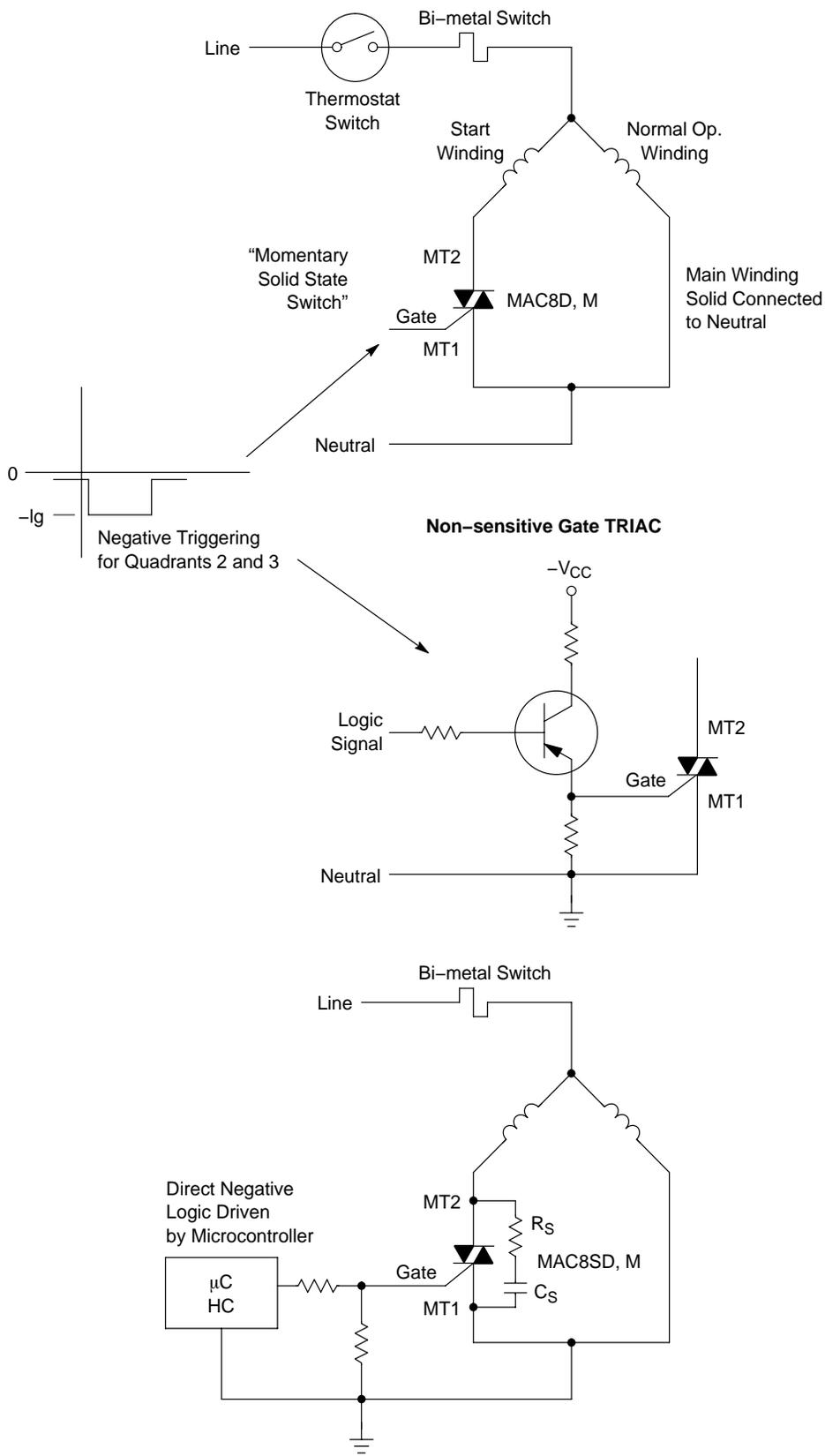
In the first diagram, the triac (MAC8D,M) is making the function of the conventional relay's momentary switch, and it can be triggered by using a transistor as shown in the above schematic or through the signals of a microcontroller. Since this triac (MAC8D,M) is a snubber–less device, it does not need a snubber network for protecting itself against dV/dt phenomena.

In the second diagram the triac (MAC8SD,M) is also performing the function of the relay's momentary switch,

but since this device is a sensitive gate triac, it only needs a very low Igt current for triggering itself, therefore, this option is especially useful in applications where the level of the current signals are small.

On the other hand, the following figure shows a practical solid state solution for controlling the compressor with the operating characteristics mentioned previously (1 Phase, 115Vac, 60Hz, 4.1 Arms) :
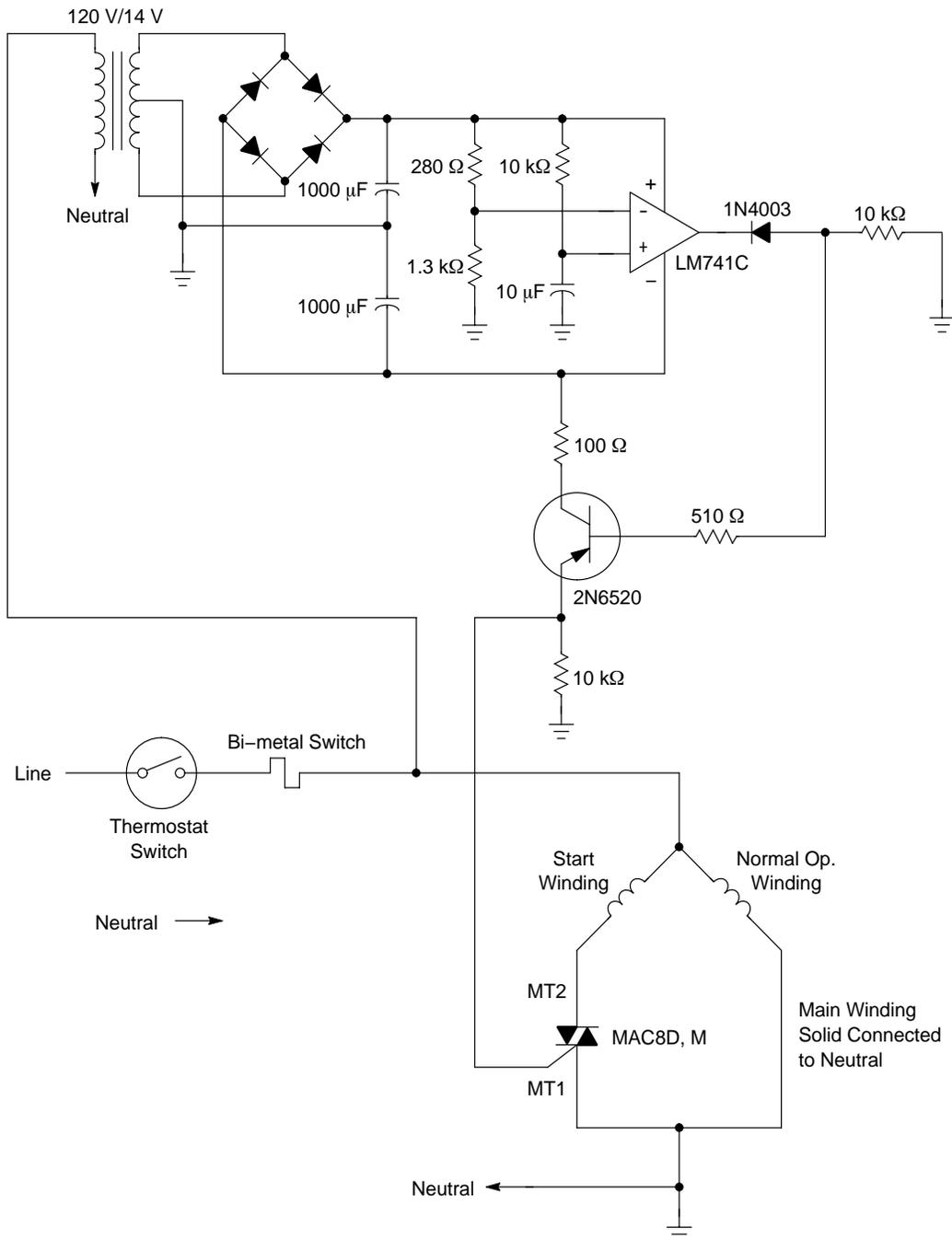
When the thermostat switch is activated, the triac (MAC8D,M) turns−on and allows current flow through the starter winding. This current is around 20 Arms because at the start of the motor (see current plot shown previously), after around 210msec, the triac turns−off and blocks the current flowing through the starter winding. In that moment, the total current flowing through the motor decreases until it reaches the nominal current (4.1 Arms) and the motor continues operating until the thermostat switch is switched off.

Since the triac operates for very short times (around 210 msec), it does not need a heat sink, therefore, it can be placed on the control board without any kind of problems.

In the previous schematic diagram the triac of 8 Arms (MAC8D,M), was selected based on the nominal and start current conditions of the compressor previously described (1 Phase, 115Vac, 60Hz, 4.1Arms). Therefore, it is important to mention that in these kind of applications, the triacs must be selected taking into consideration the characteristics of each kind of motor to control (nominal and start currents, frequency, Vac, power, etc). Also, it is important to remember that it is not possible to have a general reference for selecting the right triacs for each motor control application.

In conclusion, the solid state solution described previously, provides a more reliable control than the conventional momentary switch controlled by a relay since the thyristors do not cause any kind of sparks when they start to operate. In addition, the total price of the electronic components do not exceed the price of the conventional relay approach.

In summary, it is also important to mention that extreme environmental temperatures could affect the functionality of this momentary solid state switch, but it is a fact that the triac solution is able to operate between 0°C to 65°C.

Another important consideration is to include in the power circuit of the motor the right overload switch in order to protect the motor and the triacs against overload phenomena.

AND8008/D

Solid State Control Solutions for Three Phase 1 HP Motor

ON Semiconductor

Prepared by: Alfredo Ochoa, Alex Lara & Gabriel Gonzalez
Thyristors Applications Engineers

INTRODUCTION

In all kinds of manufacturing, it is very common to have equipment that has three phase motors for doing different work functions on the production lines. These motor functions can be extruders, fans, transport belts, mixers, pumps, air compressors, etc. Therefore, it is necessary to have equipment for controlling the start and stop of the motors and in some cases for reversing them. Actually, one of the most common solutions for performing this control functions is by using three phase magnetic starters. It consists of a block with three main mechanical contacts which provide the power to the three main terminals of the motor once its coil is energized. However, the magnetic starter has a lot of disadvantages and the most common appear when they are driving high current levels that can cause arcing and sparks on their contacts each time they are activated or de–activated. Because of these kind of effects the contacts of the magnetic starters get very significantly damaged causing problems in their functionality. With time it can cause bad and inefficient operation of the motors. This is why, thyristor should be considered as a low cost alternative and indeed a powerful device for motor control applications. Thyristors can take many forms but they have certain features in common. All of them are solid state switches that act as open circuits capable of withstanding the rated voltage until triggered. When they are triggered, thyristors become low impedance current paths and remain in that condition (i.e. conduction) until the current either stops or drops below a minimum value called the holding level. Once a thyristor has been triggered, the trigger current can be removed without turning off the device.

DEFINITIONS

Three phase induction motor.

A three phase induction motor consists of a stator winding and a rotor of one of the two following types: one type is a squirrel–cage rotor with a winding consisting of conducting bars embedded in slots in the rotor iron and short circuited at each end by conducting end rings. The other type is a wound rotor with a winding similar to and having the same number of poles as the stator winding, with the terminals of the winding being connected to the slip rings or collector rings on the left end of the shaft. Carbon brushes bearing on these rings make the rotor terminals available at points external to the motor so that additional resistance can be inserted in the rotor circuit if desired.

Three phase voltages of stator frequency are induced in the rotor, and the accompanying currents are determined by the voltage magnitude and rotor impedance. Because they are induced by the rotating stator field, these rotor currents inherently produce a rotor field with the same number of poles as the stator and rotating at the same speed with respect to the stationary rotor. Rotor and stator fields are thus stationary with respect to each other in space, and a starting torque is produced. If this torque is sufficient to overcome the opposition to rotation created by the shaft load the motor will come up to its operating speed. The operating speed can never equal the synchronous speed of the stator field.

The following figure shows a three phase 1HP motor controlled through a conventional magnetic starter which has an over–load relay for protecting the motor against over–load phenomena.

Power Schematic

220 V$_{rms}$ 60 Hz
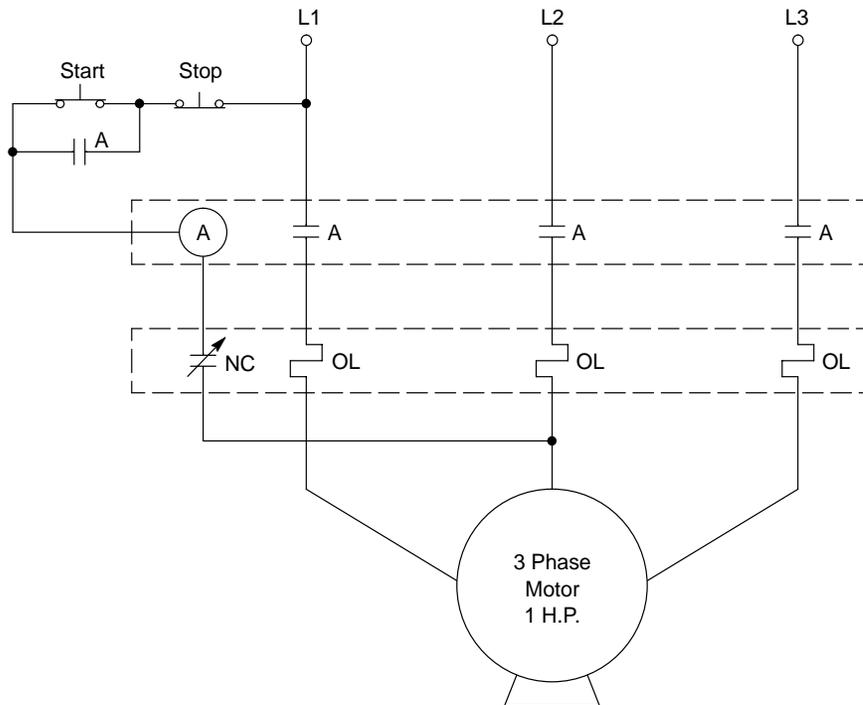
When the start button is pushed on, the coil of the magnetic starter (A) is energized, thereby, the mechanical switch contacts close allowing current−flow through the motor which starts it to operate. If the stop button is pushed, the coil (A) will be de−energized causing the motor to stop because of the mechanical switch contacts opened. In addition, if an overload phenomena exists in the circuit of the motor, the switch contact (NC) of the overload relay will open de−energizing the coil and protecting the motor against any kind of damage.

Magnetic starters have a lot of disadvantages like arcing, corrosion of the switch contacts, sparks, noisy operation, short life span, etc. Therefore, in some motor applications, it is not useful to control the motors by using magnetic starters since the results can be undesirable.

On the other hand, the following schematic diagrams show how thyristors can perform the same control function for starting and stopping a three phase 1HP motor. In addition, the diagrams below show an over load circuit for protecting the motor against overload phenomena.
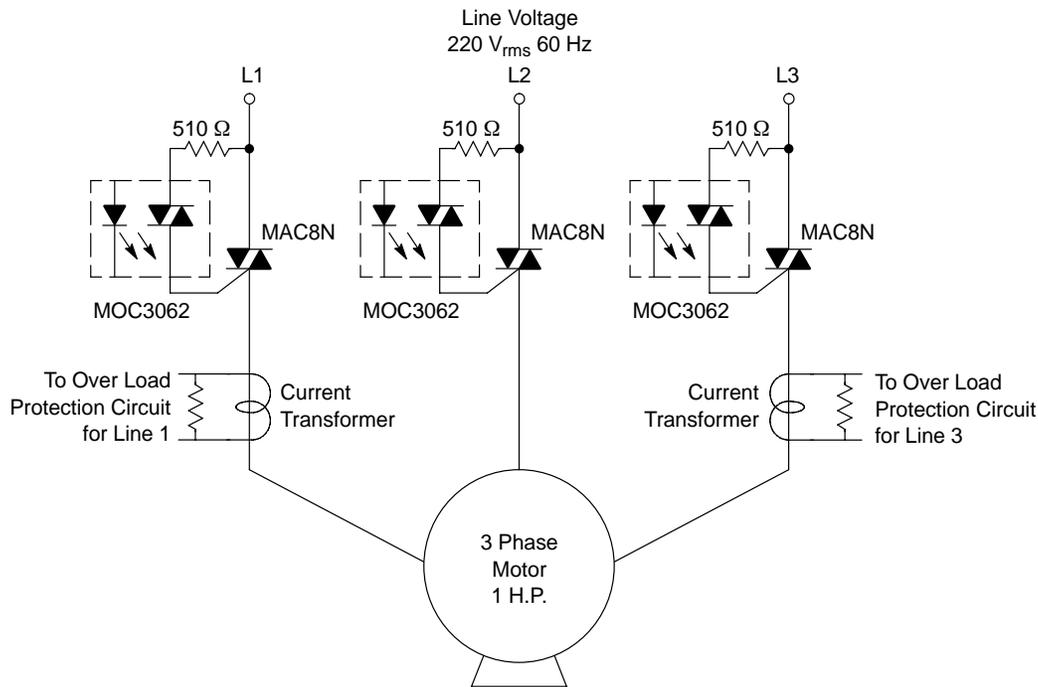
Diagram 1

Diagram 1 shows how three triacs (MAC8M) substitute the mechanical contacts of the conventional magnetic starter (shown previously) for supplying the power to the three phase 1HP motor once the triacs are triggered.

It is important to mention that the optocoupler devices (MOC3061) will supply the signal currents to the triacs and hence the motor keeping the same phase shifting (120 electrical degrees) between lines. This is because these optocuplers (MOC3061) have zero crossing circuits within them.

Another important thing must be considered as a protection for the triacs (MAC8M) against fast voltage transients, is a RC network called snubber which consists of a series resistor and capacitor placed around the triacs. These components along with the load inductance from a series CRL circuit.

Many RC combinations are capable of providing acceptable performance. However, improperly used snubbers can cause unreliable circuit operation and damage

to the semiconductor device. Snubber design involves compromises. They include cost, voltage rate, peak voltage, and turn−on stress. Practical solutions depend on the device and circuit physics.

Diagram 2 shows an electronic over−load circuit which provides very reliable protection to the motor against over load conditions. The control signals for the two electronic over−load circuits are received from the shunt resistors connected in parallel to the two current transformers placed in two of the three main lines (L1, L3) for sensing the current flowing through the motor when it is operating. The level of the voltage signals appearing in the shunt resistors is dependent on the current flowing through each main line of the motor. Therefore, if it occurs, that an over load condition in the power circuit of the motor, that voltage level will increase its value causing the activation of the electronic over−load circuits which will stop the motor by protecting it against the over−load condition experienced.

Over Load Protection Circuit for Line 1 **Diagram 2**
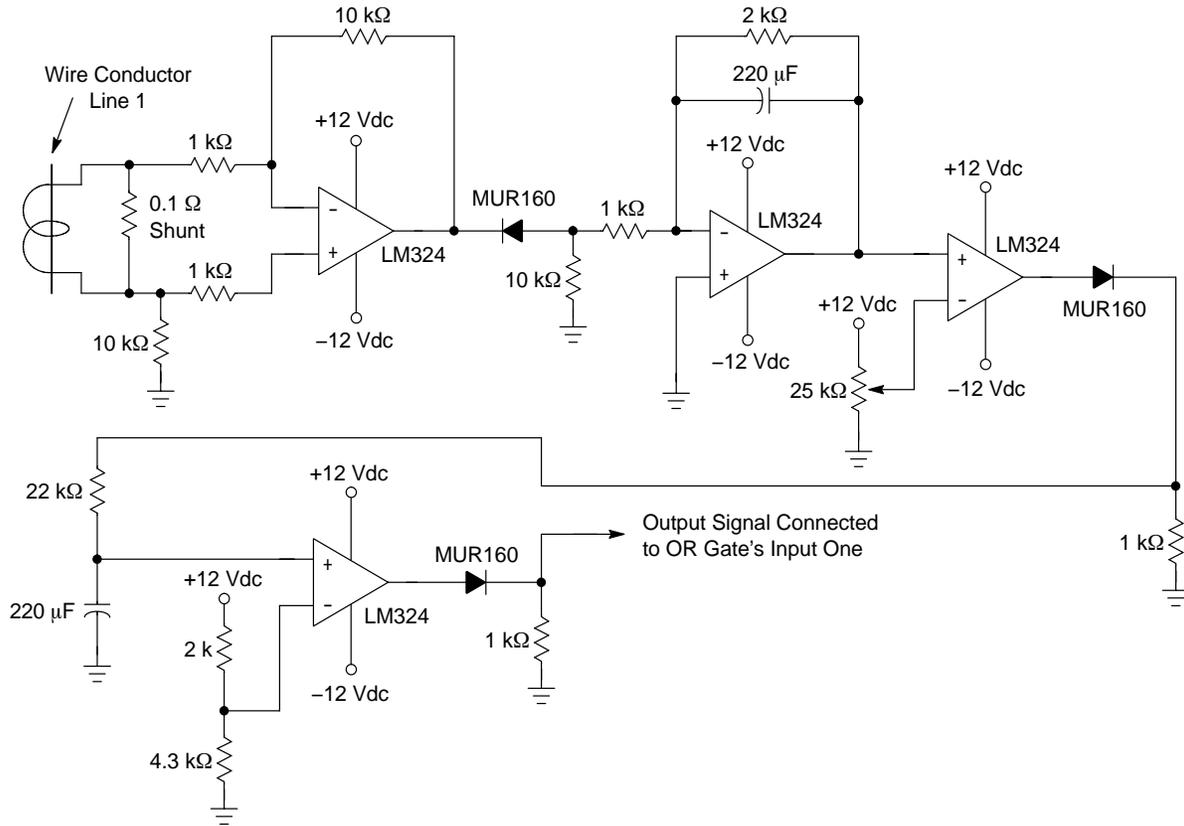
Over Load Protection Circuit for Line 3
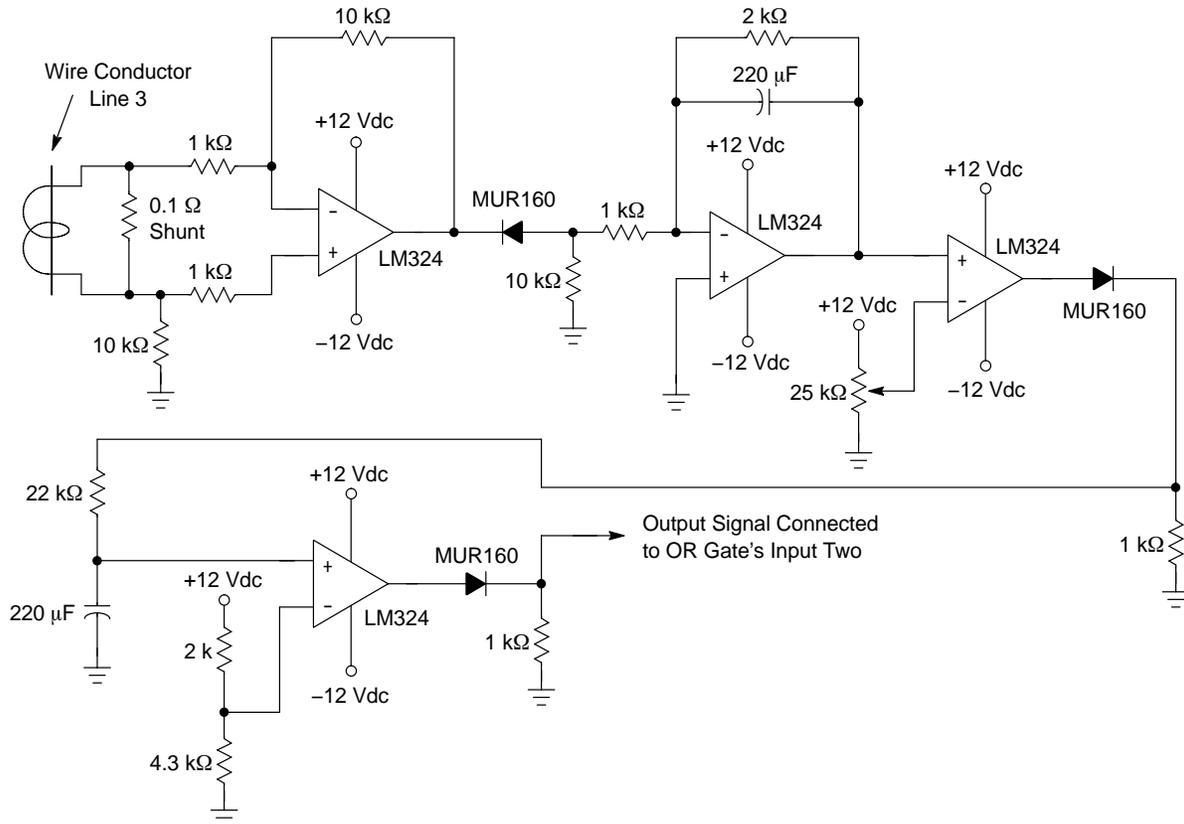
Start/Stop Control Circuit   **Diagram 3**

Output Signal from
Over Load Protection
Line 1

Output Signal from
Over Load Protection
Line 3

MC14075

Stop
Button

+12 Vdc

1 kΩ

CD

MC14013

Q̄

SD

+12 Vdc

Start
Button

1 kΩ

+12 Vdc

510 Ω

1.5 kΩ

2N2222

MOC3062

MOC3062

MOC3062
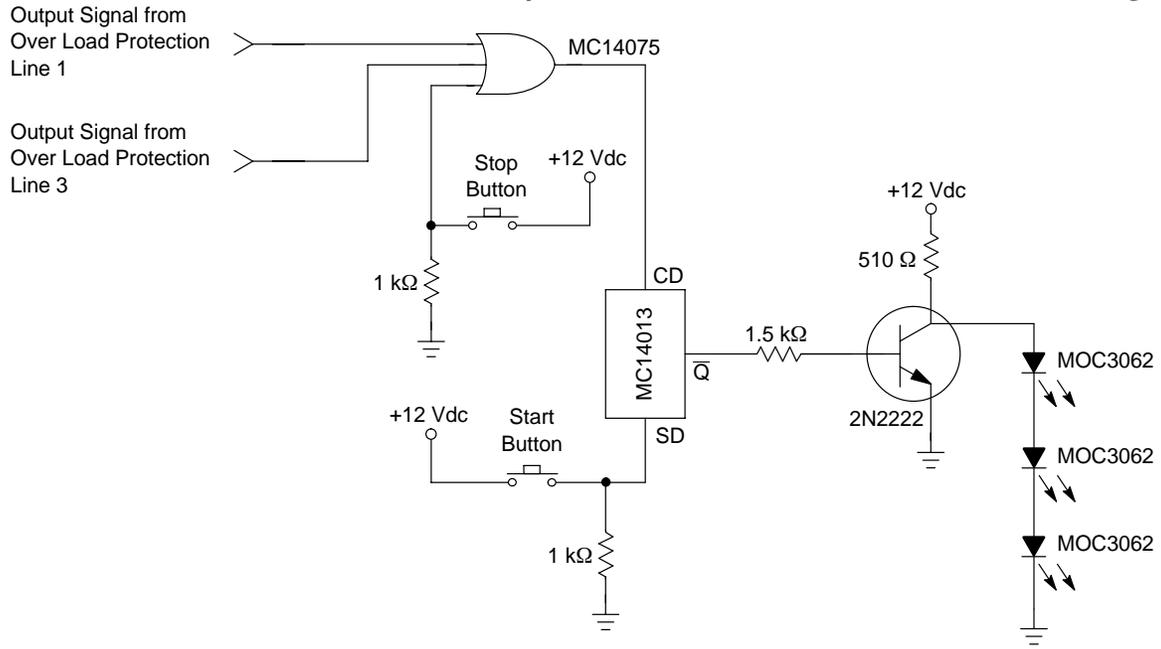
Diagram 3 shows the main electronic control circuit for controlling the start and stop of the motor each time it is needed. If the start button is pushed on, the Flip Flop (MC14013) is activated triggering the transistor (2N2222) which turns on the optocoupler's LED's which in turn the three triacs (MAC8M) get triggered and finally starts the motor. The motor will stop to operate, whenever the stop button is pushed or any overload condition occurs in the power circuit of the motor.

The following plot shows the motor's start current waveform on one of the three phases when the motor starts to operate under normal operation conditions and without driving any kind of mechanical load:

Tek Stop Single Seq 2kS/s

Ipk = 28.8 Amp
start current

Ipk = 2.8 Amp
Normal operation

128 msec

Ch1   1 V   M 25ms   Ch1   20mV

1 Sep 1999
15:00:15
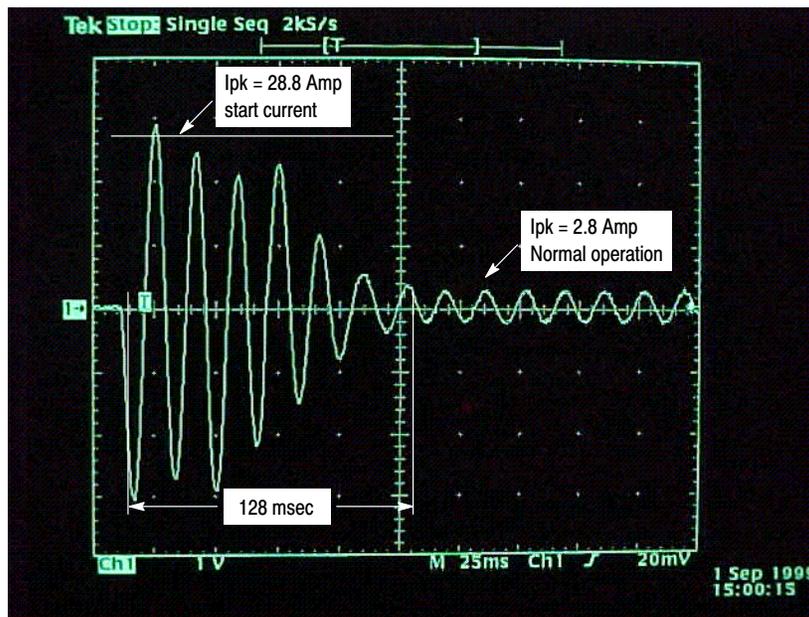
This other plot shows the motor's start current waveform of the three phases when the motor start to operate under normal operation conditions and without mechanical load.
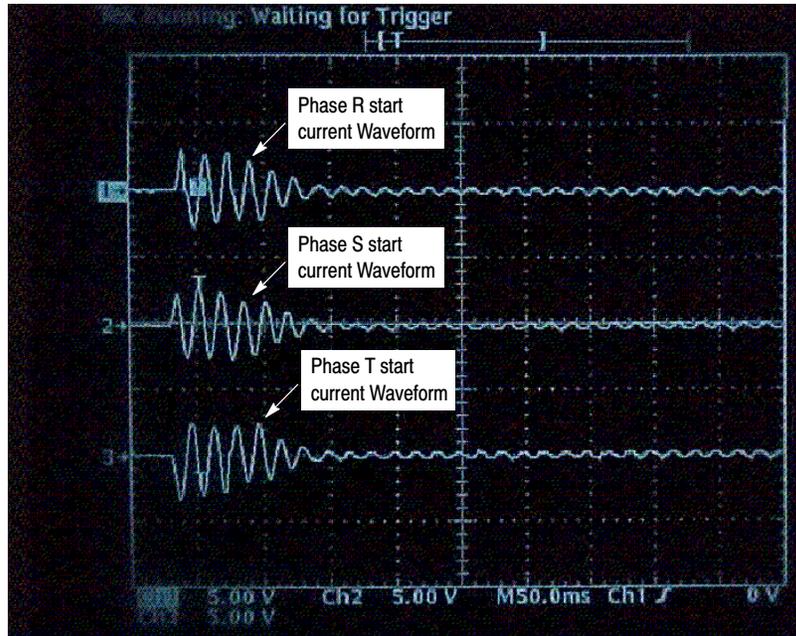
The previous plots show the maximum start current IPK of the motor when it starts to operate and how long it takes before the current reaches its nominal value. Here, It is important to mention that the triacs (MAC8N) were selected by taking into consideration the motor's start current value as well as the ITSM capability of these devices. Therefore, if it is needed to control motors with higher power (more than 1HP), first, it would be necessary to characterize them in order to know their current characteristics. Next be able to select the right triacs for controling the motor without any kind of problems.

Another important item must be considered if it is needed to control motors with higher power. These are the electronic over–load circuits, which have to be adjusted taking into consideration the level of overload current that is needed to protect, and is dependent on the kind of motor that is being controlled.

Based in the previous diagrams and plots, it has been proven that triacs can substitute the function of the magnetic starters for starting and stopping a three phase 1HP motor as well as for protecting it against overload conditions.

The following schematics show a solid state solution for controlling and reversing a three phase 1HP motor:

Reverse Control Schematic

Schematic 1 shows the control diagram for controlling and reversing the motor depending on which direction it is needed to operate. If the right–button is pushed–on, the triacs number 1, 2, and 3 (shown in the schematic 2) will be activated, thereby, the motor will operate in the right direction. If the left button is pushed–on, the triacs numbered 1, 4, and 5 will be activated causing the left operation of the motor. Because of the design of the control circuit, it is possible to reverse the motor without stopping it once it is operating in right direction. This means, it is not necessary to stop the motor in order to reverse itself.

Nevertheless, it is important to mention that the control circuit takes a delay–time (of around 3 seconds) before it activates the other triacs (1,4,5) for reversing the motor. This delay is to assure that the triacs operating (1,2,3) will be completely in the off state before it turns–on those other triacs. This delay–time is very important because if the triacs for reversing the motor are activated before the other triacs triggered have reached their completely turned–off state, it may cause a big short circuit between phases. If this happens the triacs will be damaged.

Power Schematic   **Schematic 2**

220 V$_{rms}$ 60 Hz

3 Phase
Motor
1 H.P.

Schematic 2 shows the power diagram for reversing a three phase 1HP motor. The way it makes this reverse function control is by changing the phases–order supplied to the motor through the triacs (number 4 and 5) and it is based in the motor's principle for reversing itself. This diagram also shows two current transformer placed in two of the three main lines of the motor for sending the control signals to the electronic overload circuit described previously. So this means, that the same overload concept is applicable to these schematics as well as the motor's start current waveforms and characteristics shown and explained previously.

In conclusion, it is proven that thyristors can substitute to the magnetic starters for making three phase motor control function in more efficient ways. Because thyristors are very reliable power switches, they can offer many advantages in motor applications. Some of the advantages of triacs as replacements for relays include:

- High Commutating di/dt and High Immunity to dv/dt @ 125°C

- Small size and light weight.
- Safety – freedom form arcing and spark initiated explosions.
- Long life span – contact bounce and burning eliminated.
- Fast operation – turn–on in microseconds and turn–off in milliseconds.
- Quiet operation.

The above mentioned points are only some of the big advantages that can be had if thyristors are used for making motor control function. Besides, the total cost of the previous control and power circuits does not exceed to the cost of the conventional magnetic starters.

One more consideration is that extreme environmental temperatures could effect the functionality of the electronic control circuits described herein. Therefore, if the operation is needed under extreme ambient temperatures, the designer must evaluate the parameter variation of all the electronic devices in order to assure the right operation in the application circuit.

Long Life Incandescent Lamps using SIDACs

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http://onsemi.com

APPLICATION NOTE

Abstract

Since the invention of the incandescent lamp bulb by the genius Thomas A. Edison in 1878, there has been little changes in the concept. Nowadays we are currently use them in our houses, and they are part of our comfort but, since we are more environmentally conscious and more demanding on energy cost saving products, along with their durability, we present here an application concept involved this simple incandescent lamp bulb in conjunction with the Bilateral Trigger semiconductor device called SIDAC, offering an alternative way to save money in energy consumption and also giving a longer life time to the lamp bulbs.

Theory of the SIDAC

The SIDAC is a high voltage bilateral trigger device that extends the trigger capabilities to significantly higher voltages and currents than have been previously obtainable, thus permitting new, cost effective applications. Being a bilateral device, it will switch from a blocking state to a conducting state when the applied voltage of either polarity exceeds the breakover voltage. As in other trigger devices, the SIDAC switches through a negative resistance region to the low voltage on−state and will remain on until the main terminal current is interrupted or drops below the holding current.

SIDAC's are available in the large MKP3V series and the economical, easy to insert, small MKP1V series axial lead packages. Breakdown voltages ranging from 110 to 250V are available. The MKP3V devices feature bigger chips and provide much greater surge capability along with somewhat higher RMS current ratings.

The high voltage and current ratings of SIDACs make them ideal for high energy applications where other trigger devices are unable to function alone without the aid of additional power boosting components.

The following figure shows the idealized SIDAC characteristics:
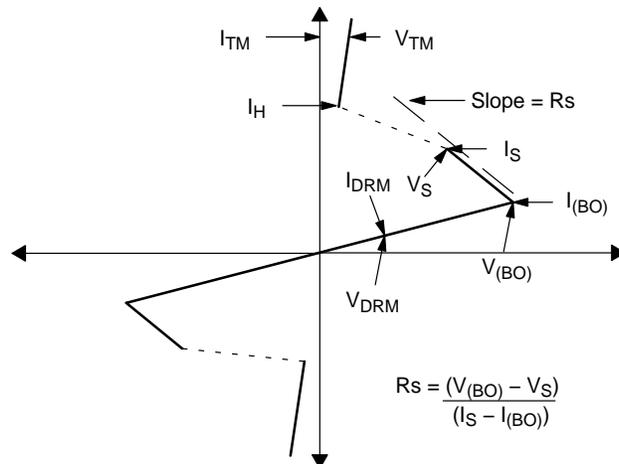
$$Rs = \frac{(V_{(BO)} - V_S)}{(I_S - I_{(BO)})}$$

Once the input voltage exceeds V(BO), the device will switch on to the forward on−voltage VTM of typically 1.1 V and can conduct as much as the specified repetitive peak on state current ITSM of 20A (10μs pulse, 1KHz repetition frequency).

SIDACs can be used in many applications as transient protectors, Over Voltage Protectors, Xeon flasher, relaxation oscillators, sodium vapor lamp starters, etc.

This paper explains one of the most typical applications for SIDACs which is a long life circuit for incandescent lamps.

The below schematic diagrams show the configurations of a SIDAC used in series with an incandescent lamp bulb through a fixed phase for the most typical levels of ac line voltages:

Option 1: ac line voltage 110V, 60Hz or 50Hz
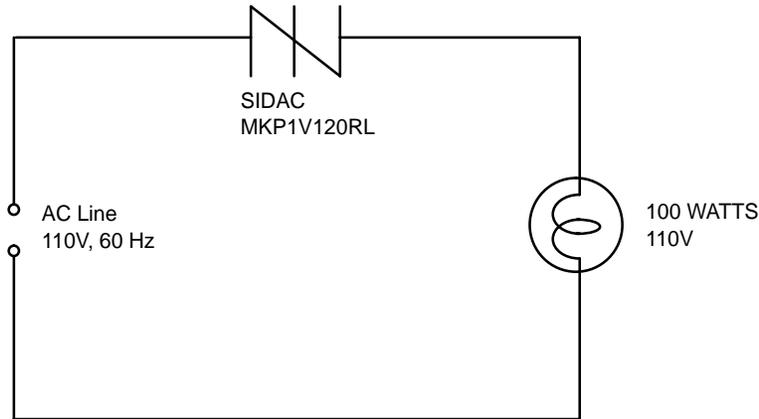
Option 2: ac line voltage 220V, 60Hz or 50 Hz

This is done in order to lower the RMS voltage to the filament, and prolong the life of the bulb. This is particularly useful when lamps are used in hard to reach locations such as outdoor lighting in signs where replacement costs are high. Bulb life span can be extended by 1.5 to 5 times depending on the type of lamp, the amount of power reduction to the filament, and the number of times the lamp is switched on from a cold filament condition.

The operating cost of the lamp is also reduced because of the lower power to the lamp; however, a higher wattage bulb is required for the same lumen output. The maximum possible energy reduction is 50% if the lamp wattage is not increased. The minimum conduction angle is 90° because the SIDAC must switch on before the peak of the line voltage. Line regulation and breakover voltage tolerances will require that a conduction angle longer than 90° be used, in order to prevent lamp turn−off under low line voltage conditions. Consequently, practical conduction angles will run between 110° and 130° with corresponding power reductions of 10% to 30%.

The following plots show the basic voltage and current waveforms in the SIDAC and load:

Incandescent Lamp of 100W, 110V, 60Hz
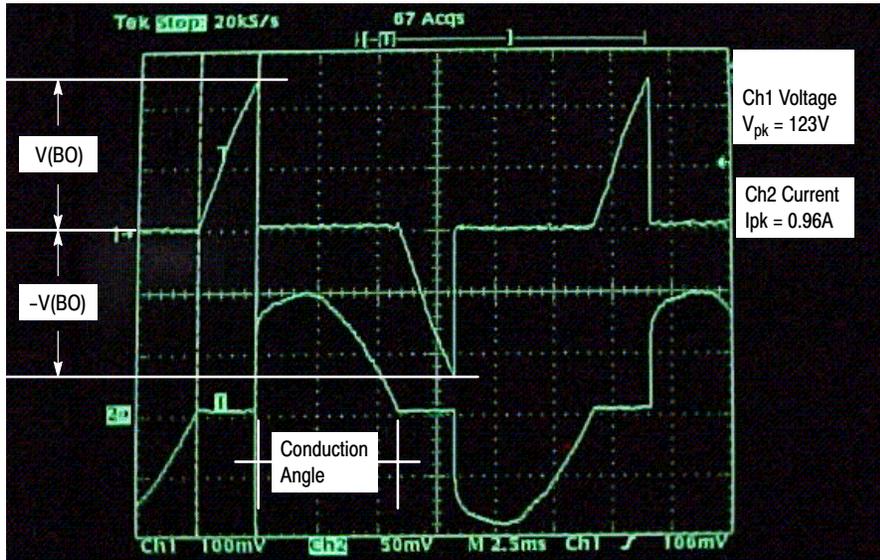
Incandescent Lamp of 50W, 220V, 60Hz
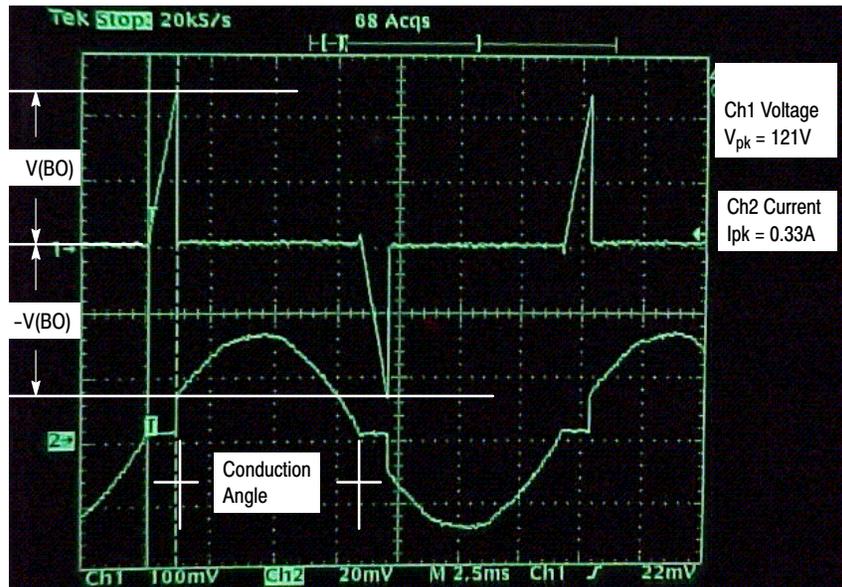
In both previous cases, once the ac line voltage reaches the V(BO) of the SIDAC (MKP1V120RL), it allows current flow to the incandescent lamp causing the turn−on of this at some specific phase−angle which is determined by the SIDAC because of its V(BO).

The fast turn−on time of the SIDAC will result in the generation of RFI which may be noticeable on AM radios operated in the vicinity of the lamp. This can be prevented by the use of an RFI filter. A possible filter can be the following: connect an inductor (100μH) in series with the SIDAC and a capacitor (0.1μF) in parallel with the SIDAC and inductor. This filter causes a ring wave of current through the SIDAC at turn on time. The filter inductor must be selected for resonance at a frequency above the upper frequency limit of human hearing and as low below the start of the AM broadcast band as possible for maximum harmonic attenuation. In addition, it is important that the filter inductor be non−saturating to prevent di/dt damage to the SIDAC.

The sizing of the SIDAC must take into account the RMS current of the lamp, thermal properties of the SIDAC, and the cold start surge current of the lamp which is often 10 to 20 times the steady state load current. When lamps burn out, at the end of their operating life, very high surge currents which could damage the SIDAC are possible because of arcing within the bulb. The large MKP3V device is recommended if the SIDAC is not to be replaced along with the bulb.

In order to establish what will be the average power that an incandescent lamp is going to offer if a SIDAC (MKP1V120RL) is connected in series within the circuit, some ideal calculations could be made for these purposes

Example: Incandescent lamp of 100W (120V, 60Hz).
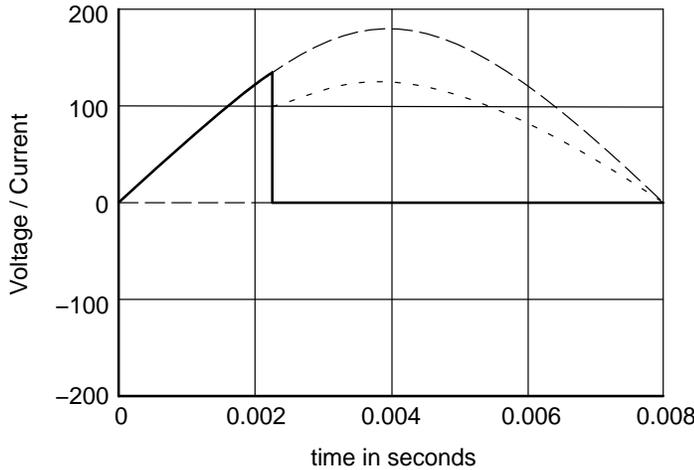
v(t): ————
i(t) x 100: - - - - - - - - - -
V_L(t): — — — — — —

v(t): Voltage waveform in the SIDAC
I(t):   Portion of current waveform applied to the load
(Multiplied by a factor of 100 to make it more graphically
visible)
V_L(t): Voltage waveform in the Load

In this case, the conduction angle is around 130° (6 msecs) in each half cycle of the sinusoidal current waveform, therefore, the average power of the lamp can be obtained by calculating the following operations:

$$i_{eff} = \sqrt{\frac{2}{T} \times \int_0^{8.33 \times 10^{-3}} i(t)^2 dt}$$

$$v_{eff} = \sqrt{\frac{2}{T} \times \int_0^{8.33 \times 10^{-3}} v(t)^2 dt}$$

$P_{av} = i_{eff} V_{Leff}$
$P_{av} = 91.357$

Based on this, it is possible to observe that the average power output is a little bit lower than the original power of the lamp (100W), even though the conduction angle is being reduced because of the SIDAC.

In conclusion, when a SIDAC is used to phase control an incandescent lamp, the operation life of the bulb is going to be extended by 1.5 to 5 times which represents a big economical advantage when compared to the total cost of the lamp if it is changed. In addition, the original power of the lamp is not going to be reduced considerably which assures the proper level of illumination for the area in which the incandescent lamp is being used for. Finally, since the SIDACs are provided in a very small axial lead package, they can be mounted within the same place that the incandescent lamp is placed.

AND8017/D

Solid State Control for Bi-Directional Motors

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APPLICATION NOTE

INTRODUCTION

Some split phase motors are able to operate in forward and reverse directions since they have two windings for these purposes. Depending on which winding is energized, the motor operates in that direction. These motors are especially used in applications for washing machines, transport belts, and all kinds of equipment in which the operation in both directions is needed. One of the most traditional way to control these kind of motors is through mechanical relays. Nevertheless, they have a lot of disadvantages which make them ineffective.

This paper is going to show how triacs can substitute the function of the mechanical relays for controlling bi–directional motors offering a higher level of quality and reliability for control purposes.

The triac is a three terminal ac semiconductor switch that is triggered into conduction when a low energy signal is applied to its gate. Unlike the silicon controlled rectifier or SCR, the triac will conduct current in either direction when turned on. The triac also differs from the SCR in that either a positive or negative gate signal will trigger the triac into conduction. The triac may be thought of as two complementary SCRs in parallel.

The triac offers the circuit designer an economical and versatile means of accurately controlling ac power. It has several advantages over conventional mechanical switches.

Since the triac has a positive 'on' and a zero current 'off' characteristics, it does not suffer from the contact bounce or arcing inherent in mechanical switches. The switching action of the triac is very fast compared to conventional relays, giving more accurate control. A triac can be triggered by dc, ac, rectified ac or pulses. Because of the low energy required for triggering a triac, the control circuit can use any of many low cost solid state devices such as transistors, sensitive gate SCRs and triacs, optically coupled drivers, and integrated circuits.

DEFINITIONS

The two–phase induction motor consists of a stator with two windings displaced 90 electrical degrees from each other in space and squirrel cage rotor or the equivalent. The ac voltages applied to the two windings are generally phase displaced from each other 90° in time. When the voltages magnitudes are equal, the equivalent of balanced two–phase voltages is applied to the stator. The resultant stator flux is then similar to a three–phase induction motor. The motor torque speed curves are also similar to those of a three–phase motor. The two–phase control motor is usually built with a high resistance rotor to give a high starting torque and a dropping torque speed characteristic.

The following schematic diagram shows an ac split phase motor:
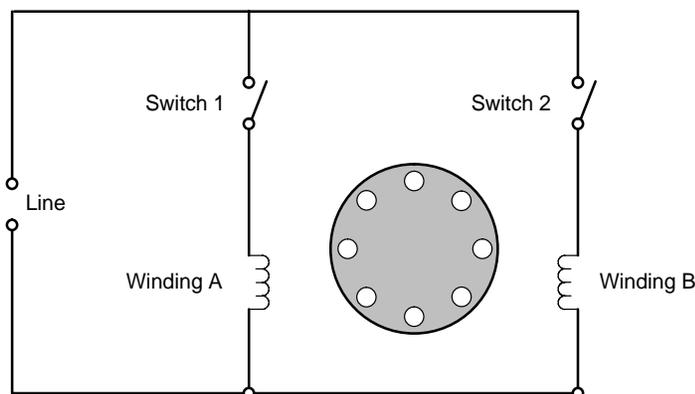
If switch 1 is activated, rotation in one direction is obtained; if switch 2 is activated, rotation in the other direction results. Since the torque is a function of the voltage supply, changing the magnitude of this changes the developed torque of the motor. The stalled torque is assumed to be linearly proportional to the rms control–winding voltage.

It is very common to add a resonant L–C circuit connected between the motor windings in order to damp the energy stored by each motor winding inductance, avoiding damage to the switches when the transition from one direction to the other occurs. In addition, this resonant L–C circuit helps to have good performance in the motor's torque each time it changes its rotation.

The following schematic diagram shows how two triacs can control the rotation of a split phase motor depending in which winding is energized. In this case the motor selected for analysis purposes has the following technical characteristics: 230Vrms, 1.9 Arms, 1/4 Hp, 60Hz, 1400 RPM.
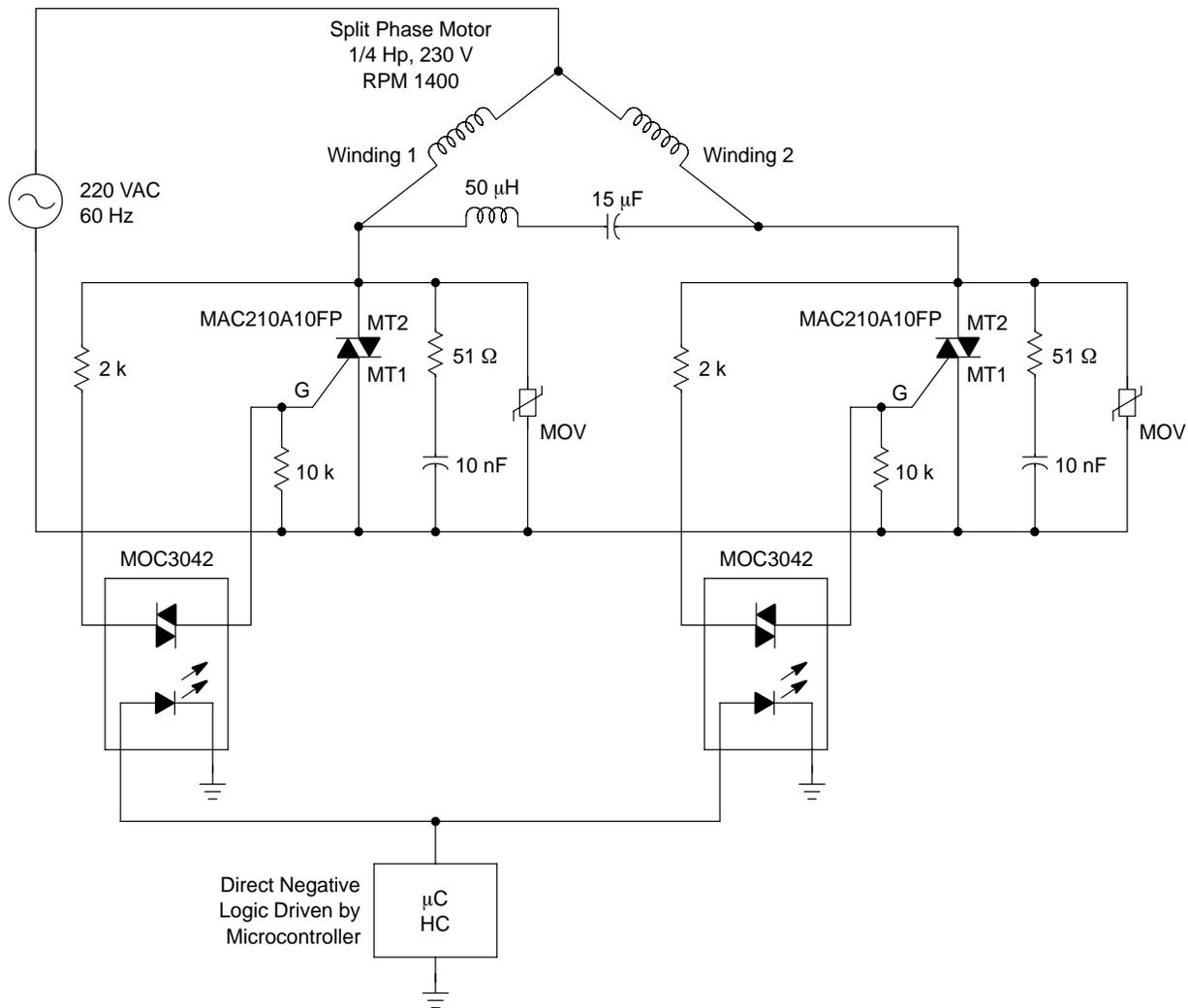
The micro is controlling the trigger of the triacs through optocouplers (MOC3042). The optocoupler protects the control circuitry (Microcontroller, Logic Gates, etc.) if a short circuit condition occurs within the power circuitry since these optocouplers insolate the control part of the general circuit. The MOVs protects the triacs against to the high voltage transients caused because of the motor rotation changes, so it is very important to add them in the power circuit, otherwise the triacs could be damaged easily. The snubber arrangement provides protection against dV/dt conditions occurring within the application circuit and the resonant L–C circuit connected between the motor's windings helps to have good performance in the torque of the motor when it changes its rotation.

In the case that the motor is locked due to some mechanical problem within the application field, the maximum current peak flowing through the triacs would be 7.2 Amps (5.02 Amps rms), therefore, the triacs (MAC210A10FP) would not be damaged since they are able to handle up to 12 A rms.

Nevertheless, it is recommended to add an overload protector in the power circuit of the motor in order to protect it against any kind of overload conditions which

could damage the motor in a short period of time since the current flowing would be higher than its nominal value.

In conclusion, it has been shown how triacs (MAC210A10FP) substitute the mechanical relay's functions to control bi–directional motors offering many important advantages like reliable control, quiet operation, long life span, small size, light weight, fast operation, among others. These are only some of the big advantages that can be obtained if thyristors are used to control bi–directional motors. Besides, the total cost of the electronic circuitry does not exceed to the cost of the conventional mechanical relays.

A very important consideration is that extreme environment temperatures could affect the functionality of the electronic devices, therefore, if operation under extreme ambient temperatures is needed, the designer must take into consideration the parameter variation of the electronic devices in order to establish if any kind of adjustment is needed within the electronic circuitry.

Another important item to be considered by the designer is that the triacs have to be mounted on a proper heatsink in order to assure that the case temperature of the device does not exceed the specifications shown in the datasheet.

SECTION 7
MOUNTING TECHNIQUES FOR THYRISTORS

Edited and Updated

INTRODUCTION

Current and power ratings of semiconductors are inseparably linked to their thermal environment. Except for lead-mounted parts used at low currents, a heat exchanger is required to prevent the junction temperature from exceeding its rated limit, thereby running the risk of a high failure rate. Furthermore, the semiconductor industry's field history indicated that the failure rate of most silicon semiconductors decreases approximately by one half for a decrease in junction temperature from 160°C to 135°C.[1] Guidelines for designers of military power supplies impose a 110°C limit upon junction temperature.[2] Proper mounting minimizes the temperature gradient between the semiconductor case and the heat exchanger.

Most early life field failures of power semiconductors can be traced to faulty mounting procedures. With metal packaged devices, faulty mounting generally causes unnecessarily high junction temperature, resulting in reduced component lifetime, although mechanical damage has occurred on occasion from improperly mounting to a warped surface. With the widespread use of various plastic-packaged semiconductors, the prospect of mechanical damage is very significant. Mechanical damage can impair the case moisture resistance or crack the semiconductor die.

(1) MIL-HANDBOOK — 2178, SECTION 2.2.
(2) "Navy Power Supply Reliability — Design and Manufacturing Guidelines" NAVMAT P4855-1, Dec. 1982 NAVPUBFORCEN, 5801 Tabor Ave., Philadelphia, PA 19120.

Figure 7.1 shows an example of doing nearly everything wrong. A tab mount TO-220 package is shown being used as a replacement for a TO-213AA (TO-66) part which was socket mounted. To use the socket, the leads are bent — an operation which, if not properly done, can crack the package, break the internal bonding wires, or crack the die. The package is fastened with a sheet-metal screw through a 1/4″ hole containing a fiber-insulating sleeve. The force used to tighten the screw tends to pull the package into the hole, causing enough distortion to crack the die. In addition the contact area is small because of the area consumed by the large hole and the bowing of the package; the result is a much higher junction temperature than expected. If a rough heatsink surface and/or burrs around the hole were displayed in the illustration, most but not all poor mounting practices would be covered.
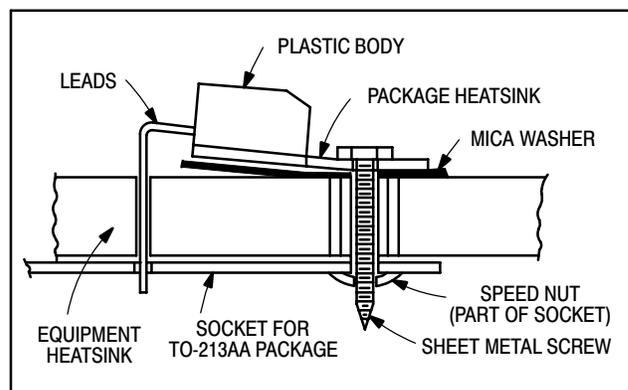
Figure 7.1. Extreme Case of Improperly Mounting A Semiconductor (Distortion Exaggerated)

In many situations the case of the semiconductor must be electrically isolated from its mounting surface. The isolation material is, to some extent, a thermal isolator as well, which raises junction operating temperatures. In addition, the possibility of arc-over problems is introduced if high voltages are present. Various regulating agencies also impose creepage distance specifications which further complicates design. Electrical isolation thus places additional demands upon the mounting procedure.

Proper mounting procedures usually necessitate orderly attention to the following:

1. Preparing the mounting surface
2. Applying a thermal grease (if required)
3. Installing the insulator (if electrical isolation is desired)
4. Fastening the assembly
5. Connecting the terminals to the circuit

In this note, mounting procedures are discussed in general terms for several generic classes of packages. As newer packages are developed, it is probable that they will fit into the generic classes discussed in this note. Unique requirements are given on data sheets pertaining to the particular package. The following classes are defined:

Stud Mount
Flange Mount
Pressfit
Plastic Body Mount
Tab Mount
Surface Mount

Appendix A contains a brief review of thermal resistance concepts. Appendix B discusses measurement difficulties with interface thermal resistance tests.

MOUNTING SURFACE PREPARATION

In general, the heatsink mounting surface should have a flatness and finish comparable to that of the semiconductor package. In lower power applications, the heatsink surface is satisfactory if it appears flat against a straight edge and is free from deep scratches. In high-power applications, a more detailed examination of the surface is required. Mounting holes and surface treatment must also be considered.

Surface Flatness

Surface flatness is determined by comparing the variance in height (Δh) of the test specimen to that of a reference standard as indicated in Figure 7.2. Flatness is normally specified as a fraction of the Total Indicator Reading (TIR). The mounting surface flatness, i.e., Δh/TIR, if less than 4 mils per inch, normal for extruded aluminum, is satisfactory in most cases.
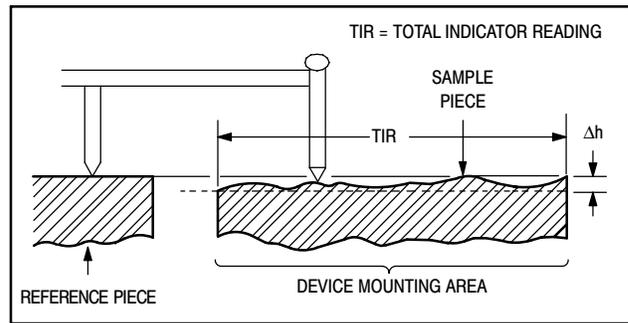
Figure 7.2. Surface Flatness Measurement

Surface Finish

Surface finish is the average of the deviations both above and below the mean value of surface height. For minimum interface resistance, a finish in the range of 50 to 60 microinches is satisfactory; a finer finish is costly to achieve and does not significantly lower contact resistance. Tests conducted by Thermalloy using a copper TO-204 (TO-3) package with a typical 32-microinch finish, showed that heatsink finishes between 16 and 64 μ-in caused less than ± 2.5% difference in interface thermal resistance when the voids and scratches were filled with a thermal joint compound.[3] Most commercially available cast or extruded heatsinks will require spotfacing when used in high-power applications. In general, milled or machined surfaces are satisfactory if prepared with tools in good working condition.

Mounting Holes

Mounting holes generally should only be large enough to allow clearance of the fastener. The large thick flange type packages having mounting holes removed from the semiconductor die location, such as the TO-3, may successfully be used with larger holes to accommodate an insulating bushing, but many plastic encapsulated packages are intolerant of this condition. For these packages, a smaller screw size must be used such that the hole for the bushing does not exceed the hole in the package.

Punched mounting holes have been a source of trouble because if not properly done, the area around a punched hole is depressed in the process. This "crater" in the heatsink around the mounting hole can cause two problems. The device can be damaged by distortion of the package as the mounting pressure attempts to conform it to the shape of the heatsink indentation, or the device may only bridge the crater and leave a significant percentage of its heat-dissipating surface out of contact with the heatsink. The first effect may often be detected immediately by visual cracks in the package (if plastic), but usually an unnatural stress is imposed, which results in an early-life failure. The second effect results in hotter operation and is not manifested until much later.

(3) Catalog #87-HS-9 (1987), page 8, Thermalloy, Inc., P.O. Box 810839, Dallas, Texas 75381-0839.

Although punched holes are seldom acceptable in the relatively thick material used for extruded aluminum heatsinks, several manufacturers are capable of properly utilizing the capabilities inherent in both fine-edge blanking or sheared-through holes when applied to sheet metal as commonly used for stamped heatsinks. The holes are pierced using Class A progressive dies mounted on four-post die sets equipped with proper pressure pads and holding fixtures.

When mounting holes are drilled, a general practice with extruded aluminum, surface cleanup is important. Chamfers must be avoided because they reduce heat transfer surface and increase mounting stress. However, the edges must be broken to remove burrs which cause poor contact between device and heatsink and may puncture isolation material.

Surface Treatment

Many aluminium heatsinks are black-anodized to improve radiation ability and prevent corrosion. Anodizing results in significant electrical but negligible thermal insulation. It need only be removed from the mounting area when electrical contact is required. Heatsinks are also available which have a nickel plated copper insert under the semiconductor mounting area. No treatment of this surface is necessary.

Another treated aluminum finish is iridite, or chromate-acid dip, which offers low resistance because of its thin surface, yet has good electrical properties because it resists oxidation. It need only be cleaned of the oils and films that collect in the manufacture and storage of the sinks, a practice which should be applied to all heatsinks.

For economy, paint is sometimes used for sinks; removal of the paint where the semiconductor is attached is usually required because of paint's high thermal resistance. However, when it is necessary to insulate the semiconductor package from the heatsink, hard anodized or painted surfaces allow an easy installation for low voltage applications. Some manufacturers will provide anodized or painted surfaces meeting specific insulation voltage requirements, usually up to 400 volts.

It is also necessary that the surface be free from all foreign material, film, and oxide (freshly bared aluminum forms an oxide layer in a few seconds). Immediately prior to assembly, it is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse.

INTERFACE DECISIONS

When any significant amount of power is being dissipated, something must be done to fill the air voids between mating surfaces in the thermal path. Otherwise the interface thermal resistance will be unnecessarily high and quite dependent upon the surface finishes.

For several years, thermal joint compounds, often called grease, have been used in the interface. They have a resistivity of approximately 60°C/W/in whereas air has 1200°C/W/in. Since surfaces are highly pock-marked with minute voids, use of a compound makes a significant reduction in the interface thermal resistance of the joint. However, the grease causes a number of problems, as discussed in the following section.

To avoid using grease, manufacturers have developed dry conductive and insulating pads to replace the more traditional materials. These pads are conformal and therefore partially fill voids when under pressure.

Thermal Compounds (Grease)

Joint compounds are a formulation of fine zinc or other conductive particles in the silicone oil or other synthetic base fluid which maintains a grease-like consistency with time and temperature. Since some of these compounds do not spread well, they should be evenly applied in a very thin layer using a spatula or lintless brush, and wiped lightly to remove excess material. Some cyclic rotation of the package will help the compound spread evenly over the entire contact area. Some experimentation is necessary to determine the correct quantity; too little will not fill all the voids, while too much may permit some compound to remain between well mated metal surfaces where it will substantially increase the thermal resistance of the joint.

To determine the correct amount, several semiconductor samples and heatsinks should be assembled with different amounts of grease applied evenly to one side of each mating surface. When the amount is correct a very small amount of grease should appear around the perimeter of each mating surface as the assembly is slowly torqued to the recommended value. Examination of a dismantled assembly should reveal even wetting across each mating surface. In production, assemblers should be trained to slowly apply the specified torque even though an excessive amount of grease appears at the edges of mating surfaces. Insufficient torque causes a significant increase in the thermal resistance of the interface.

To prevent accumulation of airborne particulate matter, excess compound should be wiped away using a cloth moistened with acetone or alcohol. These solvents should not contact plastic-encapsulated devices, as they may enter the package and cause a leakage path or carry in substances which might attack the semiconductor chip.

The silicone oil used in most greases has been found to evaporate from hot surfaces with time and become deposited on other cooler surfaces. Consequently, manufacturers must determine whether a microscopically thin coating of silicone oil on the entire assembly will pose any problems. It may be necessary to enclose components using grease. The newer synthetic base greases show far less tendency to migrate or creep than those made with a silicone oil base. However, their currently observed working temperature range are less,

they are slightly poorer on thermal conductivity and dielectric strength and their cost is higher.

Data showing the effect of compounds on several package types under different mounting conditions is shown in Table 7.1. The rougher the surface, the more valuable the grease becomes in lowering contact resistance; therefore, when mica insulating washers are used, use of grease is generally mandatory. The joint compound also improves the breakdown rating of the insulator.

Conductive Pads

Because of the difficulty of assembly using grease and the evaporation problem, some equipment manufacturers will not, or cannot, use grease. To minimize the need for grease, several vendors offer dry conductive pads which approximate performance obtained with grease. Data for a greased bare joint and a joint using Grafoil, a dry graphite compound, is shown in the data of Figure 7.3. Grafoil is claimed to be a replacement for grease when no electrical isolation is required; the data indicates it does indeed perform as well as grease. Another conductive pad available from Aavid is called KON-DUX. It is made with a unique, grain oriented, flake-like structure (patent pending). Highly compressible, it becomes formed to the surface roughness of both of the heatsink and semiconductor. Manufacturer's data shows it to provide an interface thermal resistance better than a metal interface with filled silicone grease. Similar dry conductive pads are available from other manufacturers. They are a fairly recent development; long term problems, if they exist, have not yet become evident.

Table 7.1
Approximate Values for Interface Thermal Resistance Data from Measurements Performed in ON Semiconductor Applications Engineering Laboratory

Dry interface values are subject to wide variation because of extreme dependence upon surface conditions. Unless otherwise noted the case temperature is monitored by a thermocouple located directly under the die reached through a hole in the heatsink.
(See Appendix B for a discussion of Interface Thermal Resistance Measurements.)

Package Type and Data		Interface Thermal Resistance (°C/W)						
JEDEC Outlines	Description	Test Torque In-Lb	Metal-to-Metal		With Insulator			See Note
			Dry	Lubed	Dry	Lubed	Type	
DO-203AA, TO-210AA TO-208AB	10-32 Stud 7/16″ Hex	15	0.3	0.2	1.6	0.8	3 mil Mica	
DO-203AB, TO-210AC TO-208	1/4-28 Stud 11/16″ Hex	25	0.2	0.1	0.8	0.6	5 mil Mica	
DO-208AA	Pressfit, 1/2″	—	0.15	0.1	—	—	—	
TO-204AA (TO-3)	Diamond Flange	6	0.5	0.1	1.3	0.36	3 mil Mica	1
TO-213AA (TO-66)	Diamond Flange	6	1.5	0.5	2.3	0.9	2 mil Mica	
TO-126	Thermopad 1/4″ x 3/8″	6	2.0	1.3	4.3	3.3	2 mil Mica	
TO-220AB	Thermowatt	8	1.2	1.0	3.4	1.6	2 mil Mica	1, 2

NOTES: 1. See Figures 3 and 4 for additional data on TO-3 and TO-220 packages.
2. Screw not insulated. See Figure 7.

INSULATION CONSIDERATIONS

Since most power semiconductors use are vertical device construction it is common to manufacture power semiconductors with the output electrode (anode, collector or drain) electrically common to the case; the problem of isolating this terminal from ground is a common one. For lowest overall thermal resistance, which is quite important when high power must be dissipated, it is best to isolate the entire heatsink/semiconductor structure from ground, rather than to use an insulator between the semiconductor and the heatsink. Heatsink isolation is not always possible, however, because of EMI requirements, safety reasons, instances where a chassis serves as a heatsink or where a heatsink is common to several non-isolated packages. In these situations insulators are used to isolate the individual components from the heatsink. Newer packages, such as the ON Semiconductor Isolated TO-220 Full Pack, was introduced to save the equipment manufacturer the burden of addressing the isolation problem.

Insulator Thermal Resistance

When an insulator is used, thermal grease is of greater importance than with a metal-to-metal contact, because two interfaces exist instead of one and some materials, such as mica, have a hard, markedly uneven surface. With many isolation materials reduction of interface thermal resistance of between 2 to 1 and 3 to 1 are typical when grease is used.

Data obtained by Thermalloy, showing interface resistance for different insulators and torques applied to TO-204 (TO-3) and TO-220 packages, are shown in Figure 7.3, for bare and greased surfaces. Similar materials to those shown are available from several manufacturers. It is obvious that with some arrangements, the interface thermal resistance exceeds that of the semiconductor (junction to case).

Referring to Figure 7.3, one may conclude that when high power is handled, beryllium oxide is unquestionably the best. However, it is an expensive choice. (It should not be cut or abraided, as the dust is highly toxic.) Thermafilm is filled polyimide material which is used for isolation (variation of Kapton). It is a popular material for low power applications because of its low cost ability to withstand high temperatures, and ease of handling in contrast to mica which chips and flakes easily.

(1) **Thermalfilm,** .002 (.05) thick.
(2) **Mica,** .003 (.08) thick.
(3) **Mica,** .002 (.05) thick.
(4) **Hard anodized,** .020 (.51) thick.
(5) **Aluminum oxide,** .062 (1.57) thick.
(6) **Beryllium oxide,** .062 (1.57) thick.
(7) **Bare joint** — no finish.
(8) **Grafoil,** .005 (.13) thick.*
*Grafoil is not an insulating material.

**(a). TO-204AA (TO-3)
Without Thermal Grease**

**(b). TO-204AA (TO-3)
With Thermal Grease**

(1) **Thermalfilm,** .022 (.05) thick.
(2) **Mica,** .003 (.08) thick.
(3) **Mica,** .002 (.05) thick.
(4) **Hard anodized,** .020 (.51) thick.
(5) **Thermalsil II,** .009 (.23) thick.
(6) **Thermalsil III,** .006 (.15) thick.
(7) **Bare joint** — no finish.
(8) **Grafoil,** .005 (.13) thick*
*Grafoil is not an insulating material.

**(c). TO-220
Without Thermal Grease**

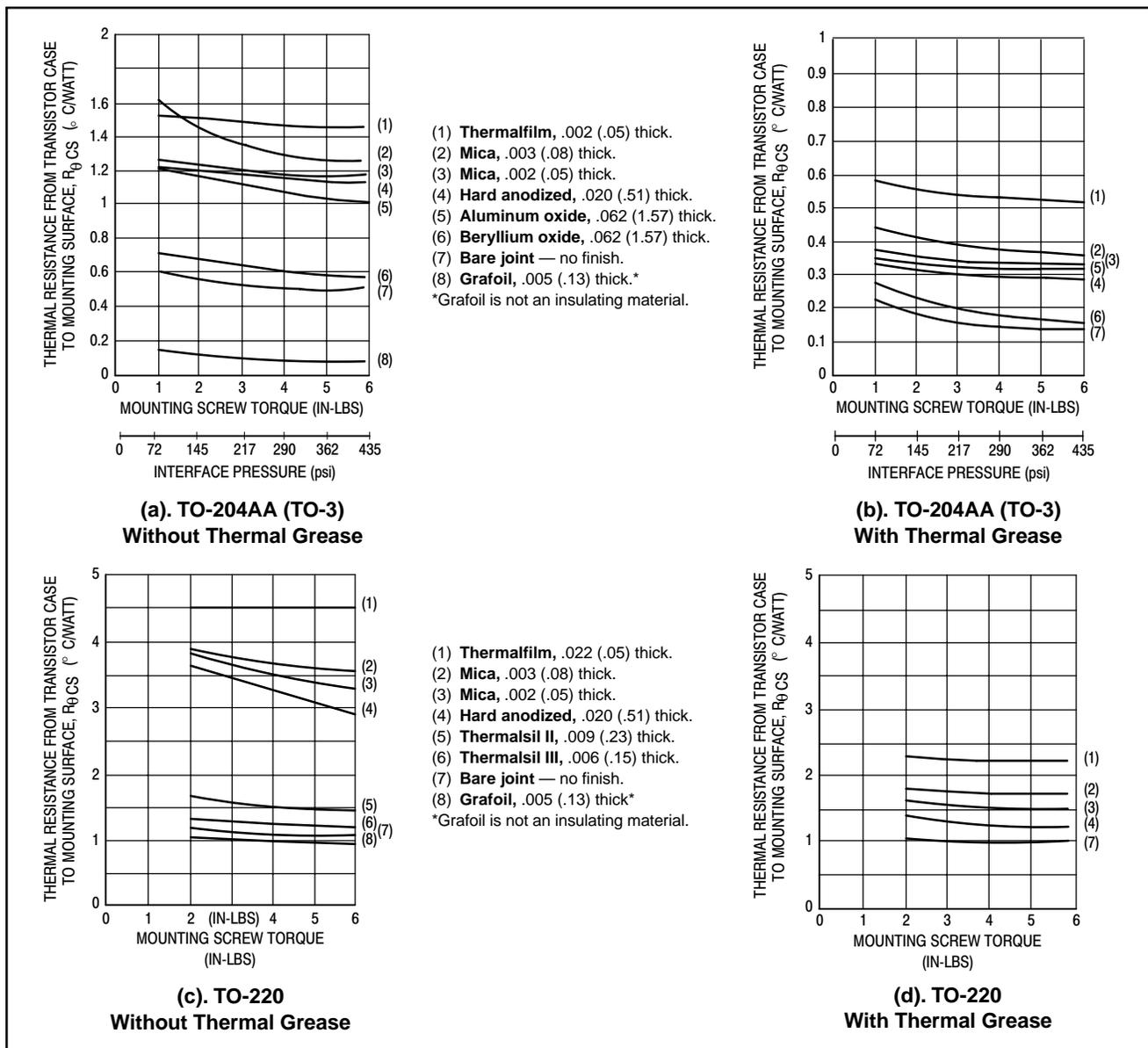**(d). TO-220
With Thermal Grease**

Figure 7.3. Interface Thermal Resistance for TO-204, TO-3 and TO-220 Packages using Different Insulating Materials as a Function of Mounting Screw Torque (Data Courtesy Thermalloy)

A number of other insulating materials are also shown. They cover a wide range of insulation resistance, thermal resistance and ease of handling. Mica has been widely used in the past because it offers high breakdown voltage and fairly low thermal resistance at a low cost but it certainly should be used with grease.

Silicone rubber insulators have gained favor because they are somewhat conformal under pressure. Their ability to fill in most of the metal voids at the interface reduces the need for thermal grease. When first introduced, they suffered from cut-through after a few years in service. The ones presently available have solved this problem by having imbedded pads of Kapton of fiberglass. By comparing Figures 7.3(c) and 7.3(d), it can be noted that Thermasil, a filled silicone rubber, without grease has about the same interface thermal resistance as greased mica for the TO-220 package.

A number of manufacturers offer silicone rubber insulators. Table 7.2 shows measured performance of a number of these insulators under carefully controlled, nearly identical conditions. The interface thermal resistance extremes are over 2:1 for the various materials. It is also clear that some of the insulators are much more tolerant than others of out-of-flat surfaces. Since the tests were performed, newer products have been introduced. The Bergquist K-10 pad, for example, is described as having about 2/3 the interface resistance of the Sil Pad 1000 which would place its performance close to the Chomerics 1671 pad. AAVID also offers an isolated pad called Rubber-Duc, however it is only available vulcanized to a heatsink and therefore was not included in the comparison. Published data from AAVID shows $R_{\theta CS}$ below 0.3°C/W for pressures above 500 psi. However, surface flatness and other details are not specified so a comparison cannot be made with other data in this note.

The thermal resistance of some silicone rubber insulators is sensitive to surface flatness when used under a fairly rigid base package. Data for a TO-204AA (TO-3) package insulated with Thermasil is shown on Figure 7.4. Observe that the "worst case" encountered (7.5 mils) yields results having about twice the thermal resistance of the "typical case" (3 mils), for the more conductive insulator. In order for Thermasil III to exceed the performance of greased mica, total surface flatness must be under 2 mils, a situation that requires spot finishing.

(1) Thermalsil II, .009 inches (.23 mm) thick.
(2) Thermalsil III, .006 inches (.15 mm) thick.
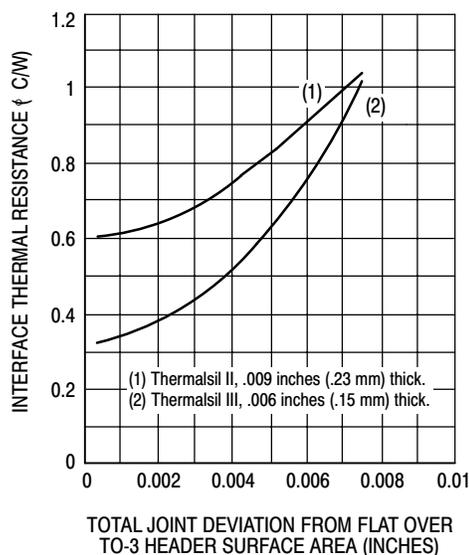
Data courtesy of Thermalloy

Figure 7.4. Effect of Total Surface Flatness on Interface Resistance Using Silicon Rubber Insulators

Silicon rubber insulators have a number of unusual characteristics. Besides being affected by surface flatness and initial contact pressure, time is a factor. For example, in a study of the Cho-Therm 1688 pad thermal interface impedance dropped from 0.90°C/W to 0.70°C/W at the end of 1000 hours. Most of the change occurred during the first 200 hours where $R_{\theta CS}$ measured 0.74°C/W. The torque on the conventional mounting hardware had decreased to 3 in-lb from an initial 6 in-lb. With non-conformal materials, a reduction in torque would have increased the interface thermal resistance.

Because of the difficulties in controlling all variables affecting tests of interface thermal resistance, data from different manufacturers is not in good agreement. Table 7.3 shows data obtained from two sources. The relative performance is the same, except for mica which varies widely in thickness. Appendix B discusses the variables which need to be controlled. At the time of this writing ASTM Committee D9 is developing a standard for interface measurements.

Table 7.2 Thermal Resistance of Silicone Rubber Pads

Manufacturer	Product	$R_{\theta CS}$ @ 3 Mils*	$R_{\theta CS}$ @ 7.5 Mils*
Wakefield	Delta Pad 173-7	.790	1.175
Bergquist	Sil Pad K-4	.752	1.470
Stockwell Rubber	1867	.742	1.015
Bergquist	Sil Pad 400-9	.735	1.205
Thermalloy	Thermalsil II	.680	1.045
Shin-Etsu	TC-30AG	.664	1.260
Bergquist	Sil Pad 400-7	.633	1.060
Chomerics	1674	.592	1.190
Wakefield	Delta Pad 174-9	.574	.755
Bergquist	Sil Pad 1000	.529	.935
Ablestik	Thermal Wafers	.500	.990
Thermalloy	Thermalsil III	.440	1.035
Chomerics	1671	.367	.655

* Test Fixture Deviation from flat from Thermalloy EIR86-1010.

Table 7.3 Performance of Silicon Rubber Insulators Tested per MIL-I-49456

Material	Measured Thermal Resistance (°C/W)	
	Thermalloy Data[1]	Berquist Data[2]
Bare Joint, greased	0.033	0.008
BeO, greased	0.082	—
Cho-Therm, 1617	0.233	—
Q Pad (non-insulated)	—	0.009
Sil-Pad, K-10	0.263	0.200
Thermasil III	0.267	—
Mica, greased	0.329	0.400
Sil-Pad 1000	0.400	0.300
Cho-therm 1674	0.433	—
Thermasil II	0.500	—
Sil-Pad 400	0.533	0.440
Sil-Pad K-4	0.583	0.440

1. From Thermalloy EIR 87-1030
2. From Berquist Data Sheet

The conclusions to be drawn from all this data is that some types of silicon rubber pads, mounted dry, will out perform the commonly used mica with grease. Cost may be a determining factor in making a selection.

Insulation Resistance

When using insulators, care must be taken to keep the mating surfaces clean. Small particles of foreign matter can puncture the insulation, rendering it useless or seriously lowering its dielectric strength. In addition, particularly when voltages higher than 300 V are encountered, problems with creepage may occur. Dust and other foreign material can shorten creepage distances significantly; so having a clean assembly area is important. Surface roughness and humidity also lower insulation resistance. Use of thermal grease usually raises the withstand voltage of the insulating system but excess must be removed to avoid collecting dust. Because of these factors, which are not amenable to analysis, hi-pot testing should be done on prototypes and a large margin of safety employed.

Insulated Electrode Packages

Because of the nuisance of handling and installing the accessories needed for an insulated semiconductor mounting, equipment manufacturers have longed for cost-effective insulated packages since the 1950's. The first to appear were stud mount types which usually have a layer of beryllium oxide between the stud hex and the can. Although effective, the assembly is costly and requires manual mounting and lead wire soldering to terminals on top of the case. In the late eighties, a number of electrically isolated parts became available from various semiconductor manufacturers. These offerings presently consist of multiple chips and integrated circuits as well as the more conventional single chip devices.

The newer insulated packages can be grouped into two categories. The first has insulation between the semiconductor chips and the mounting base; an exposed area of the mounting base is used to secure the part. Case 806 (ICePAK) and Case 388 (TO-258AA) (see Figure 7.6) are examples of parts in this category. The second category contains parts which have a plastic overmold covering the metal mounting base. The Fully Isolated, Case 221C, illustrated in Figure 7.8, is an example of parts in the second category.

Parts in the first category — those with an exposed metal flange or tab — are mounted the same as their non-insulated counterparts. However, as with any mounting system where pressure is bearing on plastic, the overmolded type should be used with a conical compression washer, described later in this note.

FASTENER AND HARDWARE CHARACTERISTICS

Characteristics of fasteners, associated hardware, and the tools to secure them determine their suitability for use in mounting the various packages. Since many problems have arisen because of improper choices, the basic characteristics of several types of hardware are discussed next.

Compression Hardware

Normal split ring lock washers are not the best choice for mounting power semiconductors. A typical #6 washer flattens at about 50 pounds, whereas 150 to 300 pounds is needed for good heat transfer at the interface. A very useful piece of hardware is the conical, sometimes called a Belleville washer, compression washer. As shown in Figure 7.5, it has the ability to maintain a fairly constant pressure over a wide range of its physical deflection — generally 20% to 80%. When installing, the assembler applies torque until the washer depresses to half its original height. (Tests should be run prior to setting up the assembly line to determine the proper torque for the fastener used to achieve 50% deflection.) The washer will absorb any cyclic expansion of the package, insulating washer or other materials caused by temperature changes. Conical washers are the key to successful mounting of devices requiring strict control of the mounting force or when plastic hardware is used in the mounting scheme. They are used with the large face contacting the packages. A new variation of the conical washer includes it as part of a nut assembly. Called a Sync Nut, the patented device can be soldered to a PC board and the semiconductor mounted with 6-32 machine screw.[4]

(4) ITW Shakeproof, St. Charles Road, Elgin, IL 60120.
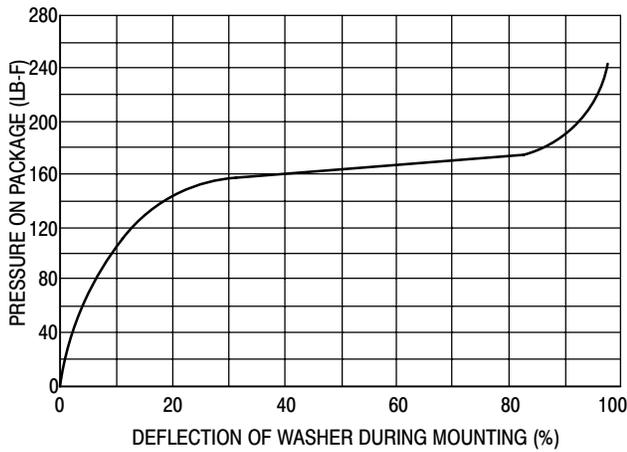
Figure 7.5. Characteristics of the Conical Compression Washers Designed for Use with Plastic Body Mounted Semiconductors

Clips

Fast assembly is accomplished with clips. When only a few watts are being dissipated, the small board mounted or free-standing heat dissipators with an integral clip, offered by several manufacturers, result in a low cost assembly. When higher power is being handled, a separate clip may be used with larger heatsinks. In order to provide proper pressure, the clip must be specially designed for a particular heatsink thickness and semiconductor package.

Clips are especially popular with plastic packages such as the TO-220 and TO-126. In addition to fast assembly, the clip provides lower interface thermal resistance than other assembly methods when it is designed for proper pressure to bear on the top of the plastic over the die. The TO-220 package usually is lifted up under the die location when mounted with a single fastener through the hole in the tab because of the high pressure at one end.

Machine Screws

Machine screws, conical washers, and nuts (or sync-nuts) can form a trouble-free fastener system for all types of packages which have mounting holes. However, proper torque is necessary. Torque ratings apply when dry; therefore, care must be exercised when using thermal grease to prevent it from getting on the threads as inconsistent torque readings result. Machine screw heads should not directly contact the surface of plastic packages types as the screw heads are not sufficiently flat to provide properly distributed force. Without a washer, cracking of the plastic case may occur.

Self-Tapping Screws

Under carefully controlled conditions, sheet-metal screws are acceptable. However, during the tapping process with a standard screw, a volcano-like protrusion will develop in the metal being threaded; an unacceptable surface that could increase the thermal resistance may result. When standard sheet metal screws are used, they must be used in a clearance hole to engage a speednut. If a self tapping process is desired, the screw type must be used which roll-forms machine screw threads.

Rivets

Rivets are not a recommended fastener for any of the plastic packages. When a rugged metal flange-mount package is being mounted directly to a heatsink, rivets can be used provided press-riveting is used. Crimping force must be applied slowly and evenly. Pop-riveting should never be used because the high crimping force could cause deformation of most semiconductor packages. Aluminum rivets are much preferred over steel because less pressure is required to set the rivet and thermal conductivity is improved.

The hollow rivet, or eyelet, is preferred over solid rivets. An adjustable, regulated pressure press is used such that a gradually increasing pressure is used to pan the eyelet. Use of sharp blows could damage the semiconductor die.

Solder

Until the advent of the surface mount assembly technique, solder was not considered a suitable fastener for power semiconductors. However, user demand has led to the development of new packages for this application. Acceptable soldering methods include conventional belt-furnace, irons, vapor-phase reflow, and infrared reflow. It is important that the semiconductor temperature not exceed the specified maximum (usually 260°C) or the die bond to the case could be damaged. A degraded die bond has excessive thermal resistance which often leads to a failure under power cycling.

Adhesives

Adhesives are available which have coefficients of expansion compatible with copper and aluminum.[5] Highly conductive types are available; a 10 mil layer has approximately 0.3°C/W interface thermal resistance. Different types are offered: high strength types for non-field-serviceable systems or low strength types for field-serviceable systems. Adhesive bonding is attractive when case mounted parts are used in wave soldering assembly because thermal greases are not compatible with the conformal coatings used and the greases foul the solder process.

Plastic Hardware

Most plastic materials will flow, but differ widely in this characteristic. When plastic materials form parts of the fastening system, compression washers are highly valuable to assure that the assembly will not loosen with time and temperature cycling. As previously discussed, loss of contact pressure will increase interface thermal resistance.

(5) Robert Batson, Elliot Fraunglass and James P. Moran, "Heat Dissipation Through Thermalloy Conductive Adhesives," EMTAS '83. Conference, February 1–3, Phoenix, AZ; Society of Manufacturing Engineers, One SME Drive, P.O. Box 930, Dearborn, MI 48128.

FASTENING TECHNIQUES

Each of the various classes of packages in use requires different fastening techniques. Details pertaining to each type are discussed in following sections. Some general considerations follow.

To prevent galvanic action from occurring when devices are used on aluminum heatsinks in a corrosive atmosphere, many devices are nickel- or gold-plated. Consequently, precautions must be taken not to mar the finish.

Another factor to be considered is that when a copper based part is rigidly mounted to an aluminium heatsink, a bimetallic system results which will bend with temperature changes. Not only is the thermal coefficient of expansion different for copper and aluminium, but the temperature gradient through each metal also causes each component to bend. If bending is excessive and the package is mounted by two or more screws the semiconductor chip could be damaged. Bending can be minimized by:

1. Mounting the component parallel to the heatsink fins to provide increased stiffness.
2. Allowing the heatsink holes to be a bit oversized so that some slip between surfaces can occur as temperature changes.
3. Using a highly conductive thermal grease or mounting pad between the heatsink and semicondutor to minimize the temperature gradient and allow for movement.

Tab Mount

The tab mount class is composed of a wide array of packages as illustrated in Figure 7.6. Mounting considerations for all varieties are similar to that for the popular TO-220 package, whose suggested mounting arrangements and hardware are shown in Figure 7.7. The rectangular washer shown in Figure 7.7(a) is used to minimize distortion of the mounting flange; excessive distortion could cause damage to the semiconductor chip. Use of the washer is only important when the size of the mounting hole exceeds 0.140 inch (6–32 clearance). Larger holes are needed to accommodate the lower insulating bushing when the screw is electrically connected to the case; however, the holes should not be larger than necessary to provide hardware clearance and should never exceed a diameter of 0.250 inch. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch-pounds is suggested when using a 6–32 screw.

Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. To minimize this problem, ON Semiconductor TO-220 packages have a chamfer on one end. TO-220 packages of other manufacturers may need a spacer or combination spacer and isolation bushing to raise the screw head above the top surface of the plastic.

The popular TO-220 Package and others of similar construction lift off the mounting surface as pressure is applied to one end. (See Appendix B, Figure B1.) To counter this tendency, at least one hardware manufacturer offers a hard plastic cantilever beam which applies more even pressure on the tab.[6] In addition, it separates the mounting screw from the metal tab. Tab mount parts may also be effectively mounted with clips as shown in Figure 7.10(c). To obtain high pressure without cracking the case, a pressure spreader bar should be used under the clip. Interface thermal resistance with the cantilever beam or clips can be lower than with screw mounting.

(6) Catalog, Edition 18, Richco Plastic Company, 5825 N. Tripp Ave., Chicago, IL 60546.

CASE 221A-07
(TO-220AB)

CASE 221B-04
(TO-220AC)

CASE 314B
(5 PIN TO-220)

CASE 314D

CASE 339

CASE 340-02
(TO-218)

CASE 387-01
(TO-254AA)
CASE 388-01
(TO-258AA)

CASE 806-05
(ICePAK)
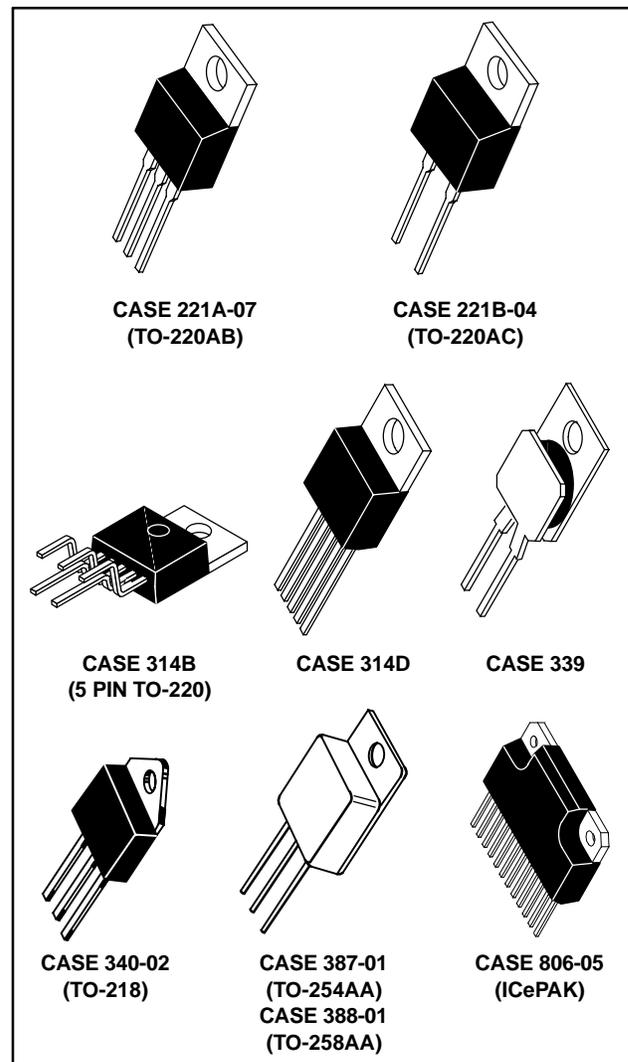
Figure 7.6. Several Types of Tab-Mount Parts

(a). Preferred Arrangement for Isolated or Non-Isolated Mounting. Screw is at Semiconductor Case Potential. 6-32 Hardware is Used.

Use Parts Listed Below

(b). Alternate Arrangement for Isolated Mounting when Screw must be at Heat Sink Potential. 4-40 Hardware is used.

Use Parts Listed below.

6-32 HEX HEAD SCREW

4-40 PAN OR HEX HEAD SCREW

FLAT WASHER

INSULATING BUSHING

(1) RECTANGULAR STEEL WASHER

SEMICONDUCTOR (CASE 221, 221A)

SEMICONDUCTOR (CASE 221,221A)

(2) RECTANGULAR INSULATOR

RECTANGULAR INSULATOR

HEATSINK

HEATSINK

(2) BUSHING

(3) FLAT WASHER

COMPRESSION WASHER

(4) CONICAL WASHER

6-32 HEX NUT

4-40 HEX NUT

(1) Used with thin chassis and/or large hole.
(2) Used when isolation is required.
(3) Required when nylon bushing is used.

Figure 7.7. Mounting Arrangements for Tab Mount TO-220

In situations where a tab mount package is making direct contact with the heatsink, an eyelet may be used, provided sharp blows or impact shock is avoided.

Plastic Body Mount

The Thermopad and fully isolated plastic power packages shown in Figure 7.8 are typical of packages in this group. They have been designed to feature minimum size with no compromise in thermal resistance. For the Thermopad (Case 77) parts this is accomplished by die-bounding the silicon chip on one side of a thin copper sheet; the opposite side is exposed as a mounting surface.
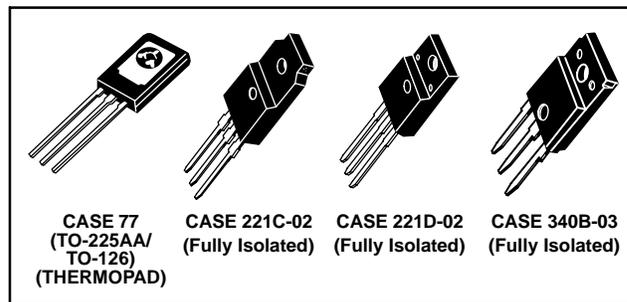
The copper sheet has a hole for mounting; plastic is molded enveloping the chip but leaving the mounting hole open. The low thermal resistance of this construction is obtained at the expense of a requirement that strict attention be paid to the mounting procedure.

The fully isolated power package (Case 221C-02) is similar to a TO-220 except that the tab is encased in plastic. Because the mounting force is applied to plastic, the mounting procedure differs from a standard TO-220 and is similar to that of the Thermopad.

Several types of fasteners may be used to secure these packages; machine screws, eyelets, or clips are preferred. With screws or eyelets, a conical washer should be used which applies the proper force to the package over a fairly wide range of deflection and distributes the force over a fairly large surface area. Screws should not be tightened with any type of air-driven torque gun or equipment which may cause high impact. Characteristics of a suitable conical washer is shown in Figure 7.5.

Figure 7.9 shows details of mounting Case 77 devices. Clip mounting is fast and requires minimum hardware, however, the clip must be properly chosen to insure that the proper mounting force is applied. When electrical isolation is required with screw mounting, a bushing inside the mounting hole will insure that the screw threads do not contact the metal base.

The fully isolated power package, (Case 221C, 221D and 340B) permits the mounting procedure to be greatly simplified over that of a standard TO-220. As shown in Figure 7.10(c), one properly chosen clip, inserted into two slotted holes in the heatsink, is all the hardware needed. Even though clip pressure is much lower than obtained with a screw, the thermal resistance is about the same for either method. This occurs because the clip bears directly on top of the die and holds the package flat while the screw causes the package to lift up somewhat under the die. (See Figure B1 of Appendix B.) The interface should consist of a layer of thermal grease or a highly conductive thermal pad. Of course, screw mounting shown in Figure 7.10(b) may also be used but a conical compression washer should be included. Both methods afford a major reduction in hardware as compared to the conventional mounting method with a TO-220 package which is shown in Figure 7.10(a).

CASE 77 (TO-225AA/ TO-126) (THERMOPAD)

CASE 221C-02 (Fully Isolated)

CASE 221D-02 (Fully Isolated)

CASE 340B-03 (Fully Isolated)

Figure 7.8. Plastic Body-Mount Packages

MACHINE SCREW OR SHEET METAL SCREW

HEAT SINK SURFACE

COMPRESSION WASHER

THERMOPAD PACKAGE

INSULATING WASHER (OPTIONAL)

MACHINE OR SPEED NUT

(a). Machine Screw Mounting

EYELET

COMPRESSION WASHER

INSULATING WASHER (OPTIONAL)

(b). Eyelet Mounting

(c). Clips
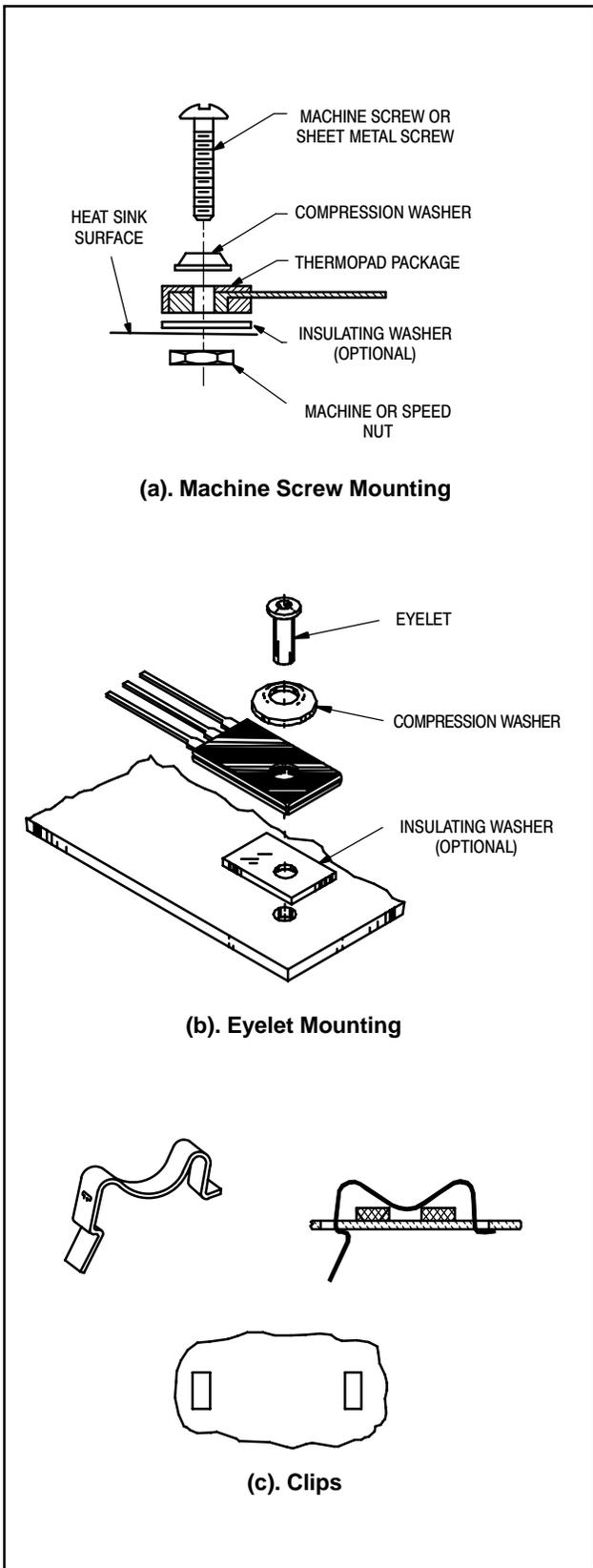
Figure 7.9. Recommended Mounting Arrangements for TO-225AA (TO-126) Thermopad Packages

4-40 SCREW

PLAIN WASHER
INSULATING BUSHING

INSULATOR

HEATSINK

COMPRESSION WASHER

NUT

(a). Screw-Mounted TO-220

6-32 SCREW

PLAIN WASH-ER

HEATSINK

COMPRESSION WASHER

NUT

(b). Screw-Mounted Fully Isolated

CLIP

HEATSINK

(c). Clip-Mounted Fully Isolated

Figure 7.10. Mounting Arrangements for the Fully Isolated Power Package as Compared to a Conventional TO-220

Surface Mount

Although many of the tab mount parts have been surface mounted, special small footprint packages for mounting power semiconductors using surface mount assembly techniques have been developed. The DPAK, shown in Figure 11, for example, will accommodate a die up to 112 mils x 112 mils, and has a typical thermal resistance around 2°C/W junction to case. The thermal resistance values of the solder interface is well under 1°C/W. The printed circuit board also serves as the heatsink.
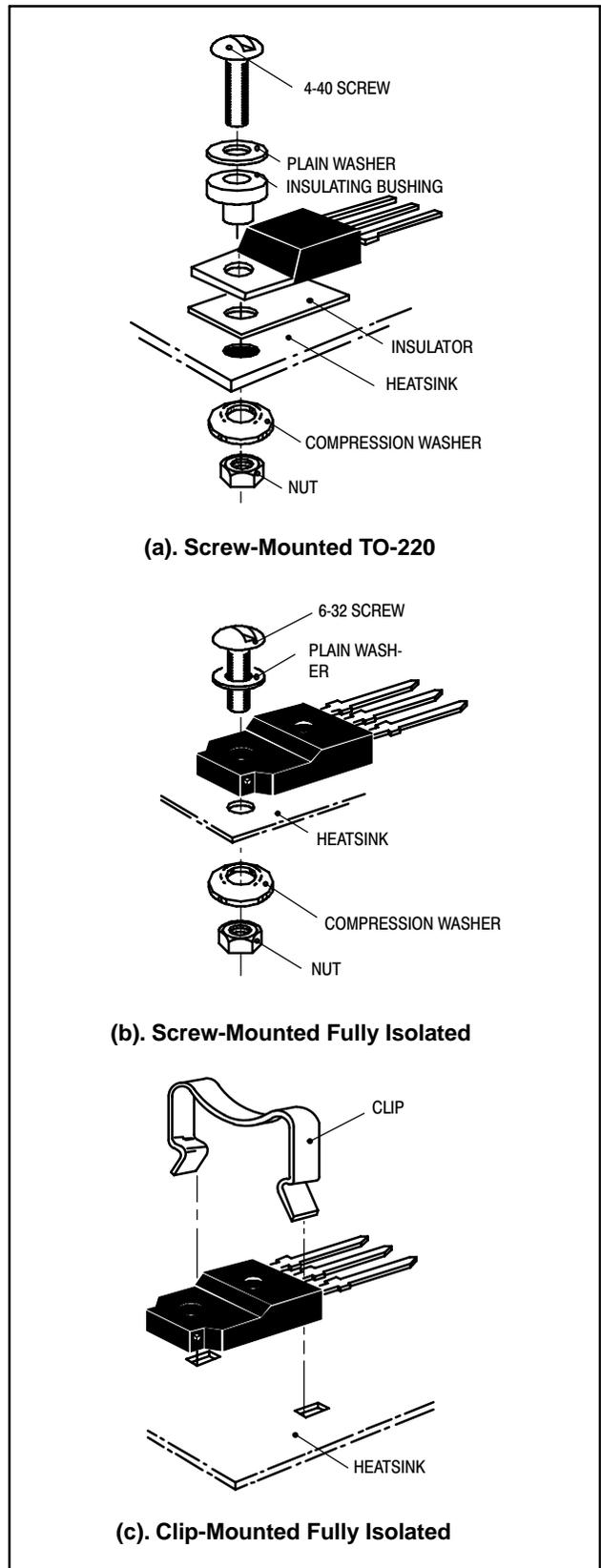
Standard Glass-Epoxy 2-ounce boards do not make very good heatsinks because the thin foil has a high thermal resistance. As Figure 7.12 shows, thermal resistance assymtotes to about 20°C/W at 10 square inches of board area, although a point of diminishing returns occurs at about 3 square inches.

Boards are offered that have thick aluminium or copper substrates. A dielectric coating designed for low thermal resistance is overlayed with one or two ounce copper foil for the preparation of printed conductor traces. Tests run on such a product indicate that case to substrate thermal resistance is in the vicinity of 1°C/W, exact values depending upon board type.[7] The substrate may be an effective heatsink itself, or it can be attached to a conventional finned heatsink for improved performance.

Since DPAK and other surface mount packages are designed to be compatible with surface mount assembly techniques, no special precautions are needed other than to insure that maximum temperature/time profiles are not exceeded.

(7) Herb Fick, "Thermal Management of Surface Mount Power Devices," Power conversion and Intelligent Motion, August 1987.
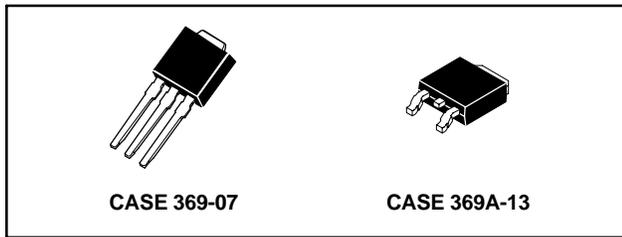

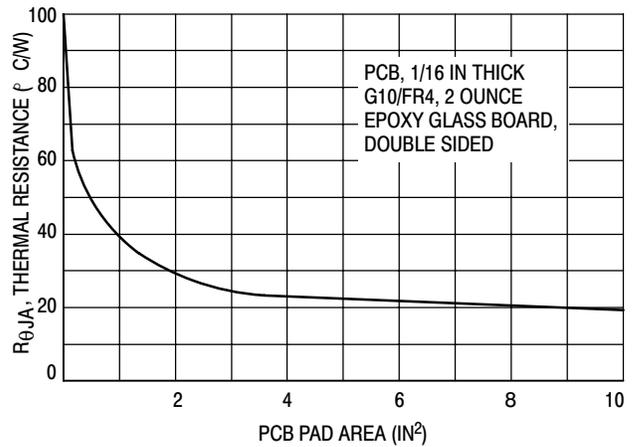**Figure 7.11. Surface Mount D-PAK Parts**

Figure 7.12. Effect of Footprint Area on Thermal Resistance of DPAK Mounted on a Glass-Epoxy Board

FREE AIR AND SOCKET MOUNTING

In applications where average power dissipation is on the order of a watt or so, most power semiconductors may be mounted with little or no heatsinking. The leads of the various metal power packages are not designed to support the packages; their cases must be firmly supported to avoid the possibility of cracked seals around the leads. Many plastic packages may be supported by their leads in applications where high shock and vibration stresses are not encountered and where no heatsink is used. The leads should be as short as possible to increase vibration resistance and reduce thermal resistance. As a general practice however, it is better to support the package. A plastic support for the TO-220 Package and other similar types is offered by heatsink accessory vendors.

In many situations, because its leads are fairly heavy, the CASE 77 (TO-225AA)(TO-127) package has supported a small heatsink; however, no definitive data is available. When using a small heatsink, it is good practice to have the sink rigidly mounted such that the sink or the board is providing total support for the semiconductor. Two possible arrangements are shown in Figure 7.13. The arrangement of part (a) could be used with any plastic package, but the scheme of part (b) is more practical with Case 77 Thermopad devices. With the other package types, mounting the transistor on top of the heatsink is more practical.

(a). Simple Plate, Vertically Mounted

(b). Commercial Sink, Horizontally Mounted
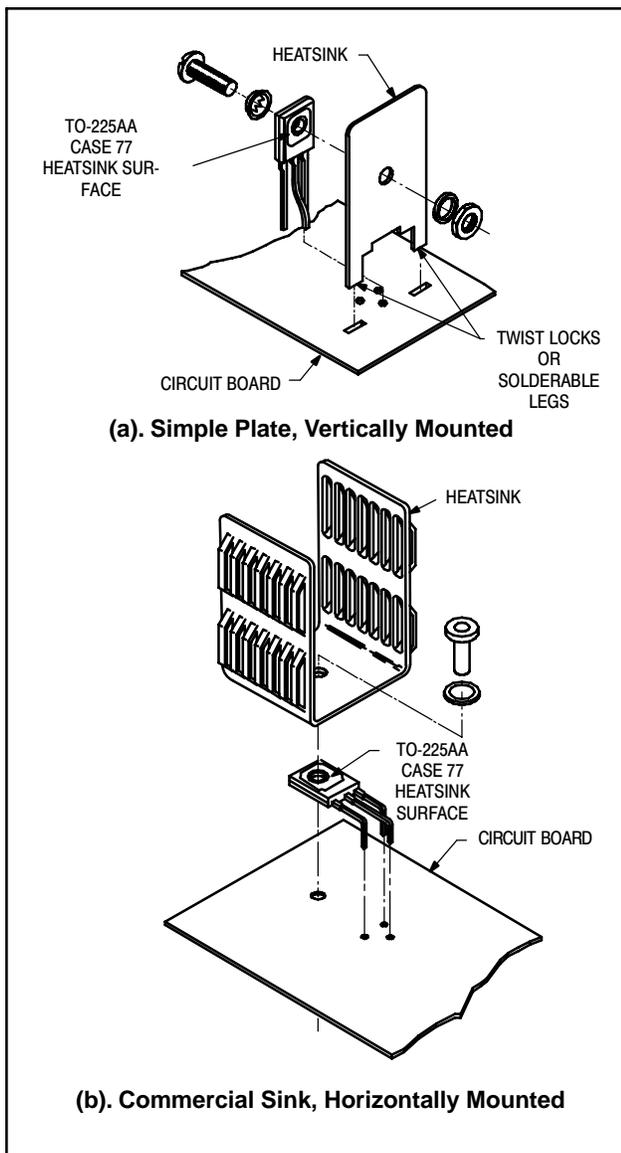
Figure 7.13. Methods of Using Small Heatsinks With Plastic Semiconductor Packages

In certain situations, in particular where semiconductor testing is required or prototypes are being developed, sockets are desirable. Manufacturers have provided sockets for many of the packages available from ON Semiconductor. The user is urged to consult manufacturers' catalogs for specific details. Sockets with Kelvin connections are necessary to obtain accurate voltage readings across semiconductor terminals.

CONNECTING AND HANDLING TERMINALS

Pins, leads, and tabs must be handled and connected properly to avoid undue mechanical stress which could cause semiconductor failure. Change in mechanical dimensions as a result of thermal cycling over operating temperature extremes must be considered. Standard metal, plastic, and RF stripline packages each have some special considerations.

Plastic Packages

The leads of the plastic packages are somewhat flexible and can be reshaped although this is not a recommended procedure. In many cases, a heatsink can be chosen which makes lead-bending unnecessary. Numerous-lead and tab-forming options are available from ON Semiconductor on large quantity orders. Preformed leads remove the users risk of device damage caused by bending.

If, however, lead-bending is done by the user, several basic considerations should be observed. When bending the lead, support must be placed between the point of bending and the package. For forming small quantities of units, a pair of pliers may be used to clamp the leads at the case, while bending with the fingers or another pair of pliers. For production quantities, a suitable fixture should be made.

The following rules should be observed to avoid damage to the package.

1. A leadbend radius greater than 1/16 inch is advisable for TO-225AA (CASE 77) and 1/32 inch for TO-220.
2. No twisting of leads should be done at the case.
3. No axial motion of the lead should be allowed with respect to the case.

The leads of plastic packages are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement imposes axial stress on the leads, a condition which may be caused by thermal cycling, some method of strain relief should be devised. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions. Highly flexible or braided wires are good for providing strain relief.

Wire-wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. The leads may be soldered; the maximum soldering temperature, however, must not exceed 260°C and must be applied for not more than 10 seconds at a distance greater than 1/8 inch from the plastic case.

CLEANING CIRCUIT BOARDS

It is important that any solvents or cleaning chemicals used in the process of degreasing or flux removal do not affect the reliability of the devices. Alcohol and unchlorinated Freon solvents are generally satisfactory for use with plastic devices, since they do not damage the package. Hydrocarbons such as gasoline and chlorinated Freon may cause the encapsulant to swell, possibly damaging the transistor die.

When using an ultrasonic cleaner for cleaning circuit boards, care should be taken with regard to ultrasonic energy and time of application. This is particularly true if any packages are free-standing without support.

THERMAL SYSTEM EVALUATION

Assuming that a suitable method of mounting the semiconductor without incurring damage has been achieved, it is important to ascertain whether the junction temperature is within bounds.

In applications where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. In this case, use must be made of transient thermal resistance data. For a full explanation of its use, see ON Semiconductor Application Note, AN569.

Other applications, notably RF power amplifiers or switches driving highly reactive loads, may create severe current crowding conditions which render the traditional concepts of thermal resistance or transient thermal impedance invalid. In this case, transistor safe operating area, thyristor di/dt limits, or equivalent ratings as applicable, must be observed.

Fortunately, in many applications, a calculation of the average junction temperature is sufficient. It is based on the concept of thermal resistance between the junction and a temperature reference point on the case. (See Appendix A.) A fine wire thermocouple should be used, such as #36 AWG, to determine case temperature. Average operating junction temperature can be computed from the following equation:

$$T_J = T_C + R_{\theta JC} \times P_D$$

where
T_J = junction temperature (°C)
T_C = case temperature (°C)
$R_{\theta JC}$ = thermal resistance junction-to-case as specified on the data sheet (°C/W)
P_D = power dissipated in the device (W)

The difficulty in applying the equation often lies in determining the power dissipation. Two commonly used empirical methods are graphical integration and substitution.

Graphical Integration

Graphical integration may be performed by taking oscilloscope pictures of a complete cycle of the voltage and current waveforms, using a limit device. The pictures should be taken with the temperature stabilized. Corresponding points are then read from each photo at a suitable number of time increments. Each pair of voltage and current values are multiplied together to give instantaneous values of power. The results are plotted on linear graph paper, the number of squares within the curve counted, and the total divided by the number of squares along the time axis. The quotient is the average power dissipation. Oscilloscopes are available to perform these measurements and make the necessary calculations.

Substitution

This method is based upon substituting an easily measurable, smooth dc source for a complex waveform. A switching arrangement is provided which allows operating the load with the device under test, until it stabilizes in temperature. Case temperature is monitored. By throwing the switch to the "test" position, the device under test is connected to a dc power supply, while another pole of the switch supplies the normal power to the load to keep it operating at full power level. The dc supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The dc voltage and current values are multiplied together to obtain average power. It is generally necessary that a Kelvin connection be used for the device voltage measurement.

APPENDIX A
THERMAL RESISTANCE CONCEPTS

The basic equation for heat transfer under steady-state conditions is generally written as:

$$q = hA\Delta T \qquad (1)$$

where
- q = rate of heat transfer or power dissipation (P_D)
- h = heat transfer coefficient,
- A = area involved in heat transfer,
- ΔT = temperature difference between regions of heat transfer.

However, electrical engineers generally find it easier to work in terms of thermal resistance, defined as the ratio of temperature to power. From Equation 1, thermal resistance, R_θ, is

$$R_\theta = \Delta T/q = 1/hA \qquad (2)$$

The coefficient (h) depends upon the heat transfer mechanism used and various factors involved in that particular mechanism.

An analogy between Equation (2) and Ohm's Law is often made to form models of heat flow. Note that T could be thought of as a voltage thermal resistance corresponds to electrical resistance (R); and, power (q) is analogous to current (I). This gives rise to a basic thermal resistance model for a semiconductor as indicated by Figure A1.

The equivalent electrical circuit may be analyzed by using Kirchoff's Law and the following equation results:

$$T_J = P_D(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A \qquad (3)$$

where
- T_J = junction temperature,
- P_D = power dissipation
- $R_{\theta JC}$ = semiconductor thermal resistance (junction to case),
- $R_{\theta CS}$ = interface thermal resistance (case to heatsink),
- $R_{\theta SA}$ = heatsink thermal resistance (heatsink to ambient),
- T_A = ambient temperature.

The thermal resistance junction to ambient is the sum of the individual components. Each component must be minimized if the lowest junction temperature is to result.

The value for the interface thermal resistance, $R_{\theta CS}$, may be significant compared to the other thermal-resistance terms. A proper mounting procedure can minimize $R_{\theta CS}$.

The thermal resistance of the heatsink is not absolutely constant; its thermal efficiency increases as ambient temperature increases and it is also affected by orientation of the sink. The thermal resistance of the semiconductor is also variable; it is a function of biasing and temperature. Semiconductor thermal resistance specifications are normally at conditions where current density is fairly uniform. In some applications such as in RF power amplifiers and short-pulse applications, current density is not uniform and localized heating in the semiconductor chip will be the controlling factor in determining power handling ability.
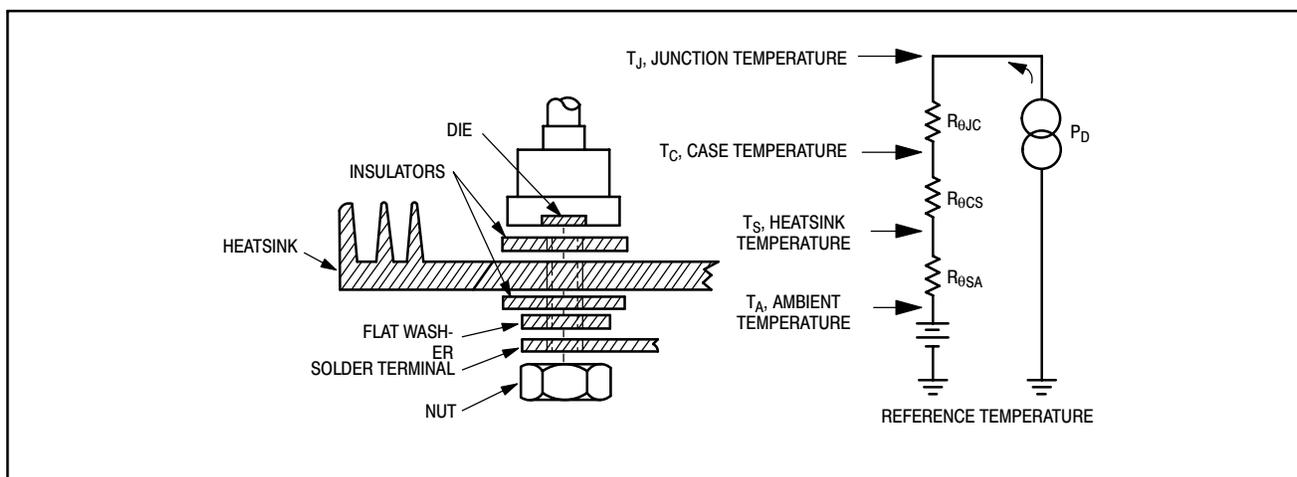
Figure A1. Basic Thermal Resistance Model Showing Thermal to Electrical Analogy for a Semiconductor

MEASUREMENT OF INTERFACE THERMAL RESISTANCE

Measuring the interface thermal resistance $R_{\theta CS}$ appears deceptively simple. All that's apparently needed is a thermocouple on the semiconductor case, a thermocouple on the heatsink, and a means of applying and measuring DC power. However, $R_{\theta CS}$ is proportional to the amount of contact area between the surfaces and consequently is affected by surface flatness and finish and the amount of pressure on the surfaces. The fastening method may also be a factor. In addition, placement of the thermocouples can have a significant influence upon the results. Consequently, values for interface thermal resistance presented by different manufacturers are not in good agreement. Fastening methods and thermocouple locations are considered in this Appendix.

When fastening the test package in place with screws, thermal conduction may take place through the screws, for example, from the flange ear on a TO-3 package directly to the heatsink. This shunt path yields values which are artificially low for the insulation material and dependent upon screw head contact area and screw material. MIL-I-49456 allows screws to be used in tests for interface thermal resistance probably because it can be argued that this is "application oriented."

Thermalloy takes pains to insulate all possible shunt conduction paths in order to more accurately evaluate insulation materials. The ON Semiconductor fixture uses an insulated clamp arrangement to secure the package which also does not provide a conduction path.

As described previously, some packages, such as a TO-220, may be mounted with either a screw through the tab or a clip bearing on the plastic body. These two methods often yield different values for interface thermal resistance. Another discrepancy can occur if the top of the package is exposed to the ambient air where radiation and convection can take place. To avoid this, the package should be covered with insulating foam. It has been estimated that a 15 to 20% error in $R_{\theta CS}$ can be incurred from this source.

Another significant cause for measurement discrepancies is the placement of the thermocouple to measure the semiconductor case temperature. Consider the TO-220 package shown in Figure B1. The mounting pressure at one end causes the other end — where the die is located — to lift off the mounting surface slightly. To improve contact, ON Semiconductor TO-220 Packages are slightly concave. Use of a spreader bar under the screw lessens the lifting, but some is inevitable with a package of this structure. Three thermocouple locations are shown:

a. The ON Semiconductor location is directly under the die reached through a hole in the heatsink. The thermocouple is held in place by a spring which forces the thermocouple into intimate contact with the bottom of the semi's case.

b. The JEDEC location is close to the die on the top surface of the package base reached through a blind hole drilled through the molded body. The thermocouple is swaged in place.

c. The Thermalloy location is on the top portion of the tab between the molded body and the mounting screw. The thermocouple is soldered into position.
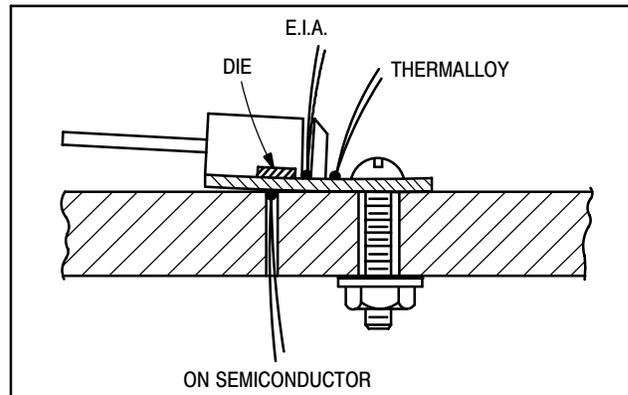
Figure B1. JEDEC TO-220 Package Mounted to Heatsink Showing Various Thermocouple Locations and Lifting Caused by Pressure at One End

Temperatures at the three locations are generally not the same. Consider the situation depicted in the figure. Because the only area of direct contact is around the mounting screw, nearly all the heat travels horizontally along the tab from the die to the contact area. Consequently, the temperature at the JEDEC location is hotter than at the Thermalloy location and the ON Semiconductor location is even hotter. Since junction-to-sink thermal resistance must be constant for a given test setup, the calculated junction-to-case thermal resistance values decrease and case-to-sink values increase as the "case" temperature thermocouple readings become warmer. Thus the choice of reference point for the "case" temperature is quite important.

There are examples where the relationship between the thermocouple temperatures are different from the previous situation. If a mica washer with grease is installed between the semiconductor package and the heatsink, tightening the screw will not bow the package; instead, the mica will be deformed. The primary heat conduction path is from the die through the mica to the heatsink. In this case, a small temperature drop will exist across the vertical dimension of the package mounting base so that the thermocouple at the EIA location will be the hottest. The thermocouple temperature at the Thermalloy location will be lower but close to the temperature at the EIA location as the lateral heat flow is generally small. The ON Semiconductor location will be coolest.

The EIA location is chosen to obtain the highest temperature on the case. It is of significance because power ratings are supposed to be based on this reference point. Unfortunately, the placement of the thermocouple is tedious and leaves the semiconductor in a condition unfit for sale.

The ON Semiconductor location is chosen to obtain the highest temperature of the case at a point where, hopefully, the case is making contact to the heatsink. Once the special heatsink to accommodate the thermocouple has been fabricated, this method lends itself to production testing and does not mark the device. However, this location is not easily accessible to the user.

The Thermalloy location is convenient and is often chosen by equipment manufacturers. However, it also blemishes the case and may yield results differing up to 1°C/W for a TO-220 package mounted to a heatsink without thermal grease and no insulator. This error is small when compared to the thermal resistance of heat dissipaters often used with this package, since power dissipation is usually a few watts. When compared to the specified junction-to-case values of some of the higher power semiconductors becoming available, however, the difference becomes significant and it is important that the semiconductor manufacturer and equipment manufacturer use the same reference point.

Another EIA method of establishing reference temperatures utilizes a soft copper washer (thermal grease is used) between the semiconductor package and the heatsink. The washer is flat to within 1 mil/inch, has a finish better than 63 μ-inch, and has an imbedded thermocouple near its center. This reference includes the interface resistance under nearly ideal conditions and is therefore application-oriented. It is also easy to use but has not become widely accepted.

A good way to improve confidence in the choice of case reference point is to also test for junction-to-case thermal resistance while testing for interface thermal resistance. If the junction-to-case values remain relatively constant as insulators are changed, torque varied, etc., then the case reference point is satisfactory.

SECTION 8
RELIABILITY AND QUALITY

Edited and Updated

USING TRANSIENT THERMAL RESISTANCE DATA IN HIGH POWER PULSED THYRISTOR APPLICATIONS

INTRODUCTION

For a certain amount of dc power dissipated in a semiconductor, the junction temperature reaches a value which is determined by the thermal conductivity from the junction (where the power is dissipated) to the air or heat sink. When the amount of heat generated in the junction equals the heat conducted away, a steady–state condition is reached and the junction temperature can be calculated by the simple equation:

$$T_J = P_D R_{\theta JR} + T_R \qquad (1a)$$

where T_J = junction temperature
          T_R = temperature at reference point
          P_D = power dissipated in the junction
          $R_{\theta JR}$ = steady–state thermal resistance from junction to the temperature reference point.

Power ratings of semiconductors are based upon steady–state conditions, and are determined from equation (1a) under worst case conditions, i.e.:

$$P_{D(max)} = \frac{T_{J(max)} - T_R}{R_{\theta JR(max)}} \qquad (1b)$$

$T_{J(max)}$ is normally based upon results of an operating life test or serious degradation with temperature of an important device characteristic. T_R is usually taken as 25°C, and $R_{\theta JR}$ can be measured using various techniques. The reference point may be the semiconductor case, a lead, or the ambient air, whichever is most appropriate. Should the reference temperature in a given application exceed the reference temperature of the specification, P_D must be correspondingly reduced.

Thermal resistance allows the designer to determine power dissipation under steady state conditions. Steady state conditions between junction and case are generally achieved in one to ten seconds while minutes may be required for junction to ambient temperature to become stable. However, for pulses in the microsecond and millisecond region, the use of steady–state values will not yield true power capability because the thermal response of the system has not been taken into account.

Note, however, that semiconductors also have pulse power limitations which may be considerably lower – or even greater – than the allowable power as deduced from thermal response information. For transistors, the second breakdown portion of the pulsed safe operating area defines power limits while surge current or power ratings are given for diodes and thyristors. These additional ratings must be used in conjunction with the thermal response to determine power handling capability.

To account for thermal capacity, a time dependent factor r(t) is applied to the steady–state thermal resistance. Thermal resistance, at a given time, is called transient thermal resistance and is given by:

$$R_{\theta JR(t)} = r(t) \cdot R_{\theta JR} \qquad (2)$$

The mathematical expression for the transient thermal resistance has been determined to be extremely complex. The response is, therefore, plotted from empirical data. Curves, typical of the results obtained, are shown in Figure 8.1. These curves show the relative thermal response of the junction, referenced to the case, resulting from a step function change in power. Observe that the total percentage difference is about 10:1 in the short pulse ($\sqrt{t}$) region. However, the values of thermal resistance vary over 20:1.

Many ON Semiconductor data sheets have a graph similar to that of Figure 8.2. It shows not only the thermal response to a step change in power (the D = 0, or single pulse curve) but also has other curves which may be used to obtain an effective r(t) value for a train of repetitive pulses with different duty cycles. The mechanics of using the curves to find T_J at the end of the first pulse in the train, or to find $T_{J(pk)}$ once steady state conditions have been achieved, are quite simple and require no background in the subject. However, problems where the applied power pulses are either not identical in amplitude or width, or the duty cycle is not constant, require a more thorough understanding of the principles illustrated in the body of this report.

USE OF TRANSIENT THERMAL RESISTANCE DATA

Part of the problem in applying thermal response data stems from the fact that power pulses are seldom rectangular, therefore to use the r(t) curves, an equivalent rectangular model of the actual power pulse must be determined. Methods of doing this are described near the end of this note.

Before considering the subject matter in detail, an example will be given to show the use of the thermal response data sheet curves. Figure 8.2 is a representative graph which applies to a 2N5886 transistor.

Pulse power P_D = 50 Watts
Duration t = 5 milliseconds
Period τ_p = 20 milliseconds
Case temperature, T_C = 75°C
Junction to case thermal resistance,
    $R_{\theta JC}$ = 1.17°C/W

The temperature is desired, a) at the end of the first pulse b) at the end of a pulse under steady state conditions.

For part (a) use:

$$T_J = r(5 \text{ ms}) \, R_{\theta JC} P_D + T_C$$

The term r(5 ms) is read directly from the graph of Figure 8.2 using the D = 0 curve,

$$\therefore T_J = 0.49 \times 1.17 \times 50 + 75 = 28.5 + 75 = 103.5$$

The peak junction temperature rise under steady conditions is found by:

$$T_J = r(t, D) \, R_{\theta JC} \, P_D + T_C$$

$D = t/\tau_p = 5/20 - 0.25$. A curve for D= 0.25 is not on the graph; however, values for this duty cycle can be interpolated between the D = 0.2 and D = 0.5 curves. At 5 ms, read r(t) ≈ 0.59.

$$T_J = 0.59 \times 1.17 \times 50 + 75 = 34.5 + 75 = 109.5°C$$

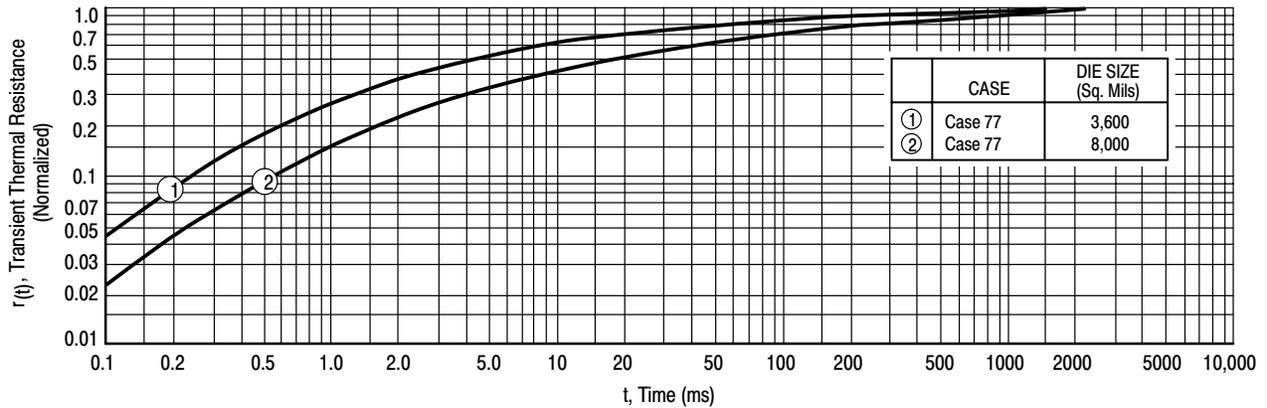Figure 8.1. Thermal Response, Junction to Case, of Case 77 Types For a Step of Input Power

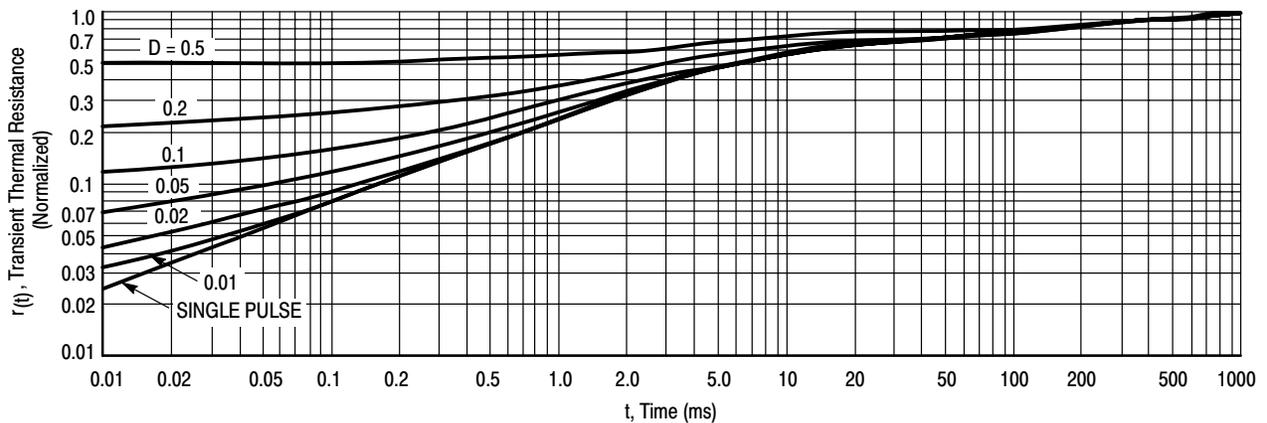|	CASE	DIE SIZE (Sq. Mils)
①	Case 77	3,600
②	Case 77	8,000

Figure 8.2. Thermal Response Showing the Duty Cycle Family of Curves

The average junction temperature increase above ambient is:

$$T_{J(average)} - T_C = R_{\theta JC} P_D D$$
$$= (1.17)(50)(0.25) \quad (3)$$
$$= 14.62°C$$

Note that T_J at the end of any power pulse does not equal the sum of the average temperature rise (14.62°C in the example) and that due to one pulse (28.5°C in example), because cooling occurs between the power pulses.

While junction temperature can be easily calculated for a steady pulse train where all pulses are of the same amplitude and pulse duration as shown in the previous example, a simple equation for arbitrary pulse trains with random variations is impossible to derive. However, since the heating and cooling response of a semiconductor is essentially the same, the superposition principle may be used to solve problems which otherwise defy solution.

Using the principle of superposition each power interval is considered positive in value, and each cooling interval negative, lasting from time of application to infinity. By multiplying the thermal resistance at a particular time by the magnitude of the power pulse applied, the magnitude of the junction temperature change at a particular time can be obtained. The net junction temperature is the algebraic sum of the terms.

The application of the superposition principle is most easily seen by studying Figure 8.3.

Figure 8.3(a) illustrates the applied power pulses. Figure 8.3(b) shows these pulses transformed into pulses lasting from time of application and extending to infinity; at t_o, P_1 starts and extends to infinity; at t_1, a pulse $(-P_1)$ is considered to be present and thereby cancels P_1 from time t_1, and so forth with the other pulses. The junction temperature changes due to these imagined positive and negative pulses are shown in Figure 8.3(c). The actual junction temperature is the algebraic sum as shown in Figure 8.3(d).

Problems may be solved by applying the superposition principle exactly as described; the technique is referred to as Method 1, the pulse–by–pulse method. It yields satisfactory results when the total time of interest is much less than the time required to achieve steady state conditions, and must be used when an uncertainty exists in a random pulse train as to which pulse will cause the highest temperature. Examples using this method are given in Appendix A under Method 1.

For uniform trains of repetitive pulses, better answers result and less work is required by averaging the power pulses to achieve an average power pulse; the temperature is calculated at the end of one or two pulses following the average power pulse. The essence of this method is shown in Figure 8.6. The duty cycle family of curves shown in Figure 8.2 and used to solve the example problem is based on this method; however, the curves may only be used for a uniform train after steady state conditions are achieved. Method 2 in Appendix A shows equations for calculating the temperature at the end of the n_{th} or $n + 1$ pulse in a uniform train. Where a duty cycle family of curves is available, of course, there is no need to use this method.
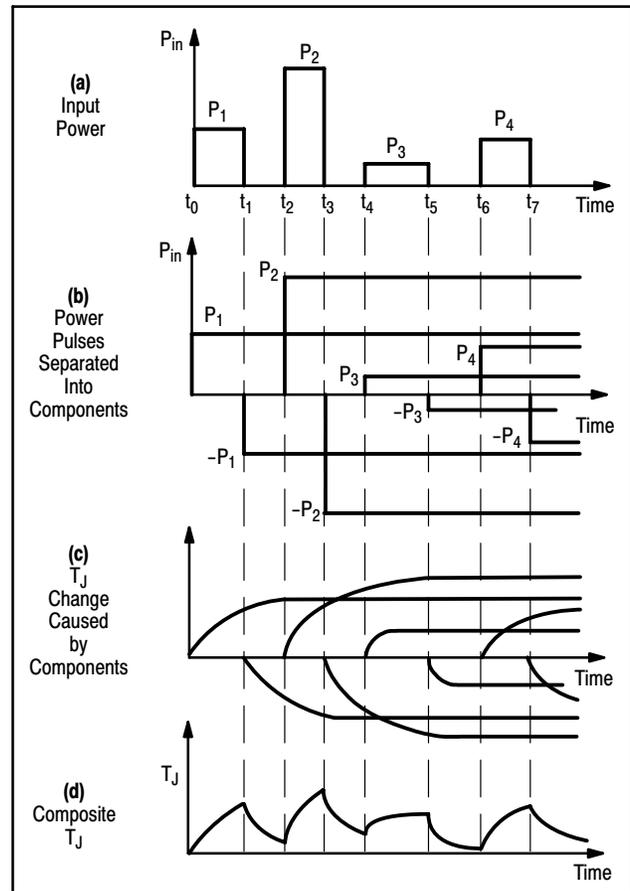

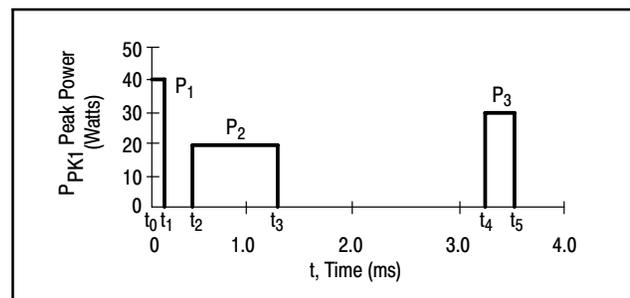**Figure 8.3. Application of Superposition Principle**

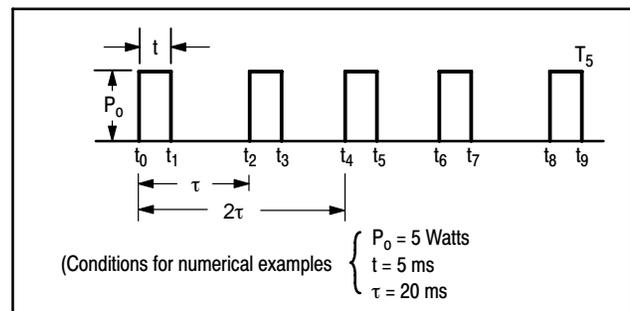**Figure 8.4. Non–Repetitive Pulse Train (Values Shown Apply to Example in Appendix)**

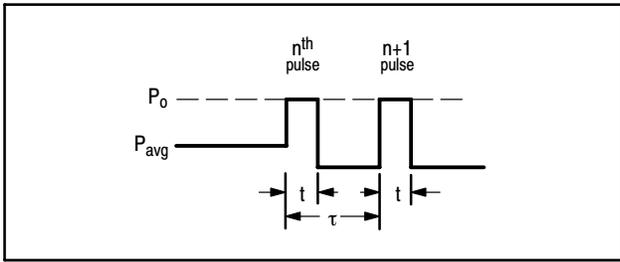**Figure 8.5. A Train of Equal Repetitive Pulses**

Figure 8.6. Model For a Repetitive Equal Pulse Train

Temperature rise at the end of a pulse in a uniform train before steady state conditions are achieved is handled by Method 3 (a or b) in the Appendix. The method is basically the same as for Method 2, except the average power is modified by the transient thermal resistance factor at the time when the average power pulse ends.

A random pulse train is handled by averaging the pulses applied prior to situations suspected of causing high peak temperatures and then calculating junction temperature at the end of the n_{th} or $n + 1$ pulse. Part c of Method 3 shows an example of solving for temperature at the end of the 3rd pulse in a three pulse burst.

HANDLING NON–RECTANGULAR PULSES

The thermal response curves, Figure 8.1, are based on a step change of power; the response will not be the same for other waveforms. Thus far in this treatment we have assumed a rectangular shaped pulse. It would be desirable to be able to obtain the response for any arbitrary waveform, but the mathematical solution is extremely unwieldy. The simplest approach is to make a suitable equivalent rectangular model of the actual power pulse and use the given thermal response curves; the primary rule to observe is that the energy of the actual power pulse and the model are equal.

Experience with various modeling techniques has lead to the following guidelines:

For a pulse that is nearly rectangular, a pulse model having an amplitude equal to the peak of the actual pulse, with the width adjusted so the energies are equal, is a conservative model. (See Figure 8.7(a)).

Sine wave and triangular power pulses model well with the amplitude set at 70% of the peak and the width adjusted to 91% and 71%, respectively, of the baseline width (as shown on Figure 8.7(b)).

A power pulse having a $\sin^2$ shape models as a triangular waveform.

Power pulses having more complex waveforms could be modeled by using two or more pulses as shown in Figure 8.7(c).

A point to remember is that a high amplitude pulse of a given amount of energy will produce a higher rise in junction temperature than will a lower amplitude pulse of longer duration having the same energy.
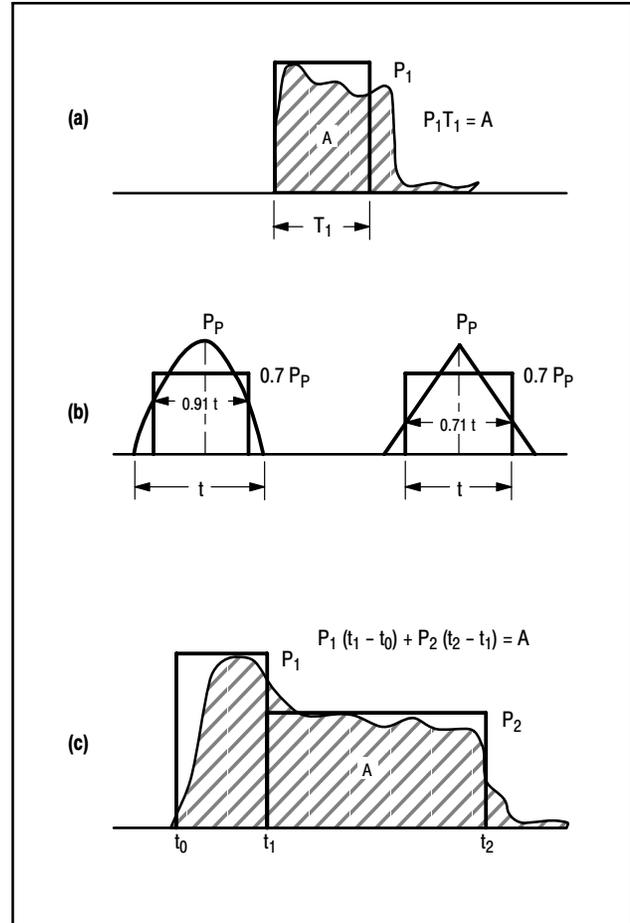

Figure 8.7. Modeling of Power Pulses

As an example, the case of a transistor used in a dc to ac power converter will be analyzed. The idealized waveforms of collector current, I_C, collector to emitter voltage, V_{CE}, and power dissipation P_D, are shown in Figure 8.8.

A model of the power dissipation is shown in Figure 8.8(d). This switching transient of the model is made, as was suggested, for a triangular pulse.

For example, T_J at the end of the rise, on, and fall times, T_1, T_2 and T_3 respectively, will be found.

Conditions:

TO–3 package,

$R_{\theta JC} = 0.5°C/W$, $I_C = 60A$, $V_{CE(off)} = 60$ V
$T_A = 50°C$
$t_f = 80$ μs, $t_r = 20$ μs
$V_{CE(sat)} = 0.3$ V @ 60 A
Frequency = 2 kHz $\therefore \tau = 500$ μs
$P_{on} = (60)(0.3) = 18$ W
$P_f = 30 \times 30 = 900$ W $= P_r$

Assume that the response curve in Figure 8.1 for a die area of 58,000 square mils applies. Also, that the device is mounted on an MS−15 heat sink using Dow Corning DC340 silicone compound with an air flow of 1.0 lb/min flowing across the heat−sink. (From MS−15 Data Sheet, $R_{\theta CS} = 0.1°C/W$ and $R_{\theta SA} = 0.55°C/W$).

Procedure: Average each pulse over the period using equation 1−3 (Appendix A, Method 2), i.e.,

$$P_{avg} = 0.7\, P_r\, 0.71\, \frac{t_r}{\tau} + P_{on}\, \frac{t_{on}}{\tau} + 0.7\, P_f\, 0.71\, \frac{t_f}{\tau}$$

$$= (0.7)(900)(0.71)\frac{(20)}{500} + (18)\frac{(150)}{500}$$

$$\quad + (0.7)(900)(0.71)\frac{80}{500}$$

$$= 17.9 + 5.4 + 71.5$$

$$= 94.8\ W$$

From equation 1−4, Method 2A:

$$T_1 = [P_{avg} + (0.7\, P_r - P_{avg}) \cdot r(t_1 - t_o)]\, R_{\theta JC}$$

At this point it is observed that the thermal response curves of Figure 8.1 do not extend below 100 μs. Heat transfer theory for one dimensional heat flow indicates that the response curve should follow the $\sqrt{t}$ law at small times. Using this as a basis for extending the curve, the response at 14.2 μs is found to be 0.023.

Figure 8.8. Idealized Waveforms of I_C, V_{CE} and P_D in a DC to AC Inverter

We then have:

$T_1 = [94.8 + (630 − 94.8).023] (0.5)$

$= (107.11)(0.5) = 53.55°C$

For T_2 we have, by using superposition:

$T_2 = [P_{avg} − P_{avg} \cdot r(t_2 − t_o) + 0.7\, P_r \cdot$
$\quad r(t_2 − t_o) − 0.7\, P_r \cdot r(t_2 − t_1) + P_{on} \cdot$
$\quad r(t_2 − t_1)]\, R_{\theta JC}$

$= [P_{avg} + (0.7\, P_r − P_{avg}) \cdot r(t_2 − t_o) +$
$\quad (P_{on} − 0.7\, P_r) \cdot r(t_2 − t_1)]\, R_{\theta JC}$

$= [94.8 + (630 − 94.8) \cdot r(164\ \mu s) + (18 − 630)$
$\quad \cdot r(150\ \mu s)] (0.5)$

$= [94.8 + (535.2)(.079) − (612)(.075)] (0.5)$

$= [94.8 + 42.3 − 45.9] (0.5)$

$= (91.2)(0.5) = 45.6°C$

For the final point T_3 we have:

$T_3 = [P_{avg} − P_{avg} \cdot r(t_3 − t_o) + 0.7\, P_r \cdot$
$\quad r(t_3 − t_o) − 0.7\, P_r \cdot r(t_3 − t_1) + P_{on} \cdot$
$\quad r(t_3 − t_1) − P_{on} \cdot r(t_3 − t_2)$
$\quad + 0.7\, P_f \cdot r(t_3 − t_2)]\, R_{\theta JC}$
$\quad [P_{avg} + (0.7\, P_r − Pavg) \cdot r(t_3 − t_o) +$
$\quad (P_{on} − 0.7\, P_r) \cdot r(t_3 − t_1) + (0.7\, P_f − P_{on})$
$\quad \cdot \quad r(t_3 − t_2)]\, R_{\theta JC}$

$= [94.8 + (535.2) \cdot r(221\ \mu s) + (−612) \cdot r(206.8\ \mu s)$
$\quad + (612) \cdot r(56.8 \mu s)] (0.5)$

$= [94.8 + (535.2)(0.09) − (612)(0.086) +$
$\quad (612)(0.045)] (0.5)$

$= [94.8 + 481.7 − 52.63 + 27.54] (0.5)$

$= (117.88)(0.5) = 58.94°C$

The junction temperature at the end of the rise, on, and fall times, T_{J1}, T_{J2}, and T_{J3}, is as follows:

$$T_{J1} = T_1 + T_A + R_{\theta CA} \cdot P_{avg}$$

$$R_{\theta CA} = R_{\theta CS} = R_{\theta SA} = 0.1 + 0.55$$

$$T_{J1} = 53.55 + 50 + (0.65)(94.8) = 165.17°C$$

$$T_{J2} = T_2 + T_A + R_{\theta CA} \cdot P_{avg}$$

$$= 45.6 + 50 + (0.65)(94.8)$$

$$= 157.22°C$$

$$T_{J3} = T_3 + T_A + R_{\theta CA} \cdot P_{avg}$$

$$= 58.94 + 50 + (0.65)(94.8)$$

$$= 170.56°C$$

$$T_{J(avg)} = P_{avg} (R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A$$

$$= (94.8)(0.5 + 0.1 + 0.55) + 50$$

$$= (94.8)(1.15) + 50 = 159.02°C$$

Inspection of the results of the calculations T_1, T_2, and T_3 reveal that the term of significance in the equations is the average power. Even with the poor switching times there was a peak junction temperature of 11.5°C above the average value. This is a 7% increase which for most applications could be ignored, especially when switching times are considerably less. Thus the product of average power and steady state thermal resistance is the determining factor for junction temperature rise in this application.

SUMMARY

This report has explained the concept of transient thermal resistance and its use. Methods using various degrees of approximations have been presented to determine the junction temperature rise of a device. Since the thermal response data shown is a step function response, modeling of different wave shapes to an equivalent rectangular pulse of pulses has been discussed.

The concept of a duty cycle family of curves has also been covered; a concept that can be used to simplify calculation of the junction temperature rise under a repetitive pulse train.

APPENDIX A METHODS OF SOLUTION

In the examples, a type 2N3647 transistor will be used; its steady state thermal resistance, $R_{\theta JC}$, is 35°C/W and its value for r(t) is shown in Figure A1.

Definitions:

P_1, P_2, P_3 ... P_n = power pulses (Watts)

T_1, T_2, T_3 ... T_n = junction to case temperature at end of P_1, P_2, P_3 ... P_n

t_0, t_1, t_2, ... t_n = times at which a power pulse begins or ends

$r(t_n - t_k)$ = transient thermal resistance factor at end of time interval $(t_n - t_k)$.

Table 8.1. Several Possible Methods of Solutions

1. Junction Temperature Rise Using Pulse–By–Pulse Method
   A. Temperature rise at the end of the n_{th} pulse for pulses with unequal amplitude, spacing, and duration.
   B. Temperature rise at the end of the n_{th} pulse for pulses with equal amplitude, spacing, and duration.
2. Temperature Rise Using Average Power Concept Under Steady State Conditions For Pulses Of Equal Amplitude, Spacing, And Duration
   A. At the end of the n_{th} pulse.
   B. At the end of the (n + 1) pulse.
3. Temperature Rise Using Average Power Concept Under Transient Conditions.
   A. At the end of the n_{th} pulse for pulses of equal amplitude, spacing and duration.
   B. At the end of the n + 1 pulse for pulses of equal amplitude, spacing and duration.
   C. At the end of the n_{th} pulse for pulses of unequal amplitude, spacing and duration.
   D. At the end of the n + 1 pulse for pulses of unequal amplitude, spacing and duration.

METHOD 1A – FINDING T_J AT THE END OF THE Nth PULSE IN A TRAIN OF UNEQUAL AMPLITUDE, SPACING, AND DURATION

General Equation:

$$T_n = \sum_{i=1}^{n} P_i [r(t_{2n-1} - t_{2i-2}) \qquad (1-1)$$
$$- r(t_{n-1} - t_{2i-1})]R_{\theta JC}$$

where n is the number of pulses and P_i is the peak value of the ith pulse.

To find temperature at the end of the first three pulses, Equation 1–1 becomes:

$$T_1 = P_1 r(t_1) R_{\theta JC} \qquad (1-1A)$$

$$T_2 = [P_1 r(t_3) - P_1 r(t_3 - t_1) \qquad (1-1B)$$
$$+ P_2 r(t_3 - t_2)] R_{\theta JC}$$

$$T_3 = [P_1 r(t_5) - P_1 r(t_5 - t_1) + P_2 r(t_5 - t_2) \qquad (1-1C)$$
$$- P_2 r(t_5 - t_3) + P_3 r(t_5 - t_4)] R_{\theta JC}$$

Example:

Conditions are shown on Figure 4 as:

$P_1 = 40$ W	$t_0 = 0$	$t_3 = 1.3$ ms
$P_2 = 20$ W	$t_1 = 0.1$ ms	$t_4 = 3.3$ ms
$P_3 = 30$ W	$t_2 = 0.3$ ms	$t_5 = 3.5$ ms

Therefore,

$t_1 - t_0 = 0.1$ ms	$t_3 - t_1 = 1.2$ ms
$t_2 - t_1 = 0.2$ ms	$t_5 - t_1 = 3.4$ ms
$t_3 - t_2 = 1$ ms	$t_5 - t_2 = 3.2$ ms
$t_4 - t_3 = 2$ ms	$t_5 - t_3 = 2.2$ ms
$t_5 - t_4 = 0.2$ ms	

Procedure:

Find $r(t_n - t_k)$ for preceding time intervals from Figure 8.2, then substitute into Equations 1–1A, B, and C.

$T_1 = P_1 \, r(t_1) \, R_{\theta JC} = 40 \cdot 0.05 \cdot 35 = 70°C$

$T_2 = [P_1 \, r(t_3) - P_1 \, r(t_3 - t_1) + P_2 \, r(t_3 - t_2)] \, R_{\theta JC}$

$\quad = [40 \, (0.175) - 40 \, (0.170) + 20 \, (0.155)] \, 35$

$\quad = [40 \, (0.175 - 0.170) + 20 \, (0.155)] \, 35$

$\quad = [0.2 + 3.1] \, 35 = 115.5°C$

$T_3 = [P_1 \, r(t_5) - P_1 \, r(t_5 - t_1) + P_2 \, r(t_5 - t_2)$
$\quad\quad - P_2 \, r(t_5 - t_3) + P_3 \, r(t_5 - t_4)] \, \theta_{JC}$

$T_3 = [40 \, (0.28) - 40 \, (0.277) + 20 \, (0.275) - 20 \, (0.227)$
$\quad\quad + 30 \, (0.07)] \, 35$

$\quad = [40 \, (0.28 - 0.277) + 20 \, (0.275 - 0.227)$
$\quad\quad + 30 \, (0.07)] \, 35$

$\quad = [0.12 + 0.96 + 2.1]† \; 35 = 3.18 \cdot 35 = 111.3°C$

Note, by inspecting the last bracketed term in the equations above that very little residual temperature is left from the first pulse at the end of the second and third pulse. Also note that the second pulse gave the highest value of junction temperature, a fact not so obvious from inspection of the figure. However, considerable residual temperature from the second pulse was present at the end of the third pulse.

METHOD 1B – FINDING T_J AT THE END OF THE Nth PULSE IN A TRAIN OF EQUAL AMPLITUDE, SPACING, AND DURATION

The general equation for a train of equal repetitive pulses can be derived from Equation 1–1. $P_i = P_D$, $t_i = t$, and the spacing between leading edges or trailing edges of adjacent pulses is τ.

General Equation:

$$T_n = P_D R_{\theta JC} \sum_{i=1}^{n} r[(n-i)\,\tau + t] \qquad (1–2)$$
$$- r[(n-i)\,\tau]$$

Expanding:

$T_n = P_D \, R_{\theta JC} \, r[(n-1)\,\tau + t] - r[(n-1)\,\tau]$
$\quad + r[(n-2)\,\tau + t] - r[(n-2)\,\tau] + r[(n-3)$
$\quad \tau + t] - r[(n-3)\,\tau] + \ldots + r[(n-i)\,\tau + t]$
$\quad - r[(n-i)\,\tau] \ldots \ldots + r(t)] \qquad (1–2A)$

---

†Relative amounts of temperature residual from P_1, P_2, and P_3 respectively are indicated by the terms in brackets.

For 5 pulses, equation 1–2A is written:

$T_5 = P_D \, R_{\theta JC} \, [r(4\,\tau + t) - r(4\tau) + r(3\tau + t)]$
$\quad - r(3\tau) + r(2\tau + t) - r(2\tau) + r(\tau + t)$
$\quad - r(\tau) + r(t)]$

Example:

Conditions are shown on Figure 8.5 substituting values into the preceding expression:

$T_5 = (5) \, (35) \, [r(4.20 + 5) - r(4.20) + r(3.20 + 5)$
$\quad + r(3.20) + r(2.20 + 5) - r(2.20) + r(20 + 5)$
$\quad - r(20) + r(5)]$

$T_5 = (5) \, (35) \, [0.6 - 0.76 + 0.73 - 0.72 + 0.68$
$\quad - 0.66 + 0.59 - 0.55 + 0.33] - (5)(35)(0.40)$

$T_5 = 70.0°C$

Note that the solution involves the difference between terms nearly identical in value. Greater accuracy will be obtained with long or repetitive pulse trains using the technique of an average power pulse as used in Methods 2 and 3.

METHOD 2 – AVERAGE POWER METHOD, STEADY STATE CONDITION

The essence of this method is shown in Figure 8.6. Pulses previous to the n_{th} pulse are averaged. Temperature due to the n_{th} or $n + 1$ pulse is then calculated and combined properly with the average temperature.

Assuming the pulse train has been applied for a period of time (long enough for steady state conditions to be established), we can average the power applied as:

$$P_{avg} = P_D \, \frac{t}{\tau} \qquad (1–3)$$

METHOD 2A – FINDING TEMPERATURE AT THE END OF THE N_{th} PULSE

Applicable Equation:

$$T_n = [P_{avg} + (P_D - P_{avg}) \, r(t)] \, R_{\theta JC} \qquad (1–4)$$

or, by substituting Equation 1–3 into 1–4,

$$Tn = \left[\frac{t}{\tau} + \left(1 - \frac{t}{\tau}\right) r(t) \right] P_D \, R_{\theta JC} \qquad (1–5)$$

The result of this equation will be conservative as it adds a temperature increase due to the pulse $(P_D - P_{avg})$ to the average temperature. The cooling between pulses has not been accurately accounted for; i.e., T_J must actually be less than $T_{J(avg)}$ when the nth pulse is applied.

Example: Find T_n for conditions of Figure 8.5.
Procedure: Find P_{avg} from equation (1–3) and substitute values in equation (1–4) or (1–5).

$$T_n = [(1.25) + (5.0 - 1.25)(0.33)] \ (35)$$
$$= 43.7 + 43.2 = 86.9°C$$

METHOD 2B – FINDING TEMPERATURE AT THE END OF THE N + 1 PULSE

Applicable Equation:

$$T_{n+1} = [P_{avg} + (P_D - P_{avg}) \ r(t + \tau)$$
$$+ P_D \ r(t) - P_D \ r(\tau)] \ R_{\theta JC} \qquad (1–6)$$

or, by substituting equation 1–3 into 1–6,

$$T_{n+1} = \left[\frac{t}{\tau} + \left(1 - \frac{t}{\tau}\right) r(t + \tau) \right.$$
$$\left. + r(t) - r(\tau) \right] P_D R_{\theta JC} \qquad (1–7)$$

Example: Find T_n for conditions of Figure 8.5.
Procedure: Find P_{avg} from equation (1–3) and substitute into equation (1–6) or (1–7).

$$T_{n+1} = [(1.25) + (5 - 1.25)(0.59) + (5)(0.33)$$
$$- (5)(0.56)] \ (35) = 80.9°C$$

Equation (1–6) gives a lower and more accurate value for temperature than equation (1–4). However, it too gives a higher value than the true T_J at the end of the n + 1th pulse. The error occurs because the implied value for T_J at the end of the nth pulse, as was pointed out, is somewhat high. Adding additional pulses will improve the accuracy of the calculation up to the point where terms of nearly equal value are being subtracted, as shown in the examples using the pulse by pulse method. In practice, however, use of this method has been found to yield reasonable design values and is the method used to determine the duty cycle of family of curves – e.g., Figure 8.2.

Note that the calculated temperature of 80.9°C is 10.9°C higher than the result of example 1B, where the temperature was found at the end of the 5th pulse. Since the thermal response curve indicates thermal equilibrium in 1 second, 50 pulses occurring 20 milliseconds apart will be required to achieve stable average and peak temperatures; therefore, steady state conditions were not achieved at the end of the 5th pulse.

METHOD 3 – AVERAGE POWER METHOD, TRANSIENT CONDITIONS

The idea of using average power can also be used in the transient condition for a train of repetitive pulses. The previously developed equations are used but P_{avg} must be modified by the thermal response factor at time $t_{(2n-1)}$.

METHOD 3A – FINDING TEMPERATURE AT THE END OF THE N_{th} PULSE FOR PULSES OF EQUAL AMPLITUDE, SPACING AND DURATION

Applicable Equation:

$$T_n = \left[\frac{t}{\tau} r \ t_{(2n-1)} + \left(1 - \frac{t}{\tau}\right) r(t) \right] \ P_D \ R_{\theta JC} \qquad (1–8)$$

Conditions: (See Figure 8.5)
Procedure: At the end of the 5th pulse (See Figure 8.7) . . .

$$T_5 = [5/20 \cdot r(85) + (1 - 5/20)r(5)] \ (5)(35)$$
$$= [(0.25)(0765) + (0.75)(0.33)] \ (175)$$
$$= 77°C$$

This value is a little higher than the one calculated by summing the results of all pulses; indeed it should be, because no cooling time was allowed between P_{avg} and the nth pulse. The method whereby temperature was calculated at the n + 1 pulse could be used for greater accuracy.

METHOD 3B – FINDING TEMPERATURE AT THE END OF THE N + 1 PULSE FOR PULSES OF EQUAL AMPLITUDE, SPACING AND DURATION

Applicable Equation:

$$T_{n+1} = \left[\frac{t}{\tau} r(t_{2n-1}) + \left(1 - \frac{t}{\tau}\right) \right.$$
$$\left. r(t + \tau) + r(t) - r(\tau) \right] P_D \ R_{\theta JC} \qquad (1–9)$$

Example: Conditions as shown on Figure 8.5. Find temperature at the end of the 5th pulse.

For n + 1 = 5, n = 4, $t_{2n-1} = t_7 = 65$ ms,

$$T_5 = \left[\frac{5}{20} \ r(65 \ ms) + \left(1 - \frac{5}{20}\right) r(25 \ ms) \right.$$
$$\left. + r(5 \ ms) - r(20 \ ms) \right] (5)(35)$$
$$T_5 = [(0.25)(0.73) + (0.75)(0.59) + 0.33 - 0.55](5)(35)$$
$$T_5 = 70.8°C$$

The answer agrees quite well with the answer of Method 1B where the pulse–by–pulse method was used for a repetitive train.

METHOD 3C – FINDING T_J AT THE END OF THE N_{th} PULSE IN A RANDOM TRAIN

The technique of using average power does not limit itself to a train of repetitive pulses. It can be used also where the pulses are of unequal magnitude and duration. Since the method yields a conservative value of junction temperature rise it is a relatively simple way to achieve a first approximation. For random pulses, equations 1–4 through 1–7 can be modified. It is necessary to multiply P_{avg} by the thermal response factor at time $t_{(2n-1)}$. P_{avg} is determined by averaging the power pulses from time of application to the time when the last pulse starts.

Applicable Equations:

$$\text{General: } P_{avg} = \sum_{i=1}^{n} P_i \; \frac{t_{(2i-1)} - t_{(2i-2)}}{t_{(2n)} - t_{(2i-2)}} \qquad (1\text{–}10)$$

For 3 Pulses:

$$P_{avg} = P_1 \; \frac{t_1 - t_0}{t_4 - t_0} + P_2 \; \frac{t_3 - t_2}{t_4 - t_2} \qquad (1\text{–}11)$$

Example: Conditions are shown on Figure 8.4 (refer to Method 1A).
Procedure: Find P_{avg} from equation 1–3 and the junction temperature rise from equation 1–4.
Conditions: Figure 8.4

$$P_{avg} = 40 \cdot \frac{0.1}{3.3} + 20 \; \frac{1}{3} = 1.21 + 6.67$$
$$= 7.88 \text{ Watts}$$
$$T_3 = [P_{avg} \, r(t_5) + (P_3 - P_{avg}) \, r(t_5 - t_4)] \, R_{\theta JC}$$
$$= [7.88 \, (0.28) + (30 - 7.88) \cdot 0.07] \, 35$$
$$= [2.21 + 1.56] \, 35 = 132°C$$

This result is high because in the actual case considerable cooling time occurred between P_2 and P_3 which allowed T_J to become very close to T_C. Better accuracy is obtained when several pulses are present by using equation 1–10 in order to calculate $T_J - t_C$ at the end of the $n^{th} + 1$ pulse. This technique provides a conservative quick answer if it is easy to determine which pulse in the train will cause maximum junction temperature.

METHOD 3D – FINDING TEMPERATURE AT THE END OF THE N + 1 PULSE IN A RANDOM TRAIN

The method is similar to 3C and the procedure is identical. P_{avg} is calculated from Equation 1–10 modified by $r(t_{2n-1})$ and substituted into equation 1–6, i.e.,

$$T_{n+1} = [P_{avg} \, r(t_{2n-1}) + (P_D - P_{ave}) \, r(t_{2n-1} - t_{2n-2}) + P_D \, r(t_{2n+1} - t_{2n}) - P_D \, r(t_{2n+1} - t_{2n-1})] \, R_{\theta JC}$$

The previous example cannot be worked out for the n + 1 pulse because only 3 pulses are present.

Table 8.2. Summary Of Numerical Solution For The Repetitive Pulse Train Of Figure 5

Temperature Desired	Temperature Obtained, °C		
	Pulse by Pulse	Average Power Nth Pulse	Average Power N + 1 Pulse
At End of 5th Pulse	70.0 (1B)	77 (3A)	70.8 (3B)
Steady State Peak	–	86.9 (2A)	80.9 (2B)

Note: Number in parenthesis is method used.
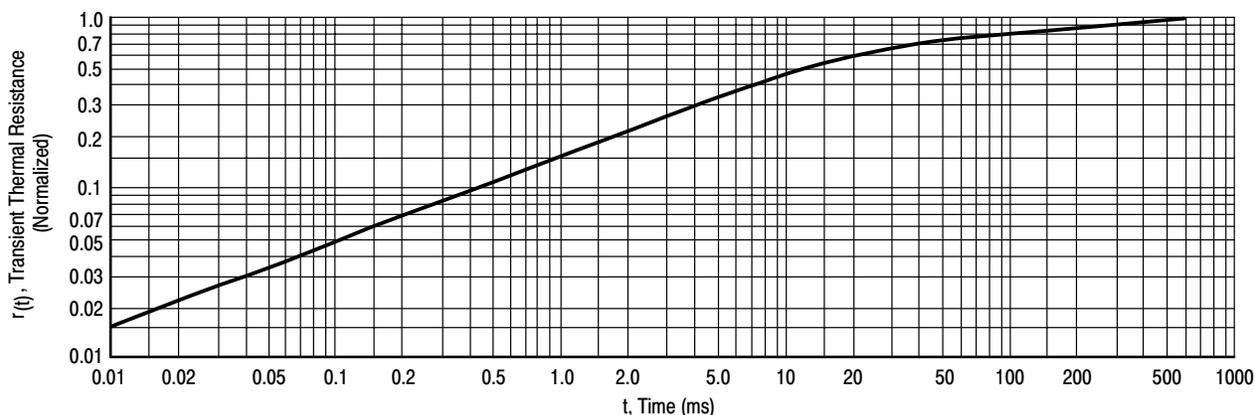
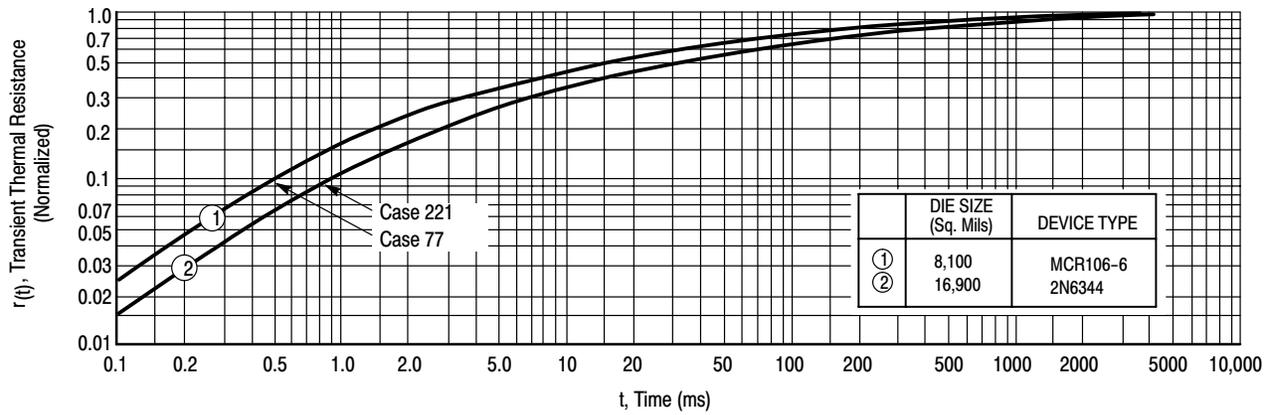**Figure 8.9. 2N3467 Transient Thermal Response**

Figure 8.10. Case 77 and TO–220 Thermal Response

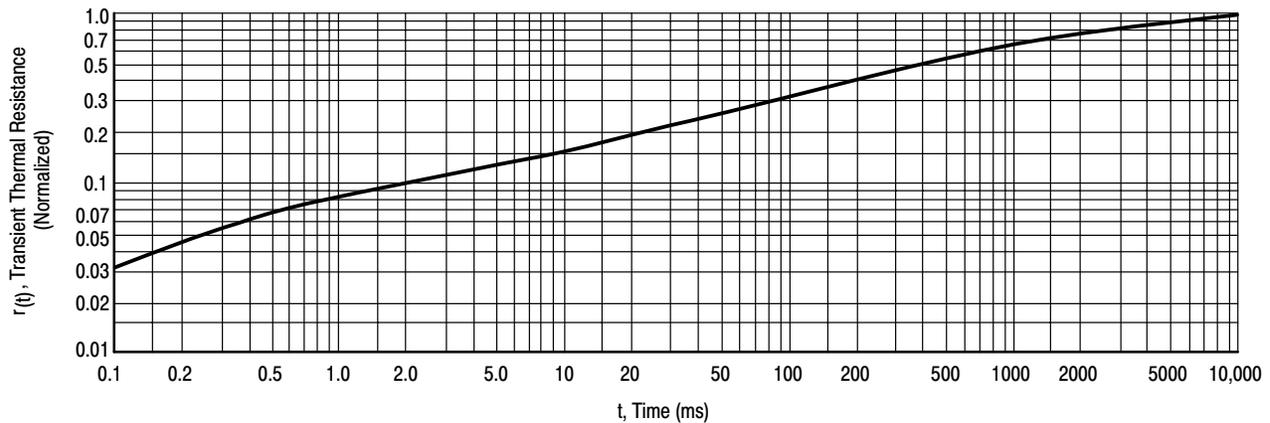|	DIE SIZE (Sq. Mils)	DEVICE TYPE
①	8,100	MCR106–6
②	16,900	2N6344

Figure 8.11. TO–92 Thermal Response, Applies to All Commonly Used Die

As the price of semiconductor devices decreases, reliability and quality have become increasingly important in selecting a vendor. In many cases these considerations even outweigh price, delivery and service.

The reason is that the cost of device fallout and warranty repairs can easily equal or exceed the original cost of the devices. Consider the example shown in Figure 8.12. Although the case is simplistic, the prices and costs are realistic by today's standards. In this case, the cost of failures raised the device cost from 15 cents to 21 cents, an increase of 40%. Clearly, then, investing in quality and reliability can pay big dividends.

With nearly three decades of experience as a major semiconductor supplier, ON Semiconductor is one of the largest manufacturers of discrete semiconductors in the world today. Since semiconductor prices are strongly influenced by manufacturing volume, this leadership has permitted ON Semiconductor to be strongly competitive in the marketplace while making massive investments in equipment, processes and procedures to guarantee that the company's after–purchase costs will be among the lowest in the industry.

Given:
Purchase = 100,000 components @ 15¢ each
Assumptions: Line Fallout = 0.1%
            Warranty Failures = 0.01%

Components Cost = 100,000 × 15¢ = $15,000
Line Fallout Cost =   100 × $40 =   4,000
  @ $40 per repair
Warranty Cost =   10 × $200 =   2,000
  @ $200 per repair   _____
                                     $21,000
Adjusted Cost
Per Component = $21,000 ÷ 100,000 = 21¢

Definitions:
Line Fall out = Module or subassembly failure requiring troubleshooting, parts replacement and retesting
Warranty Failure = System field failure requiring in warranty repair

Figure 8.12. Component Costs to the User (Including Line Fallout and Warranty Costs)

Quality and reliability are two essential elements in order for a semiconductor company to be successful in the marketplace today. Quality and reliability are interrelated because reliability is quality extended over the expected life of the product.

Quality is the assurance that a product will fulfill customers' expectations.

Reliability is the probability that a product will perform its intended function satisfactorily for a prescribed life under certain stated conditions.

The quality and reliability of ON Semiconductor thyristors are achieved with a four step program:

1. Thoroughly tested designs and materials
2. Stringent in–process controls and inspections
3. Process average testing along with 100% quality assurance redundant testing
4. Reliability verifications through audits and reliability studies

ESSENTIALS OF RELIABILITY

Paramount in the mind of every semiconductor user is the question of device performance versus time. After the applicability of a particular device has been established, its effectiveness depends on the length of trouble free service it can offer. The reliability of a device is exactly that — an expression of how well it will serve the customer. Reliability can be redefined as the probability of failure free performance, under a given manufacturer's specifications, for a given period of time. The failure rate of semiconductors in general, when plotted versus a long period of time, exhibit what has been called the "bath tub curve" (Figure 8.13).
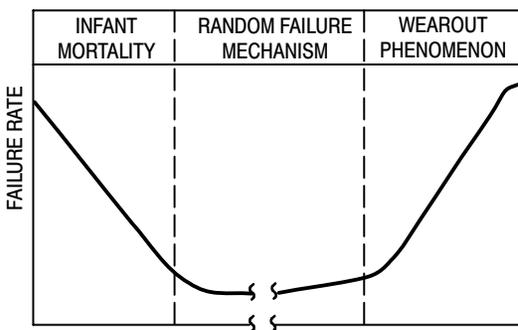

Figure 8.13. Failure Rate of Semiconductor

RELIABILITY MECHANICS

Since reliability evaluations usually involve only samples of an entire population of devices, the concept of the central limit theorem applies and a failure rate is calculated using the λ^2 distribution through the equation:

$$\lambda \le \frac{\lambda^2 \, (\alpha, \, 2r + 2)}{2 \, nt}$$

λ^2 = chi squared distribution

$$\text{where } \alpha = \frac{100 - cl}{100}$$

λ = Failure rate
cl = Confidence limit in percent
r = Number of rejects
n = Number of devices
t = Duration of tests

The confidence limit is the degree of conservatism desired in the calculation. The central limit theorem states that the values of any sample of units out of a large population will produce a normal distribution. A 50% confidence limit is termed the best estimate, and is the mean of this distribution. A 90% confidence limit is a very conservative value and results in a higher λ which represents the point at which 90% of the area of the distribution is to the left of that value (Figure 8.14).
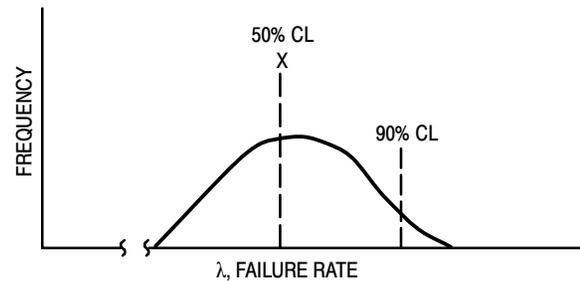

Figure 8.14. Confidence Limits and the Distribution of Sample Failure Rates

The term $(2r + 2)$ is called the degrees of freedom and is an expression of the number of rejects in a form suitable to λ^2 tables. The number of rejects is a critical factor since the definition of rejects often differs between manufacturers. Due to the increasing chance of a test not being representative of the entire population as sample size and test time are decreased, the λ^2 calculation produces surprisingly high values of λ for short test durations even though the true long term failure rate may be quite low. For this reason relatively large amounts of data must be gathered to demonstrate the real long term failure rate. Since this would require years of testing on thousands of devices, methods of accelerated testing have been developed.

Years of semiconductor device testing have shown that temperature will accelerate failures and that this behavior fits the form of the Arrhenius equation:

$$R(t) = R_0(t)e^{-\sigma K T}$$

Where R(t) = reaction rate as a function of time and temperature
R_0 = A constant
t = Time
T = Absolute temperature, °Kelvin (°C + 273°)
o = Activation energy in electron volts (ev)
K = Boltzman's constant = 8.62×10^{-5} ev/°K

This equation can also be put in the form:
AF = Acceleration factor
T2 = User temperature
T1 = Actual test temperature

The Arrhenius equation states that reaction rate increases exponentially with the temperature. This produces a straight line when plotted on log–linear paper with a slope expressed by o. o may be physically interpreted as the energy threshold of a particular reaction or failure mechanism. The overall activation energy exhibited by ON Semiconductor thyristors is 1 ev.

RELIABILITY QUALIFICATIONS/EVALUATIONS OUTLINE:

Some of the functions of ON Semiconductor Reliability and Quality Assurance Engineering are to evaluate new products for introduction, process changes (whether minor or major), and product line updates to verify the integrity and reliability of conformance, thereby ensuring satisfactory performance in the field. The reliability evaluations may be subjected to a series of extensive reliability testing, such as in the tests performed section, or special tests, depending on the nature of the qualification requirement.

AVERAGE OUTGOING QUALITY (AOQ)

With the industry trend to average outgoing qualities (AOQ) of less than 100 PPM, the role of device final test, and final outgoing quality assurance have become a key ingredient to success. At ON Semiconductor, all parts are 100% tested to process average limits then the yields are monitored closely by product engineers, and abnormal areas of fallout are held for engineering investigation. ON Semiconductor also 100% redundant tests all dc

parameters again after marking the device to further reduce any mixing problems associated with the first test. Prior to shipping, the parts are again sampled, tested to a tight sampling plan by our Quality Assurance department, and finally our outgoing final inspection checks for correct paperwork, mixed product, visual and mechanical inspections prior to packaging to the customers.

AVERAGE OUTGOING QUALITY (AOQ)

$$AOQ = \text{Process Average} \times \text{Probability of Acceptance} \times 10^6 \text{ (PPM)}$$

$$\text{Process Average} = \frac{\text{No. of Reject Devices}}{\text{No. of Devices Tested}}$$

$$\text{Probability of Acceptance} = (1 - \frac{\text{No. of Lots Rejected}}{\text{No. of Lots Tested}})$$

$$10^6 = \text{To Convert to Parts Per Million}$$

$$AOQ = \frac{\text{No. of Reject Devices}}{\text{No. of Devices Tested}} \times$$

$$(1 - \frac{\text{No. of Lots Rejected}}{\text{No. of Lots Tested}}) \times 10^6 \text{(PPM)}$$

THYRISTOR RELIABILITY

The reliability data described herein applies to ON Semiconductor's extensive offering of thyristor products for low and medium current applications. The line includes not only the pervasive Silicon Controlled Rectifiers (SCRs) and TRIACs, but also a variety of Programmable Unijunction Transistors (PUTs), SIDACs and other associated devices used for SCR and TRIAC triggering purposes. Moreover, these devices are available in different package styles with overlapping current ranges to provide an integral chip–and–package structure that yields lowest cost, consistent with the overriding consideration of high reliability.

Some of the various packages and the range of electrical specifications associated with the resultant products are shown in Figure 8.15.

To evaluate the reliability of these structures, production line samples from each type of package are being subjected to a battery of accelerated reliability tests deliberately designed to induce long–term failure. Though the tests are being conducted on a continuing basis, the results so far are both meaningful and impressive. They are detailed on the following pages in the hope that they will provide for the readers a greater awareness of the potential for thyristors in their individual application.
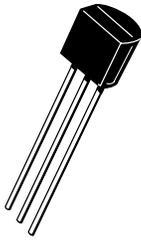
TO−92
Case 029/TO−226AA
Devices Available:
SCRs, TRIACs, PUTs
Current Range: to 0.8 A
Voltage Range: 30 to 600 V

TO−225AA
Case 077/TO−126
Devices Available:
SCRs, TRIACs
Current Range: to 4 A
Voltage Range: 200 to 600 V
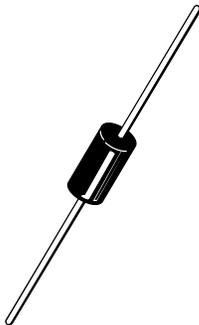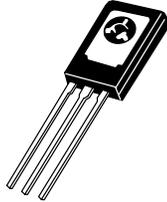
Case 267/Axial Lead
(Surmetic 50)
Devices Available:
SIDAC
Voltage Range: 120 to 240 V

TO−220AB
Case 221A
Devices Available:
SCRs, TRIACs
Current Range: to 55 A
Voltage Range: 50 to 800 V
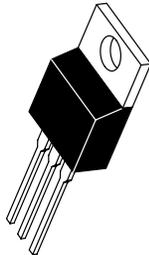
Figure 8.15. Examples of ON Semiconductor's Thyristor Packages

THYRISTOR CONSTRUCTION THROUGH A TIME TESTED DESIGN AND ADVANCED PROCESSING METHODS

A pioneer in discrete semiconductor components and one of the world's largest suppliers thereof, ON Semiconductor has pyramided continual process and material improvements into thyristor products whose inherent reliability meets the most critical requirements of the market.

These improvements are directed towards long−term reliability in the most strenuous applications and the most adverse environments.

DIE GLASSIVATION

All ON Semiconductor thyristor die are glass−sealed with an ON Semiconductor patented passivation process making the sensitive junctions impervious to moisture and impurity penetration. This imparts to low−cost plastic devices the same freedom from external contamination formerly associated only with hermetically sealed metal packages. Thus, metal encapsulation is required primarily for higher current devices that would normally exceed the power−dissipation capabilities of plastic packages — or for applications that specify the hermetic package.

VOID−FREE PLASTIC ENCAPSULATION

A fifth generation plastic package material, combined with improved copper piece−part designs, maximize package integrity during thermal stresses. The void−free encapsulation process imparts to the plastic package a mechanical reliability (ability to withstand shock and vibration) even beyond that of metal packaged devices.

IN−PROCESS CONTROLS AND INSPECTIONS

INCOMING INSPECTIONS

Apparently routine procedures, inspection of incoming parts and materials, are actually among the most critical segments of the quality and reliability assurance program. That's because small deviations from materials specifications can traverse the entire production cycle before being detected by outgoing Quality Control, and, if undetected, could affect long−term reliability. At ON Semiconductor, piece−part control involves the services of three separate laboratories . . . Radiology, Electron Optics and Product Analysis. All three are utilized to insure product integrity:

Raw Wafer Quality, in terms of defects, orientation, flatness and resistivity;
Physical Dimensions, to tightly specified tolerances;
Metal Hardness, to highly controlled limits;
Gaseous Purity and Doping Level;
Mold Compounds, for void−free plastic encapsulation.

IN−PROCESS INSPECTIONS

As illustrated in Figure 8.16, every major manufacturing step is followed by an appropriate in−process QA inspection. Quality control in wafer processing, assembly and final test impart to ON Semiconductor standard thyristors a reliability level that easily exceeds most industrial, consumer and military requirements . . . built−in quality assurance aimed at insuring failure−free shipments of ON Semiconductor products.

RELIABILITY AUDITS

Reliability audits are performed following assembly. Reliability audits are used to detect process shifts which can have an adverse effect on long–term reliability. Extreme stress testing on a real–time basis, for each product run, uncovers process abnormalities that may have escaped the stringent in–process controls. Typical tests include HTRB/FB (high–temperature reverse bias and forward bias) storage life and temperature cycling. When abnormalities are detected, steps are taken to correct the process.

OUTGOING QC

The most stringent in–process controls do not guarantee strict adherence to tight electrical specifications. ON Semiconductor's 100% electrical parametric test does — by eliminating all devices that do not conform to the specified characteristics. Additional parametric tests, on a sampling basis, provide data for continued improvement of product quality. And to help insure safe arrival after shipment, antistatic handling and packaging methods are employed to assure that the product quality that has been built in stays that way.

From rigid incoming inspection of piece parts and materials to stringent outgoing quality verification, assembly and process controls encompass an elaborate system of test and inspection stations that ensure step–by–step adherence to a prescribed procedure designed to yield a high standard of quality.
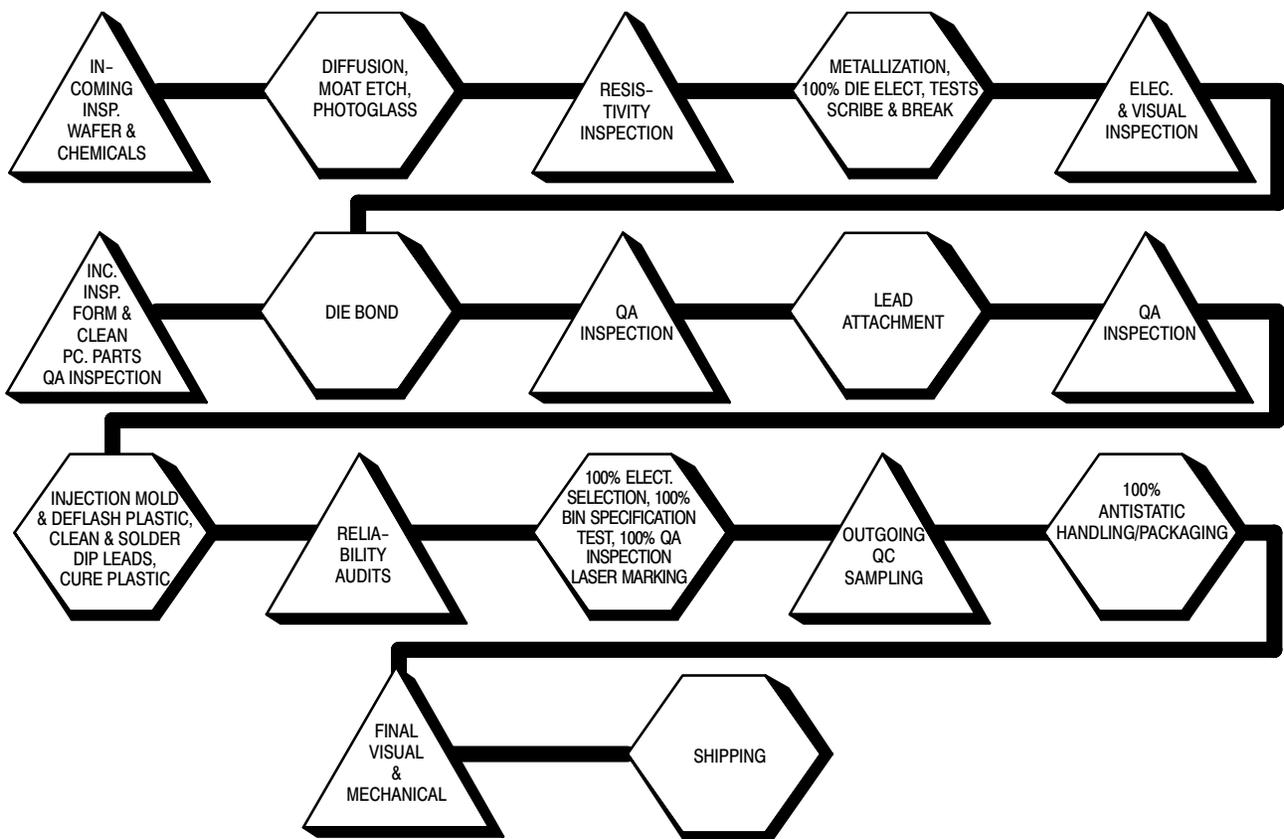

Figure 8.16. In–Process Quality Assurance Inspection Points for Thyristors

RELIABILITY TESTS

Only actual use of millions of devices, under a thousand different operating conditions, can conclusively establish the reliability of devices under the extremes of time, temperature, humidity, shock, vibration and the myriads of other adverse variables likely to be encountered in practice.

But thorough testing, in conjunction with rigorous statistical analysis, is the next–best thing. The series of torture tests described in this document instills a high confidence level regarding thyristor reliability. The tests are conducted at maximum device ratings and are designed to deliberately stress the devices in their most susceptible failure models. The severity of the tests compresses into a relatively short

test cycle the equivalent of the stresses encountered during years of operation under more normal conditions. The results not only indicate the degree of reliability in terms of anticipated failures; they trigger subsequent investigations into failure modes and failure mechanisms that serve as the basis of continual improvements. And they represent a clear−cut endorsement that, for ON Semiconductor thyristors, low−cost and high quality are compatible attributes.

BLOCKING LIFE TEST

This test is used as an indicator of long−term operating reliability and overall junction stability (quality). All semiconductor junctions exhibit some leakage current under reverse−bias conditions. Thyristors, in addition, exhibit leakage current under forward−bias conditions in the off state. As a normal property of semiconductors, this junction leakage current increases proportionally with temperature in a very predictable fashion.

Leakage current can also change as a function of time — particularly under high−temperature operation. Moreover, this undesirable "drift" can produce catastrophic failures when devices are operated at, or in excess of, rated temperature limits for prolonged periods.
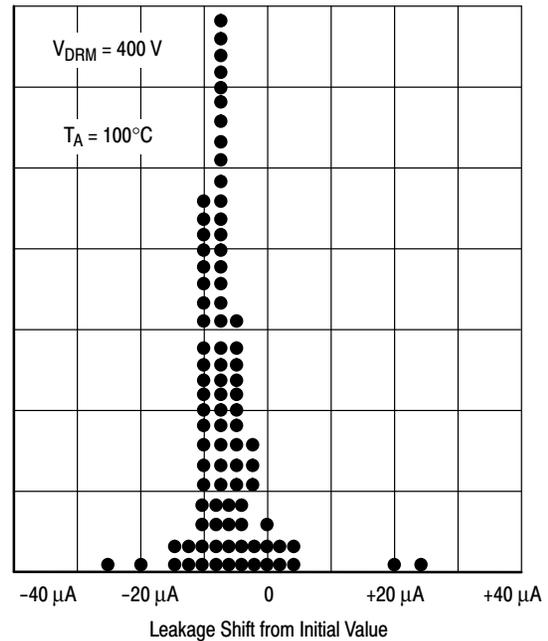
The blocking life test operates representative numbers of devices at rated (high) temperature and reverse−bias voltage limits to define device quality (as measured by leakage drifts) and reliability (as indicated by the number of catastrophic failures*). The results of these tests are shown in Table 8.3. Table 8.4 shows leakage−current drift after 1000 hours HTRB.

Table 8.4. Leakage−Current Drift after 1000 Hours HTRB

The favorable blocking−life−test drift results shown here are attributed to ON Semiconductor's unique "glassivated junction" process which imparts a high degree of stability to the devices.

HIGH TEMPERATURE STORAGE LIFE TEST

This test consists of placing devices in a high−temperature chamber. Devices are tested electrically prior to exposure to the high temperature, at various time intervals during the test, and at the completion of testing. Electrical readout results indicate the stability of the devices, their potential to withstand high temperatures, and the internal manufacturing integrity of the package. Readouts at the various intervals offer information as to the time period in which failures occur. Although devices are not exposed to such extreme high temperatures in the field, the purpose of this test is to accelerate any failure mechanisms that could occur during long periods at actual storage temperatures. Results of this test are shown in Table 8.5.

Table 8.3. Blocking Life Test
High Temperature Reverse Bias (HTRB)
and High Temperature Forward Bias (HTFB)

Case	Test Conditions T_A @ Rated Voltage	Sample Size	Duration (Hours)	Total Device Hours	Catastrophic Failures*
Case 029/TO−226AA (TO−92)	100°C	1000	1000	1,000,000	1
Case 077/TO−225AA (TO−126)	110°C	1000	1000	1,000,000	0
Case 221A/TO−220AB	100°C	1000	1000	1,000,000	0
Case 267/Axial Lead (Surmetic 50)	125°C	150	1000	150,000	0

* Failures are at maximum rated values. The severe nature of these tests is normally not seen under actual conditions.

Table 8.5. High Temperature Storage Life

Case	Test Conditions	Sample Size	Duration (Hours)	Total Device Hours	Catastrophic Failures*
Case 029/TO−226AA (TO−92)	T_A = 150°C	1000-2000	400	1,500,000	0
Case 077/TO−225AA (TO−126)	**	1000-2000	350	550,000	0
Case 221A/TO−220		1000	300	300,000	0
Case 267/Axial Lead (Surmetic 50)		1000	100	100,000	0

* Failures are at maximum rated values. The severe nature of these tests is normally not seen under actual conditions.
** Same for all.

STRESS TESTING — POWER CYCLING AND THERMAL SHOCK

POWER CYCLING TEST

How do the devices hold up when they are repeatedly cycled from the off state to the on state and back to the off state under conditions that force them to maximum rated junction temperature during each cycle? The Power Cycling Test was devised to provide the answers.

In this test, devices are subjected to intermittent operating file (IOL), on–state power until the junction temperature (T_J) has increased to 100°C. The devices are then turned off and T_J decreases to near ambient, at which time the cycle is repeated.

This test is important to determine the integrity of the chip and lead frame assembly since it repeatedly stresses the devices. It is unlikely that these worst–case conditions would be continuously encountered in actual use. Any reduction in T_J results in an exponential increase in operating longevity. Table 8.6 shows the results of IOL testing.

THERMAL SHOCK CONDITIONS BEYOND THE NORM

Excesses in temperature not only cause variations in electrical characteristics, they can raise havoc with the mechanical system. Under temperature extremes, contraction and expansion of the chip and package can cause physical dislocations of mechanical interfaces and induce catastrophic failure.

To evaluate the integrity of ON Semiconductor thyristors under the most adverse temperature conditions, they are subjected to thermal shock testing.

AIR–TO–AIR (TEMPERATURE CYCLING)

This thermal shock test is conducted to determine the ability of the devices to withstand exposure to extreme high and low temperature environments and to the shock of alternate exposures to the temperature extremes. Results of this test are shown in Table 8.6.

Table 8.6. Air–to–Air

Case	Test Conditions	Sample Size	Number of cycles	Total Device Cycles	Catastrophic Failures*
Case 029/TO–226AA (TO–92)	–40°C or –65°C	900	400	360,000	0
Case 077/TO–225AA (TO–126)	to +150°C	500	400	200,000	0
Case 221A/TO–220	Dwell—15 minutes at each extreme	400	400	160,000	0
Case 267/Axial Lead (Surmetic 50)	Immediate Transfer	100	400	40,000	0

* Failures are at maximum rated values. The severe nature of these tests is normally not seen under actual conditions.

ENVIRONMENTAL TESTING

MOISTURE TESTS

Humidity has been a traditional enemy of semiconductors, particularly plastic packaged devices. Most moisture–related degradations result, directly or indirectly, from penetration of moisture vapor through passivating materials, and from surface corrosion. At ON Semiconductor, this erstwhile problem has been effectively controlled through the use of a unique junction "glassivation" process and selection of package materials. The resistance to moisture–related failures is indicated by the tests described here.

BIASED HUMIDITY TEST

This test was devised to determine the resistance of component parts and constituent materials to the combined deteriorative effects of prolonged operation in a high–temperature/high–humidity environment. H^{3}TRB test results are shown in Table 8.7.

Table 8.7. Biased Humidity Test
High Humidity, High Temperature, Reverse Bias (H^{3}TRB)

Case	Test Conditions	Sample Size	Duration Hours	Total Device Cycles	Catastrophic Failures*
Case 029/TO–226AA (TO–92)	Relative Humidity 85% T_A = 85°C	400	500–1000	300,000	0
Case 077/TO–225AA	Reverse Voltage–Rated or 200 V Maximum	200	500–1000	150,000	0
Case 221A/TO–220		100	500–1000	75,000	0
Case 267/Axial Lead (Surmetic 50)		30	1000	30,000	0

* Failures are at maximum rated values. The severe nature of these tests is normally not seen under actual conditions.

SECTION 9
APPENDICES

APPENDIX I

USING THE TWO TRANSISTOR ANALYSIS

DEFINITIONS:

$I_C \equiv$ Collector current
$I_B \equiv$ Base current
$I_{CS} \equiv$ Collector leakage current (saturation component)
$I_A \equiv$ Anode current
$I_K \equiv$ Cathode current
$\alpha \equiv$ Current amplification factor
$I_G \equiv$ Gate current

The subscript "i" indicates the appropriate transistor.

FOR TRANSISTOR #1:

$I_{C1} = \alpha_1 I_A + I_{CSI}$

and

$I_{B1} = I_A - I_{C1}$

Combining these equations,

$I_{B1} = (1 - \alpha_1) I_A - I_{CS1}$ (1)

LIKEWISE, FOR TRANSISTOR #2

$I_{C2} = \alpha_2 I_K + I_{CS2}$ (2)

$I_{B1} = I_{C2}$

and by combining Equations (1) and (2) and substituting $I_K = I_A + I_G$, it is found that

$I_A = \dfrac{\alpha_2 I_G + I_{CS1} + I_{CS2}}{1 - \alpha_1 - \alpha_2}$ (3)

Equation (3) relates I_A to I_G, and note that as $\alpha_1 + \alpha_2 = 1$, I_A goes to infinity. I_A can be put in terms of I_K and α's as follows:

$I_{B1} = I_{C2}$

Combining equations (1) and (2):

$I_A = \dfrac{I_{CS1} + I_{CS2}}{1 - \alpha_1 - (\frac{I_K}{I_A}) \alpha_2}$

$I_A \longrightarrow \infty$ if denominator approaches zero, i.e., if

$\dfrac{I_K}{I_A} = \dfrac{1 - \alpha_1}{\alpha_2}$

Note that just prior to turn–on there is a majority carrier build–up in the P_2 "base." If the gate bias is small there will actually be hole current flowing out from P_2 into the gate circuit so that I_G is negative, $I_K = I_A + I_G$ is less than I_A so: (see Figure 3.2 for the directions of current components)

$\dfrac{I_K}{I_A} < 1$ which corresponds to $\alpha_1 + \alpha_2 > 1$
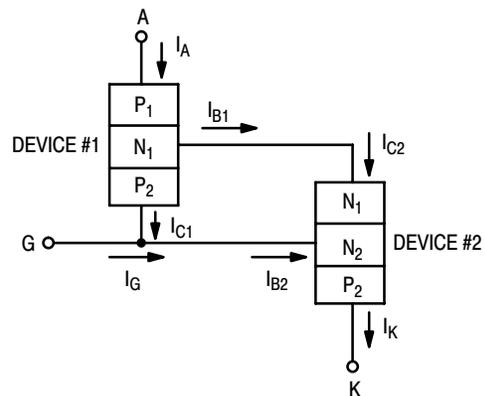
Figure 9.1. Schematic Diagram of the Two Transistor Model of a Thyristor

APPENDIX II

CHARGE AND PULSE WIDTH

In the region of large pulse widths using current triggering, where transit time effects are not a factor, we can consider the input gate charge for triggering, Q_{in}, as consisting of three components:

1. Triggering charge Q_{tr}, assumed to be constant.
2. Charge lost in recombination, Q_r, during current regeneration prior to turn−on.
3. Charge drained, Q_{dr}, which is by−passed through the built−in gate cathode shunt resistance (the presence of this shunting resistance is required to increase the dv/dt capability of the device).

Mathematically, we have

$$Q_{in} = Q_{tr} + Q_{dr} + Q_r = I_G\tau \qquad (1)$$

Q_r is assumed to be proportional to Q_{in}; to be exact,

$$Q_r = Q_{in} (1 - \exp^{-\tau/\tau_1}) \qquad (2)$$

where I_G = gate current,
 τ = pulse width of gate current,
 τ_1 = effective life time of minority carriers in the bases

The voltage across the gate to cathode P−N junction during forward bias is given by V_{GK} (usually 0.6 V for silicon).* The gate shunt resistance is R_s (for the MCR729, typically 100 ohms), so the drained charge can be expressed by

$$Q_{dr} = \frac{V_{GC}}{R_s} \tau \qquad (3)$$

Combining equations (1), (2), and (3), we get

$$Q_{in} = I_G\tau = (Q_{tr} + \frac{V_{GC}}{R_s} \tau) \exp. \tau/\tau_1 \qquad (4)$$

Note that at region A and C of Figure 3.3(c) Q_{in} has an increasing trend with pulse width as qualitatively described by Equation (4).

Assume life time at the temperature range of operation increases as some power of temperature

$$\tau_1 = KT^m \qquad (5)$$

where K and m are positive real numbers. Combining Equations (4) and (5), we can get the slope of Q_{in} with respect to temperature to be

$$slope = \frac{dQ_{in}}{dT} = -m(Q_{tr} + \frac{V_{GC}}{R_s}\tau) \frac{\tau}{\tau_1} \frac{\exp.\tau/\tau_1}{T} \qquad (6)$$

In reality, Q_{tr} is not independent of temperature, in which case the Equation (6) must be modified by adding an additional term to become:

$$slope = -m(Q_{tr} + \frac{V_{GC}}{R_s}\tau) \frac{\tau}{\tau_1} \frac{\exp.\tau/\tau_1}{T} + \frac{dQ_{tr}}{dT} \exp^{\tau/\tau_1} \quad (7)$$

Physically, not only does Q_{tr} decrease with temperature so that dQ_{tr}/dT is a negative number, but also $|dQ_{tr}/dTI$ decreased with temperature as does $|d\alpha/dTI$ in the temperature range of interest.

Equation (6) [or (7)] indicates two things:

1. The rate of change of input trigger charge decreases as temperature (life time) increases.
2. The larger the pulse width of gate trigger current, the faster the rate of change of Q_{in} with respect to change in temperature. Figure 3.11 shows these trends.

*V_{GC} is not independent of I_G. For example, for the MCR729 the saturation V_{GC} is typically 1 V, but at lower I_G's the V_{GC} is also smaller, e.g. for I_G = 5 mA, V_{GC} is typically 0.3 V.

APPENDIX III

TTL SOA TEST CIRCUIT

   Using the illustrated test circuit, the two TTL packages (quad, 2–input NAND gates) to be tested were powered by the simple, series regulator that is periodically shorted by the clamp transistor, Q2, at 10% duty cycle rate. By varying the input to the regulator V1 and the clamp pulse width, various power levels can be supplied to the TTL load. Thus, as an example, V_{CC} could be at 5 V for 90 ms and 10 V for 10 ms, simulating a transient on the bus or a possibly shorted power supply pass transistor for that duration. These energy levels are progressively increased until the gate (or gates) fail, as detected by the status of the output LEDs, the voltage and current waveforms and the device case temperature.
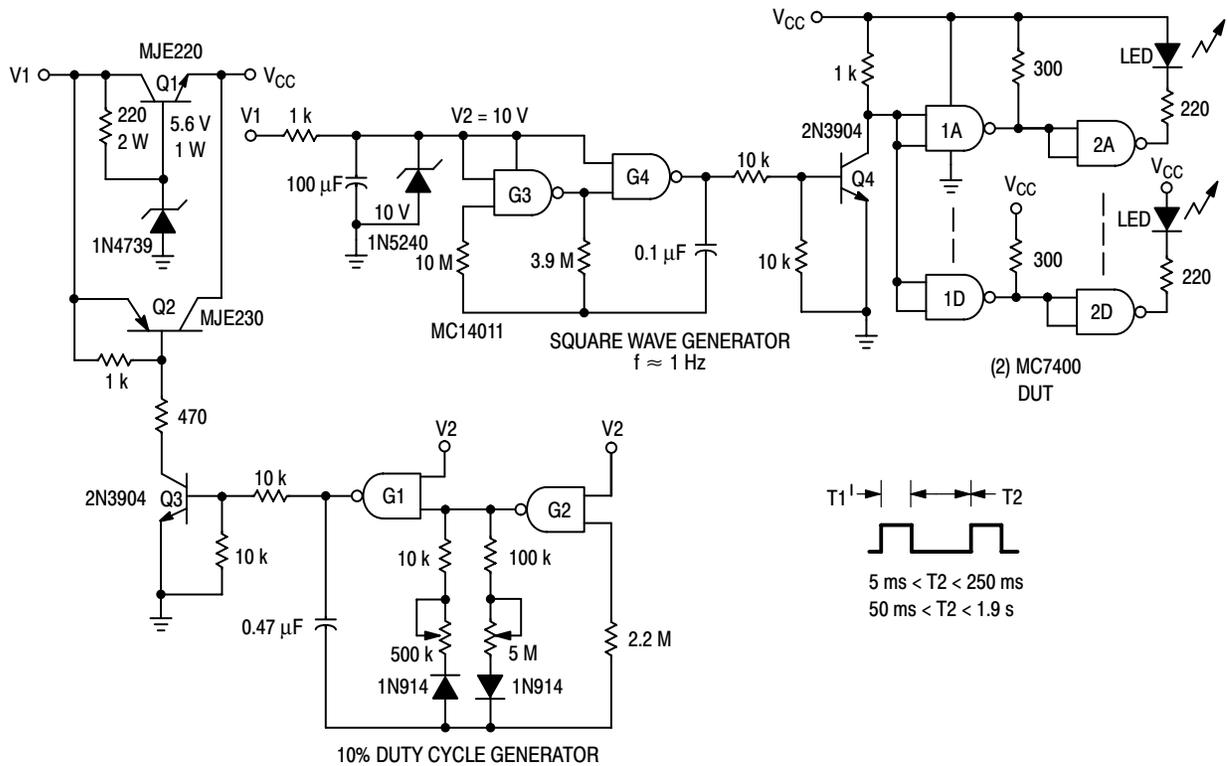
Figure 9.2. TTL SOA Test Circuit

APPENDIX IV

SCR CROWBAR LIFE TESTING

This crowbar life test fixture can simultaneously test ten SCRs under various crowbar energy and gate drive conditions and works as follows.

The CMOS Astable M.V. (Gates 1 and 2) generate an asymmetric Gate 2 output of about ten seconds high, one second low. This pulse is amplified by Darlington Q22 to turn on the capacitor charging transistors Q1–Q10 for the ten seconds. The capacitors for crowbarring are thus charged in about four seconds to whatever power supply voltage to which V_{CC1} is set. The charging transistors are then turned off for one second and the SCRs are fired by an approximately 100 μs delayed trigger derived from Gates 3 and 4. The R–C network on Gate 3 input integrates the complementary pulse from Gate 1, resulting in the delay, thus insuring non−coincident firing of the test circuit. The shaped pulse out of Gate 4 is differentiated and the positive−going pulse is amplified by Q21 and the following ten SCR gate drivers (Q11–Q20) to form the approximate 2 ms wide, 1 μs rise time, SCR gate triggers, I_{GT}. I_{GT} is set by the collector resistors of the respective gate drivers and the supply voltage, V_{CC2}; thus, for $I_{GT} \approx 100$ mA, $V_{CC2} \approx 30$ V, etc.

The LEDs across the storage capacitors show the state of the voltage on the capacitors and help determine whether the circuit is functioning properly. The timing sequence would be an off LED for the one−second capacitor dump period followed by an increasingly brighter LED during the capacitor charge time. Monitoring the current of V_{CC1} will also indicate proper operation.

The fixture's maximum energy limits are set by the working voltage of the capacitors and breakdown voltage of the transistors. For this illustration, the 60 V, 8400 μF capacitors (ESR ≈ 20 mΩ) produced a peak current of about 2500 A lasting for about 0.5 ms when V_{CC1} equals 60 V. Other energy values (lower i_{pk}, greater t_w) can be obtained by placing a current limiting resistor between the positive side of the capacitor and the crowbar SCR anode.
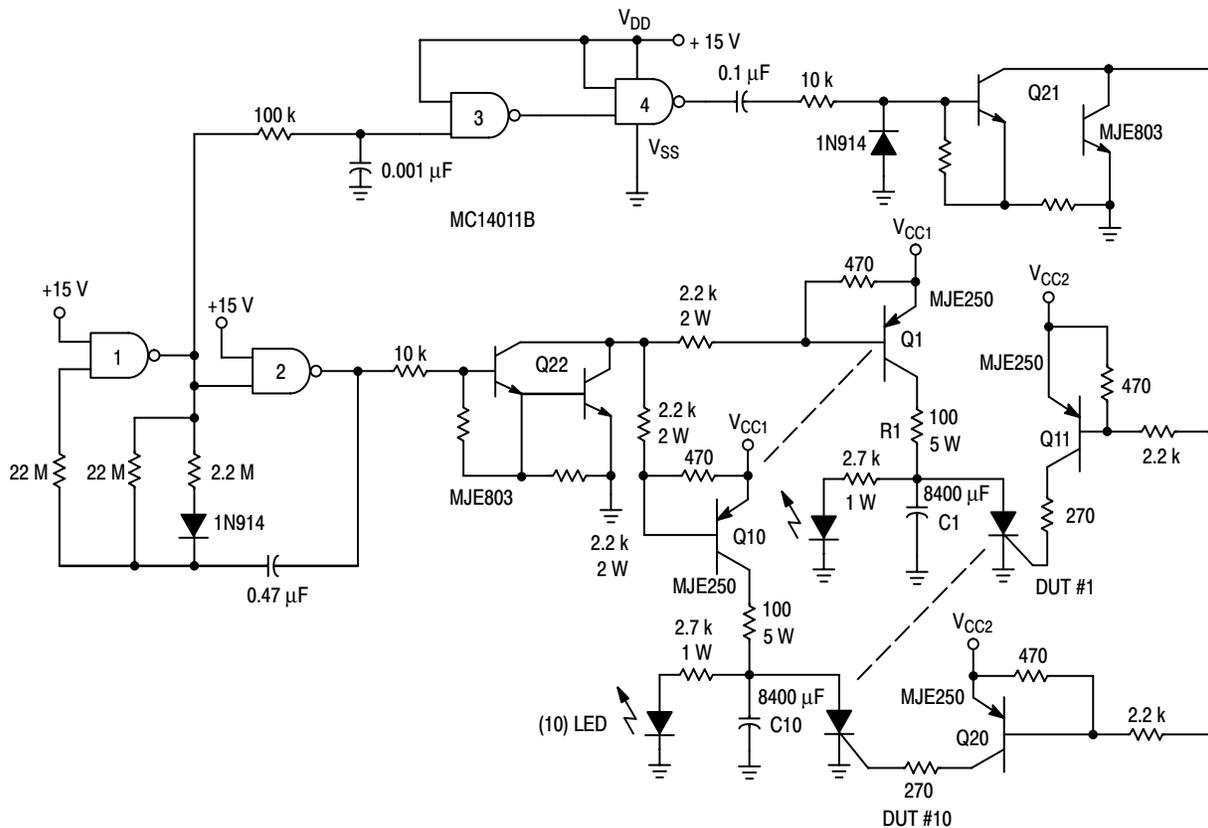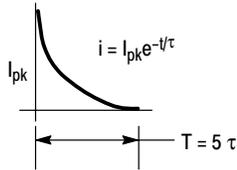

Figure 9.3. Schematic for SCR Crowbar Life Test

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APPENDIX V

DERIVATION OF THE RMS CURRENT OF AN EXPONENTIALLY DECAYING CURRENT WAVEFORM

$i = I_{pk}e^{-t/\tau}$, I_{pk}, $T = 5\tau$

$$I_{rms} = \sqrt{\frac{1}{T}\int_0^T i^2(t)dt}$$

$$= \left[\frac{1}{T}\int_0^T (I_{pk}e^{-t/\tau})^2 dt\right]^{1/2}$$

$$= \left[\frac{I_{pk}^2}{T} \frac{e^{-2t/\tau}}{(-2/\tau)}\bigg|_0^T\right]^{1/2}$$

$$= \left[\frac{I_{pk}^2}{T} \left(\frac{-\tau}{2}\right)(e^{-2T/\tau} - e^0)\right]^{1/2}$$

where $T = 5\tau$,

$$= \left[-\frac{I_{pk}^2}{10}(e^{-10} - 1)\right]^{1/2}$$

$$I_{rms} = \frac{I_{pk}}{\sqrt{10}} = 0.316\, I_{pk}$$

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APPENDIX VI

DERIVATION OF I^2t FOR VARIOUS TIMES

Thermal Equation $\quad\quad \Delta t = Z(\theta)P_D$

where $\quad\quad\quad\quad\quad Z(\theta) = r(t)R_{\theta JC}$

and $\quad\quad\quad\quad\quad\quad r(t) = K\sqrt{t}$

Therefore, for the same Δt,

$$\Delta t = K\sqrt{t_1}\, R_{\theta JC}P_{D_1} = K\sqrt{t_2}\, R_{\theta JC}\, P_{D_2},$$

$$\frac{P_{D_1}}{P_{D_2}} = \sqrt{\frac{t_2}{t_1}} = \frac{I_1^2 R}{I_2^2 R},$$

$$\frac{I_1^2}{I_2^2} = \sqrt{\frac{t_2}{t_1}}$$

Multiplying both sides by (t_1/t_2),

$$\frac{I_1^2 t_1}{I_2^2 t_2} = \left(\frac{t_2}{t_1}\right)^{1/2}\frac{t_1}{t_2} = \left(\frac{t_1}{t_2}\right)^{1/2},$$

$$I_1^2 t_1 = I_2^2 t_2 \sqrt{\frac{t_1}{t_2}}$$

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APPENDIX VII

THERMAL RESISTANCE CONCEPTS

The basic equation for heat transfer under steady−state conditions is generally written as:

$$q = hA\Delta T \qquad (1)$$

where   q = rate of heat transfer or power dissipation (P_D),
   h = heat transfer coefficient,
   A = area involved in heat transfer,
   ΔT = temperature difference between regions of heat transfer.

However, electrical engineers generally find it easier to work in terms of thermal resistance, defined as the ratio of temperature to power. From Equation (1), thermal resistance, R_θ, is

$$R_\theta = \Delta T/q = 1/hA \qquad (2)$$

The coefficient (h) depends upon the heat transfer mechanism used and various factors involved in that particular mechanism.

An analogy between Equation (2) and Ohm's Law is often made to form models of heat flow. Note that ΔT could be thought of as a voltage; thermal resistance corresponds to electrical resistance (R); and, power (q) is analogous to current (l). This gives rise to a basic thermal resistance model for a semiconductor (indicated by Figure 9.4).

The equivalent electrical circuit may be analyzed by using Kirchoff's Law and the following equation results:

$$T_J = P_D(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A \qquad (3)$$

where T_J = junction temperature,
        P_D = power dissipation,
        $R_{\theta JC}$ = semiconductor thermal resistance (junction to case),
        $R_{\theta CS}$ = interface thermal resistance (case to heat sink),
        $R_{\theta SA}$ = heat sink thermal resistance (heat sink to ambient),
        T_A = ambient temperature.

The thermal resistance junction to ambient is the sum of the individual components. Each component must be minimized if the lowest junction temperature is to result. The value for the interface thermal resistance, $R_{\theta CS}$, is affected by the mounting procedure and may be significant compared to the other thermal−resistance terms.

The thermal resistance of the heat sink is not constant; it decreases as ambient temperature increases and is affected by orientation of the sink. The thermal resistance of the semiconductor is also variable; it is a function of biasing and temperature. In some applications such as in RF power amplifiers and short−pulse applications, the concept may be invalid because of localized heating in the semiconductor chip.
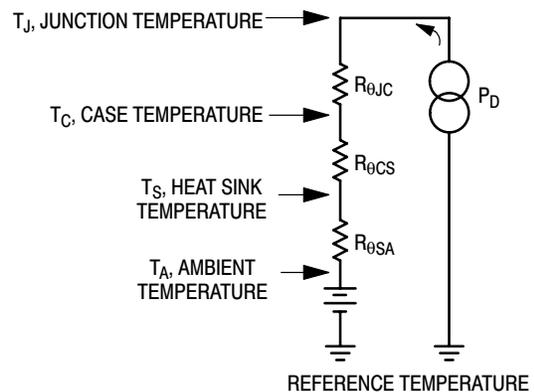
Figure 9.4. Basic Thermal Resistance Model Showing Thermal to Electrical Analogy for a Semiconductor

DERIVATION OF RFI DESIGN EQUATIONS

The relationship of flux to voltage and time is $E = N \dfrac{d\phi}{dt}$ or $E = NA_c \dfrac{dB}{dt}$ since $\phi = BA_c$ and A_c is a constant. Rearranging this equation and integrating we get:

$$\int E \, dt = NA_c (B_2 - B_1) = NA_c \, \Delta B \qquad (1)$$

which says that the volt–second integral required determines the size of the core. In an L–R circuit such as we have with a thyristor control circuit, the volt–second characteristic is the area under an exponential decay. A conservative estimate of the area under the curve may be obtained by considering a triangle whose height is the peak line voltage and the base is the allowable switching time. The area is then 1/2 bh or $\dfrac{E_p t_r}{2}$.

Substituting in Equation (1):

$$\frac{E_p t_r}{2} = N A_c \, \Delta B \qquad (2)$$

where:
 E_p is the peak line voltage
 t_r is the allowable current rise time
 N is the number of turns on the coil
 A_c is the usable core area in cm^2
 ΔB is the maximum usable flux density of the core
  material in W/m^2

Rewriting Equation (2) to change ΔB from W/m^2 to gauss, substituting $\sqrt{2}\, E_{rms}$ for E_p and solving for N, we get:

$$N = \frac{\sqrt{2}\, E_{rms}\, t_r}{2 A_c \, \Delta B} \times 10^8 = \frac{0.707\, E_{rms}\, t_r \times 10^8}{B_{MAX}\, A_c}$$

A_c in this equation is in cm^2. To change to in^2, multiply A_c by 6.452. Then:

$$N = \frac{10.93\, E_{rms}\, t_r \times 10^6}{B_{MAX} \times A_c} \qquad (3)$$

where:
 N is total turns
 E_{rms} is line voltage
 t_r is allowable current rise time in seconds
 B_{MAX} is maximum usable flux density of core material
 A_c is usable core area in square inches
 Window area necessary is:

$$A_w = N\, A_{wire} \times 3 \qquad (4)$$

The factor of 3 is an approximation which allows for insulation and winding space not occupied by wire. Substituting equation (3) in (4):

$$A_w = \frac{10.93\, E_{rms}\, t_r \times 10^6}{B_{MAX}\, A_c}\, A_{wire} \times 3$$

(The factor 10.93 may be rounded to 11 since two significant digits are all that are necessary.)

The factor $A_c A_w$ can easily be found for most cores and is an easy method for selecting a core.

$$A_c A_w = \frac{33\, E_{rms}\, t_r A_{wire} \times 10^6}{B_{MAX}}$$

In this equation, the core area is in in^2. To work with circular mils, multiply by 0.78×10^{-6} so that:

$$A_c A_w = \frac{26\, E_{rms}\, t_r A_{wire}}{B_{MAX}}$$

where A_{wire} is the wire area in circular mils.
 Inductance of an iron core inductor is

$$L = \frac{3.19\, N^2\, A_c\, 10^{-8}}{lg + \frac{1c}{\mu}}$$

Rearranging terms,

$$lg = \frac{3.19\, N^2\, A_c\, 10^{-8}}{L} - \frac{1c}{\mu}$$

APPENDIX IX

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