Using the PSoC Microcontroller External Crystal Oscillator

AN2027

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Application Note Abstract

The External Crystal Oscillator in the PSoC® microcontroller has specific requirements for correct operation in different configurations. This application note details these requirements.

Introduction

The PSoC microcontroller's External Crystal Oscillator (ECO) is used as a reference for time keeping or other low speed (<32 kHz) operations. It also acts as the reference for the phase locked loop (PLL) mode of the Internal Main Oscillator (IMO). The PLL fixes the incoming 32 kHz signal to 24 MHz on its output. This is used for operations that require an accurate high speed clock such as dual tone multifrequency signal generation and serial communications. Optimal performance from the ECO for each of these functions requires different external components and control register settings.

External Crystal Oscillator Basics

The PSoC microcontroller's 32 kHz clock uses the low accuracy Internal Low speed Oscillator (ILO) or the higher accuracy ECO for reference. The 32 kHz Select bit of Oscillator Control Register 0 (OSC_CR0) determines which source is used. The easiest way to set this bit is to set the *32K_Select* parameter in the Global Resources table of PSoC Designer™ to 'External' (highlighted in Figure 1).

Figure 1. *32K_Select* Setting for ECO Operation

Global Resources	
CPU_Clock	12_MHz
32K_Select	External
PLL_Mode	Disable
Sleep_Timer	512_Hz
24V1= 24MHz/N	1
24V2= 24V1/N	1
Analog Power	SC On/Ref Low
Ref Mux	(Vcc/2)+/-BandGap

The ECO drive circuitry must be connected to a 32,768 Hz watch crystal through the XtalIn and XtalOut pins of the PSoC MCU.

Note 32,768 Hz is used because it allows integer division to a 1 Hz clock signal, as 2^15 = 32,768.

The XtalIn and XtalOut pins must have their drive modes set to High Z (highlighted in Figure 2) for the ECO to work properly. If the pins' drive modes are not set to High Z, the drive circuitry will free-run at an incorrect frequency.

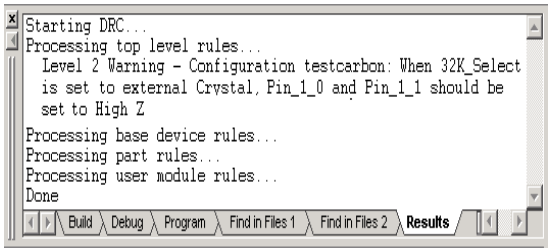
Figure 2. XtalIn and XtalOut Pin Drive Settings for ECO Operation

Name	Port	Select	Drive	Interrupt
Port_0_5	P0[5]	StdCPU	Pull Down	DisableInt
Port_0_6	P0[6]	StdCPU	Pull Down	DisableInt
Port_0_7	P0[7]	StdCPU	Pull Down	DisableInt
Port_1_0	P1[0]	XtalOut	High Z	DisableInt
Port_1_1	P1[1]	XtalIn	High Z	DisableInt
Port_1_2	P1[2]	StdCPU	Pull Down	DisableInt
Port_1_3	P1[3]	StdCPU	Pull Down	DisableInt
Port_1_4	P1[4]	StdCPU	Pull Down	DisableInt
Port_1_5	P1[5]	StdCPU	Pull Down	DisableInt
Port_1_6	P1[6]	StdCPU	Pull Down	DisableInt
Port_1_7	P1[7]	StdCPU	Pull Down	DisableInt

The pins are automatically set to High Z if the "Select" parameters are set to XtalOut and XtalIn in the Pin Description Table. The correct configuration of P1[0] and P1[1] is confirmed by running the Design Rule Checker in PSoC Designer (Tools > Design Rule Checker); the results are viewed in the output window.

Figure 3 shows the output of the DRC when P1[0] and P1[1] are not correctly configured.

Figure 3. Design Rule Checker Output



External Crystal Oscillator Operation

The ECO operates as a low power oscillator. To accomplish this, it is designed as low amplitude, high impedance analog circuit. It must be treated as such during component placement and circuit layout. Layout is critical to performance. Also note that the presence of contaminants on the PCB impacts the performance of the oscillator.

The crystal and the feedback capacitors must be placed close to the pins of the microcontroller. They must be placed over a common-ground plane. High speed digital signals (signals with low rise and fall times) should not be routed close to the ECO circuit. Also, digital signals should not be routed near the ECO external components. When possible, the pins immediately adjacent to the ECO pins must be left unconnected, or they must be used for lower speed signals. Low speed signals may be driven with the “strong slow” setting.

Because the ECO circuit is high impedance and low amplitude, a standard oscilloscope probe cannot be used to view the signal. The load of a standard oscilloscope probe distorts the waveform and impacts its performance. One option is to use a unity gain op-amp to buffer the signal so that it is viewed with an oscilloscope. Figure 4 shows the ECO waveform at the XtalIn pin (P1[1]) captured with the aid of the circuit shown in Figure 5.

Figure 4. ECO Waveform

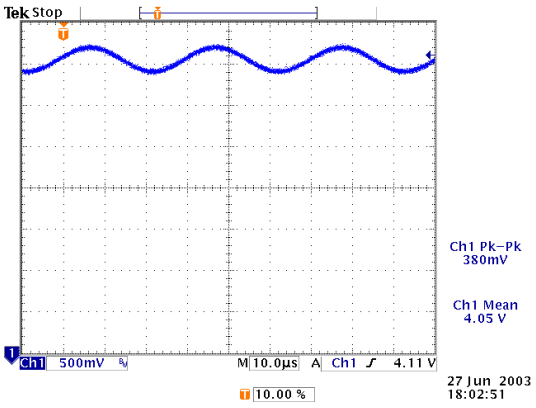
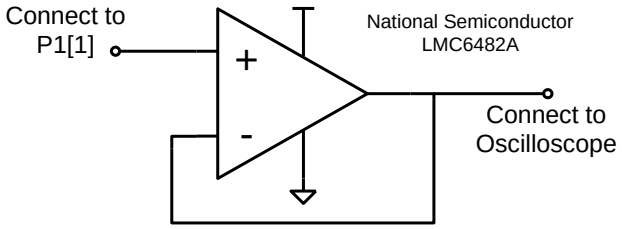


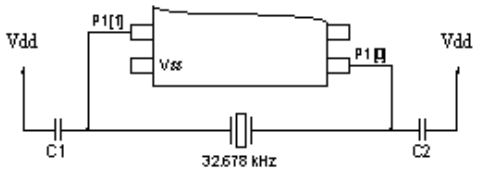
Figure 5. Unity Gain Buffer



The analog signal has a DC offset of approximately 4V and peak-to-peak amplitude of approximately 400 mV.

Figure 6 shows the external circuit that is used for the ECO. Note that the feedback capacitors are connected to Vdd. This is the optimal configuration because the ECO driver is referenced to Vdd. If the capacitors are incorrectly connected to Vss, the ECO operates at the correct frequency, but is slightly more susceptible to power supply noise.

Figure 6. ECO Electrical Connections



For standard ECO operation (when not used as a reference for the IMO PLL), the configurations described in the Device Family Data Sheets should be used.

- 32.768 kHz, 12.5 pF, 1µW watch crystal
- Temperature stable(NPO) ceramic capacitors
- $C_1 = C_2 = 25\ pF - C_P - C_B$

C_1 and C_2 are the ECO feedback capacitors shown in Figure 6, C_P is the package capacitance and C_B is the board capacitance.

The package capacitances for the various PSoC MCU packages are found in the Clocking section of the Device Family Data Sheets. The board capacitance depends on PCB geometry. For example, a layout with 0.20” long, 0.010” wide traces over a ground plane on a 4-layer 0.062” thick PCB, has a board parasitic capacitance of 0.3 pF on each pin.

Table 1 shows standard capacitor values that are used with the various PSoC microcontroller packages, assuming 0.3 pF board capacitance as in the previous example.

Table 1. Example ECO Capacitor Values for Balanced Feedback Configuration

Package	Typical C_P	C_1	C_2
8 Pin DIP	0.9 pF	22 pF	22 pF
20 Pin DIP	2.0 pF	22 pF	22 pF
20 Pin SOIC	1.0 pF	22 pF	22 pF
20 Pin SSOP	0.5 pF	22 pF	22 pF
28 Pin DIP	2.0 pF	22 pF	22 pF
28 Pin SOIC	1.0 pF	22 pF	22 pF
28 Pin SSOP	0.5 pF	22 pF	22 pF
44 Pin TQFP	0.5 pF	22 pF	22 pF
48 Pin DIP	5.0 pF	20 pF	20 pF
48 Pin SSOP	0.6 pF	22 pF	22 pF

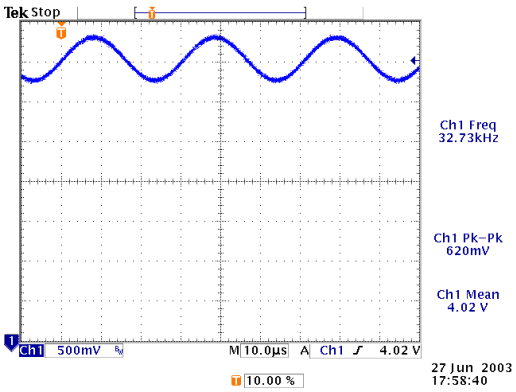
ECO and PLL Mode

The IMO is configured in PLL to the ECO. This results in an IMO with a more accurate frequency and less voltage and temperature drift than what is accomplished with the IMO alone. The IMO operates with 2.5% accuracy over the full temperature and voltage range without using the PLL lock mode.

When configuring the IMO in PLL mode, a number of changes must be made. The design must use an unbalanced feedback capacitor configuration and include a local bypass capacitor. Also, an increased drive current must be used. These modifications are described in the following sections.

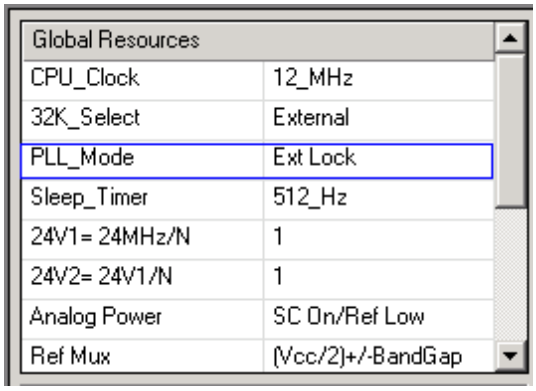
The use of unbalanced feedback capacitors boosts the amplitude of the signal at XtalIn (P1[1]). See Figure 7 for a waveform at P1[1], captured with the aid of the circuit shown in Figure 5. The amplitude at XtalIn is now approximately 600 mV_{p-p}.

Figure 7. ECO Waveform with Unbalanced Capacitors



The PLL Mode bit of the *OSC_CR0* register enables the PLL mode of the IMO. The easiest way to set this bit is to set the *PLL_Mode* parameter to '*Ext Lock'* in the Global Resources window of PSoC Designer (highlighted in Figure 8).

Figure 8. *PLL_Mode* Setting for IMO Operation



In general, a PLL requires a low jitter reference to remain stable. Because the PSoC microcontroller's ECO uses a low amplitude signal, the presence of noise causes the apparent position of the clock edges to jitter from cycle to cycle. The base frequency of the ECO remains accurate but the jitter can cause the IMO to be unstable. The purpose of the unbalanced feedback capacitors is to reduce the jitter caused by noise on the 32 kHz waveform.

When using the PLL mode of the IMO, PCB layout is the most critical factor in minimizing jitter on the ECO. By carefully designing the PCB, the amount of noise present in the ECO circuit is minimized. But there are other required modifications that increase the stability of the ECO. These include using unbalanced feedback capacitors, providing a local Vdd bypass, and increasing the ECO drive current. A combination of all three modifications is required to ensure proper PLL operation.

Use of Unbalanced Feedback Capacitors

By using an unbalanced pair of feedback capacitors, the amplitude of the input signal can be increased, reducing the ECO's noise susceptibility. In this case, the series capacitance of the feedback capacitors still needs to be 12.5 pF. An unbalanced pair of capacitors causes an increase in the operating current and does not improve the performance of the ECO itself. So this change is not recommended for standard ECO operation.

The capacitance on each pin is comprised of package capacitance, in parallel with the board parasitic capacitance, in parallel with the external capacitor (see Equations 1 and 2).

XtalIn (Port 1, Pin 1) Capacitance

$$C_{P1[1]} = C_1 + C_B + C_P \quad \text{Equation 1}$$

XtalOut (Port 1, Pin 0) Capacitance

$$C_{P1[0]} = C_2 + C_B + C_P \quad \text{Equation 2}$$

For this configuration, the total capacitance on the XtalOut pin (Port 1, Pin 0) should be near 100 pF. Equation 3 shows the total capacitance at the XtalOut pin ($C_{P1[0]}$) if a 100 pF capacitor is used.

XtalOut (Port 1, Pin 0) Capacitance

$$C_{P1[0]} = 100pF + C_{B0} + C_P \quad \text{Equation 3}$$

Where C_P is the package capacitance and C_{B0} is the board parasitic capacitance on XtalOut.

The feedback capacitor at the XtalIn pin is chosen so that the series capacitance at the crystal pins totals 12.5 pF. Equation 4 shows the calculation for the ideal value of C_1 (the capacitor on P1[1]: XtalIn).

XtalIn (Port 1, Pin 1) Capacitance

$$C_1 = \frac{(C_2 + C_P + C_{B0}) * 12.5pF}{(C_2 + C_P + C_{B0}) - 12.5pF} - C_P - C_{B1} \quad \text{Equation 4}$$

Where C_P is the package capacitance and C_{B1} is the board parasitic capacitance on XtalIn.

Table 2 lists typical package capacitances and standard capacitor values for C_1 and C_2 closest to the calculated ideal values for various packages. Board parasitic capacitance is assumed to be 0.3 pF for these calculations.

Table 2. ECO Capacitor Values for Unbalanced Feedback

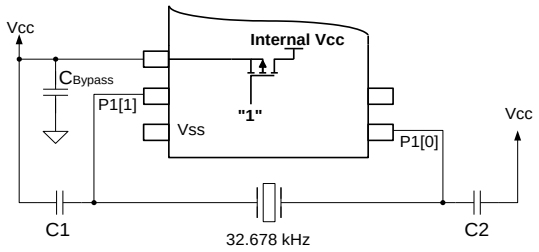
Package	Typical C_P	C_1	C_2
8 Pin DIP	0.9 pF	12 pF	100 pF
20 Pin DIP	2.0 pF	12 pF	100 pF
20 Pin SOIC	1.0 pF	12 pF	100 pF
20 Pin SSOP	0.5 pF	12 pF	100 pF
28 Pin DIP	2.0 pF	12 pF	100 pF
28 Pin SOIC	1.0 pF	12 pF	100 pF
28 Pin SSOP	0.5 pF	12 pF	100 pF
44 Pin TQFP	0.5 pF	12 pF	100 pF
48 Pin DIP	5.0 pF	9 pF	100 pF
48 Pin SSOP	0.6 pF	12 pF	100 pF

Note An error of 1 pF in C_1 or C_2 results in approximately three parts per million of additional error in the output frequency.

Provide a Local Bypass when using PLL Lock Mode.

When using the PLL configuration of the IMO, additional filtering of the Vcc power is required. For this purpose, a local Vcc bypass capacitor is added near the XtalIn pin (Port 1, Pin 3). To do this, configure the pin's drive mode to Resistive Pull Down and write a '1' to the Data Register (*PRT1DR*). Connect the pin to Vcc and connect a 0.1 µF capacitor between the pin and Vss (as shown in Figure 9). This connects the internal power bus to Vcc through the pin pull up FET; providing a local low impedance connection to Vcc.

Figure 9. PLL Mode Electrical Configuration



A drive mode of Pull Down is recommended so that if a '0' is accidentally written to P1[3] it results in a 5.6 kΩ resistance between Vdd and Vss instead of a short between Vdd and Vss.

Increase ECO Drive Current

To increase the drive current of the ECO circuit, write *0x0F* to the ECO Trim register (*ECO_TR*, Bank 1, *0x0F*). This is done automatically by *boot.asm* when the *PLL_Mode* parameter is set to '*Ext Lock'*.

Startup Requirements

Both the ECO and the IMO experience periods of instability when they are first started. Therefore, the ECO output is not used as a source for the internal 32K clock or as a reference for the PLL mode of the IMO until it has had time to stabilize. The IMO experiences a frequency overshoot when the PLL is first enabled. As a consequence, the CPU clock speed must be lowered when the IMO is initially switched to PLL mode to prevent the CPU clock from exceeding its operational limit.

These circumstances require the ECO and the IMO PLL mode to follow a specific startup sequence. *boot.asm* meets this requirement if the appropriate settings (*32KSelect = External* and *PLL_Mode = Ext Lock*) are selected in the Global Resources grid in the Device Editor of PSoC Designer.

Starting the ECO

When the ECO is first enabled, its output is not connected to the 32K clock tree within the PSoC microcontroller. Instead, the 32K clock continues to be driven by the ILO until the sleep timer reaches terminal count. With this mechanism, the sleep timer is used to delay connecting to the ECO until its output has stabilized.

The steps listed below are followed by *boot.asm* when starting the ECO:

1. The sleep timer is set to one second and cleared. The sleep timer interrupt need not be enabled.
2. ECO is enabled; set the 32K Select bit of *OSC_CR0* to '1'.
3. When the sleep timer reaches terminal count (one second later), the ECO is automatically selected as the source for the 32K clock tree and can now be used as a clock source for event timing.

The *boot.asm* holds off entry to main() until all the clocks are stable. This means that calling main is delayed by about one second when using the ECO.

Starting the IMO PLL Mode

The IMO cannot be phase locked to the ECO until the ECO is stable—this takes approximately one second. Also, the CPU clock frequency cannot exceed 3 MHz when the PLL mode is first set. Both these restrictions are in place to prevent the CPU clock frequency from temporarily exceeding 12 MHz for 3V operation (or 24 MHz for 5V operation).

As mentioned earlier, *boot.asm* holds off entry to *main()* until all the clocks are stable when using the ECO. When the PLL mode is used, the following delays are also present in *boot.asm*:

- A one second delay is added whenever the ECO is enabled to wait for the ECO to become stable.
- Following the one second delay for ECO stabilization, a 16 millisecond delay is added before the PLL mode of the IMO is enabled.

To provide these delays, *boot.asm* uses the sleep timer, but does not enable the interrupt. Therefore *boot.asm* does not include a sleep timer Interrupt Service Routine (ISR). If a designer needs to use a sleep timer ISR, it is recommended that another sleep timer be created in a separate source code file and called from *boot.asm*. The sleep timer module is found in the Miscellaneous Digital User Modules category.

If some tasks must be accomplished before the one second period expires, add the initialization code to *boot.asm* (remember that the edits must be made to the template file: *boot.tpl*). Designers could also choose to write their own clock initialization code as long as the rules in this section are upheld. *boot.asm* contains a flag, *WAIT_FOR_32K*, which forces the program to wait for the clocks to stabilize before calling main. If the designer changes the flag to '0', *boot.asm* starts the ECO, but does not wait for it to stabilize and does not set the *PLL_Lock* bit. If this is done, the user must provide code elsewhere that enables the ECO through the same process as the original startup sequence. However, for this to work, the *PLL_Mode* must be disabled in the Global Resources window so that it is not enabled by *boot.asm* before the ECO is enabled by the user's code. If the PLL is used in the application, it must also be enabled by the user's code after the ECO is enabled correctly.

ECO_TR Register

When using the ECO, there are a few components that must be set by the trim register for satisfactory operation. They include Comparator or Output Buffer A and B and the Amplitude Control. Output Buffer A is an improvement from an older design while Output Buffer B is a new addition. The *ECO_TR* register is write only, which means that bitwise logical operations cannot be used to change specific bits. This register is shown in Table 3

Bit Description

Output Buffer A Bias Control [0]

This bit is used to set the startup (unregulated) bias current of the crystal oscillator output buffer A. In normal operation this bias level exceeds what is required for stable oscillation and as a result, the amplitude of the signal on the crystal increases. The signal then approaches the level set by the amplitude control bits and the bias level is reduced by the amplitude control loop until stable oscillation is maintained at the defined level.

0 = minimum bias

1 = maximum bias

Output Buffer B Bias Control [1]

This bit is used to set the bias reference level for the crystal oscillator output buffer B. Because output buffer B utilizes a fixed bias level, this operates at a fixed level independent of the oscillator amplitude settings.

0 = minimum bias

1 = maximum bias

Amplitude Control [3:2]

These bits are responsible for controlling the amplitude of the crystal oscillator. The settings are:

01 = Highest

00 = Medium High

11 = Medium Low

10 = Lowest

Table 4 shows the power consumption operating under each of these modes.

Output Buffer B Enable [4]

This bit is responsible for enabling the extra output buffer B. This buffer operates at a fixed bias level which is controlled by the bias control bit 1. That also means that bit 1 elicits no effect if bit 4 does not enable buffer B.

0 = enables operation only for buffer A

1 = enables operation for buffer B and bias generator

Output Buffer B Hysteresis Enable [5]

This bit provides approximately 30 mV of hysteresis to the output buffer. However, the value of bit 5 elicits no effect if output buffer B is not enabled by bit 4.

0 = Disables Hysteresis

1 = Enables Hysteresis

Reserved [6:7]

These bits are unused by this operation, but are assigned to functions elsewhere in the IC.

Table 3. ECO_TR Register Description

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		Output Buffer B Hysteresis	Output Buffer B Enable	MSB	LSB	Output Buffer B Bias Control	Output Buffer A Bias Control
Reserved		Output Buffer B Control		Amplitude Control		Bias Control	

Table 4. Power Consumption Test Results for Amplitude Settings

Amplitude Setting	Vdd (Volts)	ECO Vpp (Volts)	Supply Current (µAmperes)	ECO Power (µWatts)
Highest (77h)	5.5	2.38	9.11	2.36
Medium High (73h)		1.40	7.66	8.17
Medium Low (7Fh)		0.98	7.20	4.07
Lowest (7Bh)		0.72	7.02	2.14
Highest (77h)	3.0	2.17	5.56	1.96
Medium High (73h)		1.30	4.19	7.04
Medium Low (7Fh)		0.93	3.92	3.62
Lowest (7Bh)		0.68	3.65	1.90

Recommendations

Recommended settings for the trim register are provided based upon the design report by Thomas Bocek and testing carried out by James Shutt.

Under normal conditions, the recommended setting for the *ECO_TR* register is 77h. This enables output buffer B, its hysteresis, and both bias generators. It also sets the amplitude control to the highest setting. It is under this setting where the ECO has its greatest immunity to noise and off-chip layout parasitics. However, higher operating amplitude requires a greater bias level and therefore this setting also requires the most supply current. If power conservation is an issue, then reduce the amplitude control value accordingly. See Table 4 for reference.

Notes

1. Setting the *32K_Select* Global Resource to ‘Internal’ and *PLL_Mode* Global Resource to ‘External Lock’ is an invalid configuration. There is no connection from the ILO to the IMO (see the Clock Tree diagram in the CY8C27x43 Family Data Sheet). The requirement is evaluated by the Design Rule Checker provided in PSoC Designer (Tools>>Design Rule Checker).
2. The XtalIn and XtalOut pins are also used for the In-System Serial Programming. The pins can be configured to function for both operations in the same design. For more information on in-system programming, see Application Note AN2014: Design for In-System Serial Programming.
3. For the CY8C27x43 Rev A chip, bits 2 and 3 of *CPU_SCR1* register cannot be used.

Document History

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Document Number: 001-40399

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1532004	EDT	11/13/07	Submitted to ECN system
*A	2551067	MAXK/JVY	08/11/08	Rolled in changes from multiple revisions that were never formalized. Updated for more recent devices and programming software.

In March of 2007, Cypress recataloged all of its Application Notes using a new documentation number and revision code. This new documentation number and revision code (001-xxxxx, beginning with rev. **), located in the footer of the document, will be used in all subsequent revisions.
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