DDR2 Posted CAS# Additive Latency

Technical Note

Introduction

DDR2 SDRAM introduces posted CAS# additive latency (AL) to make the command and data bus efficient for sustainable bandwidths. As demonstrated by Figure 1, commands may be issued externally but held by the device internally prior to execution, for the duration of AL, in order to improve system scheduling. Specifically, it helps avoid collision on the command bus and gaps in data input/output bursts.

The AL function is controlled by an extended mode register and programmed via bits E3–E5 of the EXTENDED MODE REGISTER SET command, as shown in Figure 2. AL of 0, 1, 2, 3, or 4 clocks is supported. This Technical Note describes the AL Function of the DDR2 SDRAM device.

Additive Latency Disabled

Figure 3 illustrates an example of DDR2 bank interleave reads. During the process, a bank is opened with an ACTIVATE command. After ^{t}RCD has been satisfied, a READ WITH AUTO PRECHARGE command is issued and data is read out of the DRAM. As seen in Figure 3, sometimes a command cannot be issued in the optimal location because another command occupies the location. The ACTIVATE to Bank *z* command must be delayed by one clock to avoid collision with the READ WITH AUTO PRECHARGE command, resulting in a gap in the output data.

Additive Latency Enabled

AL allows a READ or WRITE command to be issued to the DDR2 SDRAM prior to ^{t}RCD (MIN) with the requirement that AL ≤ ^{t}RCD (MIN). Consequently, READ or WRITE cannot be issued prior to the ACTIVATE command. The READ or WRITE command is held for the time specified by AL before it is issued internally to the DDR2 SDRAM device. Thus, READ Latency (RL) is equal to the sum of AL and CAS# latency (CL). WRITE latency (WL) is equal to the READ latency minus one clock: WL = AL + CL - (1 x ^{t}CK).

Figure 4 illustrates an example of DDR2 bank interleave reads with AL = ^{t}RCD – (1 x ^{t}CK). In this configuration the ACTIVATE and READ WITH AUTO PRECHARGE commands may be issued back to back. Assume ^{t}RCD = 4 x ^{t}CK; then AL is 3 clocks. With a Burst Length of 4 requiring 2 clocks to burst data, the 2 clocks required for each ACTIVATE to READ WITH AUTO PRECHARGE pair match perfectly, resulting in continuous output of data from the DDR2 SDRAM device.

Additive latency (AL = 1) is only used for READ commands and will not affect WRITE command timing

Figure 1: External and Internal Command Issue

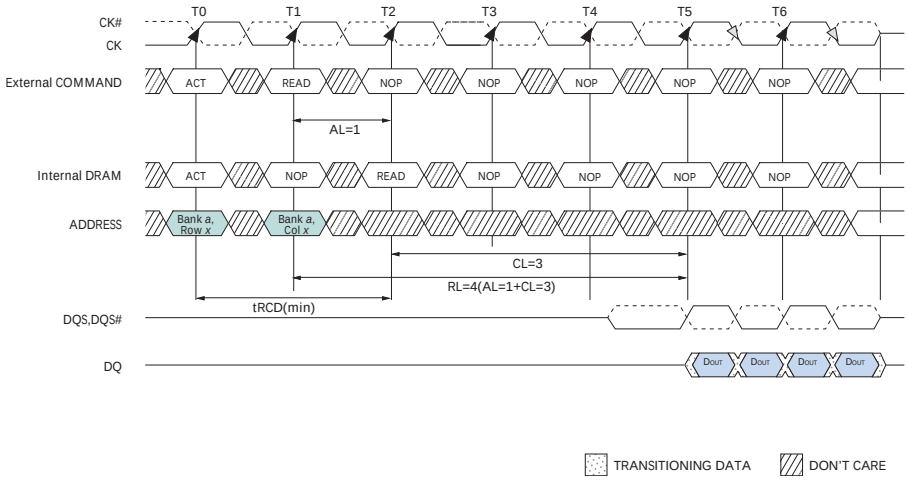
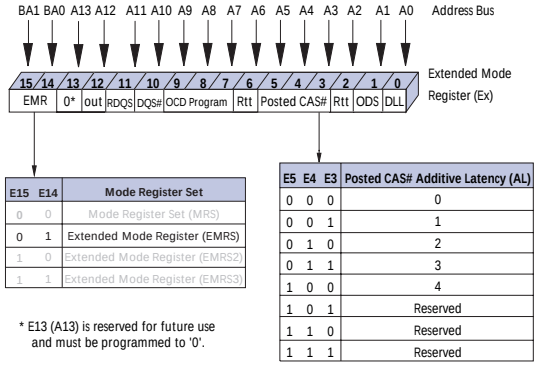


Figure 2: Progamming AL in the Extended Mode Register (EMR1)



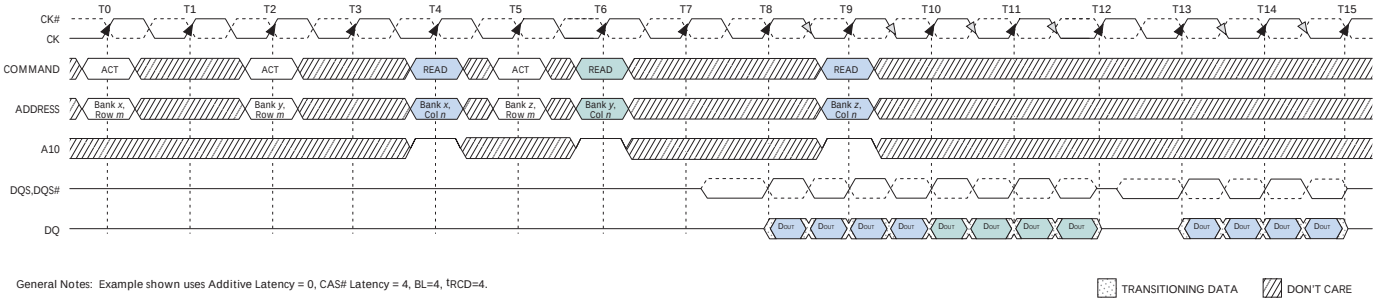
E15	E14	Mode Register Set
0	0	Mode Register Set (MRS)
0	1	Extended Mode Register (EMRS)
1	0	Extended Mode Register (EMRS2)
1	1	Extended Mode Register (EMRS3)

* E13 (A13) is reserved for future use and must be programmed to '0'.

E5	E4	E3	Posted CAS# Additive Latency (AL)
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

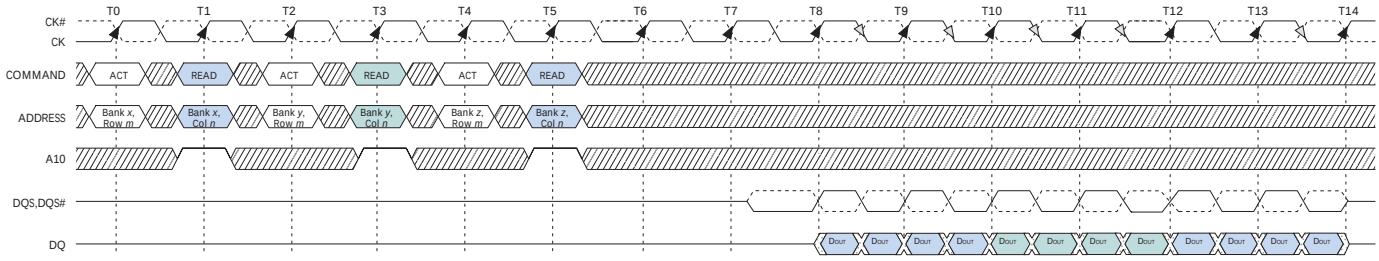
Bank Interleave Reads

Figure 3: DDR2 Bank Interleave Reads with AL = 0



General Notes: Example shown uses Additive Latency = 0, CAS# Latency = 4, BL=4, ^{t}RCD=4.

Figure 4: DDR2 Bank Interleave Reads with AL = 3



General Notes: Example shown uses Additive Latency = 3, CAS# Latency = 4, BL=4, ^{t}RCD=4.

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