Technical Note

PSRAM 101: An Introduction to Micron® CellularRAM® and PSRAM

Introduction

The mobile phone market has become increasingly cost competitive, demanding interface innovations to support the low-cost requirements inherent in this market. Micron® PSRAM provides both the high bandwidth and the low power necessary to replace SRAM or to serve as a companion chip to burst NOR Flash in wireless applications.

This technical note introduces Micron® CellularRAM and PSRAM devices; demonstrates their advantages over other memory options for use in mobile handsets; and presents available configurations. It also provides supporting information for their use in mobile applications and an example for replacing SRAM with CellularRAM or PSRAM in mobile and non-mobile-phone applications.

Micron PSRAM and CellularRAM devices have most commands, operations, and functions in common. Devices designated as CellularRAM are devices that meet or exceed the functionality and specifications defined by the CellularRAM Workgroup, and offer low-power features.

Micron, PSRAM, and the CellularRAM Workgroup

In June 2002, the CellularRAM Workgroup was formed as a vehicle to provide common specifications for a multi generation family of low-power, enhanced pseudo-static RAM (PSRAM) devices. These common specifications help standardize PSRAM to meet the requirements for wireless handsets. Micron has since established itself as a leader in PSRAM manufacturing.

PSRAM combines low-power features with high bandwidth and a lower cost/bit ratio than other solutions, making it the ideal choice for low-end to midrange cellular phone applications. Micron PSRAM also features SRAM-pin compatibility and hidden refresh.

Market Requirements

To meet market demand, Micron provides both PSRAM and CellularRAM low-cost, low-power, high-bandwidth devices designed for wireless applications.

In addition to PSRAM devices conforming to CellularRAM 1.0 and 1.5 specifications, Micron was the first to introduce a family of address- and data-multiplexed (AD-Mux) PSRAM designs; the CellularRAM Work Group has since introduced CellularRAM AD-Mux as an official specification.

Multiplexing the address pins with the DQ makes possible a substantial reduction in pin count. In a market where cost per pin is important, reducing the pin count by 16 pins represents a significant savings for both the printed circuit board and the controller design. The AD-Mux design family has enabled Micron to deliver CellularRAM performance with reduced pin count.

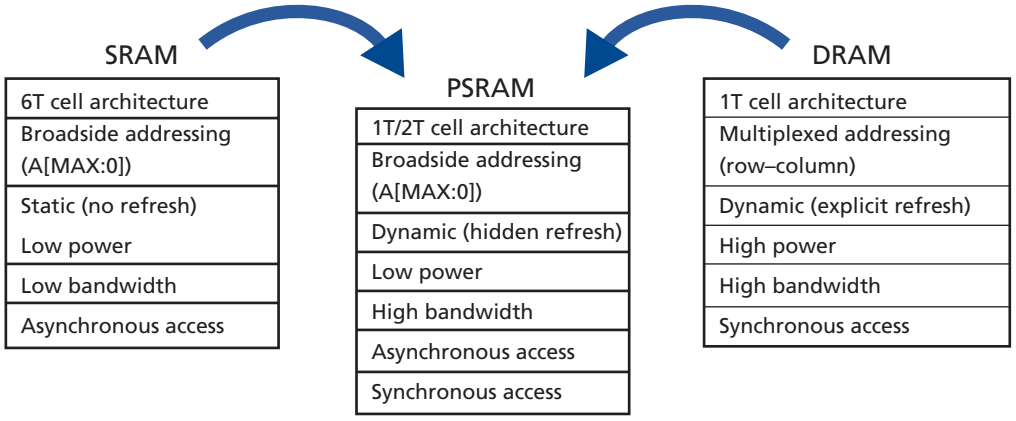
Present and past performance illustrate Micron's commitment to providing innovative memory solutions enabling the mobile marketplace.

What is a PSRAM?

Micron PSRAM products are high-speed, CMOS memory devices developed for low-power, portable (x16) applications. Micron offers asynchronous/page, asynchronous/page/burst, and burst AD-Mux devices that conform to CellularRAM Workgroup specifications.

The PSRAM async/page device provides a drop-in replacement for SRAM when configured to support the simple asynchronous SRAM interface. Micron PSRAM also supports the NOR Flash burst (async/page/burst) interface.

Figure 1: PSRAM: DRAM Core Designs with SRAM Interface



PSRAM combines SRAM broadside addressing with the 1T or 2T cell architecture of a DRAM. Using a DRAM core design makes substantial savings possible due to reduced die size.

PSRAM products incorporate a transparent self-refresh mechanism—hidden refresh—to simplify the interface. Hidden refresh does not require additional system-memory controller support and has no significant impact on device read/write performance.

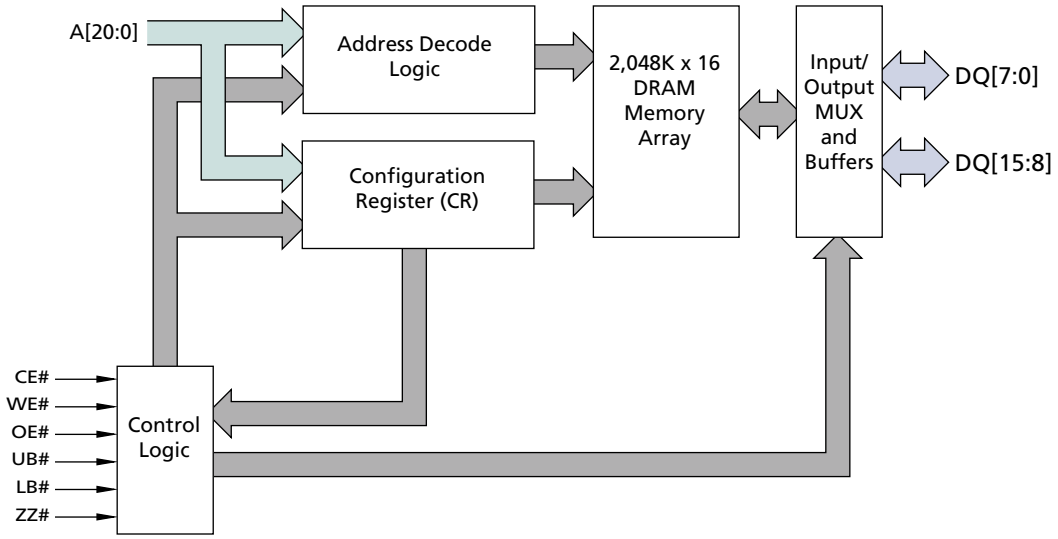
Micron PSRAM supports the low-power features present on CellularRAM designs. Features such as partial-array refresh (PAR), temperature-compensated refresh (TCR), and deep power-down (DPD) are all attractive features for the mobile environment. Low-power features are implemented by changing user-defined settings on chip registers. For the async/page design, the register is referred to as the configuration register (CR); for the async/page/burst design, it is called the refresh configuration register (RCR).

Adding support for synchronous access makes high bandwidth performance possible with minimal design change.

Async/Page Configuration: CellularRAM and PSRAM

The functional block diagram for the async/page configuration is shown in Figure 2. With the exception of the ZZ# pin used for PSRAM, all control, address and data pins required for an SRAM interface have equivalent function in the PSRAM design. The ZZ# pin provides for configuration flexibility when low power is desired. PAR, TCR, and DPD can be implemented by changes to the configuration register.

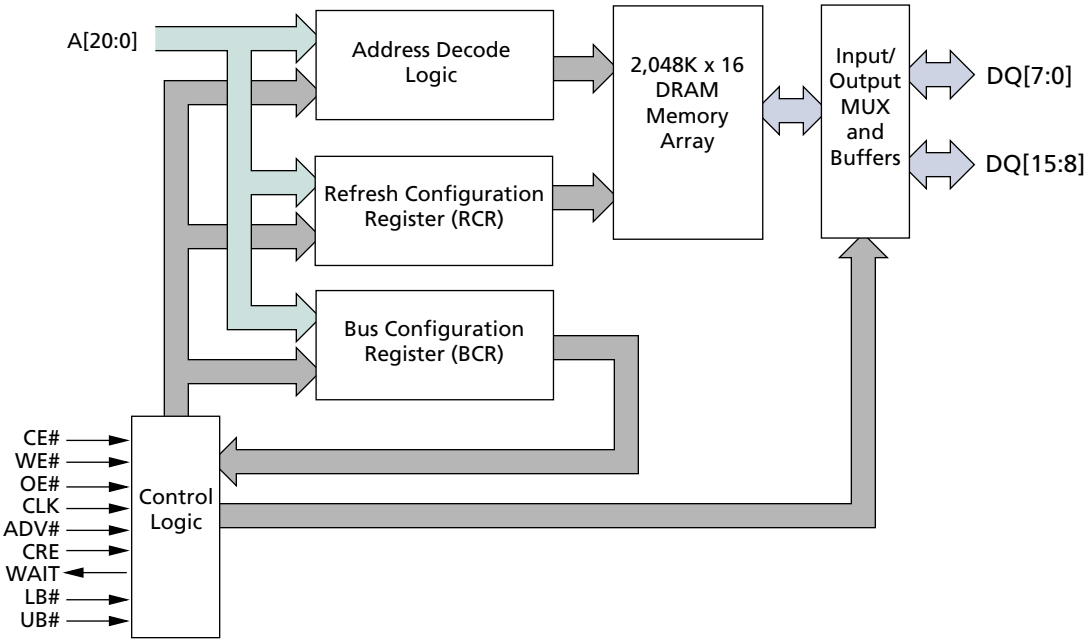
Figure 2: Async/Page Functional Block Diagram



Async/Page/Burst Configuration: CellularRAM

The functional block diagram for the async/page/burst configuration is shown in Figure 3. This configuration is fully compatible with standard NOR Flash burst interface designs. Three pins—WAIT, ADV, and CLK—have been added to provide the synchronous control pins needed for this configuration. ZZ# has been replaced by a HIGH-active control register enable (CRE) pin to access the RCR (similar to the CR available on the async/page device) and the bus configuration register (BCR). These registers are compatible with similar registers on NOR Flash devices. The PSRAM design provides burst WRITE functionality; the legacy NOR Flash burst interface does not.

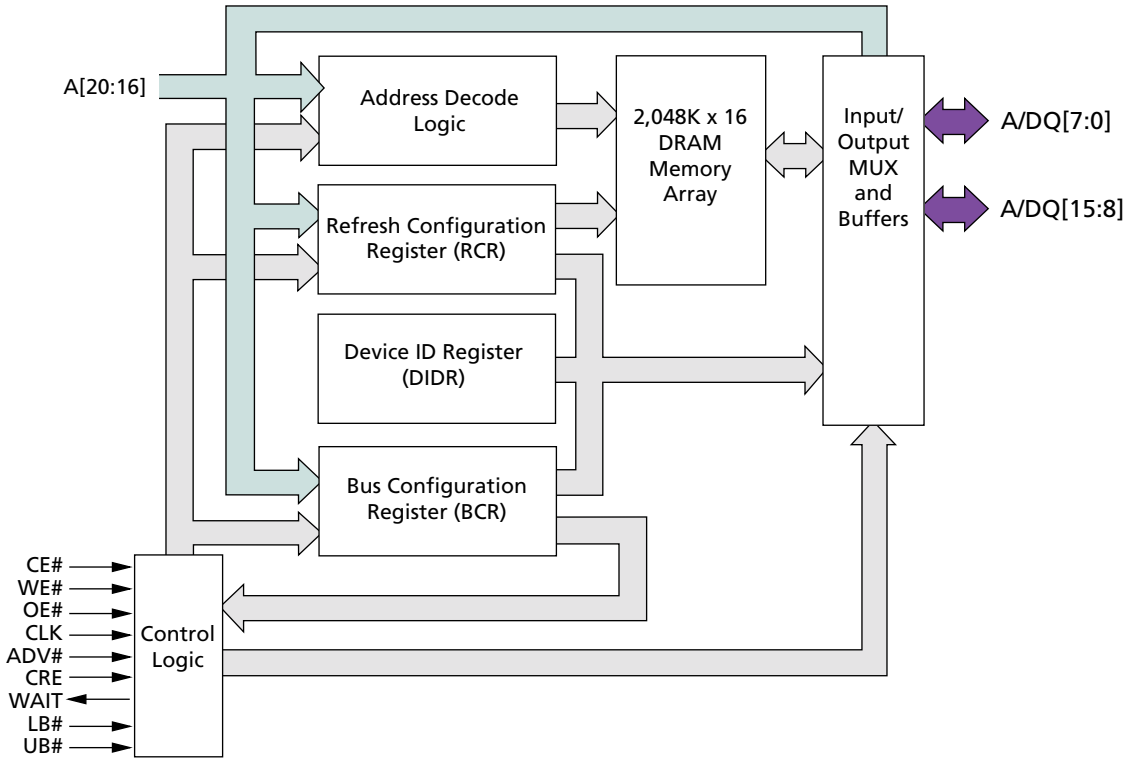
Figure 3: Async/Page/Burst Functional Block Diagram



Burst AD-Mux Configuration: CellularRAM

The burst AD-Mux configuration is very similar to async/page/burst configuration. Because the first 16 address pins are multiplexed with the DQ pins, the interface requires 16 fewer pins.

Figure 4: Burst AD-Mux Functional Block Diagram



Storage Cell Comparison

A good reason to move from SRAM-based designs to CellularRAM or PSRAM is to decrease the die size for a given density. A memory design will have three basic design blocks that influence how large the die will be for a given process geometry. These are the memory array, the peripheral logic, and the power/input/output pad structures.

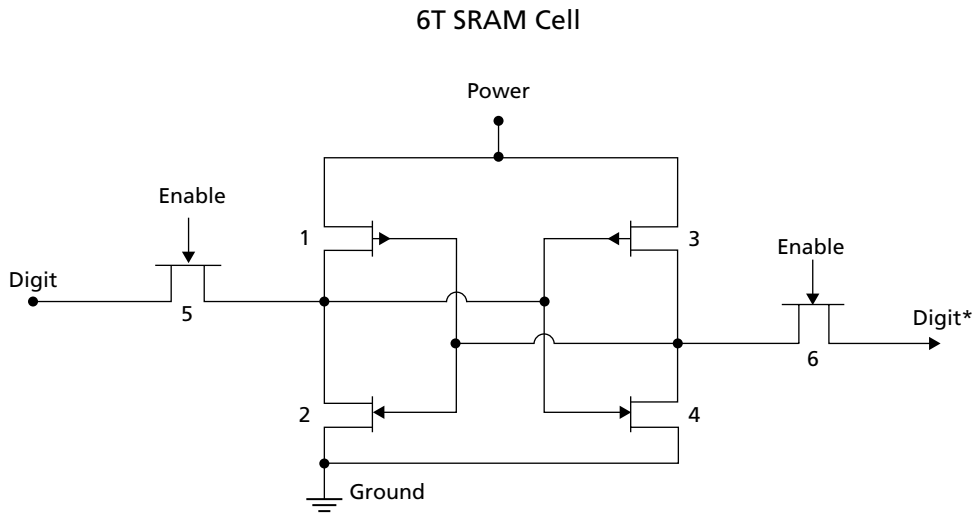
This section focuses on the memory-array as the predominant differentiator in choosing a memory type.

Memory Array

The size of the memory array is dictated by the size and number of components that make up the storage cell. In the case of SRAM, a six-transistor (6T) cross-coupled latch is used to make up the storage cell. The traditional 6T SRAM cell design is illustrated in Figure 5. Figure 6 on page 7 shows an example of the storage cell used for 1T/1C DRAM designs. CellularRAM and PSRAM devices use either a 1T/1C or a 2T/2C variation of the DRAM storage cell.

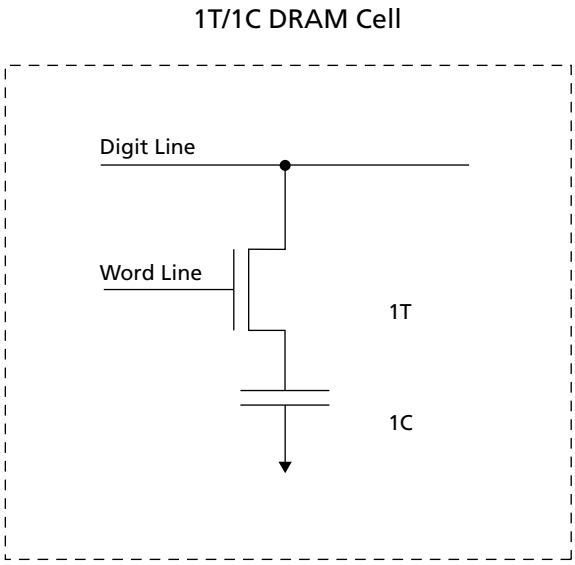
Transitioning from the SRAM 6T cell to either the 1T/1C or the 2T/2C DRAM cell results in a substantial reduction in the size of the memory array. With the reduction in the memory array size comes a corresponding decrease in die size, resulting in more die per wafer and a decrease in overall manufacturing cost.

Figure 5: SRAM Storage Cell



As illustrated in Figure 5, the 6T cell consists of 6 minimum-geometry transistors. The 1T/1C cell shown in Figure 6, made up of 1 minimum-geometry transistor and capacitor, will result in a substantially smaller area per cell.

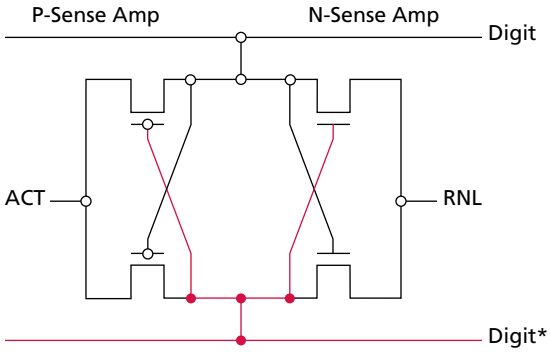
Figure 6: The 1T/1C DRAM Storage Cell Array



2T/2C Architecture

To understand the 2T/2C architecture, it is useful to review basic DRAM sense amp operation. A simplified DRAM sense amp diagram is shown in Figure 7.

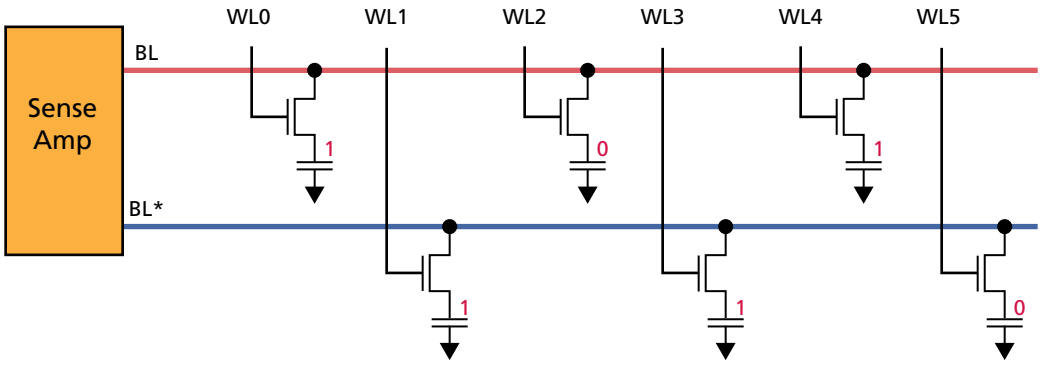
Figure 7: DRAM Sense Amp



The sense amp includes both N and P sense amps. The N sense amp will detect the lower of either the Digit line or the Digit* line and pull that line to ground. The P sense amp will detect the lower of either the Digit line or the Digit* line and pull that line to V_{CC}.

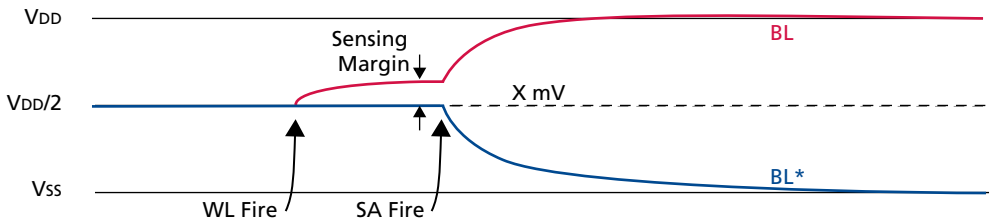
During a READ operation, first the Digit and Digit* lines at the sense amp are equilibrated to a reference voltage, typically one-half V_{CC}. Then a word line is pulled HIGH, dumping the cell-charge bit line (BL) to the Digit line, either increasing the line voltage in the case of a stored logic-1 level, or decreasing the level in the case of a logic 0. The difference between the Digit voltage and the Digit* voltage is sensed, amplified, and written back to the cell. The sensing margin associated with the 1T/1C scheme is shown in Figure 9 on page 8.

Figure 8: 1T/1C Illustration



Notes: 1. BL = bit line
WL = word line

Figure 9: 1T/1C Sensing Margin

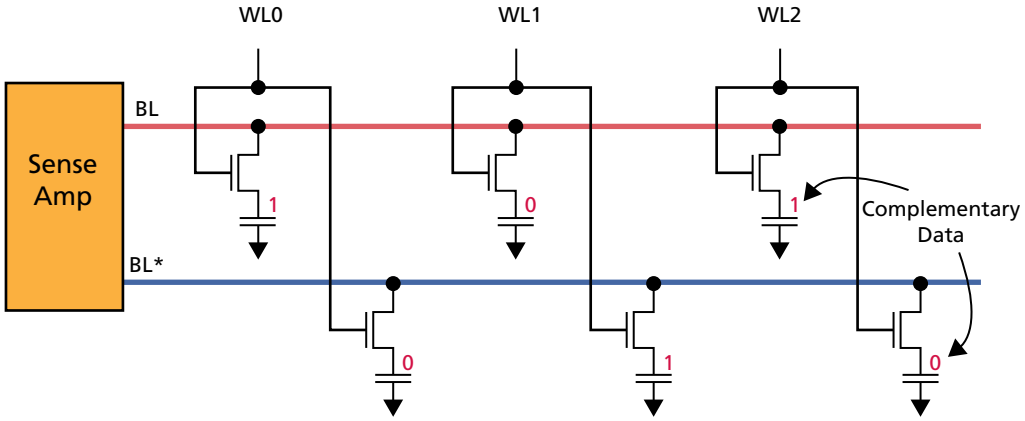


Notes: 1. BL = bit line
WL = word line
SA = sense amp

2T/2C Sensing

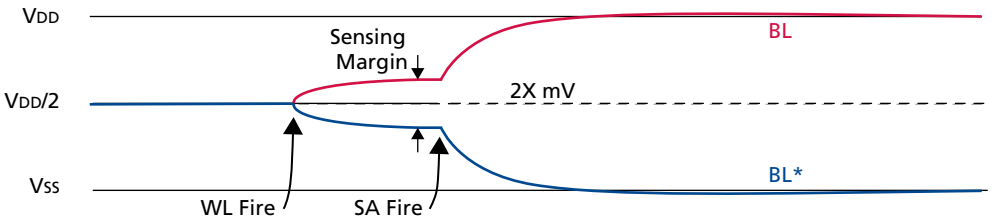
In the 2T/2C architecture, the BL* is tied to a second 1T/1C storage cell (rather than a reference voltage). The second 1T/1C storage cell always contains the logical complement of the logic level stored in the BL-connected cell. Comparing a sensed 1 level to a sensed 0 level, instead of comparing a sensed level to a reference voltage, effectively doubles the sensing margin. The 2T/2C sensing scheme is illustrated in Figures 10 and 11 on page 9.

Figure 10: 2T/2C Sensing Scheme



Notes: 1. BL = bit line
WL = word line

Figure 11: 2T/2C Sensing Margin



Notes: 1. BL = bit line
WL = word line
SA = sense amp

A 2x improvement in sensing margin results from comparing complementary data. Increased sensing margin aids the design in two ways. First, increased sensing margin ensures that valid data is sensed, effectively guarding against post-assembly cell degradation. Second, the increased margin enables the refresh oscillator to refresh less frequently, resulting in lower standby current.

Basic Operations for Broadside Addressing

The following text and drawings are from the 32Mb PSRAM design available at www.micron.com. For detailed descriptions of other densities or configurations, please refer to the applicable data sheet. The descriptions included here pertain to use of an async/page/burst device.

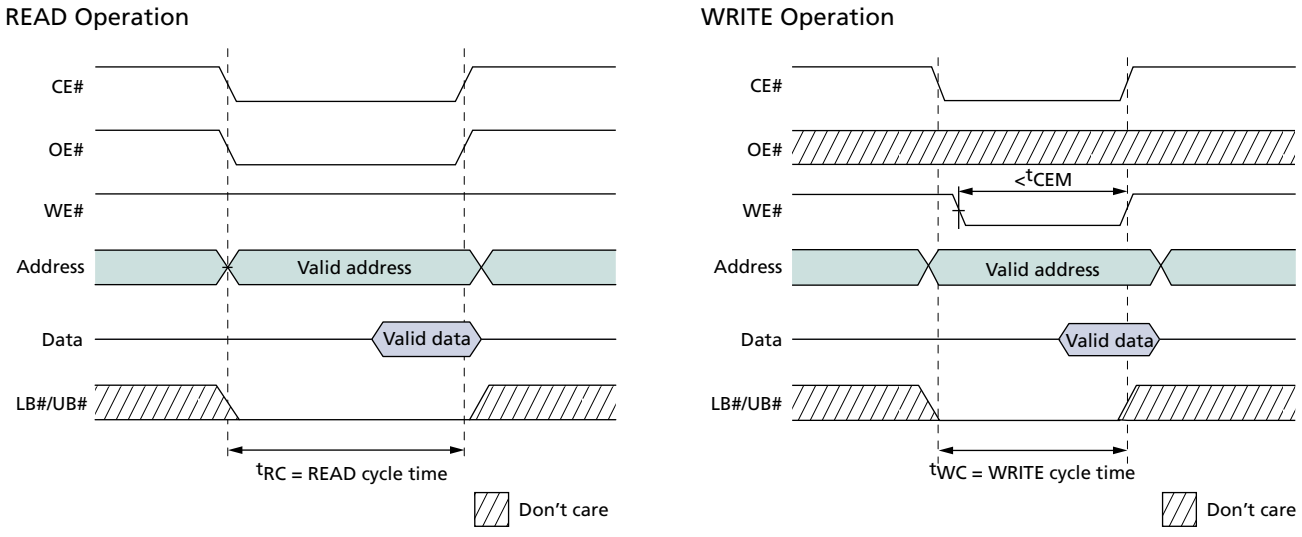
Asynchronous Mode

CellularRAM products and Micron PSRAM products power up in the asynchronous operating mode. This mode uses the industry-standard SRAM control bus (CE#, OE#, WE#, LB#/UB#). READ operations are initiated by bringing CE#, OE#, and LB#/UB# LOW while keeping WE# HIGH (see Figure 12). Valid data is driven out of the I/Os after the specified access time has elapsed.

WRITE operations occur when CE#, WE#, and LB#/UB# are driven LOW (see Figure 12). During asynchronous WRITE operations, the OE# level is a “don't care,” and WE# will override OE#. The data to be written is latched on the rising edge of CE#, WE#, or LB#/UB#, whichever occurs first. Asynchronous operations (with page mode disabled) can either use the ADV input to latch the address, or ADV can be driven LOW during the entire READ/WRITE operation.

When using an async/page/burst-configured device in an asynchronous-only application, the CLK input must be held static LOW or HIGH. WAIT will be driven while the device is enabled, and its state should be ignored. The WAIT pin can be floated for this configuration, as it is ignored for asynchronous and page mode accesses. For all configurations, WE# LOW time must be limited to ^{t}CEM.

Figure 12: READ and WRITE Operations (ADV = LOW)



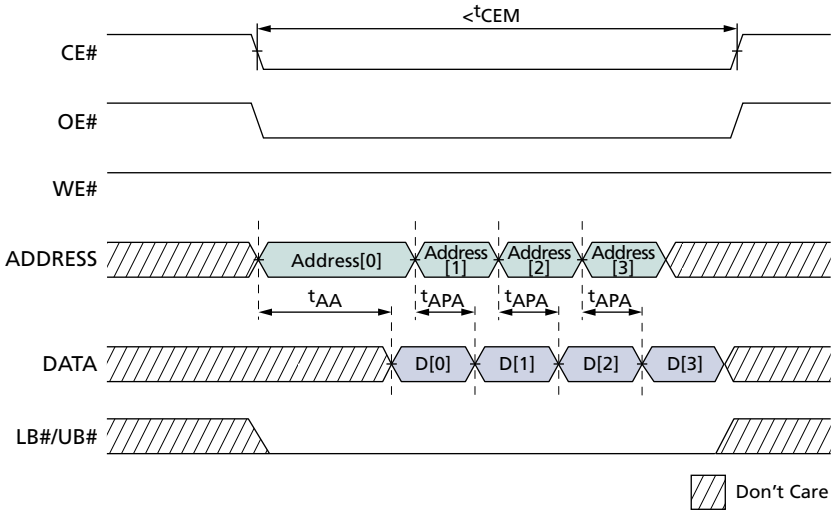
Page Mode READ Operation

Page mode is a performance-enhancing extension to the legacy asynchronous READ operation. In page-mode-capable products, an initial asynchronous READ access is performed, then adjacent addresses can be read quickly by simply changing the low-order address. The address space of each 16-bit CellularRAM page is defined by addresses A[3:0]. Any change in addresses A4 or higher will initiate a new ^{t}AA access time. Figure 13 shows the timing for a page mode access. Page mode takes advantage of the fact that adjacent addresses can be read in a shorter period of time than random addresses. WRITE operations do not include comparable page mode functionality.

During asynchronous page-mode operation, the CLK input must be held static LOW or HIGH. CE# must be driven HIGH upon completion of a page mode access. WAIT will be driven while the device is enabled, and its state should be ignored. Page mode is enabled by setting RCR[7] to HIGH. ADV must be driven LOW during all page mode READ accesses.

While page mode is selected, the CE# LOW time is limited by refresh considerations. CE# must not stay LOW longer than ^{t}CEM.

Figure 13: Page Mode READ Operation (ADV = LOW)



CellularRAM Burst Mode Operation

Burst mode operations enable high-speed synchronous READ and WRITE operations. Burst operations consist of a multiclock sequence that must be performed in an ordered fashion. After CE# goes LOW, the address to be accessed is latched on the next rising edge of CLK when ADV# is LOW. During this first clock rising edge, WE# indicates whether the operation will be a READ or a WRITE.

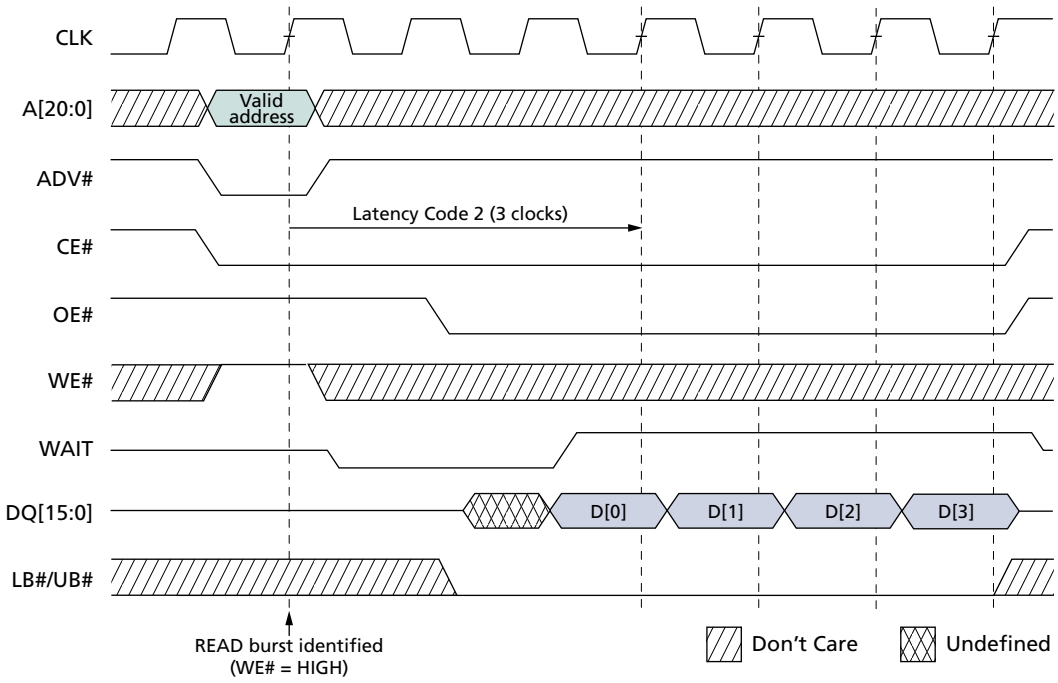
The size of a burst can be specified in the BCR as either fixed-length or continuous. Fixed-length bursts consist of 4, 8, or 16 words. Continuous bursts can start at a specified address and burst through the entire memory. The latency count stored in the BCR defines the number of clock cycles that elapse before the initial data value is transferred between the processor and the device.

The WAIT output will be asserted as soon as CE# goes LOW and will be de-asserted to indicate when data is to be transferred into or out of the memory. WAIT will again be asserted if the burst crosses the boundary between 128-word rows. When the device has restored the previous row's data and accessed the next row, WAIT will be de-asserted and the burst will continue.

If burst mode is suspended, the processor can access other devices without incurring the timing penalty of the initial latency for a new burst. Bursts are suspended by stopping CLK. CLK can be stopped HIGH or LOW. If another device will use the data bus while the burst is suspended, OE# should be taken HIGH to disable the outputs; otherwise, OE# can remain LOW. Note that the WAIT output will continue to be active, and as a result no other devices should directly share the WAIT connection to the controller. To continue the burst sequence, OE# is taken LOW, then CLK is restarted after valid data is available on the bus.

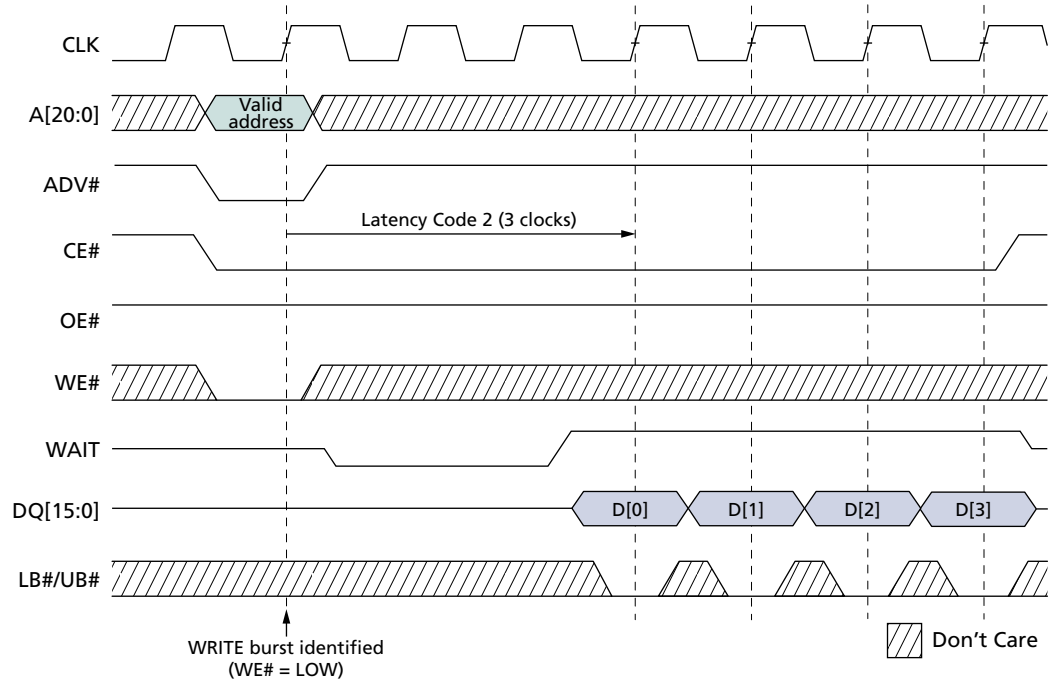
The CE# LOW time is limited by refresh considerations. CE# must not stay LOW longer than ^{t}CEM. If a burst suspension will cause CE# to remain LOW for longer than ^{t}CEM, CE# should be taken HIGH and the burst should be restarted with a new CE# LOW/ADV# LOW cycle.

Figure 14: Burst Mode READ (4-Word Burst)



Notes: 1. Nondefault BCR settings: Latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.

Figure 15: Burst Mode WRITE (4-Word Burst)



Notes: 1. Nondefault BCR settings: Latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.

CellularRAM Registers

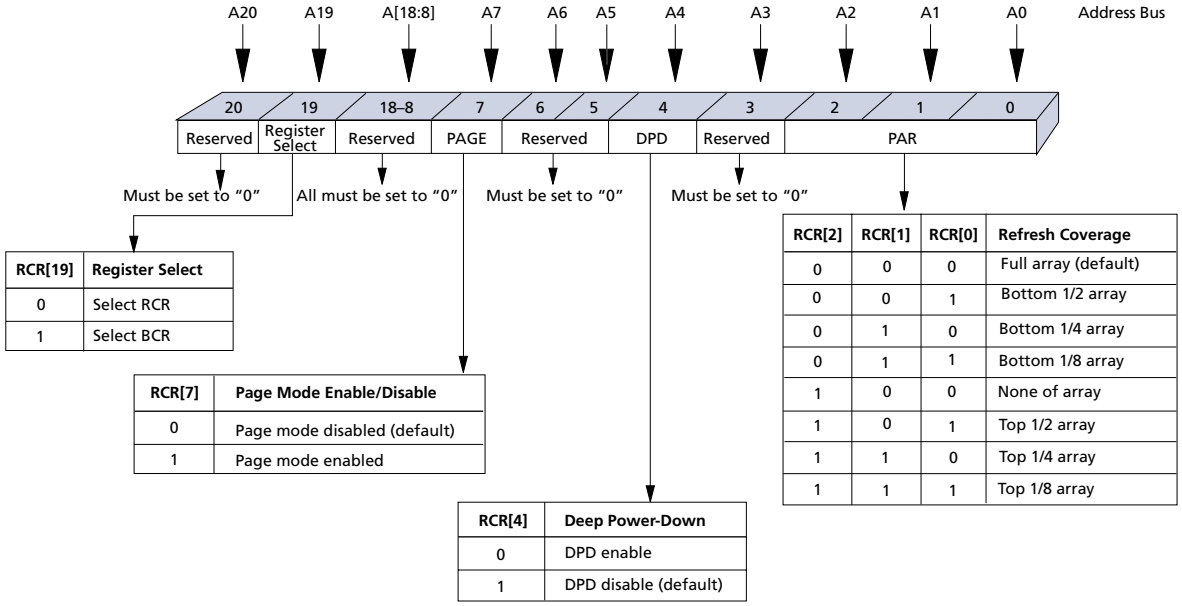
Micron CellularRAM supports user-programmable registers to configure the device for refresh operations and bus configurations.

Configuration Register/Refresh Configuration Register

The async/page device refers to the refresh register as a configuration register (CR), and the other configurations refer to this register as the refresh configuration register (RCR).

For the async/page/burst and burst AD-Mux interfaces, a bus configuration register (BCR) is also available to control the synchronous interface.

Figure 16: RCR Mapping



RCR[19]	Register Select
0	Select RCR
1	Select BCR

RCR[7]	Page Mode Enable/Disable
0	Page mode disabled (default)
1	Page mode enabled

RCR[4]	Deep Power-Down
0	DPD enable
1	DPD disable (default)

RCR[2]	RCR[1]	RCR[0]	Refresh Coverage
0	0	0	Full array (default)
0	0	1	Bottom 1/2 array
0	1	0	Bottom 1/4 array
0	1	1	Bottom 1/8 array
1	0	0	None of array
1	0	1	Top 1/2 array
1	1	0	Top 1/4 array
1	1	1	Top 1/8 array

Temperature-Compensated Refresh

The CellularRAM 1.0 specification provided for temperature-compensated-refresh (TCR) selection in the RCR[6:5] bits. For earlier devices using on-chip temperature sensors, default settings (selecting the on-die temperature sensor) enabled adequate refresh at different temperatures without changing the register settings. The device continually adjusted the refresh rate to match the current temperature. The CellularRAM 1.5 specification removes the provision that supported setting the RCR for refresh at the desired operating temperature.

Partial-Array Refresh RCR[2:0]

Partial-array refresh (PAR) restricts refresh operation to a portion of the total memory array. This feature enables the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, and none of the array. The mapping of these partitions can start at either the beginning or the end of the address map. READ and WRITE operations to address ranges receiving refresh will not be affected by a

partial -array refresh. Data stored in addresses not receiving refresh will become corrupted. When re-enabling additional portions of the array, the new portions are available immediately upon writing to the RCR.

Table 1: 32Mb Address Patterns for PAR (CR[4] = 1)

CR[2]	CR[1]	CR[0]	Active Section	Address Space	Size	Density
0	0	0	Full die	000000h–1FFFFFh	2 Meg x 16	32Mb
0	0	1	One-half of die	000000h–0FFFFFh	1 Meg x 16	16Mb
0	1	0	One-quarter of die	000000h–07FFFFh	512K x 16	8Mb
0	1	1	One-eighth of die	000000h–03FFFFh	256K x 16	4Mb
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	One-half of die	100000h–1FFFFFh	1 Meg x 16	16Mb
1	1	0	One-quarter of die	180000h–1FFFFFh	512K x 16	8Mb
1	1	1	One-eighth of die	1C0000h–1FFFFFh	256K x 16	4Mb

Deep Power-Down (RCR[4]), Default = DPD Disabled

The deep power-down bit enables and disables all refresh-related activity. This mode is used if the system does not require the storage provided by the device. Any stored data will become corrupted when DPD is enabled.

When refresh activity has been re-enabled, the device will require 150µs to perform an initialization procedure before normal operations can resume.

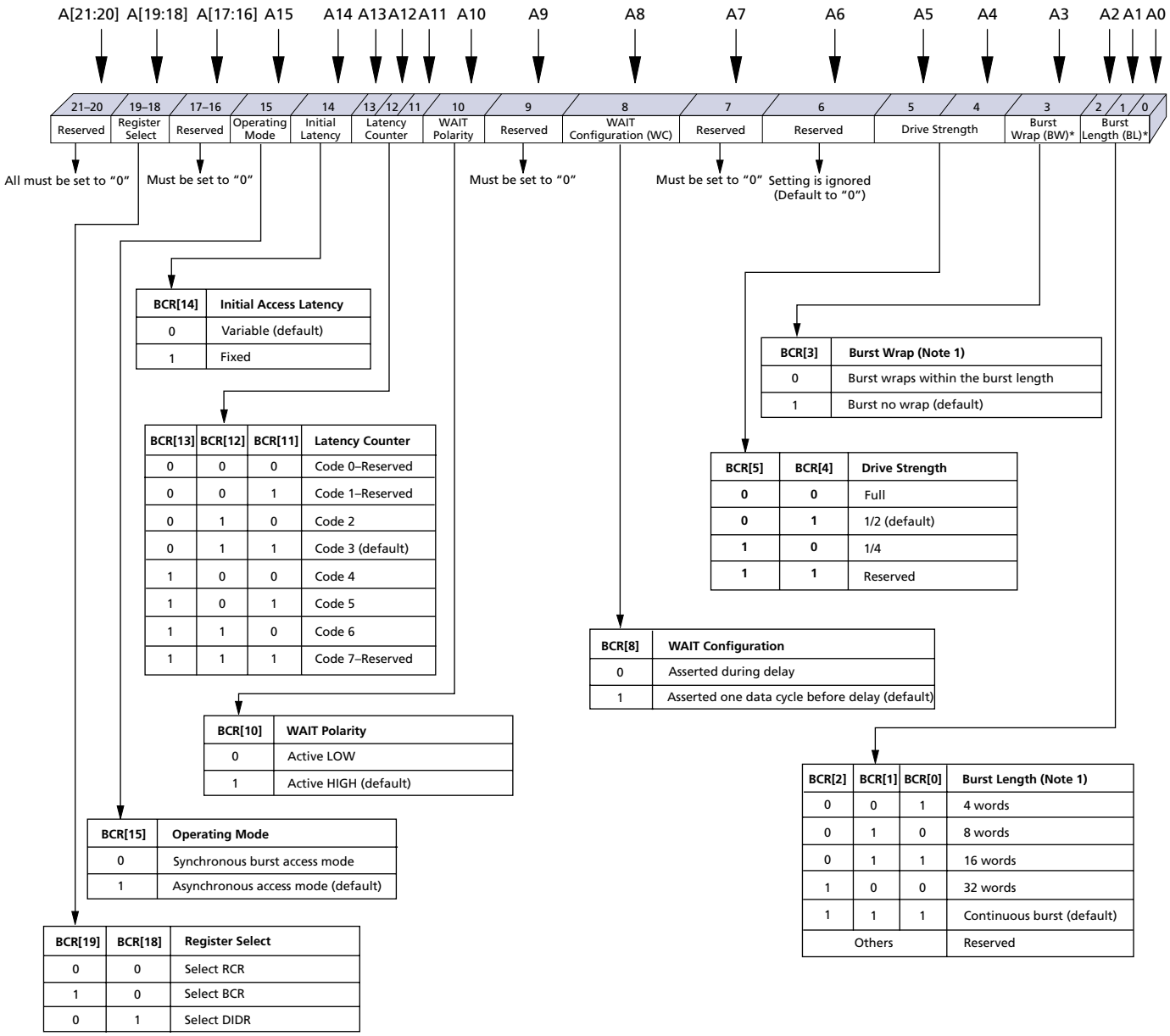
Deep power-down is enabled when RCR[4] = 0, and remains enabled until RCR[4] is set to “1.” DPD should not be enabled or disabled with the software access sequence; instead, use CRE to access the RCR.

Page Mode Operation (RCR[7]), Default = Disabled

The page mode operation bit determines whether page mode is enabled for asynchronous READ operations. In the power-up default state, page mode is disabled.

CellularRAM Bus Configuration Register

Figure 17: Bus Configuration Register Mapping



BCR[14]	Initial Access Latency
0	Variable (default)
1	Fixed

BCR[13]	BCR[12]	BCR[11]	Latency Counter
0	0	0	Code 0–Reserved
0	0	1	Code 1–Reserved
0	1	0	Code 2
0	1	1	Code 3 (default)
1	0	0	Code 4
1	0	1	Code 5
1	1	0	Code 6
1	1	1	Code 7–Reserved

BCR[10]	WAIT Polarity
0	Active LOW
1	Active HIGH (default)

BCR[15]	Operating Mode
0	Synchronous burst access mode
1	Asynchronous access mode (default)

BCR[19]	BCR[18]	Register Select
0	0	Select RCR
1	0	Select BCR
0	1	Select DIDR

BCR[3]	Burst Wrap (Note 1)
0	Burst wraps within the burst length
1	Burst no wrap (default)

BCR[5]	BCR[4]	Drive Strength
0	0	Full
0	1	1/2 (default)
1	0	1/4
1	1	Reserved

BCR[8]	WAIT Configuration
0	Asserted during delay
1	Asserted one data cycle before delay (default)

BCR[2]	BCR[1]	BCR[0]	Burst Length (Note 1)
0	0	1	4 words
0	1	0	8 words
0	1	1	16 words
1	0	0	32 words
1	1	1	Continuous burst (default)
Others			Reserved

Burst Length (BCR[2:0]) Default = Continuous Burst

Burst length defines the number of words the device outputs during burst READ and WRITE operations. The device supports a burst length of 4, 8, 16 (and in some cases 32) words. The device can also be set to continuous burst mode, where data is accessed sequentially up to the end of the row.

Burst Wrap (BCR[3]) Default = No Wrap

The burst-wrap option determines if a 4-, 8-, 16- (or 32-) word READ or WRITE burst wraps within the burst length, or steps through sequential addresses. If the wrap option is not enabled, the device accesses data from sequential addresses up to the end of the row.

Drive Strength (BCR[5:4]) Default Shown = Outputs Use Half-Drive Strength

The output driver strength can be altered to full, one-half, or one-quarter strength to adjust for different data-bus loading scenarios. The reduced-strength options are intended for stacked-chip (Flash + CellularRAM or PSRAM) environments when there is a dedicated memory bus. The reduced-drive-strength option minimizes the noise generated on the data bus during READ operations. Full output drive strength should be selected when a discrete device is used in a more heavily loaded data bus environment. Outputs are configured at half-drive strength during testing (see Table 2 for drive strength details).

Table 2: Drive Strength

BCR[5]	BCR[4]	Drive Strength	Impedance TYP(Ω)	Use Recommendation
0	0	Full	25–30	CL = 30pF to 50pF
0	1	1/2 (default)	50	CL = 15pF to 30pF, 104 MHz at light load
1	0	1/4	100	CL = 15pF or lower
1	1	Reserved		

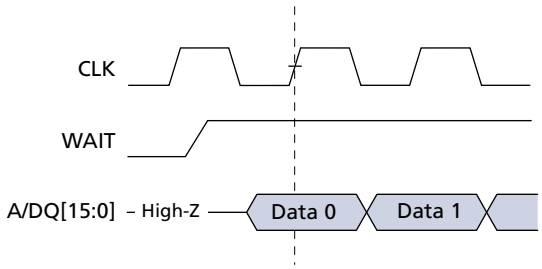
WAIT Configuration (BCR[8]) Default = WAIT Transitions One Clock Before Data Valid/Invalid

The WAIT configuration bit is used to determine when WAIT will transition between the asserted and the de-asserted state with respect to valid data presented on the data bus. The memory controller uses the WAIT signal to coordinate data transfer during synchronous READ and WRITE operations. When BCR[8] = 0, data will be valid or invalid on the clock edge immediately after WAIT transitions to the de-asserted or asserted state, respectively. When A8 = 1, the WAIT signal transitions one clock period prior to the data bus going valid or invalid (see Figure 18, and Figure 19 on page 18).

WAIT Polarity (BCR[10]) Default = WAIT Active HIGH

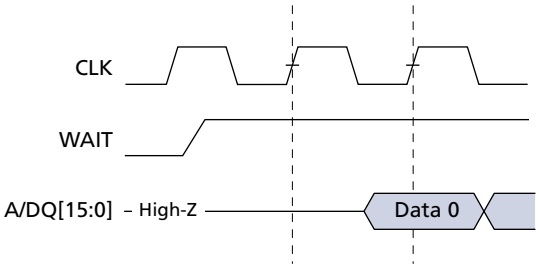
The WAIT polarity bit indicates whether an asserted WAIT output should be HIGH or LOW. This bit will determine whether the WAIT signal requires a pull-up or pull-down resistor to maintain the de-asserted state

Figure 18: WAIT Configuration (BCR[8] = 0)



Notes: 1. Data valid or invalid immediately after WAIT transitions (BCR[8] = 0).

Figure 19: WAIT Configuration (BCR[8] = 1)



Notes: 1. Valid or invalid data delayed for one clock after WAIT transitions (BCR[8] = 1).

Latency Counter (BCR[13:11]) Default = Three-Clock Latency

The latency counter bits determine the number of clocks between the beginning of a READ or WRITE operation and the first data value transferred.

Initial Access Latency (BCR[14]) Default = Variable

Variable initial access latency outputs data after the number of clocks set by the latency counter. However, WAIT must be monitored to detect delays caused by collisions with refresh operations.

Fixed initial access latency outputs the first data at a consistent time that accommodates worst-case refresh collisions. The latency counter must be configured to match the initial latency and the clock frequency. It is not necessary to monitor WAIT with fixed initial latency. After the number of clock cycles configured in the latency counter have completed, the burst begins.

Operating Mode (BCR[15]) Default = Asynchronous Operation

The operating mode bit selects either synchronous burst operation or the default asynchronous mode of operation.

Table 3: Variable Latency Configuration Codes (BCR[14] = 0)

BCR[13:11]	Latency Configuration Code	Latency[1]		Maximum Input CLK Frequency (MHz)		
		Normal	Refresh Collision	-7013	-701	-708
010	2 (3 clocks)	2	4	66 (15.0ns)	66 (15.0ns)	52 (19.2ns)
011	3 (4 clocks)—default	3	6	104 (9.62ns)	104 (9.62ns)	80 (12.5ns)
Others	Reserved	–	–	–	–	–

Notes: 1. Latency is the number of clock cycles from the initialization of a burst operation until data appears. Data is transferred on the next clock cycle. READ latency can range from the normal latency to the value shown for refresh collision. WRITE latency is fixed at the value shown for normal latency.

Table 4: Fixed Latency Configuration Codes (BCR9[1] = 1)

BCR[13:11]	Latency Configuration Code	Latency Count (N)	Maximum Input CLK Frequency (MHz)		
			-7013	-701	-708
010	2 (3 clocks)	2	33 (30ns)	33 (30ns)	33 (30ns)
011	3 (4 clocks)—default	3	52 (19.2ns)	52 (19.2ns)	52 (19.2ns)
100	4 (5 clocks)	4	66 (15ns)	66 (15ns)	66 (15ns)
101	5 (6 clocks)	5	75 (13.3ns)	75 (13.3ns)	75 (13.3ns)
110	6 (7 clocks)	6	104 (9.62ns)	104 (9.62ns)	80 (12.5ns)
Others	Reserved	–	–	–	–

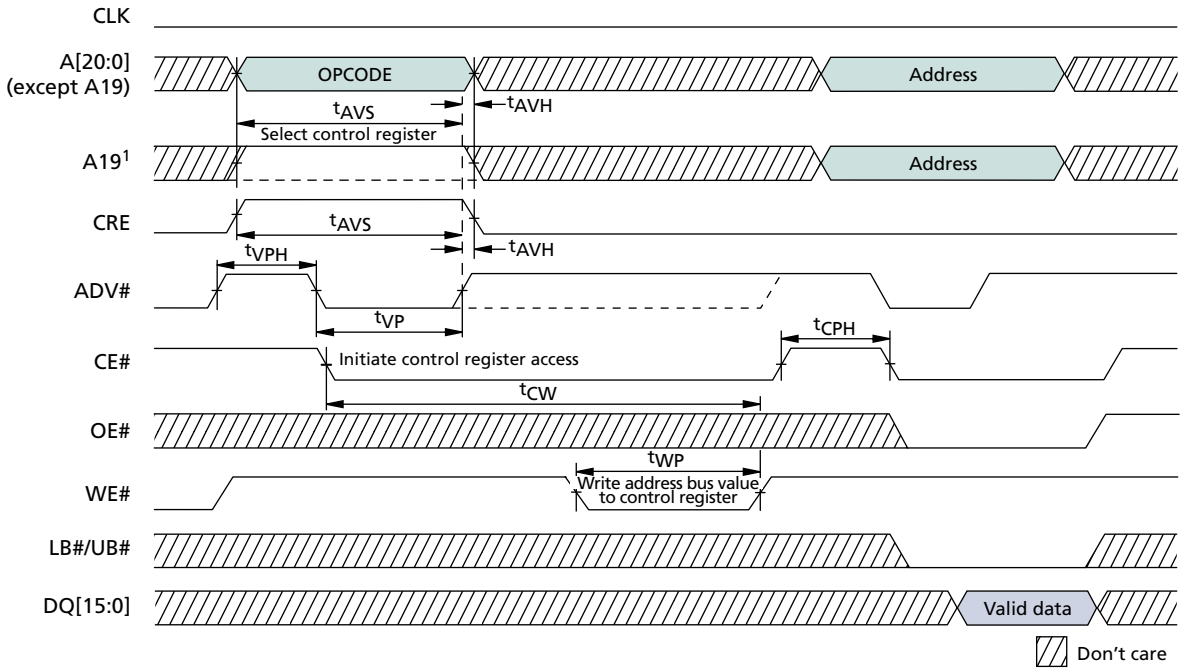
Setting the Configuration Registers

Two basic methods are available to access the configuration registers: configuration register access using CRE, and software access.

Configuration Register Access Using CRE

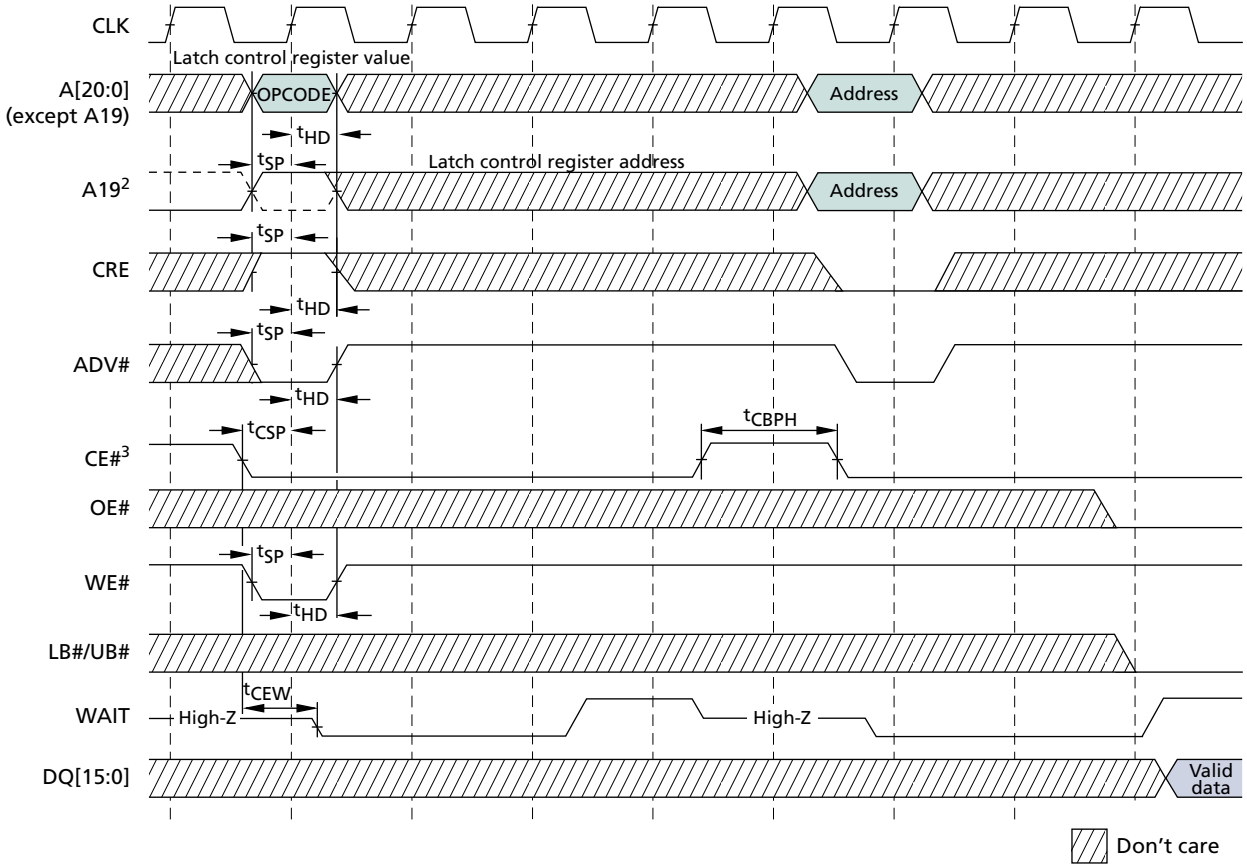
The configuration registers are loaded using either a synchronous or an asynchronous WRITE operation when the configuration register enable (CRE) input is HIGH. When CRE is LOW, a READ or WRITE operation will access the memory array. The register values are placed on address pins A[19:0]. In an asynchronous WRITE, the values are latched into the configuration register on the rising edge of ADV#, CE#, or WE#, whichever occurs first; LB# and UB# are “don’t care.” The BCR is accessed when A19 is HIGH; the RCR is accessed when A19 is LOW. For READs, address inputs other than A19 are “don't care,” and register bits 15–0 are output on DQ[15:0] (see Figures 20 through 23).

Figure 20: Asynchronous Mode Configuration Register WRITE followed by READ ARRAY Operation



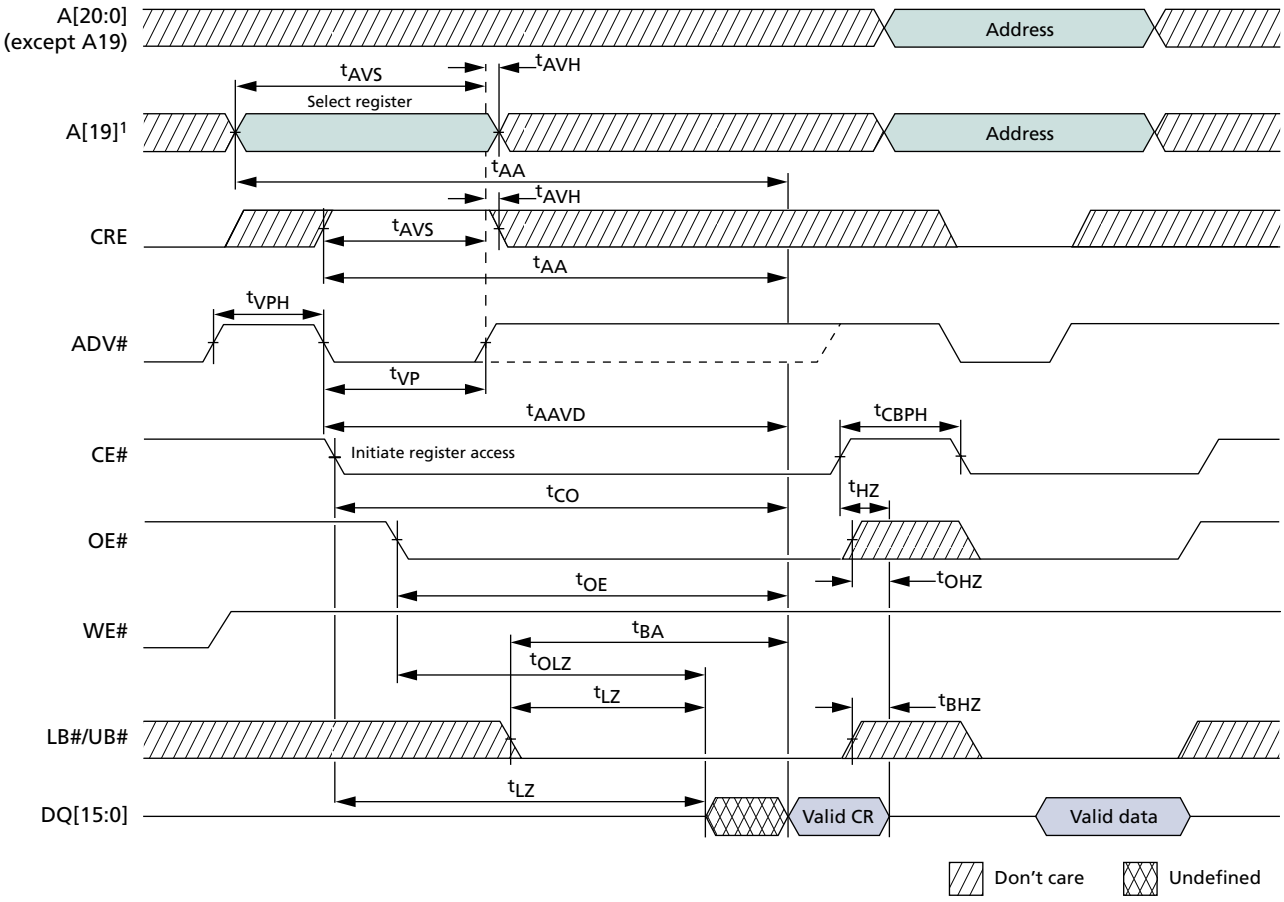
Notes: 1. A19 = LOW to load RCR, HIGH to load BCR.

Figure 21: Synchronous Mode Configuration Register WRITE followed by READ ARRAY Operation



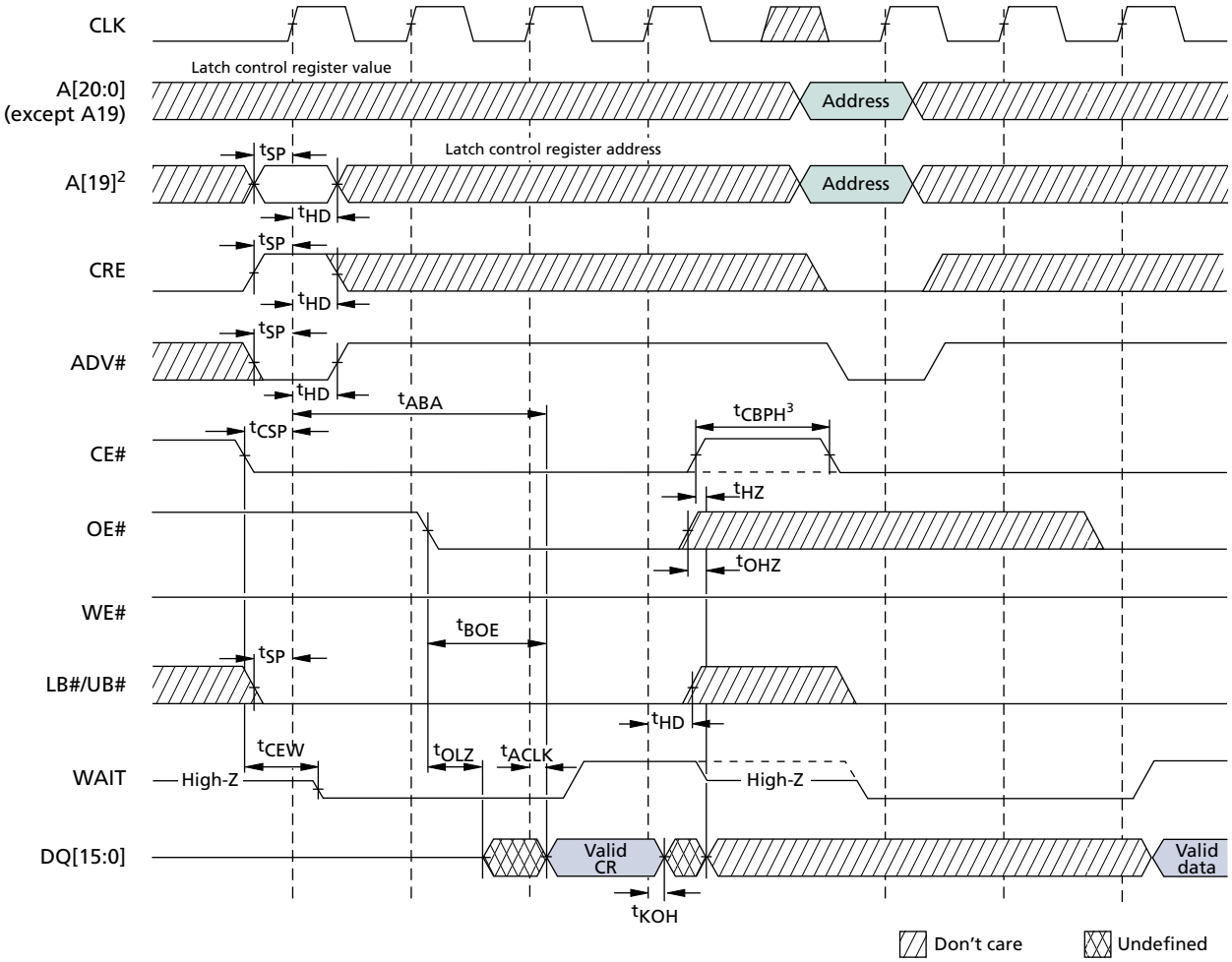
Notes:
1. Nondefault BCR settings for CR WRITE in synchronous mode followed by READ ARRAY operation: Latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.
2. A19 = LOW to load RCR, HIGH to load BCR.
3. CE# must remain LOW to complete a burst-of-one WRITE. WAIT must be monitored—additional WAIT cycles caused by refresh collisions require a corresponding number of additional CE# LOW cycles.

Figure 22: Asynchronous Mode Configuration Register READ followed by READ ARRAY Operation



Notes: 1. A19 = LOW to read RCR, HIGH to read BCR.

Figure 23: Synchronous Mode Configuration Register READ followed by READ ARRAY Operation



Notes:
1. Nondefault BCR settings for synchronous mode register READ followed by READ ARRAY operation: latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.
2. A19 = LOW to read RCR, HIGH to read BCR.
3. CE# must remain LOW to complete a burst-of-one READ. WAIT must be monitored—additional WAIT cycles caused by refresh collisions require a corresponding number of additional CE# LOW cycles.

Software Access

The configuration register can be accessed using a software sequence of asynchronous READ and asynchronous WRITE operations. The contents of the configuration registers can be read or modified using the software sequence.

The configuration registers are loaded using a four-step sequence consisting of two asynchronous READ operations followed by two asynchronous WRITE operations (see Figure 24 on page 24).

The configuration register READ sequence is virtually identical to the WRITE sequence except that an asynchronous READ is performed during the fourth operation (see Figure 25 on page 24). Note that a third READ cycle of the highest address will cancel the software access sequence until a different address is read.

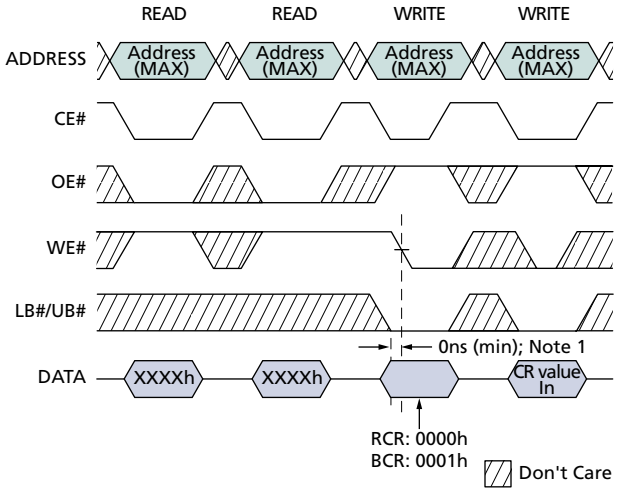
The address used during all READ and WRITE operations is the highest address of the CellularRAM device being accessed (1FFFFFh for 32Mb); the content at this address is not changed by this sequence.

The data value presented during the third operation (WRITE) in the sequence defines whether the BCR or the RCR is to be accessed. If the data is 0000h, the sequence will access the RCR; if the data is 0001h, the sequence will access the BCR. During the fourth operation, DQ[15:0] transfer data into or out of bits 15–0 of the configuration registers.

The use of the software access sequence does not affect the ability to perform the standard (CRE-controlled) method of loading the configuration registers. However, the software nature of this access mechanism eliminates the need for the CRE pin. If the software mechanism is used, the CRE pin can simply be tied to V_{SS}. The port line often used for CRE control purposes is no longer required.

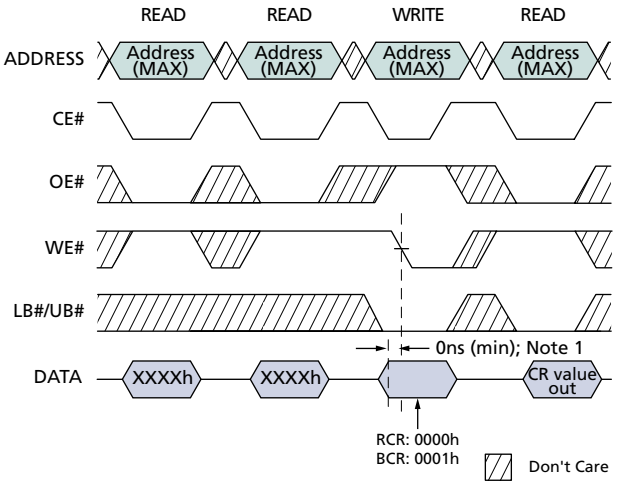
RCR software access should not be used to enter or exit DPD.

Figure 24: Load Configuration Register



Notes: 1. If the data at the falling edge of WE# is not 0000h or 0001h, it is possible that data stored at the highest memory location will be altered.

Figure 25: Read Configuration Register



Notes: 1. If the data at the falling edge of WE# is not 0000h or 0001h, it is possible that data stored at the highest memory location will be altered.

Mobile Memory Solutions

The competitive nature of the mobile marketplace demands periodic design updates to remain cost competitive. Updates provide an opportunity to make software changes, add features, or qualify new memory solutions. They also provide an opportunity to qualify new providers supplying critical components.

When a design change is contemplated, volatile memory is often evaluated to determine if the cost per bit, performance, and/or availability meet the manufacturer's criteria.

An increasing number of designers are searching for more cost-effective solutions than the SRAM used previously for volatile storage.

When an SRAM solution is re-evaluated, two options predominate:

1. Find an alternative to SRAM that demands little or no change to the existing hardware and software.
2. Redesign the application to support an alternative interface.

Micron provides a broad range of mobile memory solutions and frequently works with customers to aid in the selection process.

Choosing the Right Memory for Your Application

The following sections present the advantages and disadvantages of:

- remaining with SRAM
- redesigning to support Mobile DRAM
- changing to PSRAM or CellularRAM.

Asynchronous SRAM

SRAM designs incorporate a 4T or 6T core design for memory storage. These designs are typically low power and provide READ and WRITE performance of ≈70ns. SRAM devices are available with either 1.8V or 3.0V core supplies.

Table 5: Asynchronous SRAM Advantages and Disadvantages

Attribute	Which means
Advantages	
Proven interface	No redesign time, expense, or resource allocation
Low-power characteristics	Reduced power consumption
No controller-driven refresh requirement to retain memory content	Reduced controller overhead; retained content
Disadvantages	
4T or 6T physical size	Larger die than competing technologies
Larger die size	Higher cost
SRAM supply uncertain in required densities	Higher cost, and required parts are potentially unavailable

Mobile DRAM

Mobile DRAM incorporates a 1T/1C memory cell. It is typically available in 64Mb and higher densities.

Table 6: Mobile DRAM Advantages and Disadvantages

Attribute	Which means
Advantages	
Higher densities are widely available	Cost containment based on supply and demand
Conforms to JEDEC standards	Greater opportunity for multiple sourcing
Provides very high bandwidth	Excellent support for non-random access execution
Disadvantages	
Interface is DRAM-specific	Requires memory controller redesign
Supply uncertain in lower densities	Potential higher cost, and required parts are potentially unavailable
Higher power requirements	Less appeal for the end user
Bandwidth penalty for short burst-length random access	Reduced concurrent functionality

CellularRAM and PSRAM

CellularRAM and PSRAM incorporate either a 1T/1C or a 2T/2C cell architecture, as used in DRAM-based designs. Micron CellularRAM PSRAM? designs comply with the CellularRAM Workgroup specifications.

Table 7: CellularRAM Advantages and Disadvantages

Attribute	Which means
Advantages	
Drop-in compatible with async SRAM designs	Easy replacement at lower cost
Widely available in SRAM-compatible densities	No availability concerns
Conforms to CellularRAM Workgroup specifications	Greater opportunity for multiple sourcing
SRAM-compatible access speeds	Drop-in replacement meets or exceeds SRAM speeds
Disadvantages	
Slightly higher active and standby power consumption	Slight reduction in power efficiency

Replacing Async SRAM with PSRAM or CellularRAM Async/Page Devices

Today's consumer is inundated with mobile applications that enhance his or her day-to-day experience. The wise consumer will shop (usually via a portable, Web-based application) for the best price on the latest must-have application. Designers of mobile applications must take care to select a long-term, reliable, and cost-effective memory solution for each application. Micron can help by replacing expensive SRAM with drop-in-compatible PSRAM devices.

When a Micron PSRAM is used to replace an SRAM, the operating voltages and interface connections should be examined first to see if the PSRAM will work for a given application.

SRAM vs. PSRAM Features

Various manufacturers produce SRAM devices that have either a single- or dual-CE# interface, which provides different feature support. All SRAM devices have an asynchronous interface with the memory controller and offer READ, WRITE, and data-retention modes.

Table 8 illustrates that PSRAM provides a drop-in compatible replacement for SRAM in applications that require a 1.8V core supply, operating at 70ns, and packaged in a 48-ball BGA. To replace other configurations of SRAM with PSRAM may require more design effort, but may well be worth the effort because of the low-power features available with Micron PSRAM.

Table 8: SRAM and PSRAM Feature Differences

Function		SRAM		Micron PSRAM	Notes
		Single CE#	Dual CE#		
Voltage	Core	Various	Various	1.70–1.95V	I/O voltage must match
	I/O	1.65–1.95V	1.65–1.95V	1.70–3.30V	
Operation mode	Async READ/WRITE	Yes	Yes	Yes	
	Access time	70ns	70ns	70ns	
	Page	No	No	Yes	
Low-power support	Hardware control	Yes	Yes	Yes	
	Software control	No	No	Yes	
Package		TSOP/FBGA	TSOP/FBGA	48-ball VFBGA	

Micron PSRAM devices target similar applications as SRAM, but offer the additional value of compatibility with the CellularRAM Workgroup specification—a common, published specification that allows designers to consider multiple part vendors.

These devices can support a high-speed memory interface while meeting the additional requirement for low-power operating modes.

Micron PSRAM device features include:

- 4Mb–128Mb densities
- Small-footprint VFBGA package or known-good die (KGD)
- Burst NOR-Flash-compatible interface
- Asynchronous, page, and high-speed (up to 133 MHz) burst interface
- Low-power options including partial-array refresh (PAR), low standby current, and deep power-down (DPD)
- Temperature-compensated refresh (TCR)
- Hidden refresh control

This section compares Micron's async/page 16Mb, CellularRAM 1.0-compliant device (MT45W1MW16PD) with two SRAM devices with differing CE# interfaces:

- Single-CE#: Cypress 4Mb CY62147DV18
- Dual-CE#: Samsung 16Mb K6F1616R6C

Power Supply Considerations

SRAM devices provide a number of power supply options, depending on manufacturer and customer requirements. The primary options are:

- Single 1.8V core power supply
- Single 3.0V core power supply
- Separate core and I/O supplies

Micron PSRAM densities from 16Mb to 128Mb support a 1.8V core supply with the option to run the I/O voltage at either 1.8V or 3.0V. The 4Mb and 8Mb Micron PSRAM devices also support a 2.7V to 3.6V core voltage range.

Addition of the 3.0V core support should allow more flexibility when determining the transitional path for a design. An overview of these options is shown in Table 9.

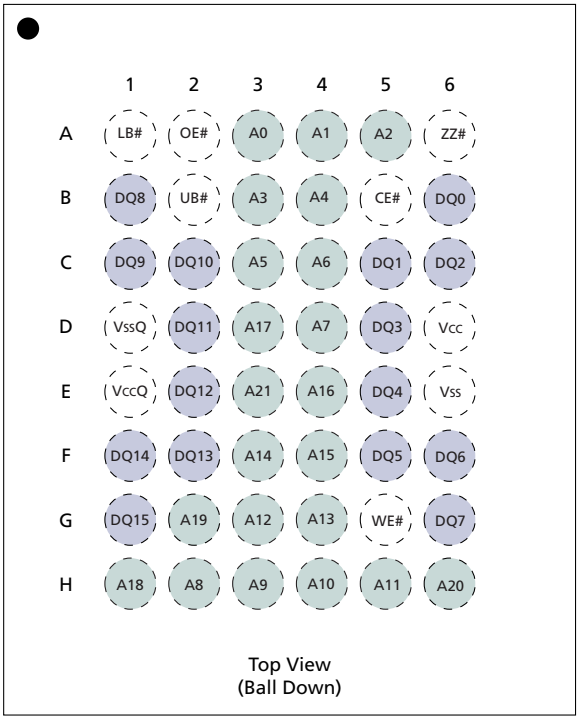
Table 9: Power Supply Options

SRAM Device Supply		Micron Device Supply		Notes
Core (VCC)	I/O (VCCQ)	Core (VCC)	I/O (VCCQ)	
1.65–1.95V	1.65–1.95V	1.70–1.95V	1.70–1.95V	1
2.7–3.3V	2.7–3.3V	1.70–1.95V	2.7–3.3V	2
2.7–3.3V	1.65–1.95V	1.70–1.95V	1.70–1.95V	3

Notes:
1. No change to power supply connections.
2. No change to the power supply needed for 4Mb and 8Mb designs; 16Mb to 128Mb densities require a supply change.
3. Reduce core voltage.

The supply differences noted in Table 9 require the system design to accommodate different supply voltages on the PSRAM device VCC balls. See Figure 26 on page 29 for the device ball assignments.

Figure 26: Micron 48-Ball VFBGA Ball Assignments



SRAM devices provide the option to reduce the core supply to a lower data-retention voltage without impacting the device's data storage ability. This reduced voltage is normally specified as 1.0V. For PSRAM devices, V_{CC} must not drop below V_{CC} (MIN) to ensure correct operation of the device interface and data storage.

Both types of devices require an initialization period, after power is applied and stable, and prior to the first access. For SRAM devices, the initialization period is ^{t}RC (READ cycle time), whereas the PSRAM device requires a longer period, ^{t}PU. Although there is a timing difference—70ns (^{t}RC) vs. 150µs (^{t}PU)—the inherent system delay until the first access makes this difference irrelevant.

Memory Controller Interface

An SRAM memory controller interface can also control PSRAM devices.

The basic control signals—WE#, OE#, and CE#—are the same for both the single- and dual-CE# SRAM and PSRAM devices. However, the control signals—CE2 (dual-chip select SRAM) and ZZ# (PSRAM device)—are different. These differences are listed in Table 10.

Like SRAM, CellularRAM and PSRAM support asynchronous READ and WRITE operations.

Table 10: Control Signal (CE2/ZZ#) Differences

Device	Signal	Notes
Micron PSRAM memory	ZZ#	Used to control PAR/DPD[1]
Dual-CE# SRAM	CE2	Used to control entry to data retention state
Single-CE# SRAM	NC	Low power achieved using supply voltage alone

Notes: 1. PAR/DPD can be also controlled via software access.

Low-Power Settings

Both the SRAM and PSRAM devices support options to reduce current consumption; however, different options are available per device (see Table 11).

Table 11: Reduced-Current Options

Device	Low-Power Current Mode	Enabled by
Single-CE# SRAM	Standby	CE# = HIGH with nominal V_{CC}
	Lower data retention	CE# = HIGH with data retention V_{CC}
Dual-CE# SRAM	Standby	CE1# and CE2 = HIGH
		CE2 = LOW with nominal V_{CC}
	Lower data retention	CE1# = HIGH with data retention V_{CC}
PSRAM Memory	PAR or DPD (ZZ# option)	CE# = HIGH; ZZ# = LOW with nominal V_{CC}
	PAR (software access option)	CE# and ZZ# = HIGH with nominal V_{CC}

Low-Power Migration Options

The ability of SRAM to enter a lower-power standby mode similar to that of PSRAM memory varies by device.

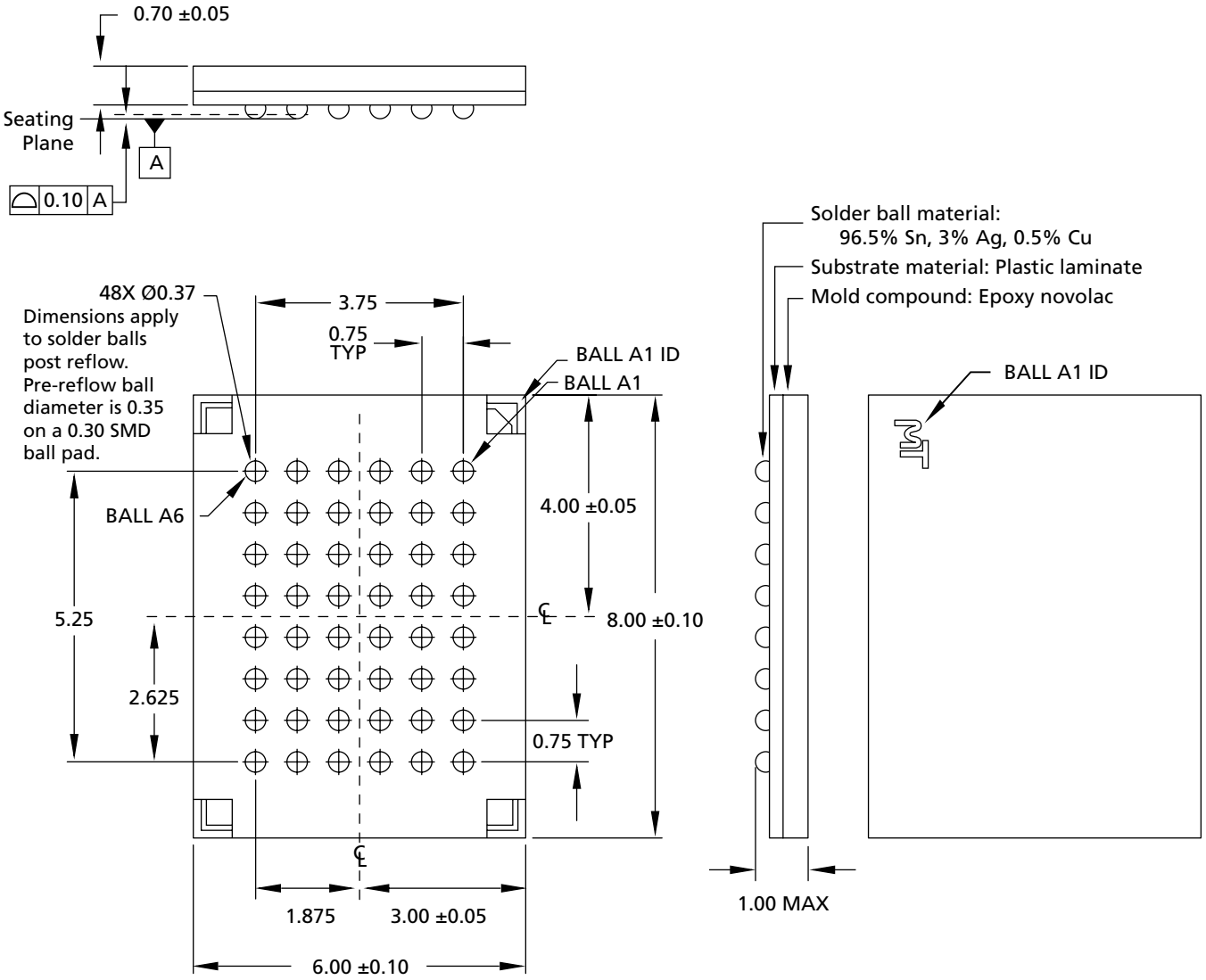
- Single-CE# SRAM lower-power standby currents require either:
  - Configuration register control via software access, or
  - The ability to control the ZZ# pin.
- Dual-CE# SRAM lower-power standby currents require either:
  - CR control via software access, or
  - The ability to change the memory controller output that controls the CE2 pin.

Package Considerations

Two package characteristics must be considered when making a PCB change to accommodate CellularRAM or PSRAM memory:

1. Package size and type: SRAM devices come in TSOP and 48-ball VBFGA packages. (Micron CellularRAM and PSRAM async/page devices are also available in a 48-ball, 0.75mm-ball-pitch VFBGA package.)
2. Ball/pin composition: The market is moving to lead-free balls/pins, which will necessitate manufacturing process changes for some designs. See Figure 27 for PSRAM package information.

Figure 27: 48-ball VFBGA Package Drawing



Notes:
1. All dimensions is in millimeters.
2. Green packaging is available upon request.

Summary

Micron CellularRAM and PSRAM devices provide a wide variety of interface and performance options for volatile memory in the mobile marketplace.

PSRAM and CellularRAM can be used as drop-in replacements for SRAM, or as feature-rich alternatives providing low-power, high-bandwidth performance.

The benefits of switching from SRAM to PSRAM for volatile memory include:

- Compatibility with previous-generation SRAM and future-generation burst NOR Flash memory
- Software access to the configuration register
- Multiple vendors (via the standardized specification)
- High-speed interface with several low-power modes

Micron PSRAM or CellularRAM should be considered viable options for replacing asynchronous SRAM in new or existing designs. The low-power features of Micron CellularRAM offer added flexibility in meeting the requirements of mobile applications.

Factors influencing tradeoffs in a choice between PSRAM/CellularRAM and Mobile DRAM exceed the scope of this document.

For further technical assistance, including technical notes and customer service notes, visit Micron's Web site, www.micron.com/products/psram, or e-mail *psramsupport@micron.com*.

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