Intel® 875P Chipset Memory Configuration Guide

White Paper

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Revision History

Revision Number	Description	Revision Date
-001	Initial Release.	

1 Overview

The Intel® 875P chipset Memory Controller Hub (MCH) is Intel's first dual-channel DDR Memory Controller Hub with Performance Acceleration Technology (PAT) for the Intel® Pentium® 4 processor. The 875P MCH is optimized to provide maximum performance when combined with DDR400 and a Pentium 4 processor with 800 MHz front-side bus. The 875P MCH is designed for maximum flexibility with support of single-channel, virtual single-channel, dual-channel, and dual-channel dynamic mode memory populations.

This document details the 875P chipset MCH memory configurations and performance. It is intended for a technical audience interested in learning about 875P MCH memory population rules and how to populate memory to provide optimal performance

1.1 Memory Technology Supported

The MCH supports DDR266 (PC 2100), DDR333 (PC 2700), DDR400 (PC 3200)–both ECC and non-ECC DIMMS.

Table 1. Memory Technology Support

DRAM Technology	Smallest Increments	Largest Increments	Maximum Capacity (4 DS DIMMs)
128 Mb	64 MB	256 MB	1024 MB
256 Mb	128 MB	512 MB	2048 MB
512 Mb	256 MB	1024 MB	4096 MB

1.2 Illegal Configurations

The following configurations are not valid:

- 64-Mb and 1-Gb Memory Technology
- x4,x32 DIMMS
- Double Sided X16 DIMMS
- Registered DIMMS.

1.3 Valid Front-Side Bus and Memory Speeds

Table 2. Valid Memory Configurations

FSB	DRAM Data Rate	DRAM Type	Single Channel Peak Bandwidth	Dual Channel Peak
400 MHz	266 MT/s	DDR1-DRAM	2.1 GB/s	4.2 GB/s
533 MHz	266 MT/s	DDR1-DRAM	2.1 GB/s	4.2 GB/s
800 MHz	266 MT/s	DDR1-DRAM	2.1 GB/s	4.2 GB/s
533 MHz	333 MT/s	DDR1-DRAM	2.7 GB/s	5.4 GB/s
800 MHz	320 MT/s	DDR1-DRAM	2.65 GB/s	5.3 GB/s
800 MHz	400 MT/s	DDR1-DRAM	3.2 GB/s	6.4 GB/s

1.4 ECC

The MCH supports single-bit Error Correcting Code (or Error Checking and Correcting) on the main memory interface. The MCH generates an 8-bit code word for each 64-bit QWord of memory. Since the code word covers a full QWord, writes of less than a QWord require a read-merge-write operation. Consider a DWord write to memory. In this case, when in ECC mode, the MCH will read the QWord where the addressed DWord will be written, merge in the new DWord, generate a code covering the new QWord and finally write the entire QWord and code back to memory. Any correctable (single-bit) errors detected during the initial QWord read are corrected before merging the new DWord.

1.5 Performance Acceleration Technology (PAT)

PAT is unique to the 875P chipset. Advanced manufacturing and test technology ensures the ability to implement enhanced logic design. These enhancements allow performance improvements of two clock cycles. These include one clock improvement to memory access and one clock improvement in DRAM chip select. These changes are internal to the chipset, allowing the external interfaces to run at standard specifications, while accelerating the internal chipset logic.

2 Intel® 875P Chipset Memory Operating Modes

The MCH supports the following modes of operation:

1. Virtual Single-Channel or Single-Channel Mode (VSC).
    a. Populate Channel A only
    b. Populate Channel B Only
    c. Populate both Channel A and B.
2. Dual-Channel Lock Step mode (DS).
    a. DS Linear Mode.

The 875P chipset also supports a special mode of addressing – dynamic addressing mode.

All the above-mentioned modes can be enabled with/without dynamic paging mode.

The following table summarizes the different operating modes MCH memory controller can operate.

Table 3. MCH Memory Controller Operating Modes

Mode	Channel	Dynamic Mode	Non-Dynamic Mode
VSC Mode	Channel A Only	Yes(1)	Yes
	Channel B Only	Yes(1)	Yes
	Both Channel A & B	Yes(1)	Yes
DS Mode	Linear	Yes	Yes

NOTES:
1. Special cases – need to meet few requirements discussed below.

2.1 Dynamic Paging Mode

When the MCH is configured to operate in this mode, Front-Side Bus (FSB) to Memory Bus address mapping undergoes a significant change compared to that of in a linear operating mode (normal operating mode). In non-dynamic paging mode, the Rank selection (Rank or ROW indicates the side of a DIMM) via chip select signals, is done based on the size of the ROW. For example, for a 512-Mb 16MX8X4b will have a ROW size of 512 MB, selected by CS0#, and only four open pages can be maintained for the full 512 MB. This will lower the memory performance (increases READ latencies) if most of the memory cycles are targeted to that single ROW resulting in opening and closing of accessed pages in that ROW.

Consider a 256 MB x16, 8-KB page size memory module – 128 MB in Rank0, and 128 MB in Rank1. When MCH was configured under non-dynamic mode operation, A[13] and A[14] of the PSB address was used for memory bank selection. Hence the bank changes on every 8-KB boundary. Example:

0 KB – (8 K – 1)B ➔ Bank 0	32 KB – (40 K – 1)B ➔ Bank 0
8 KB – (16 K – 1)B ➔ Bank 1	40 KB – (48 K – 1)B ➔ Bank 1
16 KB – (24 K – 1)B ➔ Bank 2	48 KB – (56 K – 1)B ➔ Bank 2
24 KB – (32 K – 1)B ➔ Bank 3	56 KB – (64 K – 1)B ➔ Bank 3

And this sequence repeated for the entire Rank (128 MB) on the DIMM. Since only one page can be opened per bank (four pages per ROW or Rank). There will be a larger overhead when the memory accesses are switching between banks causing the memory controller to close and open multiple pages. To minimize the overhead of opening/closing pages in memory banks, FSB address bit A[18] was used in place of A[14] for bank switching. By doing so, the Bank pairs switch for every 256 KB. In this mode the bank address change on 8-KB boundary but alternates between two banks for every 256 KB as shown below.

0 KB – (8 K – 1)B ➔ Bank 0	32 KB – (40 K – 1)B ➔ Bank 0
8 KB – (16 K – 1)B ➔ Bank 1	40 KB – (48 K – 1)B ➔ Bank 1
16 KB – (24 K – 1)B ➔ Bank 0	48 KB – (56 K – 1)B ➔ Bank 0
24 KB – (32 K – 1)B ➔ Bank 1	56 KB – (64 K – 1)B ➔ Bank 1

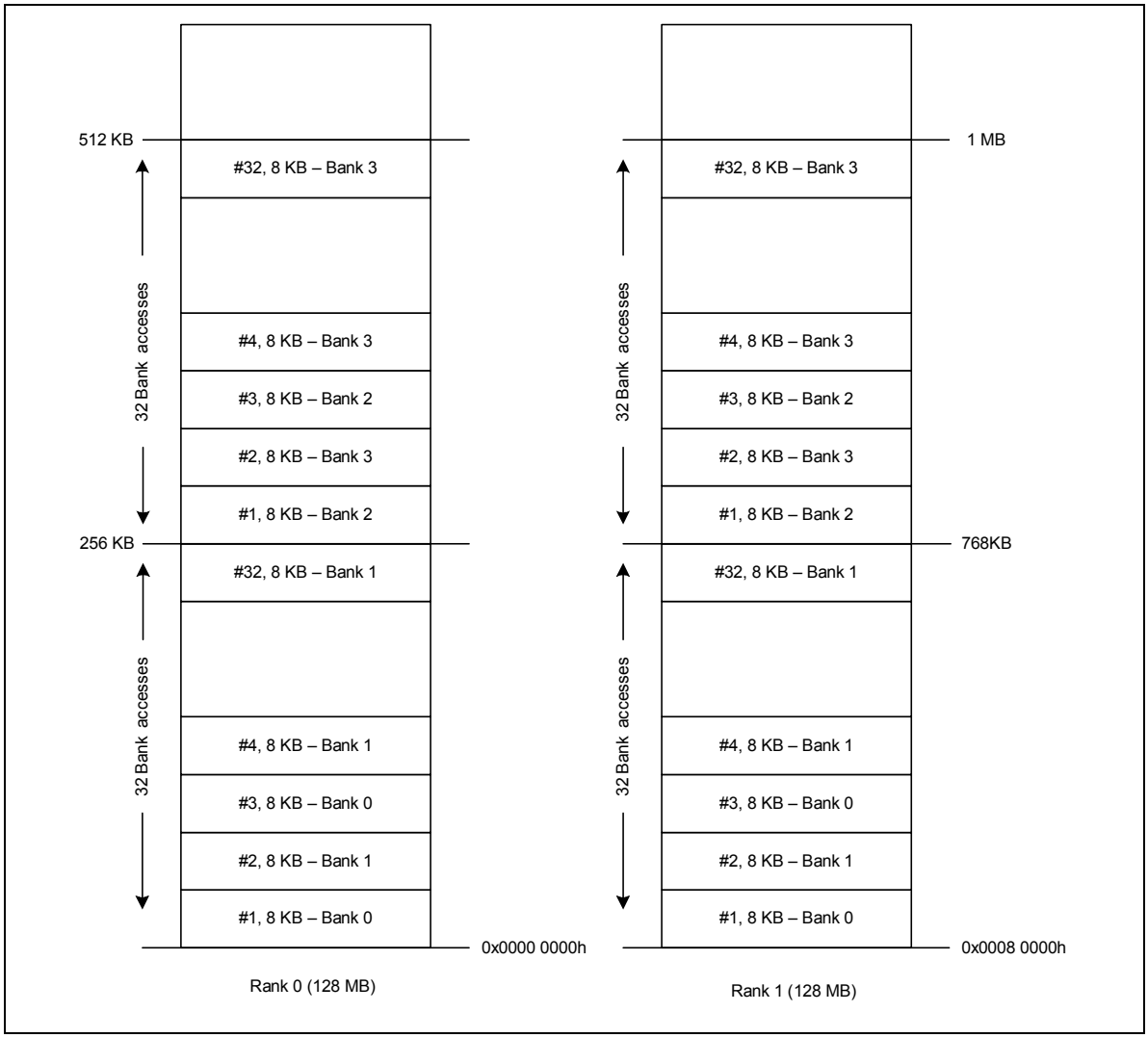
This pattern follows for the first 256 KB – Switching between Bank 0 and 1 for every 8-KB offsets. The bank organization for the next 256 KB will be organized as shown below – switching between Bank 2 and 3 for every 8-KB offsets.

256 KB – (264 K – 1)B ➔ Bank 2	288 KB – (296 K – 1)B ➔ Bank 2
264 KB – (272 K – 1)B ➔ Bank 3	296 KB – (304 K – 1)B ➔ Bank 3
272 KB – (280 K – 1)B ➔ Bank 2	304 KB – (312 K – 1)B ➔ Bank 2
280 KB – (288 K – 1)B ➔ Bank 3	312 KB – (320 K – 1)B ➔ Bank 3

Further enhancing the addressing capabilities, FSB address bits A[19] and A[20] are used for Rank selection on the memory channel. For a SS DIMM populated in only one slot, these bits are not used for Rank selection, since there will be only one rank. For a DS DIMM in only one slot or two SS DIMMs in both the slots, A[19] will be used for Rank selection between Rank 0 and Rank 1 and A[20] will be the regular row address bit on the memory bus. Similarly for two DS DIMMs populated in both the channels A[19] and A[20] are used for Rank selection – Rank 0, Rank 1, Rank 2 and Rank 3.

In this example, the memory configuration was DS DIMM, hence FSB address bit A[19] will be used for Rank selection between Rank 0 and 1. By doing this the Rank switching was done for every 512 KB, which under non-dynamic mode used to be for 128 MB. The advantage lies in having eight open pages (four per Rank) for every 512 KB, compared to that of having four open pages for 128 MB. Figure 1, below, shows the bank/rank organization in dynamic mode.

Figure 1. Bank/Rank Organization of DS DIMM in Dynamic Mode



2.2 Single-Channel and Virtual Single-Channel Mode

If either only channel A or only channel B is populated then the MCH is set to operate in single-channel mode. Data will be accessed in chunks of 64 bits (8 B) from the memory channels. If both the channels are populated with uneven memory (DIMMs) see Figure 2, then the MCH defaults to virtual single-channel mode. Virtual single-channel mode occurs when more than one channel is populated with memory, but because either non-matched DIMMS or three identical DIMMs being populated, the MCH will treat both channels as if they were a single channel. Even with similar memory configuration on both the channels, it is possible for the MCH to operate in single-channel mode when populated oddly as shown in Figure 3.

The MCH behaves identically in both single-channel and virtual single-channel modes. In this mode of operation, the populated DIMMs configuration can be identical or completely different. In addition, for SC mode, not all the slots need to be populated. For example, populating only one

DIMM in channel A is a valid configuration for SC mode. Likewise, in VSC mode odd number of slots can be populated. For dynamic mode operation, the requirement is to have an even number or ROWs (side of the DIMM) populated. In SC, dynamic mode of operation can be enabled with one Single Sided (SS), two SS or two Double Sided (DS). For VSC mode, both the channels should have identical ROW structure.

Figure 2. Single-Channel and Virtual Single-Channel Population

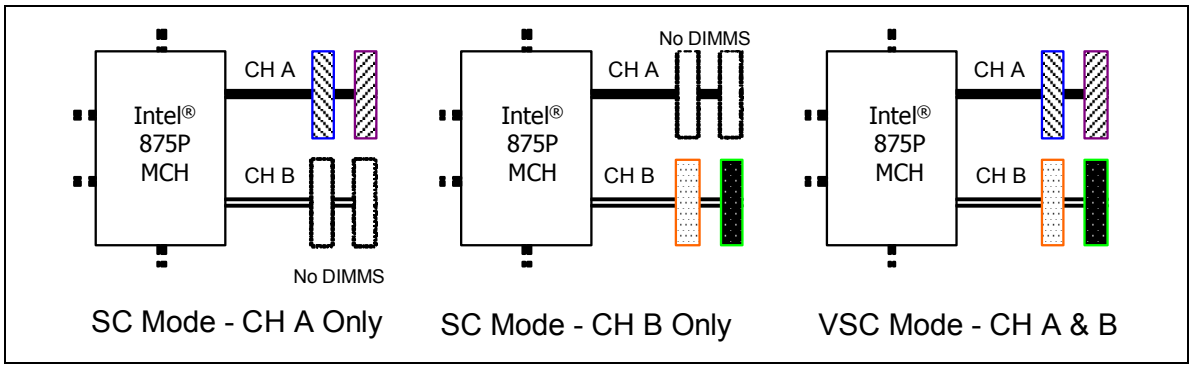
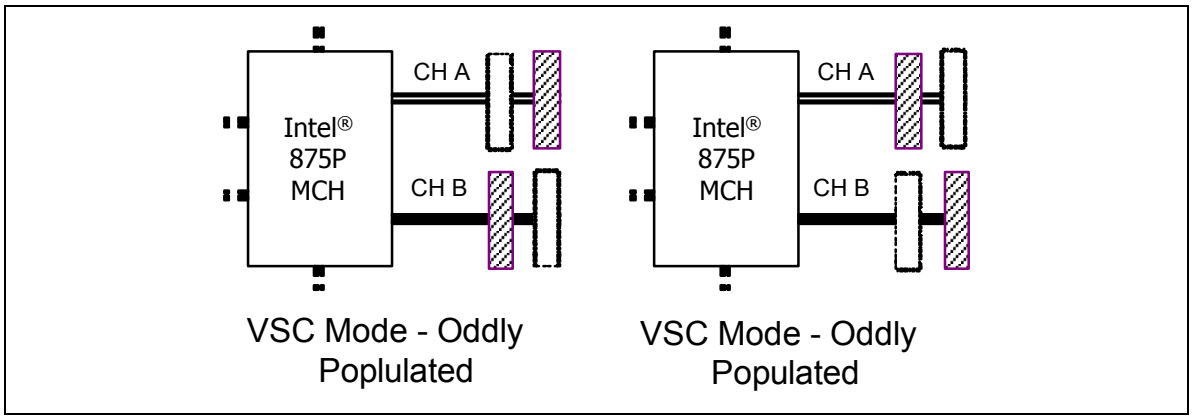


Figure 3. Single-Channel Oddly Populated Identical DIMMS



2.3 Dual-Channel Memory Configurations

In this mode of operation the data accessed by the MCH from the memory will be in chunks of 128 bits (16 B) from both the channels, hence the bandwidth in this case will be double that of in SC mode. FSB address bit 3 will dictate from which channel the data should be fetched.

Figure 4. Dynamic Mode with Two Identical DIMMS

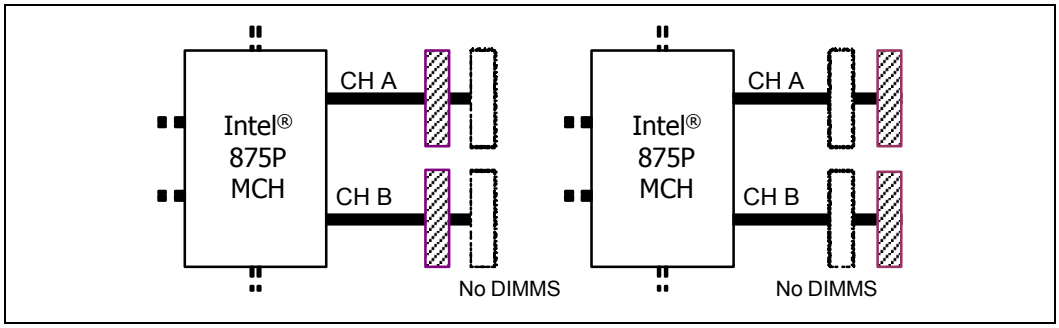


Figure 5. Dynamic Mode with Four Identical DIMMS

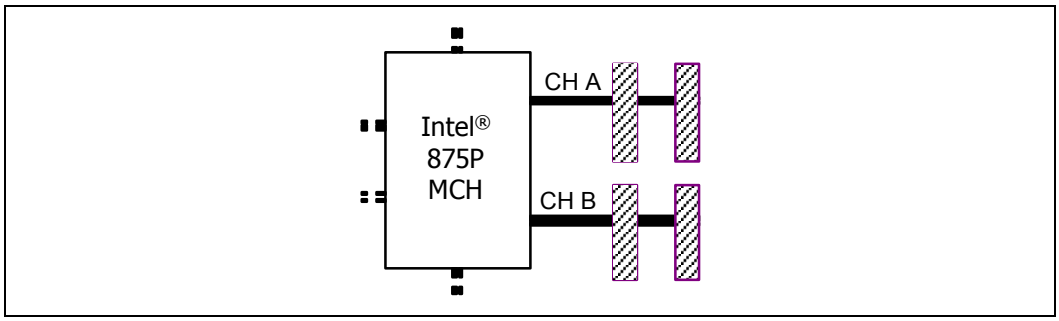
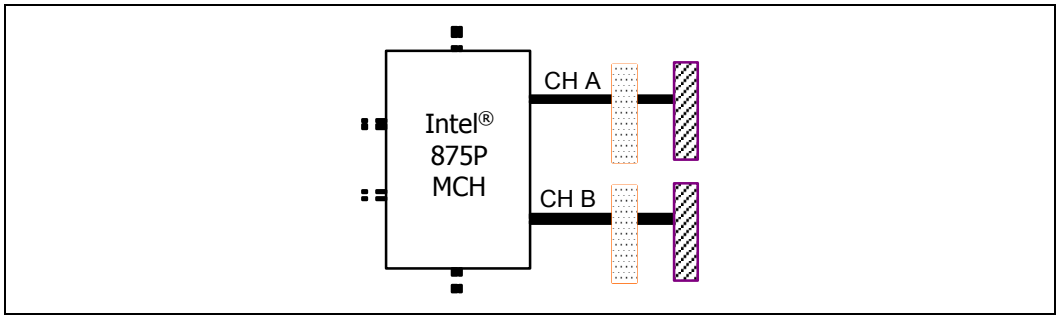


Figure 6. Normal Mode with Two Different Pairs of Matched DIMMS



NOTES: DIMMS matched in pairs.

2.4 Mixed DDR Speeds

The 875 MCH will accept mixed DDR speed population, assuming the SPD on the DIMMS are programmed with the correct information and the BIOS is programmed as outlined in Intel's BIOS reference code.

For example, a DDR400 DIMM installed with a DDR333 DIMM should run at 333 MHz. The DDR400 DIMM should downshift to DDR 333 timings, thus allowing the system to run at 333 MHz speeds. The DDR400 DIMM will only downshift to DDR333, if the timings for DDR333 are programmed in the DDR400 DIMM's SPD.

CAS, RAS, Precharge, will default to the slowest setting, assuming the DIMM SPD is programmed with the proper settings.

3 Performance Tuning

For the 875 chipset, optimal population of DIMMS enables the highest performance. Performance is as follows, from highest to lowest:

For DDR400:

Table 4. DDR400 Performance Configurations

DDR Speed	DIMMS	Ranks per DIMM	Mode	SC or DC	Performance
400 MHz	4	2	Dynamic	Dual Channel	1
400 MHz	2	2	Dynamic	Dual Channel	2
400 MHz	4	1	Dynamic	Dual Channel	2
400 MHz	2	1	Dynamic	Dual Channel	3
400 MHz	4	any	Normal	Dual Channel	4
400 MHz	any	2	Dynamic	Single Channel	5
400 MHz	any	1	Dynamic	Single Channel	6
400 MHz	Any	Any	Normal	Single Channel	7

For DDR266/DDR333:

Table 5. DDR266/DDR333 Performance Configurations

DDR Speed	DIMMS	Ranks per DIMM	Mode	SC or DC	Performance
266/333 MHz	2	2	Dynamic	Dual Channel	1
266/333 MHz	4	1	Dynamic	Dual Channel	1
266/333 MHz	2	1	Dynamic	Dual Channel	2
266/333 MHz	4	2	Dynamic	Dual Channel	3
266/333 MHz	Any	any	Normal	Dual Channel	4
266/333 MHz	2 (1 in each channel)	any	Dynamic	Single Channel	5
266/333 MHz	1	any	Dynamic	Single Channel	5
266/333 MHz	Any	any	Dynamic	Single Channel	6
266/333 MHz	Any	Any	Normal	Single Channel	7

NOTES: Single-channel dynamic mode is also possible with either a single DIMM population or population of two identical DIMMS in the same channel.

NOTES: Ranks per DIMM (1 Rank is a single-sided DIMM, 2 Ranks is a double-sided DIMM).