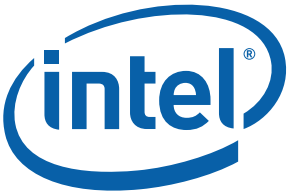
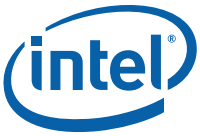


Dual-Core Intel® Xeon® Processor LV 5138 in Embedded Applications

Thermal/Mechanical Design Guidelines

September 2006

Order Number: 315225-001US



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Contents

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Tables

Revision History

Reference Number	Description	Date
001	• Initial release.	September 2006

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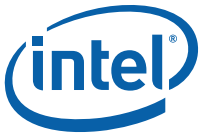

1.0 Introduction

1.1 Objective

This document describes the reference thermal solution and design parameters required for Dual-Core Intel® Xeon® Processor LV 5138 in embedded applications. It is also the intent of this document to comprehend and demonstrate the processor cooling solution features and requirements. Furthermore, this document provides an understanding of the processor thermal characteristics, and discusses guidelines for meeting the thermal requirements imposed on the entire life of the processor. The thermal/mechanical solution described in this document are intended to aid component and system designers in the development and evaluation of processor compatible thermal/mechanical solutions.

1.2 Scope

The thermal/mechanical solutions described in this document pertain only to a solution(s) intended for use with the Dual-Core Intel® Xeon® Processor LV 5138 in AdvancedTCA* form factors systems. This document contains the mechanical and thermal requirements of the processor cooling solution. In case of conflict, the data in the *Dual-Core Intel® Xeon® Processor 5100 Series Datasheet* supersedes any data in this document. Additional information is provided as a reference in the appendices.

1.3 References

Material and concepts available in the following documents may be beneficial when reading this document.

Table 1. Reference Documents (Sheet 1 of 2)

Document	Comment
European Blue Angel Recycling Standards	http://www.blauer-engel.de
Intel® Xeon® Processor Family Thermal Test Vehicle User's Guide	See Note following table
Dual-Core Intel® Xeon® Processor 5100 Series Thermal/Mechanical Design Guide	See Note following table
Dual-Core Intel® Xeon® Processor 5100 Series Thermal/Mechanical Design Guidelines	http://www.intel.com/design/xeon/guides/313357.htm
LGA771 Socket Mechanical Design Guide	See Note following table
PECI Feature Set Overview	See Note following table
Platform Environment Control Interface (PECI) Specification	See Note following table
T_{RISE} Reduction Guidelines for Rack Servers and Workstations	See Note following table
Dual-Core Intel® Xeon® Processor 5100 Series Datasheet	*Available electronically*

Note: Contact your Intel field sales representative for the latest revision and order number of this document.

Table 1. Reference Documents (Sheet 2 of 2)

Document	Comment
Dual-Core Intel® Xeon® Processor 5100 Series Enabled Components Mechanical Models (in IGES and ProE* format)	*Available electronically*
Dual-Core Intel® Xeon® Processor 5100 Series Enabled Components Thermal Models (in Flotherm* and Icepak*)	Available electronically
Dual-Core Intel® Xeon® Processor 5100 Series Mechanical Models (in IGES and ProE* format)	Available electronically
Dual-Core Intel® Xeon® Processor 5100 Series Thermal Models (in Flotherm* and Icepak*)	Available electronically
Thin Electronics Bay Specification (A Server System Infrastructure [SSI] Specification for Rack Optimized Servers)	www.ssiforum.com

Note: Contact your Intel field sales representative for the latest revision and order number of this document.

1.4 Definition of Terms

Table 2. Terms and Descriptions (Sheet 1 of 2)

Term	Description
Bypass	Bypass is the area between a passive heatsink and any object that can act to form a duct. For this example, it can be expressed as a dimension away from the outside dimension of the fins to the nearest surface.
Digital Thermal Sensor	Digital Thermal Sensor replaces the T_{DIODE} in previous products and uses the same sensor as the PROCHOT# sensor to indicate the on-die temperature. The temperature value represents the number of degrees below the TCC activation temperature.
FMB	Flexible Motherboard Guideline: an estimate of the maximum value of a processor specification over certain time periods. System designers should meet the FMB values to ensure their systems are compatible with future processor releases.
FSC	Fan Speed Control
IHS	Integrated Heat Spreader: a component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
LGA771 Socket	The Dual-Core Intel® Xeon® Processor 5100 Series interface to the baseboard through this surface mount, 771 Land socket. See the *LGA771 Socket Mechanical Design Guide* for details regarding this socket.
NEBS	Network Equipment Building Systems. Family of documents that implement directives from the Telecommunications Act of 1996 relative to industry wide general requirements for telecommunications and customer premise equipment.
P_{MAX}	The maximum power dissipated by a semiconductor component.
PECI	A proprietary one-wire bus interface that provides a communication channel between Intel processor and chipset components to external thermal monitoring devices, for use in fan speed control. PECI communicates readings from the processor's Digital Thermal Sensor. PECI replaces the thermal diode available in previous processors.
Ψ_{CA}	Case-to-ambient thermal characterization parameter (psi). A measure of thermal solution performance using total package power. Defined as $(T_{CASE} - T_{LA})$ / Total Package Power. Heat source should always be specified for Ψ measurements.
Ψ_{CS}	Case-to-sink thermal characterization parameter. A measure of thermal interface material performance using total package power. Defined as $(T_{CASE} - T_S)$ / Total Package Power.
Ψ_{SA}	Sink-to-ambient thermal characterization parameter. A measure of heatsink thermal performance using total package power. Defined as $(T_S - T_{LA})$ / Total Package Power.
T_{CASE}	The case temperature of the processor, measured at the geometric center of the topside of the IHS.
$T_{CASE-MAX}$	The maximum case temperature as specified in a component specification.

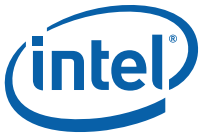

Table 2. Terms and Descriptions (Sheet 2 of 2)

Term	Description
TCC	Thermal Control Circuit: Thermal monitor uses the TCC to reduce the die temperature by using clock modulation and/or operating frequency and input voltage adjustment when the die temperature is very near its operating limits.
$T_{CONTROL}$	A processor unique value for use in fan speed control mechanisms. $T_{CONTROL}$ is a temperature specification based on a temperature reading from the processor's Digital Thermal Sensor. $T_{CONTROL}$ can be described as a trigger point for fan speed control implementation. $T_{CONTROL} = -T_{OFFSET}$.
T_{OFFSET}	An offset value from the TCC activation temperature value specified in the processor datasheet and $T_{CONTROL} = -T_{OFFSET}$. This value is programmed into each processor during manufacturing and can be obtained by reading the IA_32_TEMPERATURE_TARGET MSR. This is a static and a unique value. Ask your field sales engineer for further details.
TDP	Thermal Design Power: Thermal solution should be designed to dissipate this target power level. TDP is not the maximum power that the processor can dissipate.
Thermal Monitor	A feature on the processor that can keep the processor's die temperature within factory specifications under normal operating conditions, and with a thermal solution that satisfies the processor thermal profile specification.
Thermal Profile	Line that defines case temperature specification of a processor at a given power level.
TIM	Thermal Interface Material: The thermally conductive compound between the heatsink and the processor case. This material fills the air gaps and voids, and enhances the transfer of the heat from the processor case to the heatsink.
T_{LA}	The measured ambient temperature locally surrounding the processor. The ambient temperature should be measured just upstream of a passive heatsink or at the fan inlet for an active heatsink.
T_{SA}	The system ambient air temperature external to a system chassis. This temperature is usually measured at the chassis air inlets.
U	A unit of measure used to define server rack spacing height. 1U is equal to 1.75 in, 2U equals 3.50 in, etc.

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2.0 Thermal/Mechanical Reference Design

This chapter describes the thermal/mechanical reference design for Dual-Core Intel® Xeon® Processor LV 5138. These processors are the lower speed SKUs which support a 1066 MHz Front Side Bus (FSB). The processor is targeted for the AdvancedTCA* form factor.

2.1 Mechanical Requirements

The mechanical performance of the processor cooling solution must satisfy the requirements described in this section.

2.1.1 Processor Mechanical Parameters

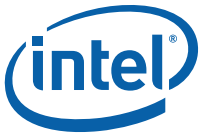
Table 3. Processor Mechanical Parameters Table

Parameter	Minimum	Maximum	Unit	Notes
Volumetric Requirements and Keepouts				1
Static Compressive Load				3
Static Board Deflection				3
Dynamic Compressive Load				3
Transient Bend				3
Shear Load		70 311	lbf N	2,4,5
Tensile Load		25 111	lbf N	2,4,6
Torsion Load		35 3.95	in*lbf N*m	2,4,7

Notes:
1. Refer to drawings in Appendix A.
2. In the case of a discrepancy, the most recent *Dual-Core Intel® Xeon® Processor 5100 Series Datasheet* and *LGA771 Socket Mechanical Design Guide* supersede targets listed in Table 3 above.
3. These socket limits are defined in the *LGA771 Socket Mechanical Design Guide*.
4. These package handling limits are defined in the *Dual-Core Intel® Xeon® Processor 5100 Series Datasheet*.
5. Shear load that can be applied to the package IHS.
6. Tensile load that can be applied to the package IHS.
7. Torque that can be applied to the package IHS.

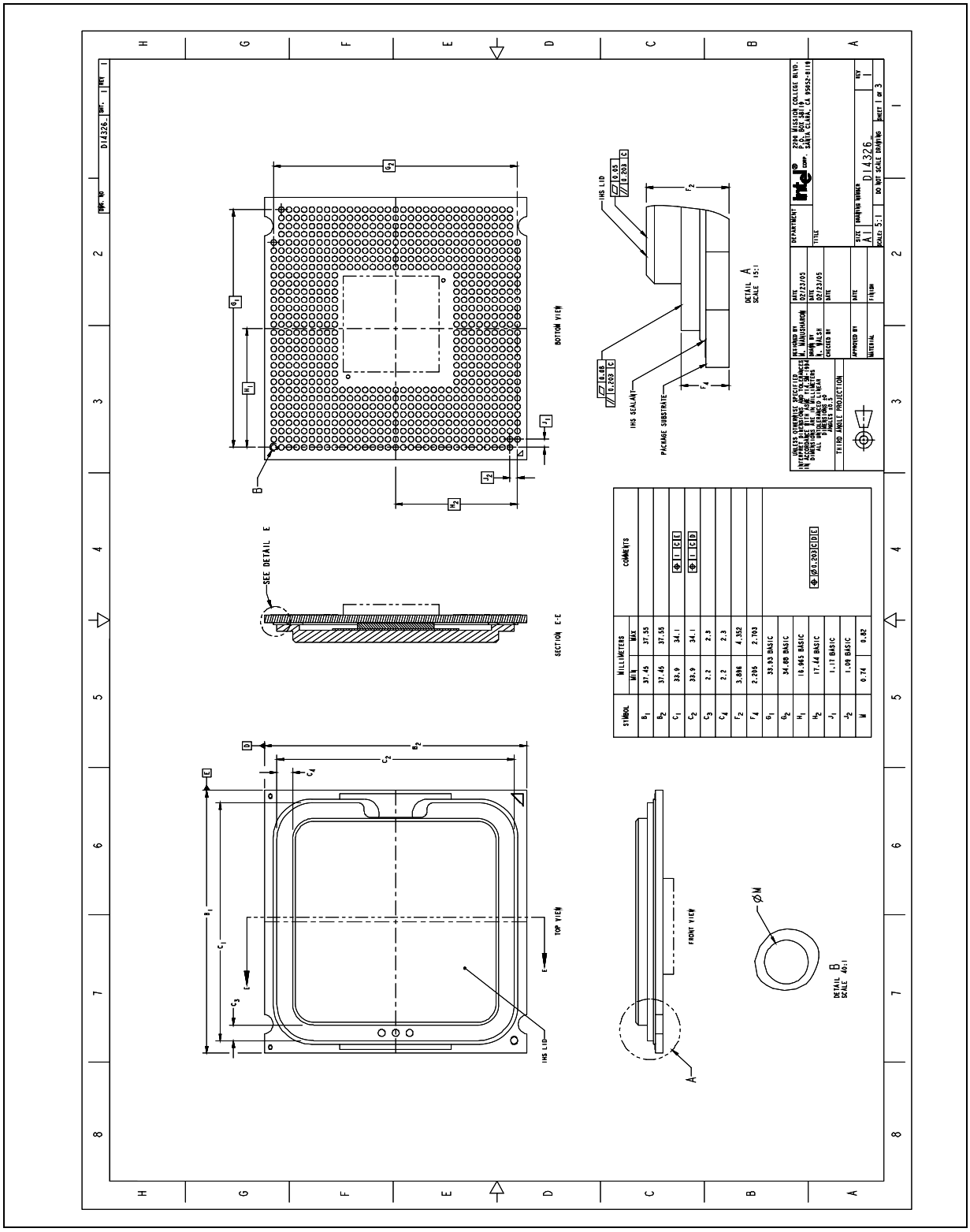
2.1.2 Dual-Core Intel® Xeon® Processor LV 5138 Package

The Dual-Core Intel Xeon Processor LV 5138 is packaged using the flip-chip land grid array (FC-LGA6) package technology. Please refer to the *Dual-Core Intel® Xeon® Processor 5100 Series Datasheet* for detailed mechanical specifications. The Intel® Xeon® Processor LV 5100 Series Processor Mechanical drawing, Figure 1, provides the



mechanical information for Dual-Core Intel Xeon Processor 5100 Series. Integrated package/socket stack-up height information is provided in the *LGA771 Socket Mechanical Design Guide*.

Figure 1. Intel® Xeon® Processor LV 5100 Series Mechanical Drawing



The package includes an integrated heat spreader (IHS). The IHS transfers the non-uniform heat from the die to the top of the IHS, out of which the heat flux is more uniform and spreads over a larger surface area (not the entire IHS area). This allows more efficient heat transfer out of the package to an attached cooling device. The IHS is designed to be the interface for contacting a heatsink. Details can be found in the *Dual-Core Intel® Xeon® Processor 5100 Series Datasheet*.

The processor connects to the baseboard through a 771-land surface mount socket. A description of the socket can be found in the *LGA771 Socket Mechanical Design Guide*.

The processor package and socket have mechanical load limits that are specified in the *Dual-Core Intel® Xeon® Processor 5100 Series Datasheet* and the *LGA771 Socket Mechanical Design Guide.* These load limits should not be exceeded during heatsink installation, removal, mechanical stress testing, or standard shipping conditions. For example, when a compressive static load is necessary to ensure thermal performance of the Thermal Interface Material (TIM) between the heatsink base and the IHS, it should not exceed the corresponding specification given in the *LGA771 Socket Mechanical Design Guide*.

The heatsink mass can also add additional dynamic compressive load to the package during a mechanical shock event. Amplification factors due to the impact force during shock must be taken into account in dynamic load calculations. The total combination of dynamic and static compressive load should not then exceed the processor/socket compressive dynamic load specified in the *LGA771 Socket Mechanical Design Guide* during a vertical shock. It is not recommended to use any portion of the processor substrate as a mechanical reference or load-bearing surface in either static or dynamic compressive load conditions.

2.1.3 Dual-Core Intel® Xeon® Processor 5100 Series Considerations

An attachment mechanism must be designed to support the heatsink since there are no features on the LGA771 socket to directly attach a heatsink. In addition to holding the heatsink in place on top of the IHS, this mechanism plays a significant role in the robustness of the system in which it is implemented, in particular:

- Ensuring thermal performance of the TIM applied between the IHS and the heatsink. TIMs, especially ones based on phase change materials, are very sensitive to applied pressure: the higher the pressure, the better the initial performance. TIMs such as thermal greases are not as sensitive to applied pressure. Refer to Section 2.4.2 and Section 2.4.7.2 for information on tradeoffs made with TIM selection. Designs should consider possible decrease in applied pressure over time due to potential structural relaxation in enabled components.
- Ensuring system electrical, thermal, and structural integrity under shock and vibration events. The mechanical requirements of the attach mechanism depend on the weight of the heatsink and the level of shock and vibration that the system must support. The overall structural design of the baseboard and system must be considered when designing the heatsink attach mechanism. Their design should provide a means for protecting LGA771 socket solder joints as well as preventing package pullout from the socket.

Note: The load applied by the attachment mechanism must comply with the package and socket specifications, along with the dynamic load added by the mechanical shock and vibration requirements, as identified in Section 2.1.1.

A potential mechanical solution for heavy heatsinks is the direct attachment of the heatsink to the chassis pan. In this case, the strength of the chassis pan can be utilized rather than solely relying on the baseboard strength. In addition to the general guidelines given above, contact with the baseboard surfaces should be minimized during installation in order to avoid any damage to the baseboard.

The Intel reference design for Dual-Core Intel® Xeon® Processor 5100 Series is using such a heatsink attachment scheme. Refer to Section 2.4 for further information regarding the Intel reference mechanical solution.

2.2 Processor Thermal Parameters and Features

2.2.1 Thermal Control Circuit and TDP

The operating thermal limits of the processor are defined by the Thermal Profile. The intent of the Thermal Profile specification is to support acoustic noise reduction through fan speed control and ensure the long-term reliability of the processor. This specification requires that the temperature at the center of the processor IHS, known as (T_{CASE}) remains within a certain temperature specification. Compliance with the T_{CASE} specification is required to achieve optimal operation and long-term reliability (See the *Intel® Xeon® Processor Family Thermal Test Vehicle User's Guide* for Case Temperature definition and measurement methods).

To ease the burden on thermal solutions, the Thermal Monitor feature and associated logic have been integrated into the silicon of the processor. One feature of the Thermal Monitor is the Thermal Control Circuit (TCC). When active, the TCC lowers the processor temperature by reducing power consumption. This is accomplished through a combination of Thermal Monitor and Thermal Monitor 2(TM2).Thermal Monitor modulates the duty cycle of the internal processor clocks, resulting in a lower effective frequency, when active, the TCC turns the processor clocks off and then back on with a predetermined duty cycle. Intel® Thermal Monitor 2 adjusts both the processor operating frequency (via the bus multiplier) and input voltage (via the VID signals). Please refer to applicable processor Datasheet for further details on TM and TM2.

PROCHOT# is designed to assert at or a few degrees higher than maximum T_{CASE} (as specified by the thermal profile) when dissipating TDP power, and cannot be interpreted as an indication of processor case temperature. This temperature delta accounts for processor package, lifetime, and manufacturing variations and attempts to ensure the Thermal Control Circuit is not activated below maximum T_{CASE} when dissipating TDP power. There is no defined or fixed correlation between the PROCHOT# assertion temperature and the case temperature. However, with the introduction of the Digital Thermal Sensor (DTS) on the Dual-Core Intel Xeon Processor 5100 Series, the DTS reports a relative temperature delta below the PROCHOT# assertion temperature (see Section 2.2.2 for more details on the Digital Thermal Sensor). Thermal solutions must be designed to the processor specifications (that is, Thermal Profile) and cannot be adjusted based on experimental measurements of T_{CASE}, PROCHOT#, or Digital Thermal Sensor on random processor samples.

By taking advantage of the Thermal Monitor features, system designers may reduce thermal solution cost by designing to the Thermal Design Power (TDP) instead of maximum power. TDP should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is based on measurements of processor power consumption while running various high power applications. This data set is used to determine those applications that are interesting from a power perspective. These applications are then evaluated in a controlled thermal environment to determine their sensitivity to activation of the thermal control circuit. This data set is then used to derive the TDP targets published in the processor Datasheet. The Thermal Monitor can protect the processor in rare workload excursions above TDP. Therefore, thermal solutions should be designed to dissipate this target power level. The thermal management logic and thermal monitor features are discussed in extensive detail in the *Dual-Core Intel® Xeon® Processor 5100 Series Datasheet.*

In addition, on-die thermal management features called THERMTRIP# and FORCEPR# are available on the Dual-Core Intel Xeon Processor 5100 Series. They provide a thermal management approach to support the continued increases in processor frequency and performance. Please see the Dual-Core Intel® Xeon® Processor 5100 Series *Datasheet* for guidance on these thermal management features.

2.2.2 Digital Thermal Sensor

The Dual-Core Intel Xeon Processor 5100 Series introduces a new on-die temperature sensor known as the Digital Thermal Sensor (DTS) that replaces the Tdiode in previous products.

The DTS uses the same sensor utilized for TCC activation. Each individual processor is calibrated so that TCC activation occurs at a DTS value of 0°C. The temperature reported by the DTS is the number of degrees below the TCC activation temperature (i.e., below 0°C), and is always negative. For example, -10 reported by DTS means 10°C away from the TCC activation. No value above the TCC activation temperature (i.e., above 0°C) will be reported, DTS will simply report 0.

The DTS utilizes a thermal sensor that is optimally located when compared with thermal diodes available with legacy processors. This is achieved as a result of a smaller foot print and decreased sensitivity to noise.

The DTS also facilitates the use of multiple thermal sensors within the processor without the burden of increasing the number of thermal sensor signal pins on the processor package. With the legacy thermal diode, each thermal sensor required dedicated signal pins. Operation of multiple DTS will be discussed more detail in Section 2.2.4.

The DTS benefits will be realized in more accurate fan speed control and TCC activation. The DTS application in fan speed control will be discussed more detail in Section 2.3.1.

2.2.3 Platform Environmental Control Interface (PECI)

The PECI interface is designed specifically to convey system management information from the processor (initially, only thermal data from the Digital Thermal Sensor). It is a proprietary single wire bus between the processor and the chipset or other health monitoring device. Data from the Digital Thermal Sensors are processed and stored in a processor register (MSR) which is queried through the Platform Environment Control Interface (PECI). The PECI specification provides a specific command set to discover, enumerate devices, and read the temperature. For an overview of the PECI interface, please refer to *PECI Feature Set Overview*. For more detail information on PECI, please refer to *Platform Environment Control Interface (PECI) Specification and Dual-Core Intel® Xeon® Processor 5100 Series Datasheet.*

2.2.4 Multiple Core Special Considerations

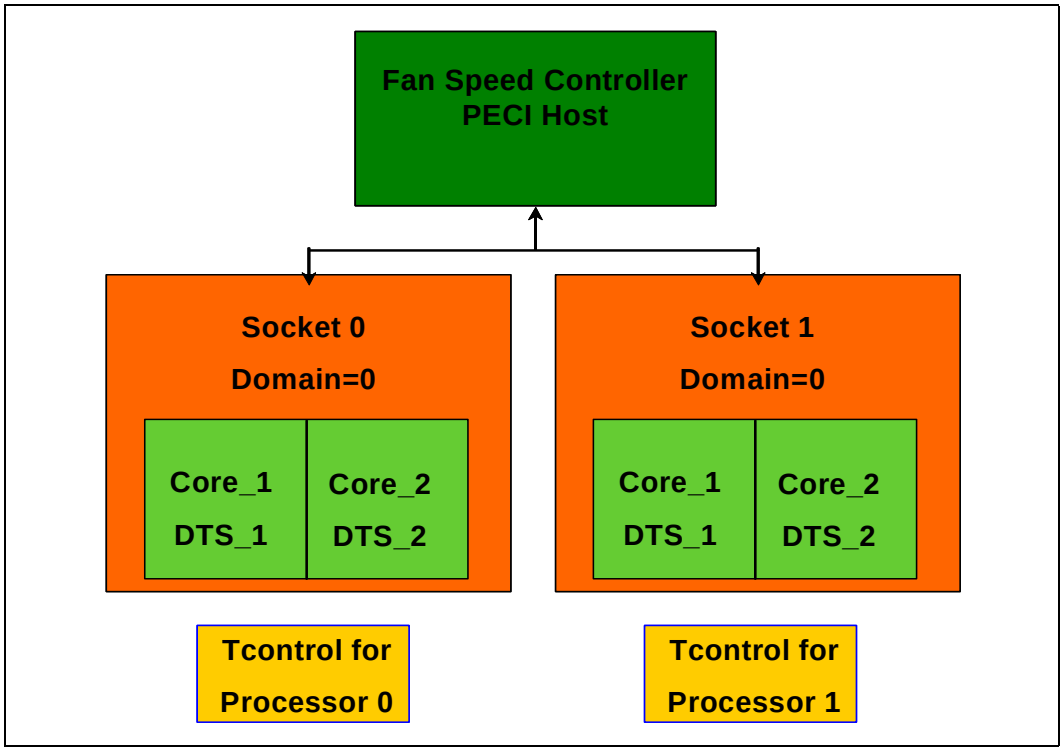
2.2.4.1 Multiple Digital Thermal Sensor Operation

When Intel designers integrate multiple Digital Thermal Sensors onto a processor to monitor multiple temperature regions, such as multiple cores, the only temperature of concern to the external cooling system is the single hottest value for the entire processor.

To simplify the process of determining the hottest location, the PECI interface to the Digital Thermal Sensors introduces the concept of domain. Figure 2 provides an illustration of the DTS domain for Dual-Core Intel Xeon Processor 5100 Series. This series contains two cores, both cores are in one domain with one Digital Thermal

Sensor per core. Some multiple core processors have a single domain, other processors will have multiple domains. Each domain receives all temperature sensor values on the processor within that domain, and provides the current hottest value for that domain when polled by an external PECI device such as a thermal management system. The BIOS will be responsible for detecting the proper processor type and providing the number of domains to the thermal management system.

Figure 2. DTS Domain for Dual-Core Intel® Xeon® Processor 5100 Series



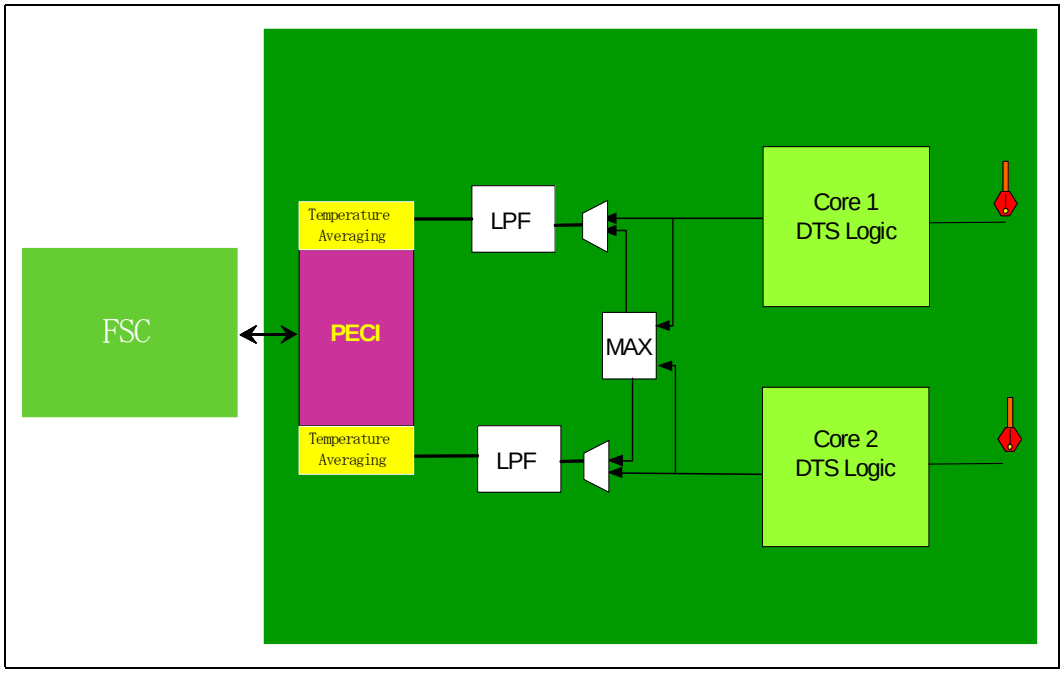
2.2.4.2 Thermal Monitor for Multiple Core Products

The thermal management for multiple core products have only one $T_{CONTROL}$ value per processor. If the DTS temperature from any domain within the processor is greater than or equal to $T_{CONTROL}$, the processor case temperature must remain at or below the temperature as specified by the thermal profile. See Section 2.2.6 for information on $T_{CONTROL}$.

2.2.4.3 Fan Speed Control for Multiple Core Intel® Xeon® Processors

There is only one pin (Pin G5) on each LGA771 socket that accesses the single domain of the Dual-Core Intel Xeon Processor 5100 Series. Through this pin, the single domain receives all temperature sensor values and provides the current hottest value to an external PECI device such as a thermal management system. Figure 3 provides an illustration of the fan speed signals for the multiple core Dual-Core Intel Xeon Processor 5100 Series.

Figure 3. Fan Speed Control for Multiple Core Dual-Core Intel® Xeon® Processor 5100 Series



The processor MSR supports temperature threshold interrupts and provides instantaneous data. To reduce the sample rate requirements on PECI and improve thermal data stability vs. time, the processor Digital Thermal Sensor and PECI interface implement an averaging algorithm. For more information on the Processor Thermal Data Sample Rate and Filtering, please refer to Dual-Core Intel® Xeon® Processor 5100 Series *Datasheet.*

2.2.4.4 PROCHOT#, THERMTRIP#, and FORCEPR#

The PROCHOT# and THERMTRIP# outputs will be shared by all cores on a processor. The first core to reach TCC activation will assert PROCHOT#. A single FORCEPR# input will be shared by each core. Table 4 provides an overview of input and output conditions for the Dual-Core Intel Xeon Processor 5100 Series thermal management features.

Table 4. Input and Output Conditions for the Multiple Core Dual-Core Intel Xeon Processor 5100 Series Thermal Management Features

Item	Processor Input	Processor Output
TM/TM2	DTS*Core X* ≥ TCC Activation Temperature	All Cores TCC Activation
PROCHOT#	DTS*Core X* ≥ TCC Activation Temperature	PROCHOT# Asserted
THERMTRIP#	DTS*Core X* ≥ THERMTRIP # Assertion Temperature	THERMTRIP# Asserted, all cores shut down
FORCEPR#	FORCEPR# Asserted	All Cores TCC Activation

Notes:
1. *X*=1,2, represents any one of the core1and core2 in Dual-Core Intel Xeon Processor 5100 Series.
2. For more information on PROCHOT#, THERMTRIP#, and FORCEPR# see the Dual-Core Intel® Xeon® Processor 5100 Series *Datasheet*.

2.2.4.5 Heatpipe Orientation for Multiple Core Processors

Thermal management of multiple core processors can be achieved without the use of heatpipe heatsinks, as demonstrated by the Intel Reference Thermal Solution discussed in Section 2.4.

To assist customers interested in designing heatpipe heatsinks, processor core locations have been provided. In some cases, this may influence the designer's selection of heatpipe orientation. For this purpose, the core geometric center locations, as illustrated in Figure 4, are provided in Table 5. Dimensions originate from the vertical edge of the IHS nearest to the pin 1 fiducial as shown in Figure 4.

Figure 4. Processor Core Geometric Center Locations

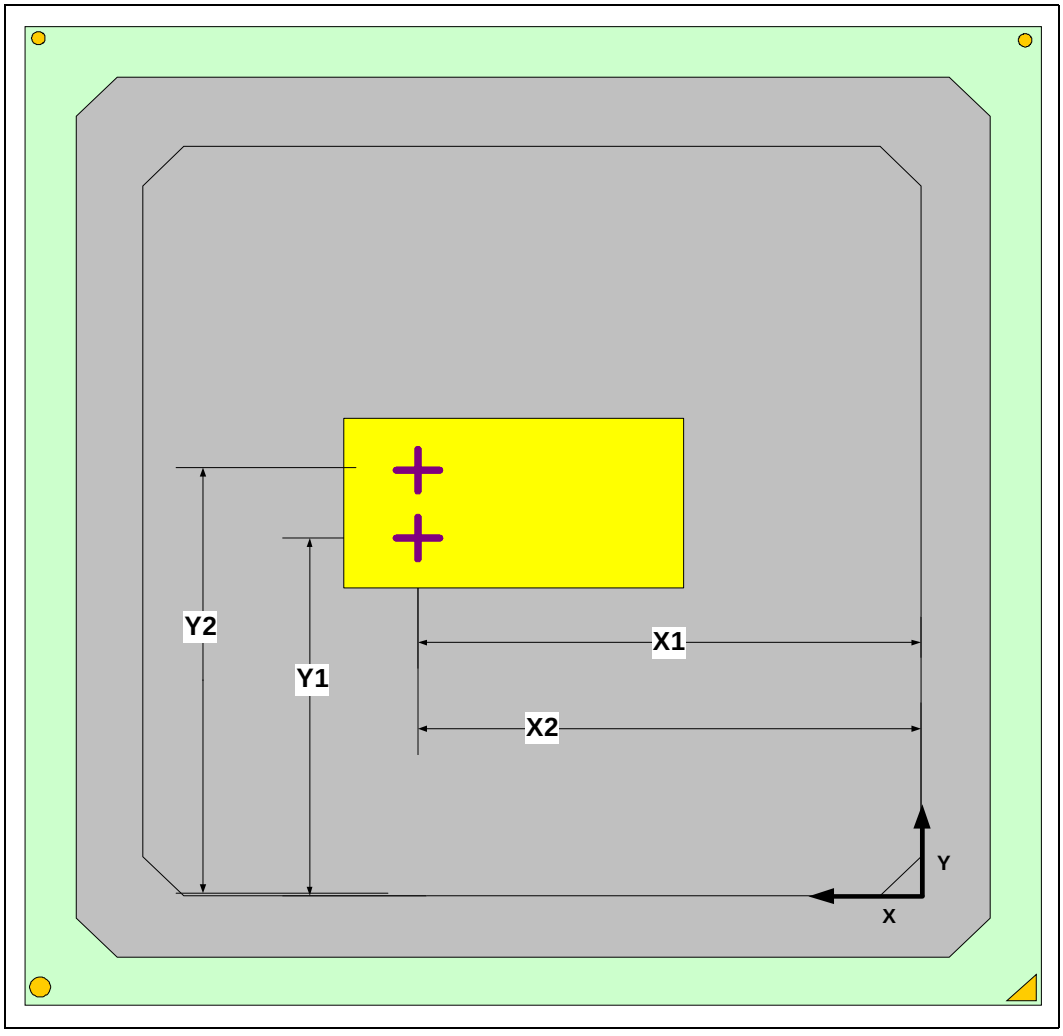


Table 5. Processor Core Geometric Center Dimensions

Feature	X Dimension	Y Dimension
Core 1	19.53 mm	12.68 mm
Core 2	19.53 mm	16.82 mm

2.2.5 Thermal Profile

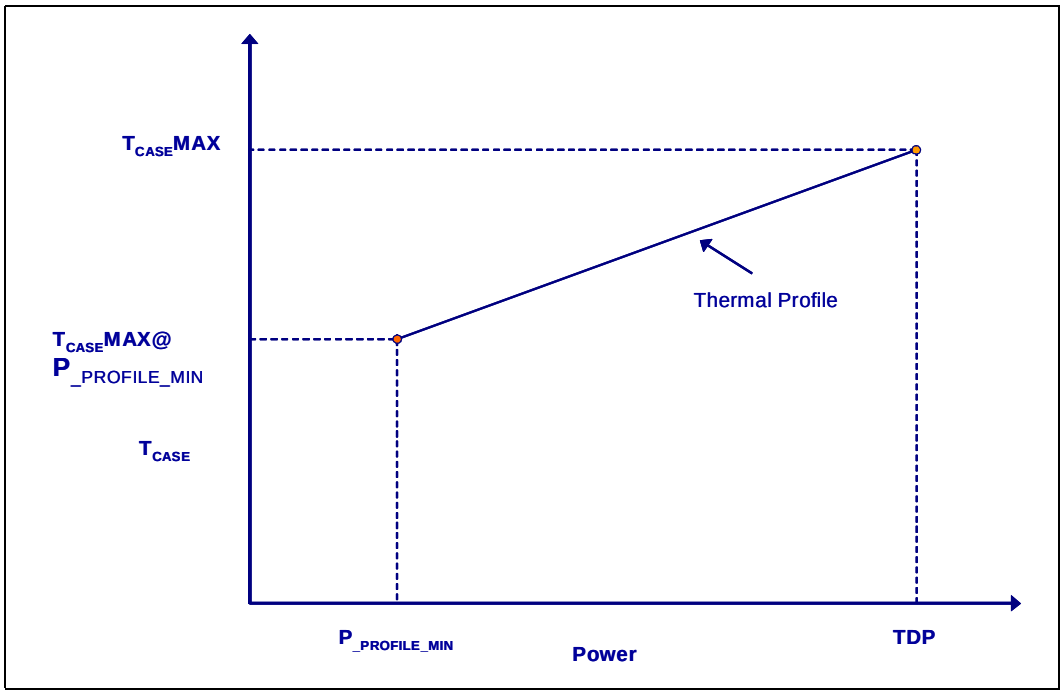
The thermal profile is a linear line that defines the relationship between a processor's case temperature and its power consumption as shown in Figure 5. The equation of the thermal profile is defined as:

Equation 1. y = ax + b

Where:

y = Processor case temperature, T_{CASE} (°C)
x = Processor power consumption (W)
a = Case-to-ambient thermal resistance, ψCA (°C/W)
b = Processor local ambient temperature, TLA (°C)

Figure 5. Thermal Profile Diagram



The higher end point of the Thermal Profile represents the processor's TDP and the associated maximum case temperature (T_{CASE_MAX}). The lower end point of the Thermal Profile represents the power value ($P_{PROFILE\_MIN}$) and the associated case temperature (T_{CASE_MAX}@ $P_{PROFILE\_MIN}$) for the lowest possible theoretical value of $T_{CONTROL}$ (see Section 2.2.6). The slope of the Thermal Profile line represents the case-to-ambient resistance of the thermal solution with the y-intercept being the local processor ambient temperature. The slope of the Thermal Profile is constant between $P_{PROFILE\_MIN}$ and TDP, which indicates that all frequencies of a processor defined by the Thermal Profile will require the same heatsink case-to-ambient resistance.

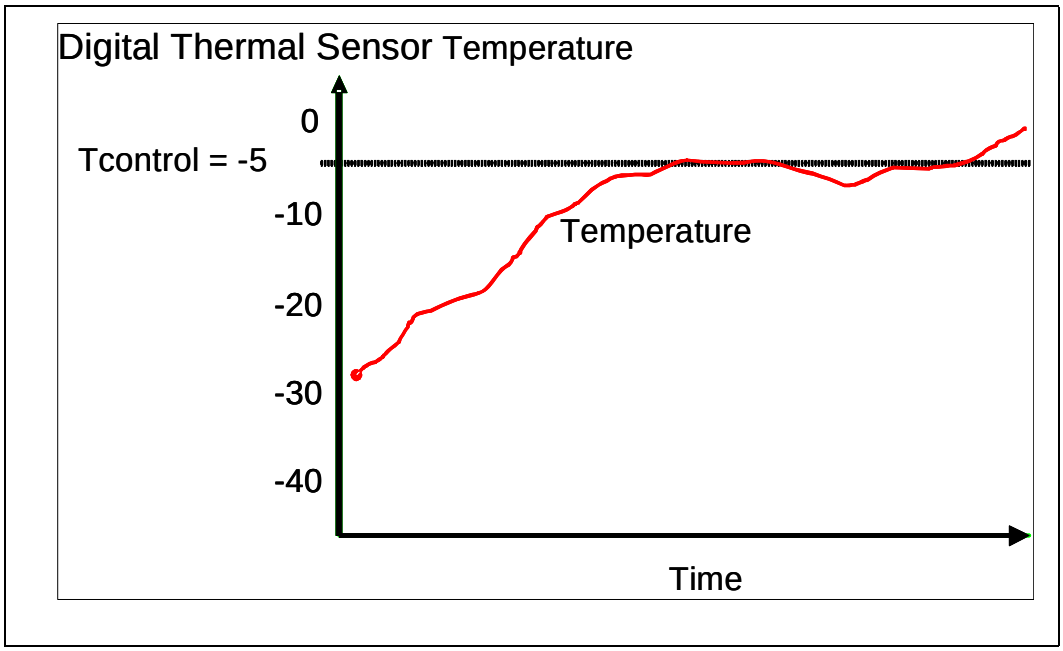
In order to satisfy the Thermal Profile specification, a thermal solution must be at or below the Thermal Profile line for the given processor when its DTS temperature is greater than $T_{CONTROL}$ (refer to Section 2.2.6). The Thermal Profile allows the customers to make a trade-off between the thermal solution case-to-ambient resistance and the processor local ambient temperature that best suits their platform implementation (refer to Section 2.3.3). There can be multiple combinations of thermal solution case-to-ambient resistance and processor local ambient temperature that can

meet a given Thermal Profile. If the case-to-ambient resistance and the local ambient temperature are known for a specific thermal solution, the Thermal Profile of that solution can easily be plotted against the Thermal Profile specification. As explained above, the case-to-ambient resistance represents the slope of the line and the processor local ambient temperature represents the y-axis intercept. Hence the T_{CASE} values of a specific solution can be calculated at the TDP and $P_{\_PROFILE\_MIN}$ power levels. Once these points are determined, they can be joined by a line, which represents the Thermal Profile of the specific solution. If that line stays at or below the Thermal Profile specification, then that particular solution is deemed as a compliant solution.

2.2.6 $T_{CONTROL}$ Definition

$T_{CONTROL}$ can be described as a trigger point for fan speed control implementation. The processor $T_{CONTROL}$ value is now a DTS value. Because the temperatures provided by the Digital Thermal Sensor are relative and no longer absolute, the $T_{CONTROL}$ value is now defined as a relative value to the TCC activation set point (i.e., 0°C). Figure 6 depicts the interaction between the $T_{CONTROL}$ value and Digital Thermal Sensor value.

Figure 6. $T_{CONTROL}$ Value and Digital Thermal Sensor Value Interaction



The value for $T_{CONTROL}$ is calibrated in manufacturing and configured for each processor individually. For the Dual-Core Intel Xeon Processor 5100 Series, the $T_{CONTROL}$ value is obtained by reading a processor model specific register (MSR).

Note: There is no $T_{CONTROL\_BASE}$ value to sum as previously required on legacy processors. The fan speed control device only needs to read the T_{OFFSET} MSR and compare this to the DTS value from the PECI interface. The equation for calculating $T_{CONTROL}$ is:

Equation 2. $T_{CONTROL} = -T_{OFFSET}$

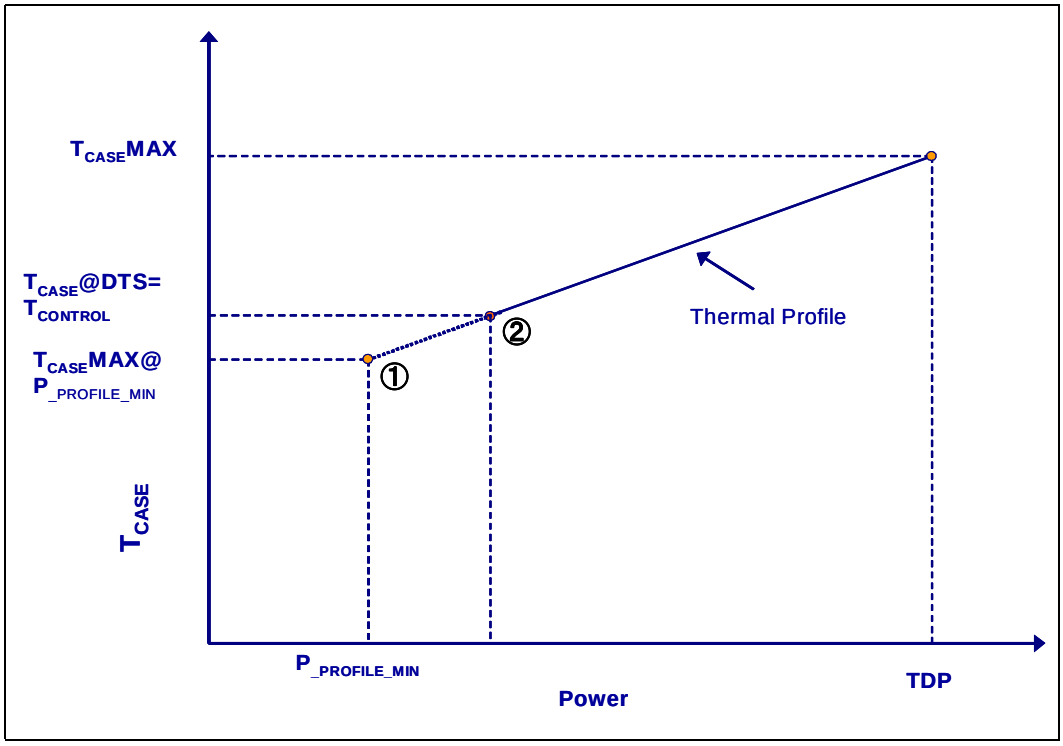
Where:

T_{OFFSET} = A DTS-based value programmed into each processor during manufacturing that can be obtained by reading the IA32_TEMPERATURE_TARGET

MSR. This is a static and a unique value. Contact Intel field sales representative for further details.

Figure 7 depicts the interaction between the Thermal Profile and $T_{CONTROL}$.

Figure 7. $T_{CONTROL}$ and Thermal Profile Interaction



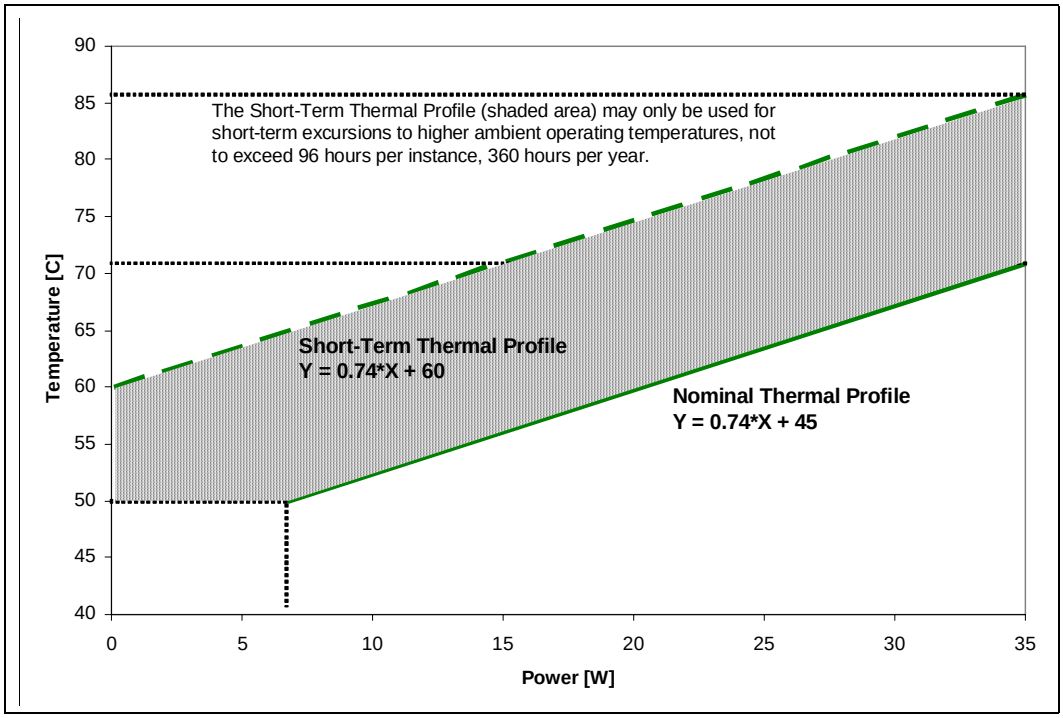
Since $T_{CONTROL}$ is based on a processor DTS temperature value, an equivalent T_{CASE} temperature must be determined to plot the T_{CASE} @ $T_{CONTROL}$ point on the Thermal Profile graph. Location 1 on the Thermal Profile represents a T_{CASE} value corresponding to $P_{\_PROFILE\_MIN}$. Location 2 on the Thermal Profile represents a T_{CASE} value corresponding to DTS = $T_{CONTROL}$. If the DTS temperature is less than $T_{CONTROL}$, then the case temperature is permitted to exceed the Thermal Profile, but the DTS temperature must remain at or below $T_{CONTROL}$. The thermal solution for the processor must be able to keep the processor's T_{CASE} at or below the T_{CASE} values defined by the Thermal Profile between the T_{CASE_MAX} @$P_{\_PROFILE\_MIN}$ and T_{CASE_MAX} points at the corresponding power levels.

Refer to Section 2.3.1 for the implementation of the $T_{CONTROL}$ value in support of fan speed control (FSC) design to achieve better acoustic performance.

2.2.7 Performance Targets

The Thermal Profile specifications for these processors are published in the *Dual-Core Intel® Xeon® Processor 5100 Series Datasheet*. These Thermal Profile specifications are shown as a reference in the subsequent discussions.

Figure 8. Thermal Profile for the Dual-Core Intel® Xeon® Processor 5138



Notes:

1. The thermal specifications shown in this graph are for reference only. Refer to the *Dual-Core Intel® Xeon® Processor 5100 Series Datasheet* for the Thermal Profile specifications. In case of conflict, the data information in the datasheet supersedes any data in this figure.
2. The Nominal Thermal Profile must be used for all normal operating conditions, or for products that do not require NEBS Level 3 compliance.
3. The Short-Term Thermal Profile may only be used for short-term excursions to higher ambient operating temperatures, not to exceed 96 hours per instance, 360 hours per year, and a maximum of 15 instances per year, as compliant with NEBS Level 3.
4. Implementation of either thermal profile should result in virtually no TCC activation.
5. Utilization of a thermal solution that exceeds the Short-Term Thermal Profile, or which operates at the Short-Term Thermal Profile for a duration longer than the limits specified in Note 3 above, do not meet the processor's thermal specifications and may result in permanent damage to the processor.

Table 6 and Table 7 describe thermal performance target for the Dual-Core Intel® Xeon® Processor 5100 Series cooling solution enabled by Intel.

Table 6. Intel Reference Heatsink Performance Targets for the Dual-Core Intel® Xeon® Processor 5138 (Nominal)

Parameter	Maximum	Unit	Notes
Altitude	Sea-level	m	Heatsink designed at 0 meters
T_{LA}	40	°C	
TDP	35	W	
T_{CASE_MAX}	70.9	°C	
T_{CASE_MAX} @ P_profile_min	50	°C	P_profile_min = 6.8W.
Airflow	2.5	CFM	Airflow through the heatsink fins
Ψ_{CA}	0.816	°C/W	Mean + 3σ

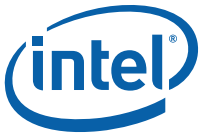


Table 7. Intel Reference Heatsink Performance Targets for the Dual-Core Intel® Xeon® Processor 5138 (NEBS Short Term)

Parameter	Maximum	Unit	Notes
Altitude	Sea-level	m	Heatsink designed at 0 meters
T_{LA}	55	°C	
TDP	35	W	
T_{CASE_MAX}	85.9	°C	
T_{CASE_MAX} @ P_profile_min	60	°C	P_profile_min= 6.8 W.
Airflow	2.5	CFM	Airflow through the heatsink fins
Ψ_{CA}	0.816	°C/W	Mean + 3σ

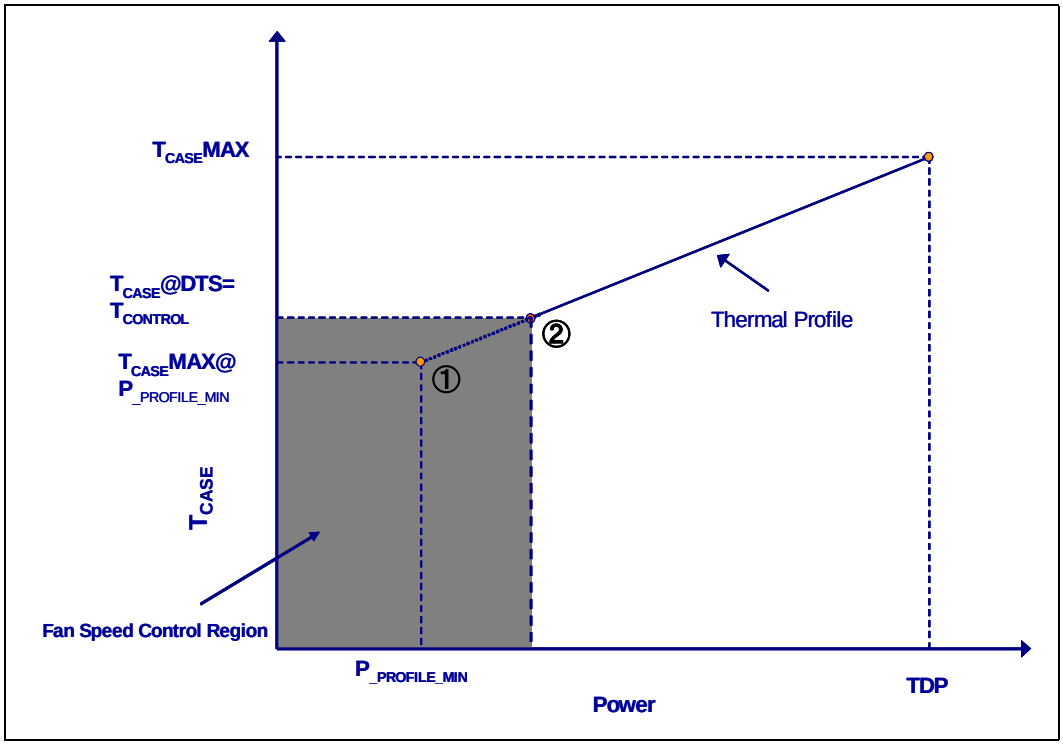
Note: In case of conflict, the processor Datasheet supersedes the information contained in this document.

2.3 Characterizing Cooling Solution Performance Requirements

2.3.1 Fan Speed Control

Fan speed control (FSC) techniques to reduce system level acoustic noise are a common practice in server designs. The fan speed is one of the parameters that determine the amount of airflow provided to the thermal solution. Additionally, airflow is proportional to a thermal solution's performance, which consequently determines the T_{CASE} of the processor at a given power level. Since the T_{CASE} of a processor is an important parameter in the long-term reliability of a processor, the FSC implemented in a system directly correlates to the processor's ability to meet the Thermal Profile and hence the long-term reliability requirements. For this purpose, the parameter called $T_{CONTROL}$ as explained in Section 2.2.6, is to be used in FSC designs to ensure that the long-term reliability of the processor is met while keeping the system level acoustic noise down. Figure 9 depicts the relationship between $T_{CONTROL}$ and FSC methodology.

Figure 9. $T_{CONTROL}$ and Fan Speed Control

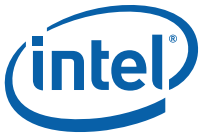


Once the $T_{CONTROL}$ value is determined as explained earlier, the DTS temperature reading from the processor can be compared to this $T_{CONTROL}$ value. A fan speed control scheme can be implemented as described in Table 8 without compromising the long-term reliability of the processor.

Table 8. Fan Speed Control, $T_{CONTROL}$ and DTS Relationship

Condition	FSC Scheme
DTS≤ $T_{CONTROL}$	FSC can adjust fan speed to maintain DTS = $T_{CONTROL}$ (low acoustic region).
DTS>$T_{CONTROL}$	FSC should adjust fan speed to keep T_{CASE} at or below the Thermal Profile specification (increased acoustic region).

There are many different ways of implementing fan speed control, including FSC based on processor ambient temperature, FSC based on processor Digital Thermal Sensor (DTS) temperature or a combination of the two. If FSC is based only on the processor ambient temperature, low acoustic targets can be achieved under low ambient temperature conditions. However, the acoustics cannot be optimized based on the behavior of the processor temperature. If FSC is based only on the Digital Thermal Sensor, sustained temperatures above $T_{CONTROL}$ drives fans to maximum RPM. If FSC is based both on ambient and Digital Thermal Sensor, ambient temperature can be used to scale the fan RPM controlled by the Digital Thermal Sensor. This would result in an optimal acoustic performance. Regardless of which scheme is employed, system designers must ensure that the Thermal Profile specification is met when the processor Digital Thermal Sensor temperature exceeds the T_{CONTOL} value for a given processor.



2.3.2 Processor Thermal Characterization Parameter Relationships

The idea of a "thermal characterization parameter", Ψ (psi), is a convenient way to characterize the performance needed for the thermal solution and to compare thermal solutions in identical conditions (heating source, local ambient conditions). A thermal characterization parameter is convenient in that it is calculated using total package power, whereas actual thermal resistance, θ (theta), is calculated using actual power dissipated between two points. Measuring actual power dissipated into the heatsink is difficult, since some of the power is dissipated via heat transfer into the socket and board. Be aware, however, of the limitations of lumped parameters such as Ψ when it comes to a real design. Heat transfer is a three-dimensional phenomenon that can rarely be accurately and easily modeled by lump values.

The case-to-local ambient thermal characterization parameter value (Ψ_{CA}) is used as a measure of the thermal performance of the overall thermal solution that is attached to the processor package. It is defined by the following equation, and measured in units of °C/W:

Equation 3. $\Psi_{CA} = (T_{CASE} - T_{LA}) / TDP$

Where:

Ψ_{CA} = Case-to-local ambient thermal characterization parameter (°C/W).
T_{CASE} = Processor case temperature (°C).
T_{LA} = Local ambient temperature in chassis at processor (°C).
TDP = TDP dissipation (W) (assumes all power dissipates through the integrated heat spreader (IHS)).

The case-to-local ambient thermal characterization parameter of the processor, Ψ_{CA}, is comprised of Ψ_{CS}, the TIM thermal characterization parameter, and of Ψ_{SA}, the sink-to-local ambient thermal characterization parameter:

Equation 4. $\Psi_{CA} = \Psi_{CS} + \Psi_{SA}$

Where:

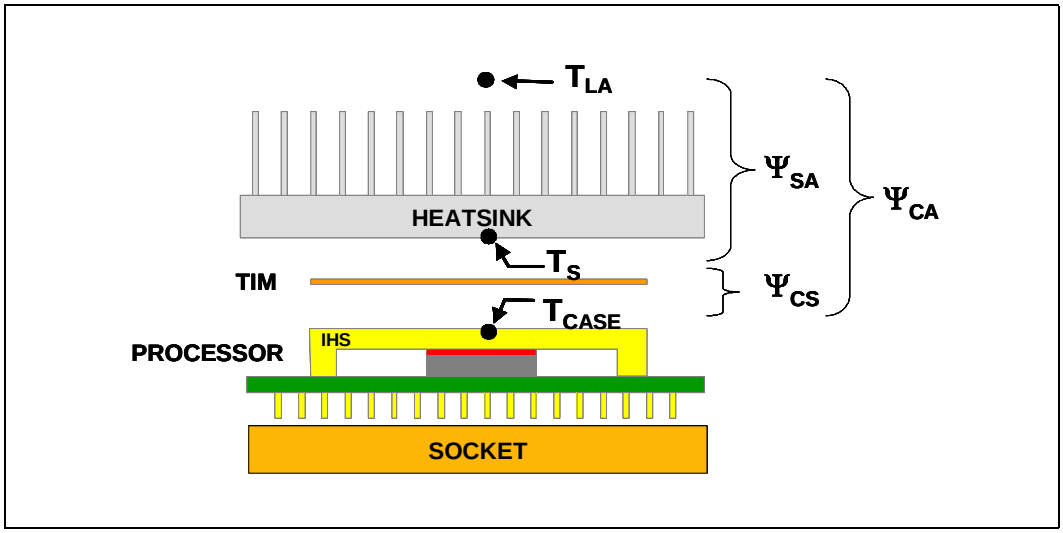
Ψ_{CS}=Thermal characterization parameter of the TIM (°C/W).
Ψ_{SA}=Thermal characterization parameter from heatsink-to-local ambient (°C/W).

Ψ_{CS} is strongly dependent on the thermal conductivity and thickness of the TIM between the heatsink and IHS.

Ψ_{SA} is a measure of the thermal characterization parameter from the bottom of the heatsink to the local ambient air. Ψ_{SA} is dependent on the heatsink material, thermal conductivity, and geometry. It is also strongly dependent on the air velocity through the fins of the heatsink.

Figure 10 illustrates the combination of the different thermal characterization parameters.

Figure 10. Processor Thermal Characterization Parameter Relationships



2.3.2.1 Example

The cooling performance, $\Psi_{CA,}$ is then defined using the principle of thermal characterization parameter described above:

- Define a target case temperature T_{CASE_MAX} and corresponding TDP, given in the processor Datasheet.
- Define a target local ambient temperature at the processor, T_{LA}.

The following provides an illustration of how one might determine the appropriate performance targets. The example power and temperature numbers used here are not related to any Intel processor thermal specifications, and are for illustrative purposes only.

Assume the Datasheet TDP is 85 W and the case temperature specification is 68 °C. Assume as well that the system airflow has been designed such that the local processor ambient temperature is 45 °C. Then the following could be calculated using equation (2-3) from above:

Equation 5. $\Psi_{CA} = (T_{CASE} - T_{LA}) / TDP = (68 - 45) / 85 = 0.27$ °C/W

To determine the required heatsink performance, a heatsink solution provider would need to determine Ψ_{CS} performance for the selected TIM and mechanical load configuration. If the heatsink solution was designed to work with a TIM material performing at $\Psi_{CS} \leq 0.05$ °C/W, solving for equation (2-4) from above, the performance of the heatsink would be:

Equation 6. $\Psi_{SA} = \Psi_{CA} - \Psi_{CS} = 0.27 - 0.05 = 0.22$ °C/W

If the local processor ambient temperature is assumed to be 40°C, the same calculation can be carried out to determine the new case-to-ambient thermal resistance:

Equation 7. $\Psi_{CA} = (T_{CASE} - T_{LA}) / TDP = (68 - 40) / 85 = 0.33\ °C/W$

It is evident from the above calculations that, a reduction in the local processor ambient temperature has a significant positive effect on the case-to-ambient thermal resistance requirement.

2.3.3 Chassis Thermal Design Considerations

2.3.3.1 Chassis Thermal Design Capabilities and Improvements

One of the critical parameters in thermal design is the local ambient temperature assumption of the processor. Keeping the external chassis temperature fixed, internal chassis temperature rise is the only component that can affect the processor local ambient temperature. Every degree gained at the local ambient temperature directly translates into a degree relief in the processor case temperature.

Given the thermal targets for the processor, it is extremely important to optimize the chassis design to minimize the air temperature rise upstream to the processor (T_{rise}), hence minimizing the processor local ambient temperature. Please refer to *T_{RISE} Reduction Guidelines for Rack Servers and Workstations* for more details.

The heat generated by components within the chassis must be removed to provide an adequate operating environment for both the processor and other system components. Moving air through the chassis brings in air from the external ambient environment and transports the heat generated by the processor and other system components out of the system. The number, size and relative position of fans, vents and other heat generating components determine the chassis thermal performance, and the resulting ambient temperature around the processor. The size and type (passive or active) of the thermal solution and the amount of system airflow can be traded off against each other to meet specific system design constraints. Additional constraints are board layout, spacing, component placement, and structural considerations that limit the thermal solution size.

In addition to passive heatsinks, fan heatsinks and system fans, other solutions exist for cooling integrated circuit devices. For example, ducted blowers, heat pipes and liquid cooling are all capable of dissipating additional heat. Due to their varying attributes, each of these solutions may be appropriate for a particular system implementation.

To develop a reliable, cost-effective thermal solution, thermal characterization and simulation should be carried out at the entire system level, accounting for the thermal requirements of each component. In addition, acoustic noise constraints may limit the size, number, placement, and types of fans that can be used in a particular design.

2.4 Thermal/Mechanical Reference Design Considerations

2.4.1 Heatsink Solutions

2.4.1.1 Heatsink Design Considerations

To remove the heat from the processor, three basic parameters should be considered:

- **The area of the surface on which the heat transfer takes place -** Without any enhancements, this is the surface of the processor package IHS. One method used to improve thermal performance is by attaching a heatsink to the IHS. A heatsink can increase the effective heat transfer surface area by conducting heat out of the IHS and into the surrounding air through fins attached to the heatsink base.

- **The conduction path from the heat source to the heatsink fins -** Providing a direct conduction path from the heat source to the heatsink fins and selecting materials with higher thermal conductivity typically improves heatsink performance. The length, thickness, and conductivity of the conduction path from the heat source to the fins directly impact the thermal performance of the heatsink. In particular, the quality of the contact between the package IHS and the heatsink base has a higher impact on the overall thermal solution performance as processor cooling requirements become strict. Thermal interface material (TIM) is used to fill in the gap between the IHS and the bottom surface of the heatsink, and thereby improves the overall performance of the thermal stackup (IHS-TIM-Heatsink). With extremely poor heatsink interface flatness or roughness, TIM may not adequately fill the gap. The TIM thermal performance depends on its thermal conductivity as well as the pressure load applied to it. Refer to Section 2.4.2 for further information on the TIM between the IHS and the heatsink base.
- **The heat transfer conditions on the surface on which heat transfer takes place -** Convective heat transfer occurs between the airflow and the surface exposed to the flow. It is characterized by the local ambient temperature of the air, T_{LA}, and the local air velocity over the surface. The higher the air velocity over the surface, the resulting cooling is more efficient. The nature of the airflow can also enhance heat transfer via convection. Turbulent flow can provide improvement over laminar flow. In the case of a heatsink, the surface exposed to the flow includes the fin faces and the heatsink base.

An active heatsink typically incorporates a fan that helps manage the airflow through the heatsink.

Passive heatsink solutions require in-depth knowledge of the airflow in the chassis. Typically, passive heatsinks see slower air speed. Therefore, these heatsinks are typically larger (and heavier) than active heatsinks due to the increase in fin surface required to meet a required performance. As the heatsink fin density (the number of fins in a given cross-section) increases, the resistance to the airflow increases: it is more likely that the air will travel around the heatsink instead of through it, unless air bypass is carefully managed. Using air-ducting techniques to manage bypass area is an effective method for maximizing airflow through the heatsink fins.

2.4.2 Thermal Interface Material

TIM application between the processor IHS and the heatsink base is generally required to improve thermal conduction from the IHS to the heatsink. Many thermal interface materials can be pre-applied to the heatsink base prior to shipment from the heatsink supplier and allow direct heatsink attach, without the need for a separate TIM dispense or attach process in the final assembly factory.

All thermal interface materials should be sized and positioned on the heatsink base in a way that ensures the entire processor IHS area is covered. It is important to compensate for heatsink-to-processor attach positional alignment when selecting the proper TIM size.

When pre-applied material is used, it is recommended to have a protective application tape over it. This tape must be removed prior to heatsink installation.

The TIM performance is susceptible to degradation (i.e., grease breakdown) during the useful life of the processor due to the temperature cycling phenomena. For this reason, the measured T_{CASE} value of a given processor can decrease over time depending on the type of TIM material.

Refer to Section 2.4.7.2 for information on the TIM used in the Intel reference heatsink solution.

2.4.3 Summary

In summary, considerations in heatsink design include:

- The local ambient temperature T_{LA} at the heatsink, airflow (CFM), the power being dissipated by the processor, and the corresponding maximum T_{CASE}. These parameters are usually combined in a single lump cooling performance parameter, Ψ_{CA} (case to air thermal characterization parameter). More information on the definition and the use of Ψ_{CA} is given in Section 2.4 and Section 2.3.2.
- Heatsink interface (to IHS) surface characteristics, including flatness and roughness.
- The performance of the TIM used between the heatsink and the IHS.
- Surface area of the heatsink.
- Heatsink material and technology.
- Development of airflow entering and within the heatsink area.
- Physical volumetric constraints placed by the system.
- Integrated package/socket stackup height information is provided in the *LGA771 Socket Mechanical Design Guide*.

2.4.4 Assembly Overview of the Intel Reference Thermal Mechanical Design

The reference design heatsinks that meet the Dual-Core Intel Xeon Processor 5100 Series thermal performance targets are called the Common Enabling Kit (CEK) heatsinks, and are available in 1U, 2U, and 2U+ form factors. A CEK style heatsink was also designed for AdvancedTCA*. Each CEK consists of the following components:

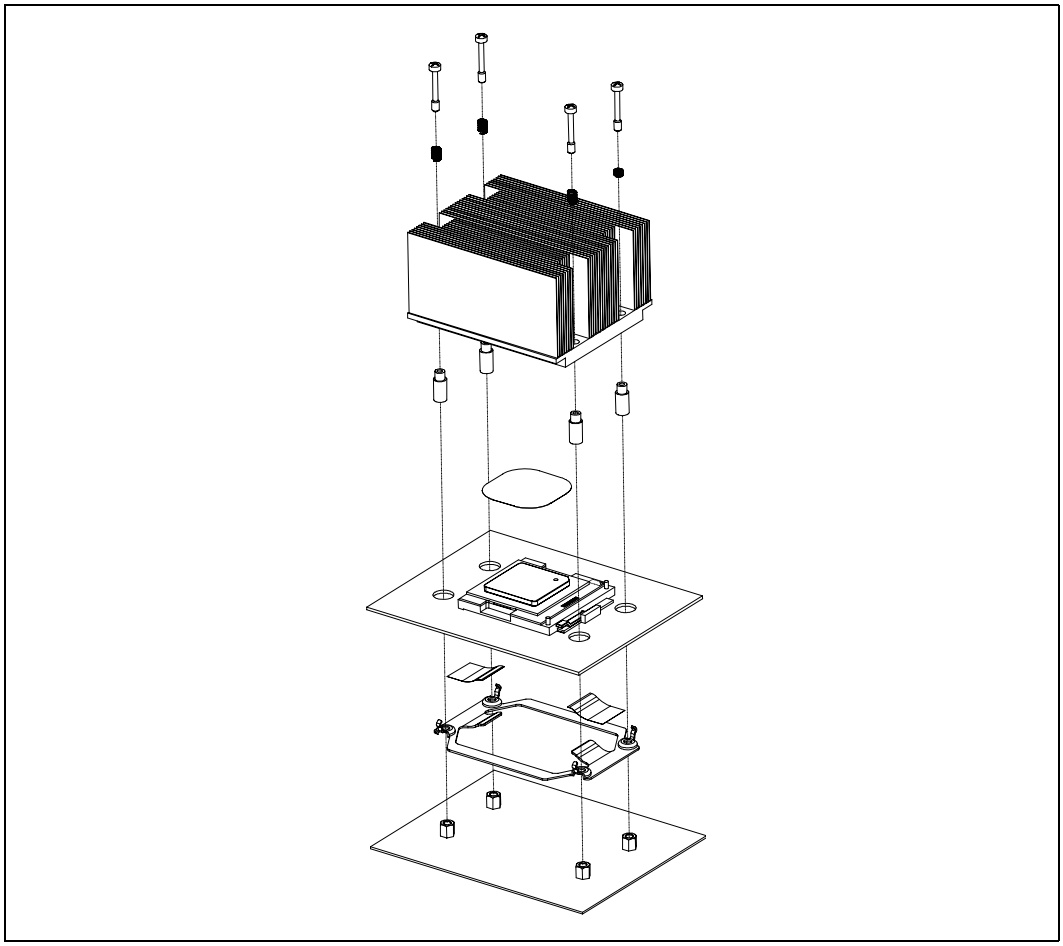
- Heatsink (with captive standoff and screws)
- Thermal Interface Material (TIM)
- CEK Spring

2.4.4.1 Geometric Envelope

The baseboard keepout zones on the primary and secondary sides and height restrictions under the enabling component region are shown in detail in Appendix A. The overall volumetric keep in zone encapsulates the processor, socket, and the entire thermal/mechanical enabling solution.

2.4.4.2 Assembly Drawing

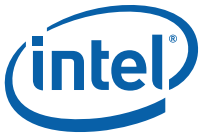
Figure 11. Exploded View of CEK Thermal Solution Components



The CEK reference thermal solution is designed to extend air-cooling capability through the use of larger heatsinks with minimal airflow blockage and bypass. CEK retention solution can allow the use of much heavier heatsink masses compared to the legacy limits by using a load path directly attached to the chassis pan. The CEK spring on the secondary side of the baseboard provides the necessary compressive load for the thermal interface material. The baseboard is intended to be isolated such that the dynamic loads from the heatsink are transferred to the chassis pan via the stiff screws and standoffs. This reduces the risk of package pullout and solder-joint failures.

The baseboard mounting holes for the CEK solution are at the same location as the hole locations used for previous Intel® Xeon® processor thermal solution. However, CEK assembly requires 10.16 mm [0.400 in.] large diameter holes to compensate for the CEK spring embosses.

The CEK solution is designed and optimized for a baseboard thickness range of 1.57 – 2.31 mm [0.062-0.093 in]. While the same CEK spring can be used for this board thickness range, the heatsink standoff height is different for a 1.57 mm [0.062 in.] thick board than it is for a 2.31 mm [0.093 in.] thick board. In the heatsink assembly, the standoff protrusion from the base of the heatsink needs to be 0.6 mm [0.024 in] longer for a 2.31 mm [0.093 in.] thick board, compared to a 1.57 mm [0.062 in.] thick



board. If this solution is intended to be used on baseboards that fall outside of this range, then some aspects of the design, including but not limited to the CEK spring design and the standoff heights, may need to change. Therefore, system designers need to evaluate the thermal performance and mechanical behavior of the CEK design on baseboards with different thicknesses.

Refer to Appendix A for drawings of the heatsinks and CEK spring. The screws and standoffs are standard components that are made captive to the heatsink for ease of handling and assembly.

Contact your Intel field sales representative for an electronic version of mechanical and thermal models of the CEK (Pro/Engineer*, IGES and Icepak*, Flotherm* formats). Pro/Engineer*, Icepak* and Flotherm* models are available on Intel Business Link (IBL).

Note: Intel reserves the right to make changes and modifications to the design as necessary.

Note: The 1U/2U thermal mechanical reference designs for the Dual-Core Intel Xeon Processor 5100 Series was verified according to the Intel validation criteria given in Appendix D.1. The AdvancedTCA solution for the Dual-Core Intel Xeon Processor 5138 has not been fully validated. Any thermal mechanical design using some of the reference components in combination with any other thermal mechanical solution needs to be fully validated according to the customer criteria. Also, if customer thermal mechanical validation criteria differ from the Intel criteria, the reference solution should be validated against the customer criteria.

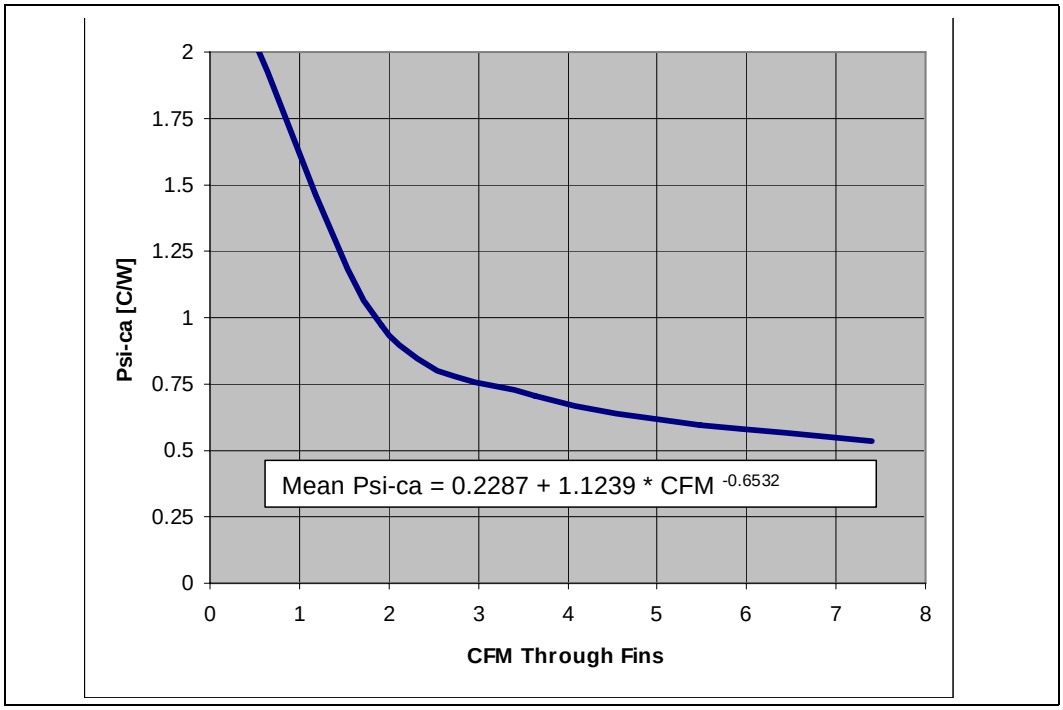
2.4.4.3 Structural Considerations of CEK

As Intel explores methods of keeping thermal solutions within the air-cooling space, the mass of the thermal solutions is increasing. Due to the flexible nature (and associated large deformation) of baseboard-only attachments, Intel reference solutions, such as CEK, are now commonly using direct chassis attach (DCA) as the mechanical retention design. The mass of the new thermal solutions is large enough to require consideration for structural support and stiffening on the chassis. Intel has published a best know method (BKM) document that provides specific structural guidance for designing DCA thermal solutions. The document is titled *Chassis Strength and Stiffness Measurement and Improvement Guidelines for Direct Chassis Attach Solutions*.

2.4.5 Thermal Solution Performance Characteristics

Figure 12 shows the performance of the AdvancedTCA* passive heatsink. These figures show the thermal performance of the heatsink versus the airflow provided. The best-fit equations for these curves are also provided to make it easier for users to determine the desired value without any error associated with reading the graph.

Figure 12. AdvancedTCA Heatsink Thermal Performance



If other custom heatsinks are intended for use with the Dual-Core Intel® Xeon® Processor 5100 Series, they must support the following interface control requirements to be compatible with the reference mechanical components:

Requirement 1: Heatsink assembly must stay within the volumetric keep-in.

Requirement 2: Maximum mass and center of gravity.

Requirement 3: Maximum and minimum compressive load.

Any custom thermal solution design must meet the loading specification as documented within this document, and should refer to the *Dual-Core Intel® Xeon® Processor 5100 Series Datasheet and LGA771 Socket Mechanical Design Guide* and for specific details on package/socket loading specifications.

2.4.6 Thermal Profile Adherence

The AdvancedTCA Intel reference thermal solution is designed to meet the Short-Term Thermal Profile for the Dual-Core Intel® Xeon® Processor LV 5138. From Table 6 the three-sigma (mean+3sigma) performance of the thermal solution is computed to be 0.816 °C/W and the processor local ambient temperature (T_{LA}) for this thermal solution is 55°C. Hence, the Thermal Profile equation for this thermal solution is calculated as:

Equation 8. y = 0.816x + 55

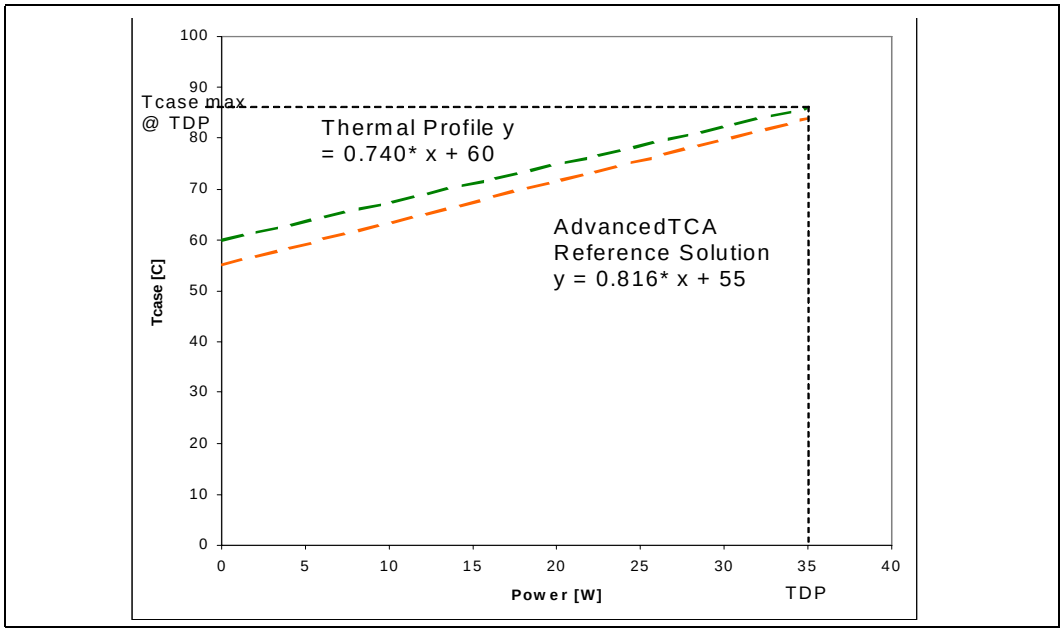
where,

y = Processor T_{CASE} value (°C)

x = Processor power value (W)

Figure 13 below shows the comparison of this reference thermal solution's Thermal Profile to the Short-Term Dual-Core Intel® Xeon® Processor LV 5138 Thermal Profile specification. The AdvancedTCA* solution meets the Thermal Profile with 1.9°C margin at the upper end (TDP). By designing to Thermal Profile, it is ensured that no measurable performance loss due to TCC activation is observed under the given environmental conditions.

Figure 13. AdvancedTCA* Thermal Adherence to Short-Term Dual-Core Intel® Xeon® Processor LV 5138 Thermal Profile



The AdvancedTCA* Intel reference thermal solution is designed to meet the Nominal Thermal Profile for the Dual-Core Intel Xeon Processor LV 5138. From Table 7 the three-sigma (mean+3sigma) performance of the thermal solution is computed to be 0.816 °C/W and the processor local ambient temperature (T_{LA}) for this thermal solution is 40 °C. Hence, the Thermal Profile equation for this thermal solution is calculated as:

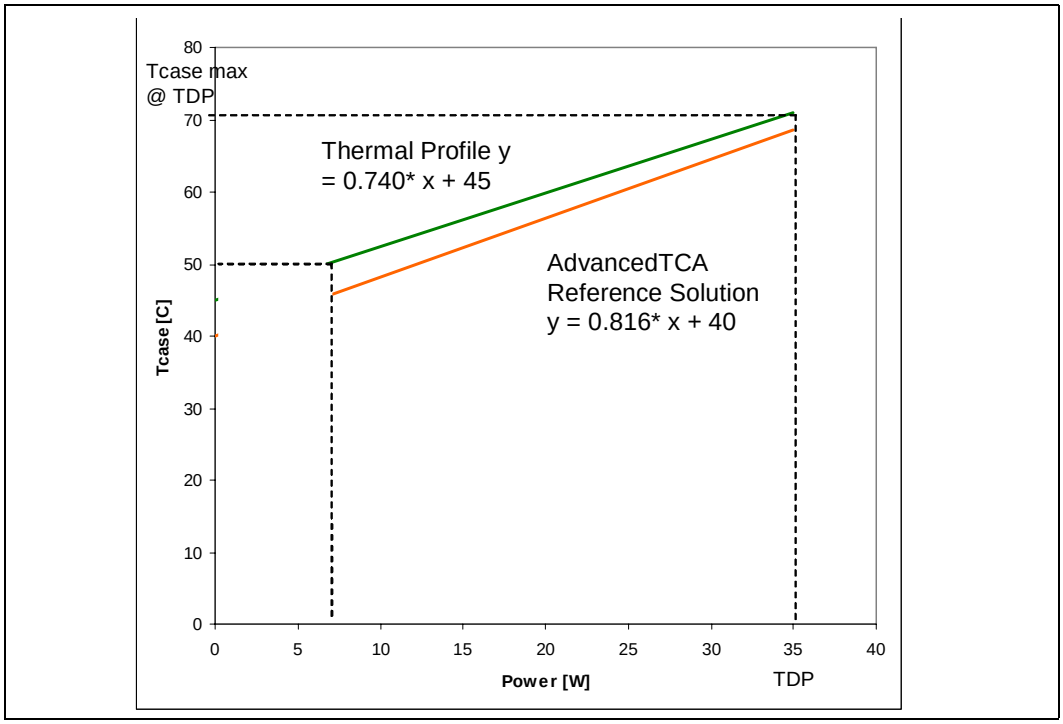
Equation 9. $y = 0.816x + 40$

where,

y = Processor T_{CASE} value (°C)
x = Processor power value (W)

Figure 13 below shows the comparison of this reference thermal solution's Thermal Profile to the Nominal Dual-Core Intel Xeon Processor LV 5138 Thermal Profile specification. The AdvancedTCA* solution meets the Thermal Profile with 2.3°C margin at the upper end (TDP). By designing to Thermal Profile, it is ensured that no measurable performance loss due to TCC activation is observed under the given environmental conditions.

Figure 14. AdvancedTCA* Thermal Adherence to Nominal Dual-Core Intel® Xeon® Processor LV 5138 Thermal Profile

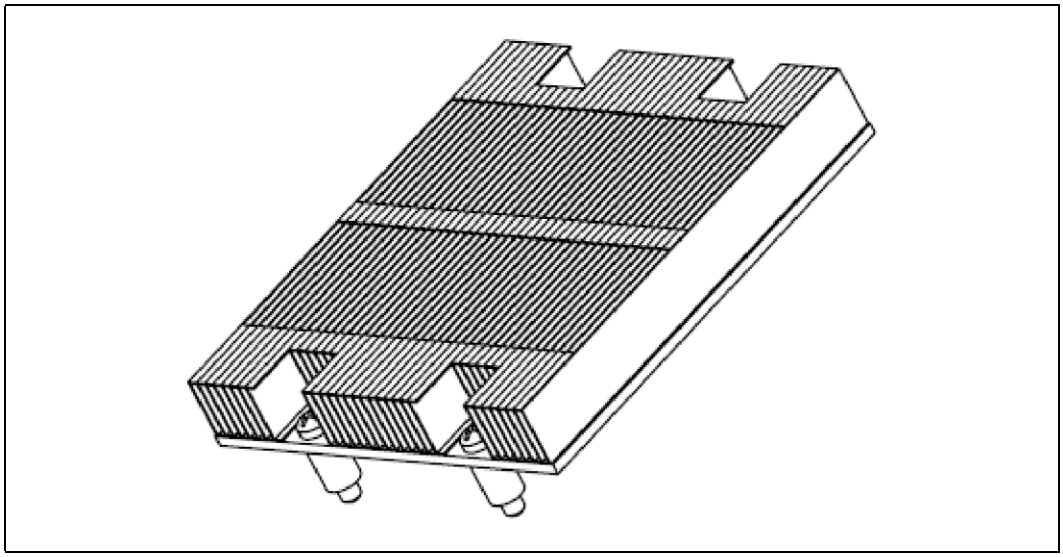


2.4.7 Components Overview

2.4.7.1 Heatsink with Captive Screws and Standoffs

The CEK reference heatsink uses snapped-fin technology for its design. It consists of a copper base and copper fins with Honeywell* PCM45F or Shin-Etsu* G751 thermal grease as the TIM. The mounting screws and standoffs are also made captive to the heatsink base for ease of handling and assembly as shown in Figure 15 for the AdvancedTCA* heatsinks, respectively.

Figure 15. Isometric View of the AdvancedTCA* CEK Heatsink



Note: Refer to Appendix A for more detailed mechanical drawings of the heatsink.

The function of the standoffs is to provide a bridge between the chassis and the heatsink for attaching and load carrying. When assembled, the heatsink is rigid against the top of the standoff, and the standoff is rigid to a chassis standoff with the CEK spring firmly sandwiched between the two. In dynamic loading situations the standoff carries much of the heatsink load, especially in lateral conditions, when compared to the amount of load transmitted to the processor package. As such, it is comprised of steel. The distance from the bottom of the heatsink to the bottom of the standoff is 8.79 mm [0.346 in.] for a board thickness of 1.57 mm [0.062 in]. The standoff will need to be modified for use in applications with a different board thickness, as defined in Section 2.4.4.2.

The function of the screw is to provide a rigid attach method to sandwich the entire CEK assembly together, activating the CEK spring under the baseboard, and thus providing the TIM preload. A screw is an inexpensive, low profile solution that does not negatively impact the thermal performance of the heatsink due to air blockage. Any fastener (i.e. head configuration) can be used as long as it is of steel construction; the head does not interfere with the heatsink fins, and is of the correct length of 20.64 mm [0.8125 in.].

Although the CEK heatsink fits into the legacy volumetric keep-in, it has a larger footprint due to the elimination of retention mechanism and clips used in the older enabled thermal/mechanical components. This allows the heatsink to grow its base and fin dimensions, further improving the thermal performance. A drawback of this enlarged size and use of copper for both the base and fins is the increased weight of the heatsink. The retention scheme employed by CEK is designed to support heavy heatsinks (approximately up to 1000 grams) in cases of shock, vibration and installation as explained in Appendix D. Some of the thermal and mechanical characteristics of the CEK heatsinks are shown in Table 9.

Table 9. CEK Heatsink Thermal Mechanical Characteristics

Size	Height (mm) [in.]	Weight (kg) [lbs]	Target Airflow Through Fins (m^3/hr) [CFM]	Mean Ψ_{ca} (°C/W)	Standard Deviation Ψ_{ca} (°C/W)
ATCA	13.36 [2.00]	0.24 [0.53]	4.59 [2.7]	0.816	0.007

2.4.7.2 Thermal Interface Material (TIM)

A TIM must be applied between the package and the heatsink to ensure thermal conduction. The CEK reference design uses Shin-Etsu* G751 thermal grease.

The recommended grease dispenses weight to ensure full coverage of the processor IHS is given below. For an alternate TIM, full coverage of the entire processor IHS is recommended.

Table 10. Recommended Thermal Grease Dispense Weight

Processor	Minimum	Maximum	Units	Notes
TIM Dispense weight		400	mg	Shin-Etsu* G751. Dispense weight is an approximate target.
TIM loading provided by CEK	18 80	30 133	lbf N	Generated by the CEK.

It is recommended that you use thermally conductive grease. Thermally conductive grease requires special handling and dispense guidelines. The following guidelines apply to Shin-Etsu G751* thermal grease. For guidance with your specific application, please contact the vendor. Vendor information is provided in Appendix E. The use of a semi-automatic dispensing system is recommended for high volume assembly to ensure an accurate amount of grease is dispensed on top of the IHS prior to assembly of the heatsink. A typical dispense system consists of an air pressure and timing controller, a hand held output dispenser, and an actuation foot switch. Thermal grease in cartridge form is required for dispense system compatibility. A precision scale with an accuracy of ±5 mg is recommended to measure the correct dispense weight and set the corresponding air pressure and duration. The IHS surface should be free of foreign materials prior to grease dispense.

Additional recommendations include recalibrating the dispense controller settings after any two hour pause in grease dispense. The grease should be dispensed just prior to heatsink assembly to prevent any degradation in material performance. Finally, the thermal grease should be verified to be within its recommended shelf life before use.

The CEK reference solution is designed to apply a compressive load of up to 200 N [45 lbf] on the TIM to improve the thermal performance.

2.4.7.3 CEK Spring

The CEK spring, which is attached on the secondary side of the baseboard, is made from 0.80 mm [0.0315 in.] thick 301 stainless steel half hard. Any future versions of the spring will be made from a similar material. The CEK spring has four embosses which, when assembled, rest on the top of the chassis standoffs. The CEK spring is located between the chassis standoffs and the heatsink standoffs. The purpose of the CEK spring is to provide compressive preload at the TIM interface when the baseboard is pushed down upon it. This spring does not function as a clip of any kind. The two tabs on the spring are used to provide the necessary compressive preload for the TIM when the whole solution is assembled. The tabs make contact on the secondary side of

the baseboard. In order to avoid damage to the contact locations on the baseboard, the tabs are insulated with a 0.127 mm [0.005 in.] thick Kapton* tape (or equivalent). Figure 16 shows an isometric view of the CEK spring design.

Figure 16. CEK Spring Isometric View

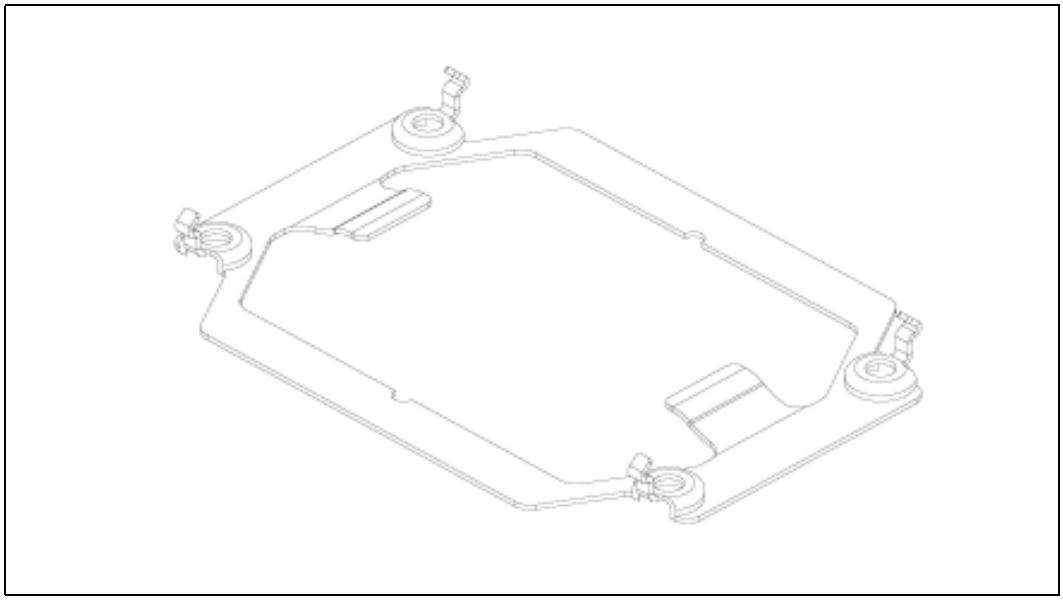
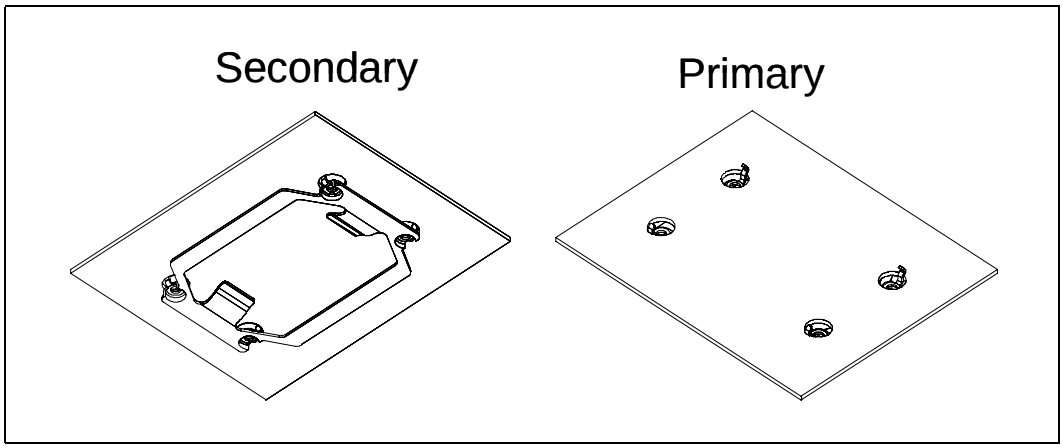


Figure 17. Isometric View of CEK Spring Attachment to the Base Board



Please refer to Appendix A for more detailed mechanical drawings of the CEK spring. Also, the baseboard keepout requirements shown in Appendix A must be met to use this CEK spring design.

Appendix A Mechanical Drawings

The mechanical drawings included in this appendix refer to the thermal mechanical enabling components for the Dual-Core Intel Xeon Processor 5100 Series.

Note: Intel reserves the right to make changes and modifications to the design as necessary.

Table 11. Mechanical Drawing List

Drawing Description	Figure Number
"AdvancedTCA* CEK Heatsink (Sheet 1 of 3)"	Figure 18
"AdvancedTCA* CEK Heatsink (Sheet 2 of 3)"	Figure 19
"AdvancedTCA* CEK Heatsink (Sheet 3 of 3)"	Figure 20
"CEK Spring (Sheet 1 of 3)"	Figure 21
"CEK Spring (Sheet 2 of 3)"	Figure 22
"CEK Spring (Sheet 3 of 3)"	Figure 23
"Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 1 of 6)"	Figure 24
"Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 2 of 6)"	Figure 25
"Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 3 of 6)"	Figure 26
"Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 4 of 6)"	Figure 27
"Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 5 of 6)"	Figure 28
"Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 6 of 6)"	Figure 29

Figure 18. AdvancedTCA* CEK Heatsink (Sheet 1 of 3)

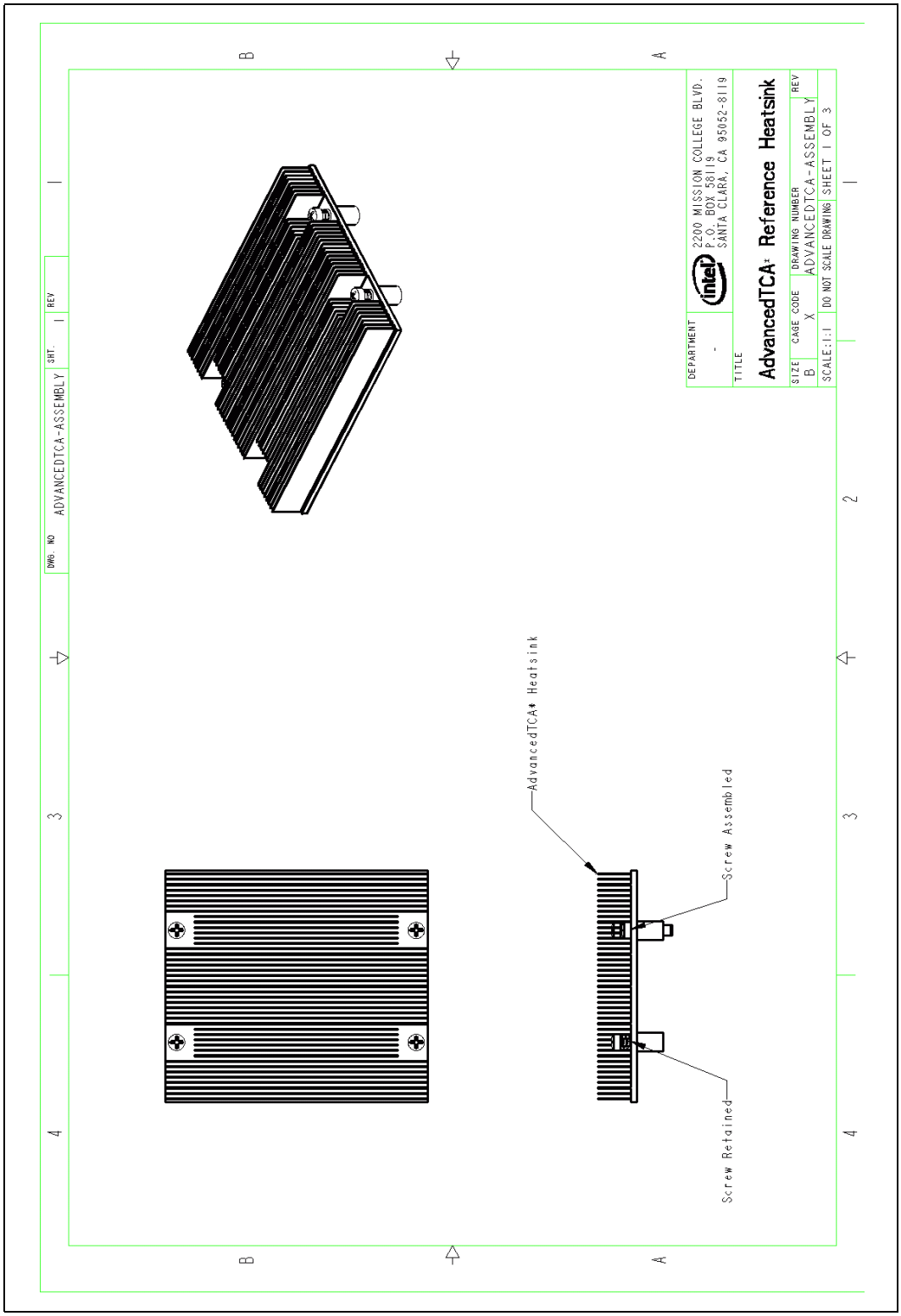


Figure 19. AdvancedTCA* CEK Heatsink (Sheet 2 of 3)

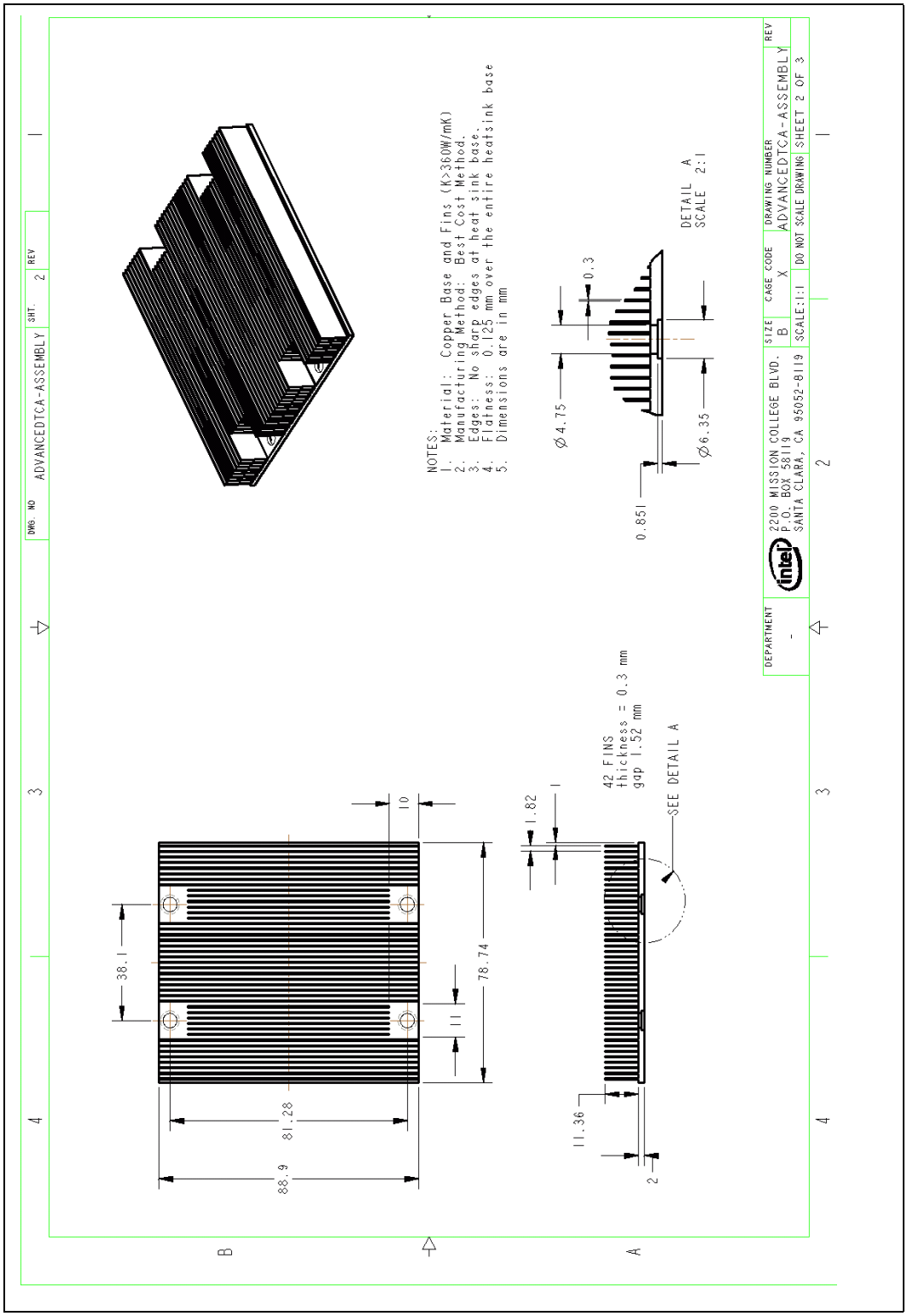


Figure 20. AdvancedTCA* CEK Heatsink (Sheet 3 of 3)

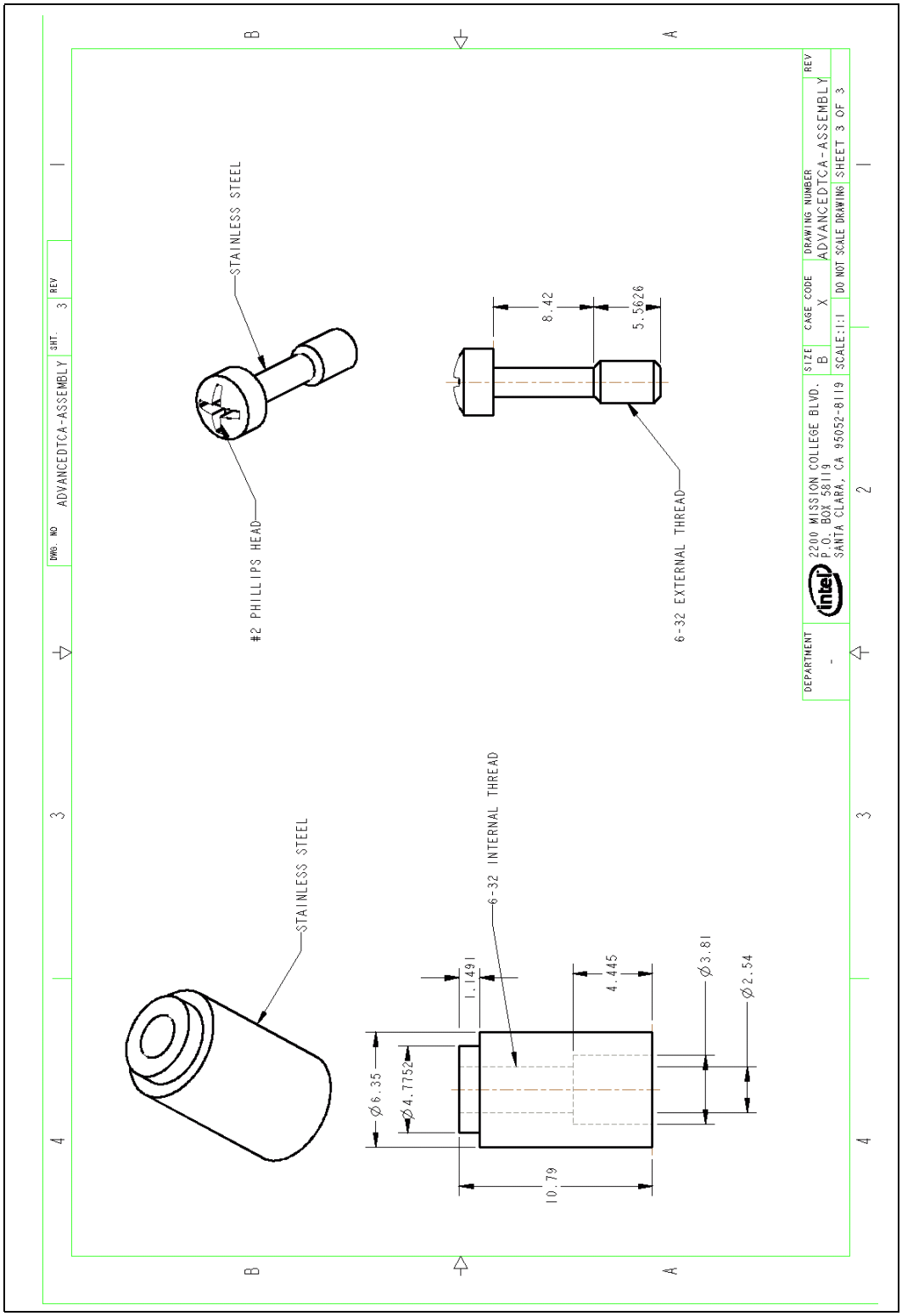


Figure 21. CEK Spring (Sheet 1 of 3)

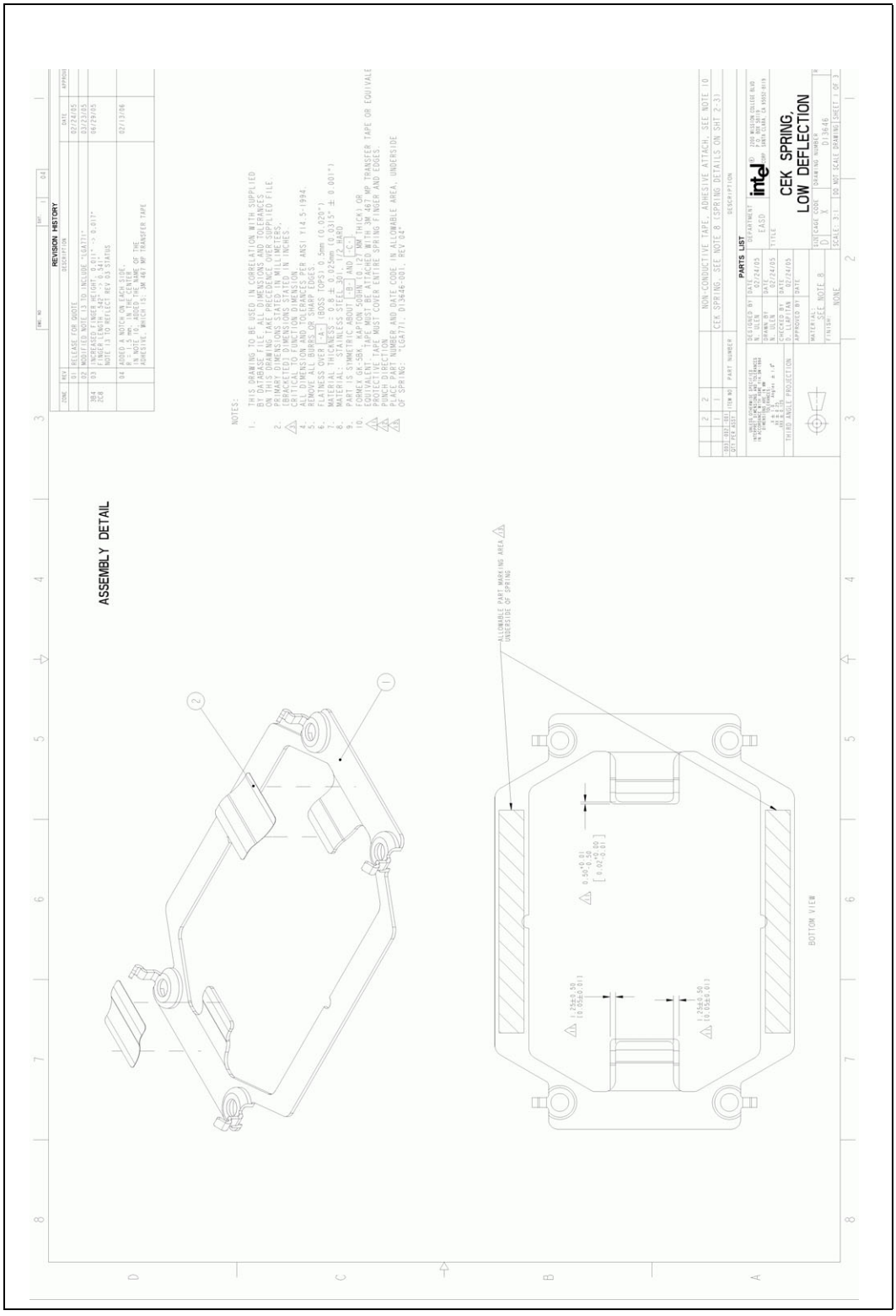


Figure 22. CEK Spring (Sheet 2 of 3)

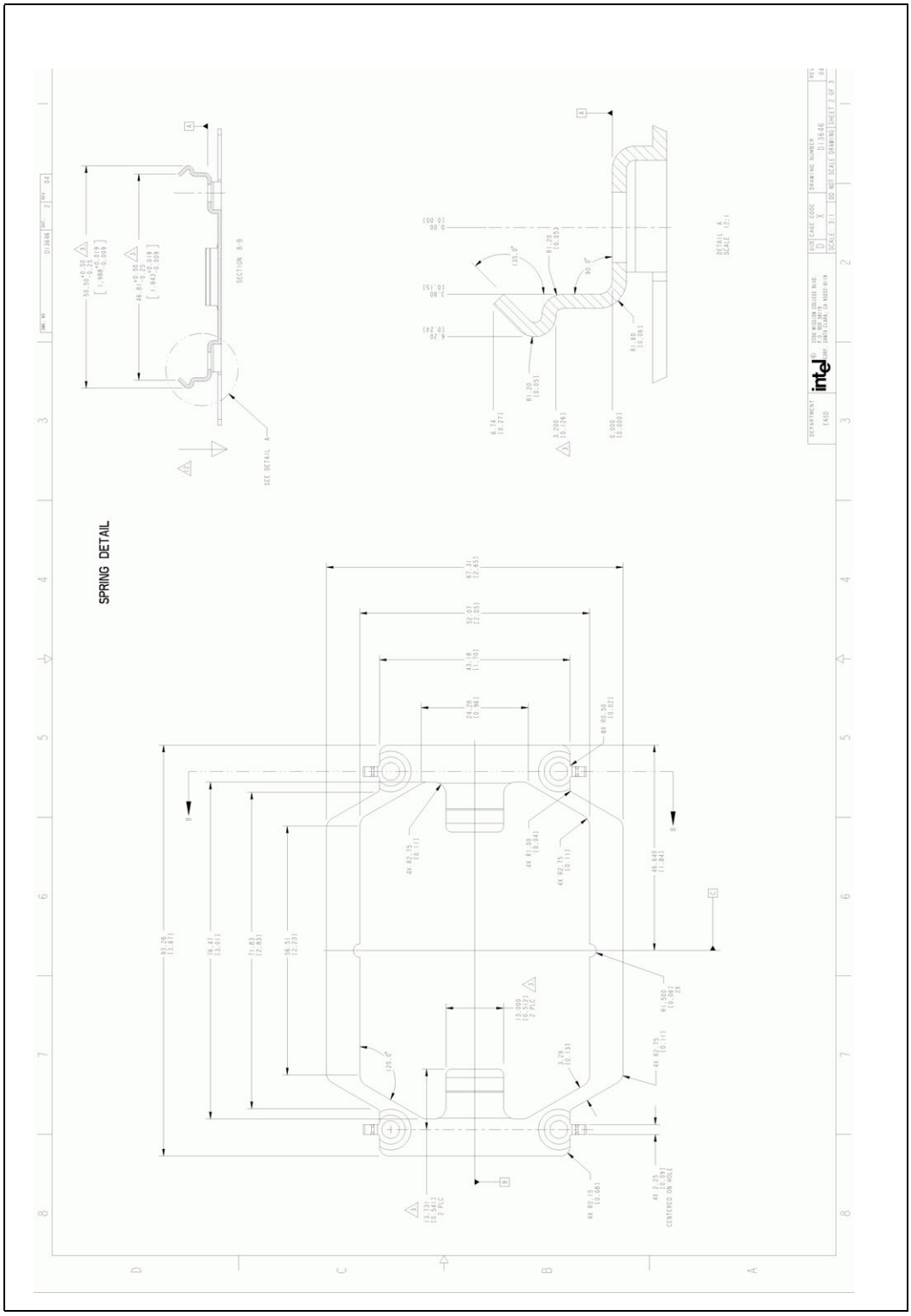


Figure 23. CEK Spring (Sheet 3 of 3)

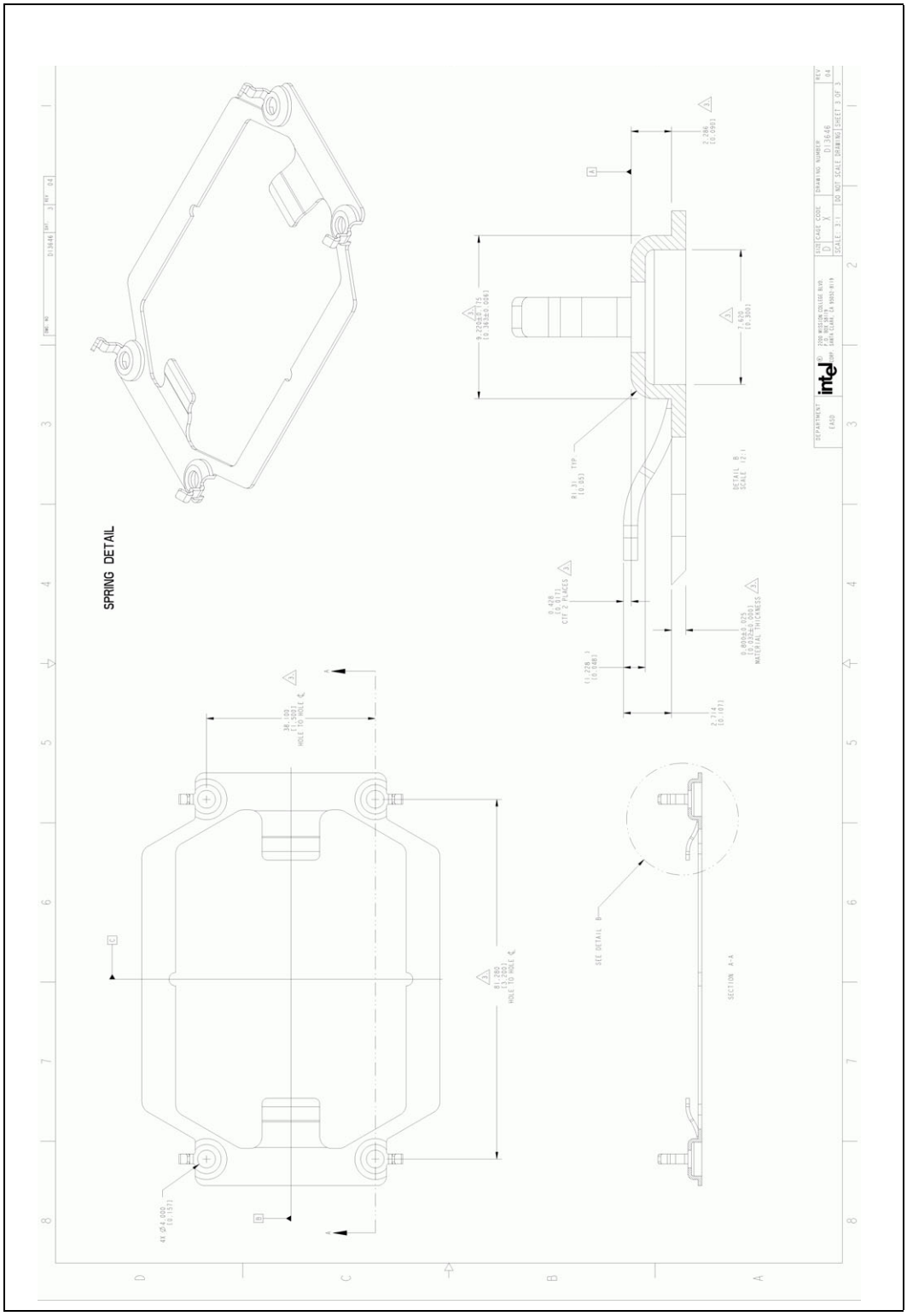


Figure 24. Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 1 of 6)

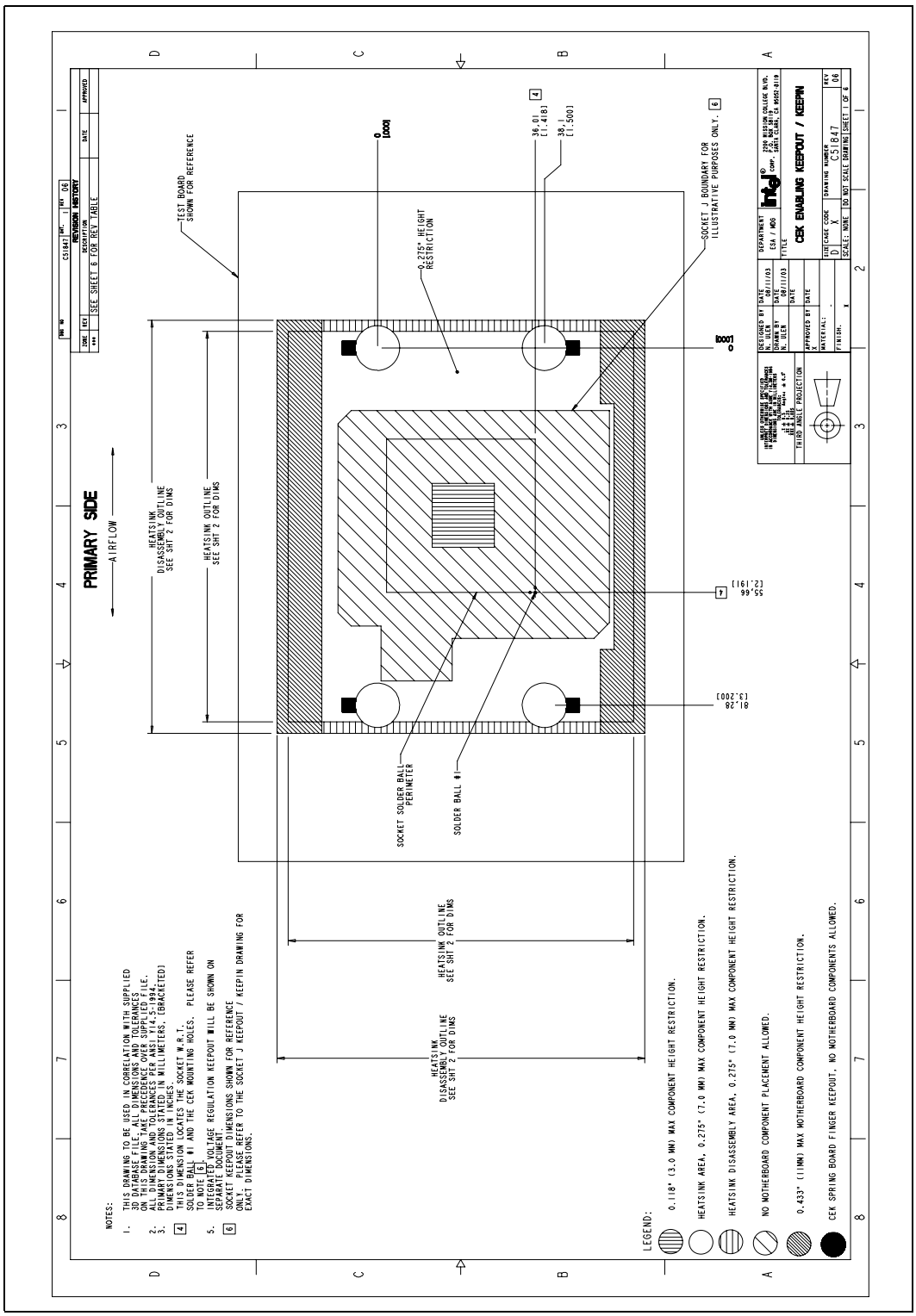


Figure 25. Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 2 of 6)

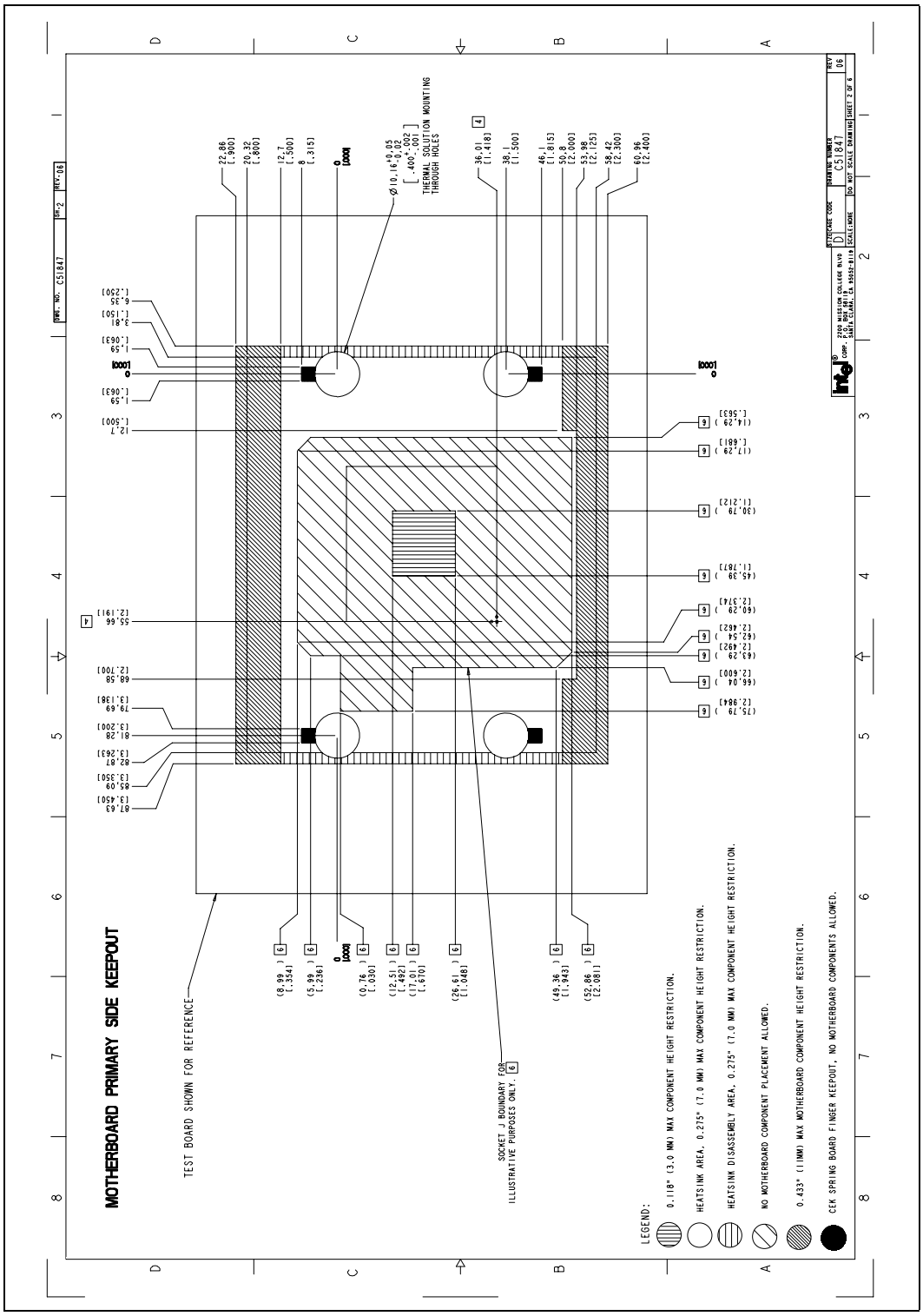


Figure 26. Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 3 of 6)

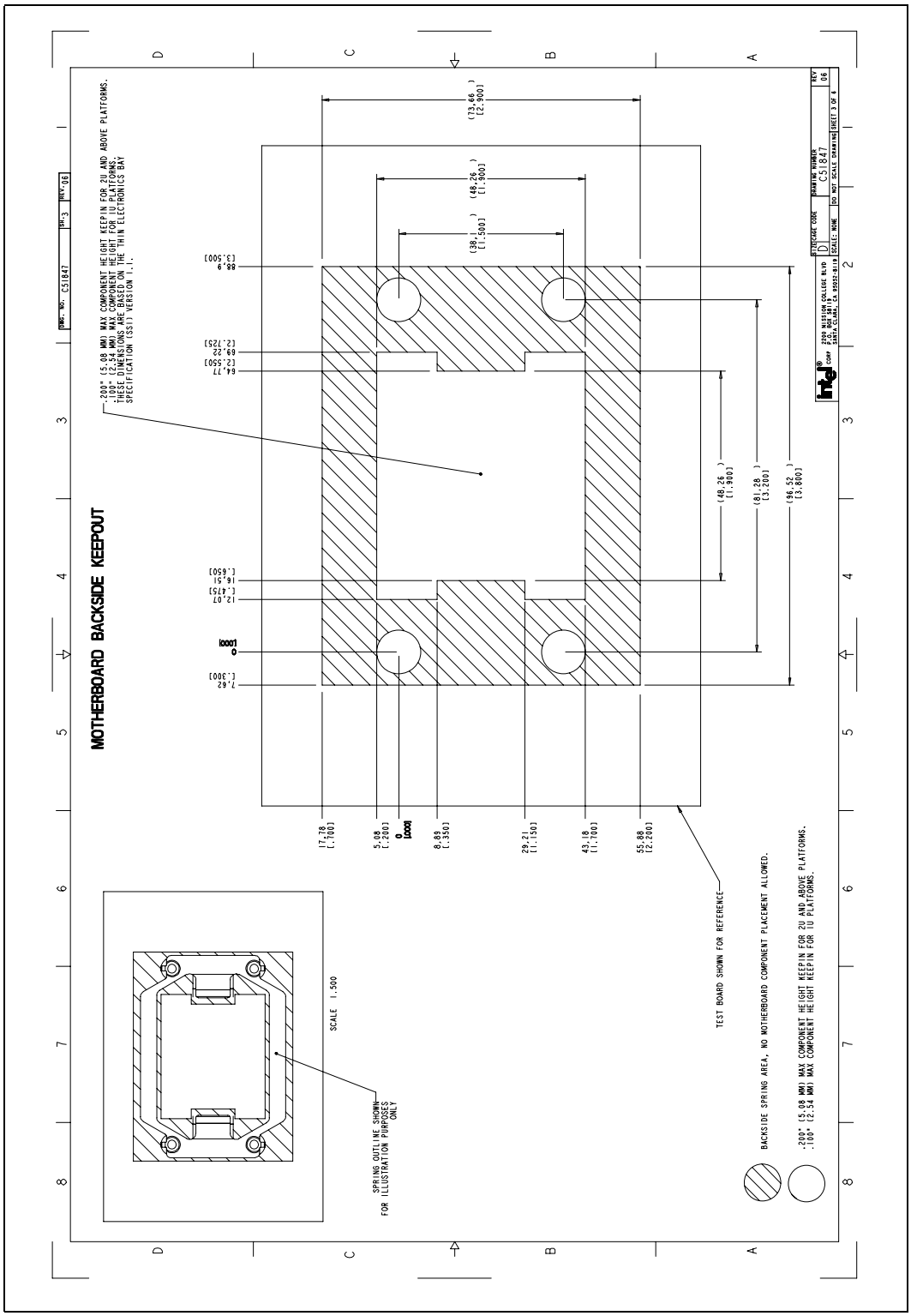


Figure 27. Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 4 of 6)

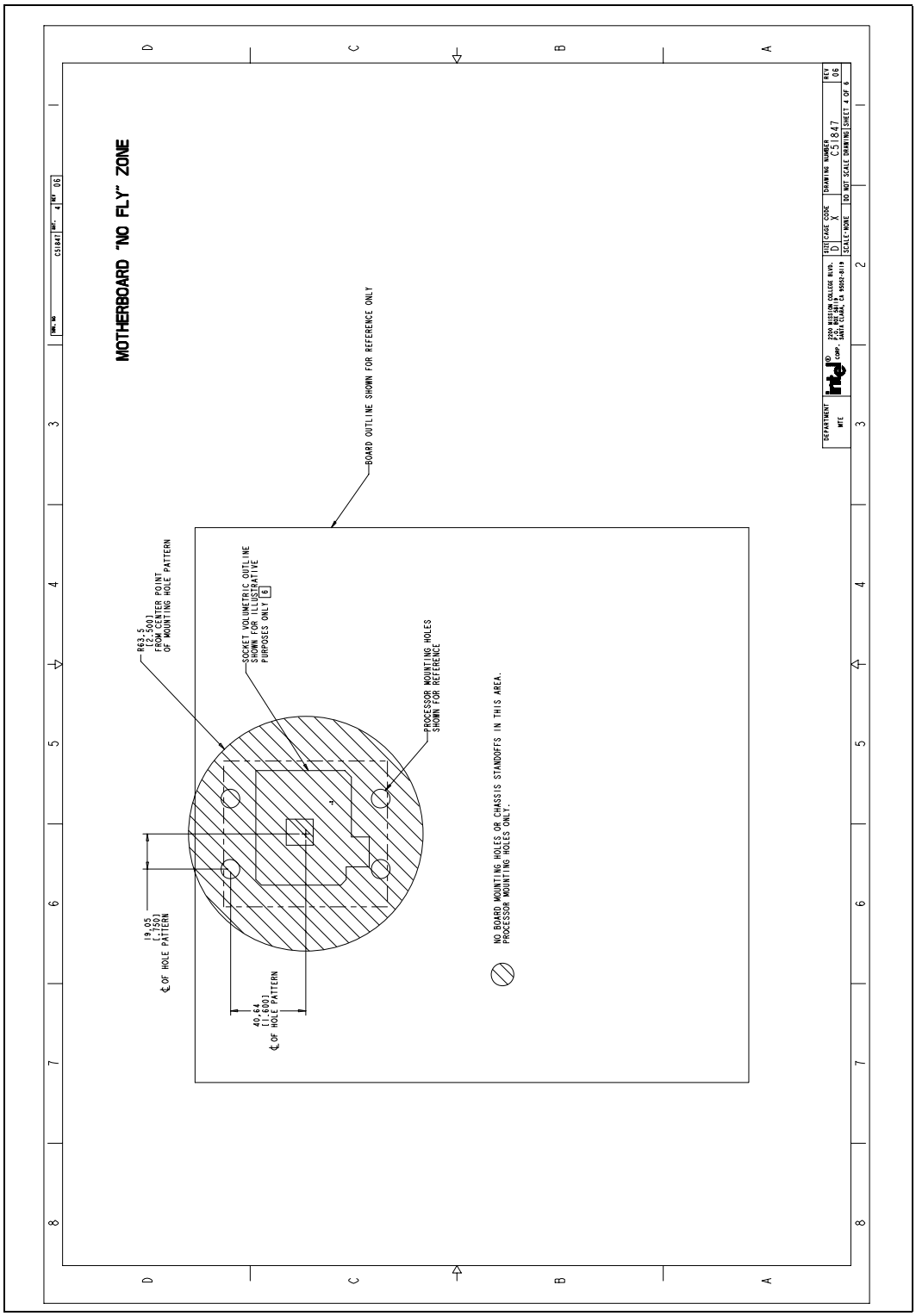


Figure 28. Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 5 of 6)

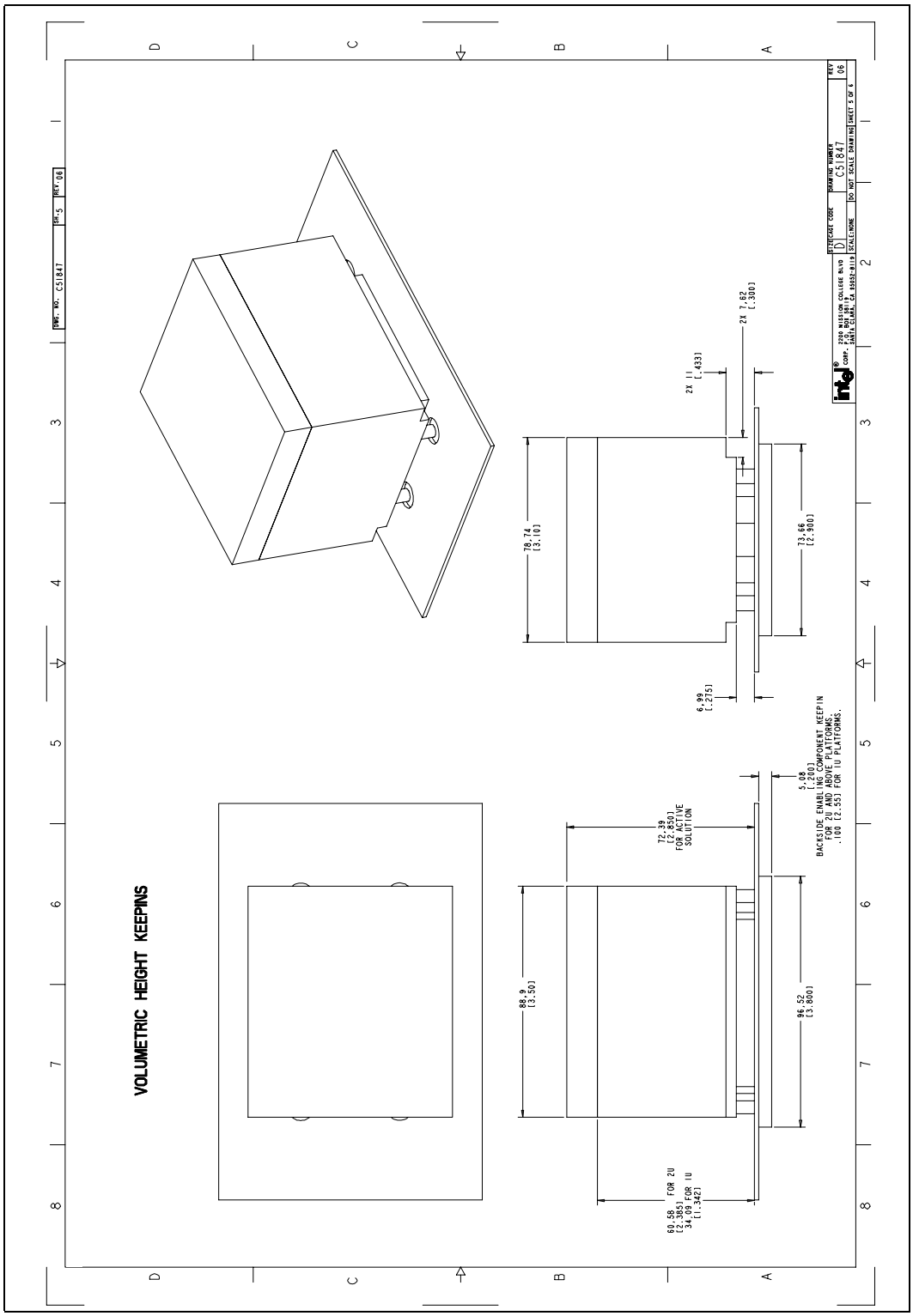
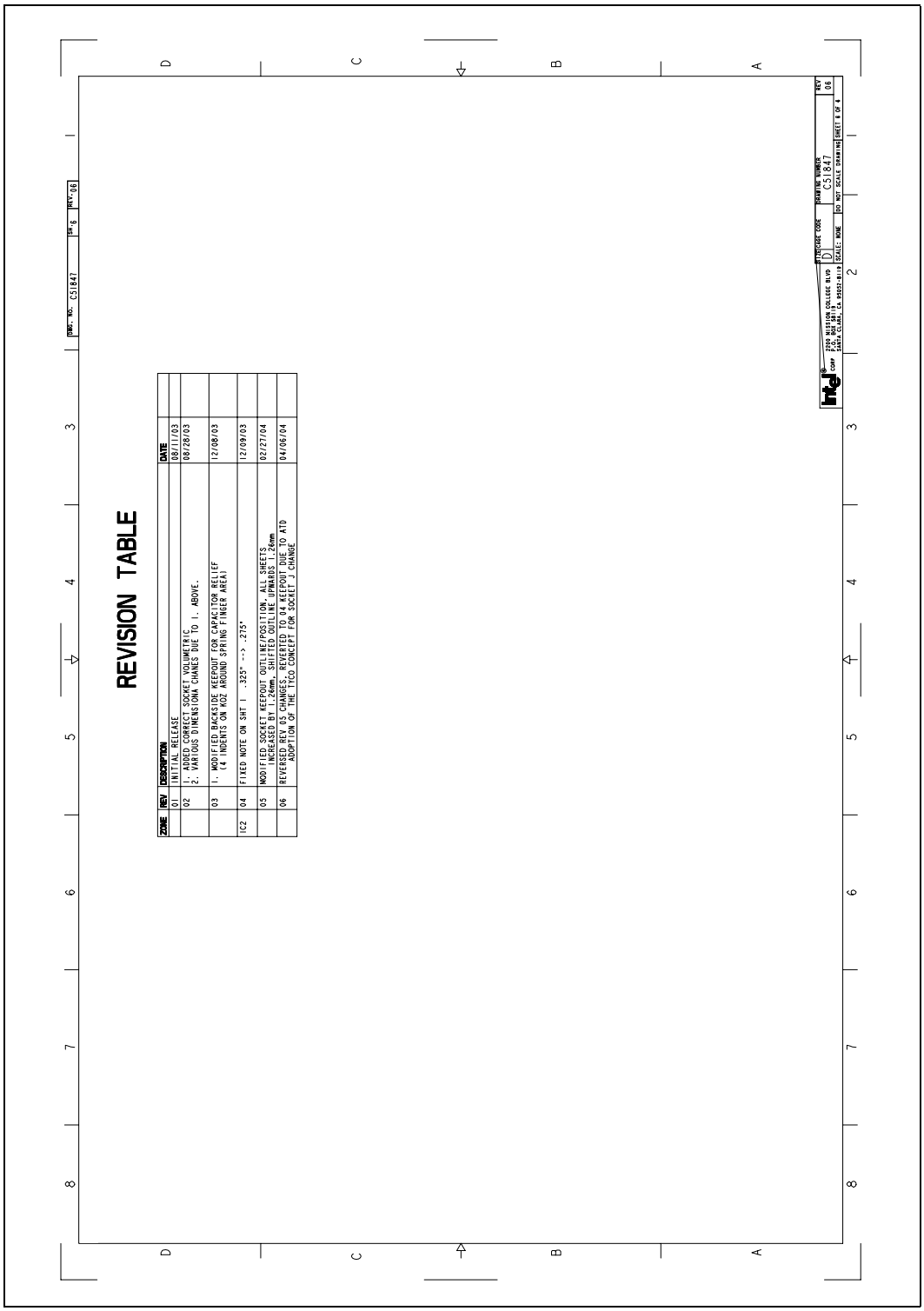
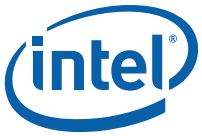


Figure 29. Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 6 of 6)





Appendix B Heatsink Clip Load Methodology

B.1 Overview

This section describes a procedure for measuring the load applied by the heatsink/clip/fastener assembly on a processor package.

This procedure is recommended to verify the preload is within the design target range for a design, and in different situations. For example:

- Heatsink preload for the LGA771 socket.
- Quantify preload degradation under bake conditions.

Note: This document reflects the current metrology used by Intel. Intel is continuously exploring new ways to improve metrology. Updates will be provided later as this document is revised as appropriate.

B.2 Test Preparation

B.2.1 Heatsink Preparation

Three load cells are assembled into the base of the heatsink under test, in the area interfacing with the processor Integrated Heat Spreader (IHS), using load cells equivalent to those listed in Section B.2.3.

To install the load cells, machine a pocket in the heatsink base, as shown in Figure 30 and Figure 31. The load cells should be distributed evenly, as close as possible to the pocket walls. Apply wax around the circumference of each load cell and the surface of the pocket around each cell to maintain the load cells in place during the heatsink installation on the processor and motherboard.

The depth of the pocket depends on the height of the load cell used for the test. It is necessary that the load cells protrude out of the heatsink base. However, this protrusion should be kept minimal, as it will create an additional load offset since the heatsink base is artificially raised. The measurement load offset depends on the whole assembly stiffness (i.e., motherboard, clip, fastener, etc.).

For example, the Dual-Core Intel Xeon Processor 5100 Series CEK Reference Heatsink Design clip and fasteners assembly have a stiffness of around 160 N/mm [915 lb/in]. If the resulting protrusion is 0.038 mm [0.0015”], then a extra load of 6.08 N [1.37 lb] will be created, and will need to be subtracted from the measured load. Figure 32 shows an example using the Dual-Core Intel Xeon Processor 5100 Series CEK Reference Heatsink designed for the Dual-Core Intel Xeon Processor 5100 Series in the 771–land grid array (LGA) package.

Note: When optimizing the heatsink pocket depth, the variation of the load cell height should also be taken into account to make sure that all load cells protrude equally from the heatsink base. It may be useful to screen the load cells prior to installation to minimize variation.

B.2.2 Alternate Heatsink Sample Preparation

As just mentioned, making sure that the load cells have minimum protrusion out of the heatsink base is paramount to meaningful results. An alternate method to make sure that the test setup will measure loads representative of the non-modified design is:

- Machine the pocket in the heatsink base to a depth such that the tips of the load cells are just flush with the heatsink base.
- Then machine back the heatsink base by around 0.25 mm [0.01”], so that the load cell tips protrude beyond the base.

Proceeding this way, the original stack height of the heatsink assembly should be preserved. This should not affect the stiffness of the heatsink significantly.

Figure 30. Load Cell Installation in Machined Heatsink Base Pocket -- Bottom View

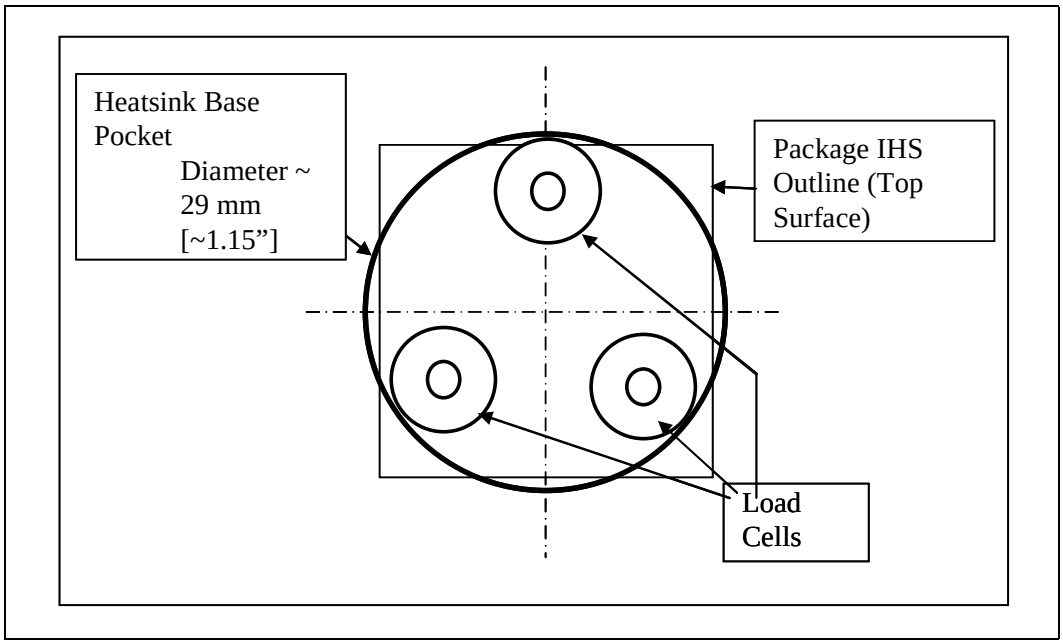


Figure 31. Load Cell Installation in Machined Heatsink Base Pocket -- Side View

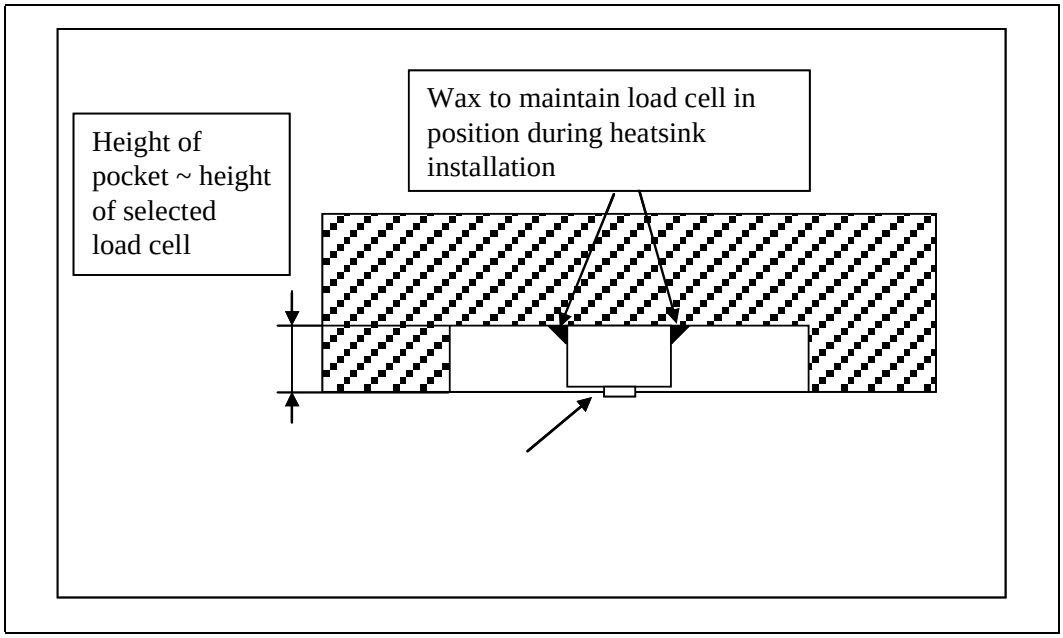
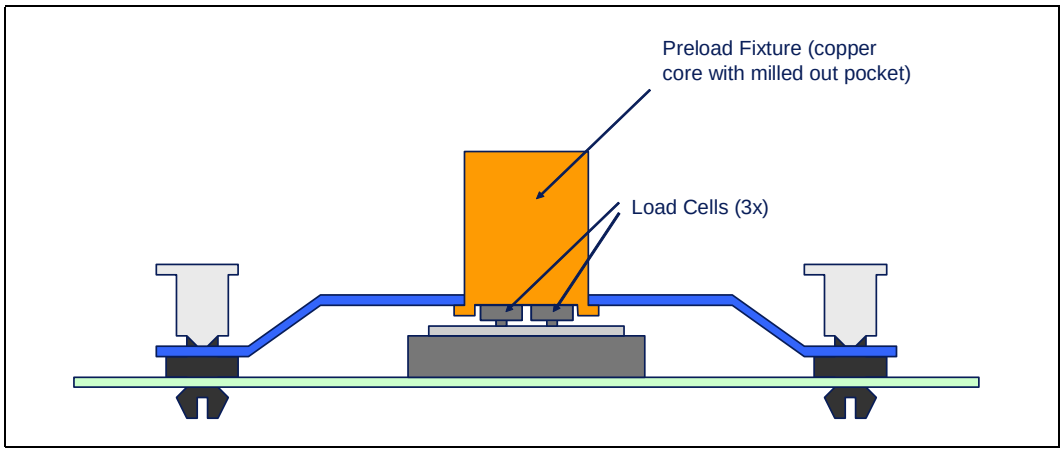


Figure 32. Preload Test Configuration



B.2.3 Typical Test Equipment

For the heatsink clip load measurement, use equivalent test equipment to the one listed Table 12.

Table 12. Typical Test Equipment

Item	Description	Part Number (Model)
Load cell Notes: 1, 5	Honeywell*-Sensotec* Model 13 subminiature load cells, compression only Select a load range depending on load level being tested. www.sensotec.com	AL322BL
Data Logger (or scanner) Notes: 2, 3, 4	Vishay* Measurements Group Model 6100 scanner with a 6010A strain card (one card required per channel).	Model 6100

Notes:
1. Select load range depending on expected load level. It is usually better, whenever possible, to operate in the high end of the load cell capability. Check with your load cell vendor for further information.
2. Since the load cells are calibrated in terms of mV/V, a data logger or scanner is required to supply 5 volts DC excitation and read the mV response. An automated model will take the sensitivity calibration of the load cells and convert the mV output into pounds.
3. With the test equipment listed above, it is possible to automate data recording and control with a 6101-PCI card (GPIB) added to the scanner, allowing it to be connected to a PC running LabVIEW* or Vishay's StrainSmart* software.
4. **IMPORTANT**: In addition to just a zeroing of the force reading at no applied load, it is important to calibrate the load cells against known loads. Load cells tend to drift. Contact your load cell vendor for calibration tools and procedure information.
5. When measuring loads under thermal stress (bake for example), load cell thermal capability must be checked, and the test setup must integrate any hardware used along with the load cell. For example, the Model 13 load cells are temperature compensated up to 71 °C, as long as the compensation package (spliced into the load cell's wiring) is also placed in the temperature chamber. The load cells can handle up to 121 °C (operating), but their uncertainty increases according to 0.02% rdg/°F.

B.2.4 Test Procedure Examples

The following sections give two examples of load measurement. However, this is not meant to be used in mechanical shock and vibration testing.

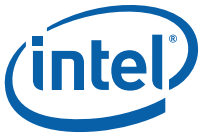
Any mechanical device used along with the heatsink attach mechanism will need to be included in the test setup (i.e., back plate, attach to chassis, etc.).

Prior to any test, make sure that the load cell has been calibrated against known loads, following load cell vendor's instructions.

B.2.5 Time-Zero, Room Temperature Preload Measurement

1. Pre-assemble mechanical components on the board as needed prior to mounting the motherboard on an appropriate support fixture that replicate the board attach to a target chassis.

   For example: If the attach mechanism includes fixtures on the back side of the board, those must be included, as the goal of the test is to measure the load provided by the actual heatsink mechanism.
2. Install the test vehicle in the socket.
3. Assemble the heatsink reworked with the load cells to motherboard as shown for the Dual-Core Intel Xeon Processor 5100 Series CEK-reference heatsink example in Figure 32, and actuate attach mechanism.
4. Collect continuous load cell data at 1 Hz for the duration of the test. A minimum time to allow the load cell to settle is generally specified by the load cell vendors (often on the order of three minutes). The time zero reading should be taken at the end of this settling time.



5. Record the preload measurement (total from all three load cells) at the target time and average the values over 10 seconds around this target time as well, i.e., in the interval for example over [target time – 5 seconds; target time + 5 seconds].

B.2.6 Preload Degradation under Bake Conditions

This section describes an example of testing for potential clip load degradation under bake conditions.

1. Preheat thermal chamber to target temperature (45 ºC or 85 ºC for example).
2. Repeat time-zero, room temperature preload measurement.
3. Place unit into preheated thermal chamber for specified time.
4. Record continuous load cell data as follows:
   Sample rate = 0.1 Hz for first three hrs
   Sample rate = 0.01 Hz for the remainder of the bake test
5. Remove assembly from thermal chamber and set into room temperature conditions
6. Record continuous load cell data for next 30 minutes at sample rate of 1 Hz.

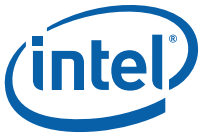
§

Appendix C Safety Requirements

Heatsink and attachment assemblies shall be consistent with the manufacture of units that meet the safety standards:

1. UL Recognition-approved for flammability at the system level. All mechanical and thermal enabling components must be a minimum UL94V-2 approved.
2. CSA Certification. All mechanical and thermal enabling components must have CSA certification.
3. Heatsink fins must meet the test requirements of UL1439 for sharp edges.

§



Appendix D Quality and Reliability Requirements

D.1 Intel Verification Criteria for the Reference Designs

D.1.1 Reference Heatsink Thermal Verification

The Intel reference heatsinks will be verified within specific boundary conditions using a TTV and the methodology described in the *Intel® Xeon® Processor Family Thermal Test Vehicle User's Guide*.

The test results, for a number of samples, are reported in terms of a worst-case mean + 3σ value for thermal characterization parameter using real processors (based on the TTV correction offset).

D.1.2 Environmental Reliability Testing

D.1.2.1 Structural Reliability Testing

The Intel reference heatsinks will be tested in an assembled condition, along with the LGA771 Socket. Details of the Environmental Requirements, and associated stress tests, can be found in the *LGA771 Socket Mechanical Design Guide*.

The use condition environment definitions provided in Appendix 13 are based on speculative use condition assumptions, and are provided as examples only.

Table 13. Use Conditions Environment

Use Environment	Speculative Stress Condition		Example Use Condition	Example 7-Yr Stress Equiv.	Example 10-Yr Stress Equiv.
Shipping and Handling	Mechanical Shock • System-level • Unpackaged • Trapezoidal • 25 g • velocity change is based on packaged weight		Total of 12 drops per system: • 2 drops per axis • ± direction	n/a	n/a
	Product Weight (lbs) < 20 lbs 20 to > 40 40 to > 80 80 to < 100 100 to < 120 ≥120	Non-palletized Product Velocity Change† (in/sec) 250 225 205 175 145 125			
	†Change in velocity is based upon a 0.5 coefficient of restitution.				
Shipping and Handling	Random Vibration • System Level • Unpackaged • 5 Hz to 500 Hz • 2.20 g RMS random • 5 Hz @ .001 g^2/Hz to 20 Hz @ 0.01 g^2/Hz (slope up) • 20 Hz to 500 Hz @ 0.01 g^2/Hz (flat) • Random control limit tolerance is ± 3 dB		Total per system: • 10 minutes per axis • 3 axes	n/a	n/a

Note: In the case of a discrepancy, information in the most recent *LGA771 Socket Mechanical Design Guidelines* supersedes that in the Table 13 above.

D.1.2.2 Recommended Test Sequence

Each test sequence should start with components (i.e., baseboard, heatsink assembly, etc.) that have not been previously submitted to any reliability testing.

The test sequence should always start with a visual inspection after assembly, and BIOS/Processor/memory test. The stress test should be then followed by a visual inspection and then BIOS/Processor/memory test.

D.1.2.3 Post-Test Pass Criteria

The post-test pass criteria are:

1. No significant physical damage to the heatsink and retention hardware.
2. Heatsink remains seated and its bottom remains mated flatly against the IHS surface. No visible gap between the heatsink base and processor IHS. No visible tilt of the heatsink with respect to the retention hardware.

3. No signs of physical damage on baseboard surface due to impact of heatsink.
4. No visible physical damage to the processor package.
5. Successful BIOS/Processor/memory test of post-test samples.
6. Thermal compliance testing to demonstrate that the case temperature specification can be met.

D.1.2.4 Recommended BIOS/Processor/Memory Test Procedures

This test is to ensure proper operation of the product before and after environmental stresses, with the thermal mechanical enabling components assembled. The test shall be conducted on a fully operational baseboard that has not been exposed to any battery of tests prior to the test being considered.

Testing setup should include the following components, properly assembled and/or connected:

- Appropriate system baseboard
- Processor and memory
- All enabling components, including socket and thermal solution parts

The pass criterion is that the system under test shall successfully complete the checking of BIOS, basic processor functions and memory, without any errors. *Intel PC Diags* is an example of software that can be utilized for this test.

D.1.3 Material and Recycling Requirements

Material shall be resistant to fungal growth. Examples of non-resistant materials include cellulose materials, animal and vegetable based adhesives, grease, oils, and many hydrocarbons. Synthetic materials such as PVC formulations, certain polyurethane compositions (e.g. polyester and some polyethers), plastics which contain organic fillers of laminating materials, paints, and varnishes also are susceptible to fungal growth. If materials are not fungal growth resistant, then MIL-STD-810E, Method 508.4 must be performed to determine material performance.

Material used shall not have deformation or degradation in a temperature life test.

Any plastic component exceeding 25 grams should be recyclable per the European Blue Angel recycling standards.

The following definitions apply to the use of the terms lead-free, Pb-free, and RoHS compliant.

Lead-free and Pb-free: Lead has not been intentionally added, but lead may still exist as an impurity below 1000 ppm.

RoHS compliant: Lead and other materials banned in RoHS Directive are either (1) below all applicable substance thresholds as proposed by the EU or (2) an approved/ pending exemption applies.

Note: RoHS implementing details are not fully defined and may change.

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Appendix E Enabled Suppliers Information

E.1 Supplier Information

E.1.1 Intel Enabled Suppliers

The Intel reference enabling solution for Dual-Core Intel Xeon Processor 5100 Series is preliminary. The Intel reference solutions have not been verified to meet the criteria outlined in Appendix D. Customers can purchase the Intel reference thermal solution components from the suppliers listed in Table 14.

For additional details, please refer to the Dual-Core Intel Xeon Processor 5100 Series thermal mechanical enabling components drawings in Appendix A.

Table 14. Suppliers for the Dual-Core Intel Xeon Processor 5100 Series Intel Reference Solution

Assembly	Component	Description	Development Suppliers	Supplier Contact Info
AdvancedTCA* Heatsink	AdvancedTCA* Heatsinks P/N: ECC-00267-01-GP	Copper Fin, Copper Base includes PCM45F TIM+cover	Cooler Master*	Cooler Master* Wendy Lin 510-770-8566, x211 wendy@coolermaster.com
	Thermal Interface Material	Grease	Shin-Etsu G751 CNDA 75610	Donna Hartigan (480) 893-8898
	CEK Spring for CEK771 Intel p/n D13646 rev04	Stainless Steel 301, Kapton* Tape on Reinforced Spring Fingers	AVC CNDA 2085011	David Chao 886-2-22996390 x619 david_chao@avc.com.tw

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