Intel®80321 I/O Processor

Design Review Checklist

June 2002

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Figures

No figures used at this time

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Revision History

Date	Revision	Description
June 2002	001	Initial Release.

1.0 Introduction

This checklist is a compilation of key signals and strap options. It is not meant to be a complete signal list or a substitute for proper study of available design guides or reference schematics. Designers use this guide in conjunction with the *Intel® 80321 I/O Processor Design Guide*, built on Intel® XScale™ microarchitecture (ARM architecture compliant) and the Intel® IQ80321 evaluation platform board schematics. References are in Table 1 below.

1.1 List of References

Table 1. List of References

Document	Document Number/Reference
Intel® 80321 I/O Processor Datasheet	273518
Intel® 80321 I/O Processor Developer's Manual	273517
Intel® 80321 I/O Processor Specification Update	273519
Intel® 80321 I/O Processor Design Guide	273520
PCI Local Bus Specification, Revision 2.2	http://www.pcisig.com/specifications/conventional_pci
PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a	http://www.pcisig.com/specifications/pci_x
PCI-X Compliance Checklist	http://www.pcisig.com/data/specifications/pci_x_checklist_1_0_a.doc
PCI 2.2 Compliance Checklist	http://www.pcisig.com/data/specifications/2_2_checklist.doc

1.2 Intel® 80321 I/O Processor Checklist

Table 2. Checklist (Sheet 1 of 5)

Category	Guideline	Compliance	
		Yes	No
PCI-X	Characteristic impedance of signal traces is 60 ±10% Ω.		
	Signal propagation delay of traces is between 150 and 190 ps/inch, inclusive. (Same as conventional PCI.)		
	Source bridge requires **IDSEL** inputs to be resistively coupled to **AD** bits, those resistors have a value of a least 2 KΩ.		
	Source bridge requires **IDSEL** inputs to be resistively coupled to **AD** bits, devices 1-4 connect to **AD[17]** through **AD[20]** respectively.		
	System includes slots for add-in cards, the system provides a circuit for sensing the connection of the **PCIXCAP** pin of all add-in cards.		
	PCIXCAP pin is connected to ground through a 0.01 ±10% µF capacitor for PCI-X 133, or through a 10 K ±5% resistor in parallel with a 0.01 ±10% mF capacitor for PCI-X 66.		
	PCIXCAP • maximum length between the resistor (if installed), cap and the connector is 0.25”. • maximum length between resistor (if installed), cap and ground is 0.1”. • this connector pin not connected to any other device pins or voltages.		
	PRSNT[1:2]# are connected to show correct power consumption.		
	All **GND** fingers are provided and are bussed together.		
	All bussed signals contain no more than ONE 10pF (max) load.		
	M66EN finger (pin 49, side B) is either an input or a no-connect. It is advisable to connect **P_M66EN** to a 0.01 µF capacitor located with-in 0.25 inches of the **M66EN** pin on a add-in connector.		
	PCI connector pins: Ensure 3.3 V pins (even if they are not actually delivering power), and any unused 5 V and V_{IO} pins on the PCI edge connector provide an ac return path. These pins must have plated edge fingers and be decoupled to the ground plane on the add-in board to ensure they continue to function as efficient ac reference points.		
	All RESERVED fingers are no-connect and are NOT bussed together.		
	Add-in card protection circuitry on **INTA/B/C/D** to prevent damage to chip. Design Guide, section 6.2.3		
	Add-in card trace length for **AD[31::0]** is between 0.75 inches and 1.5 inches, inclusive.		
	Add-in card trace length for **AD[63::32]** is between 1.75 inches and 2.75 inches, inclusive.		
	Add-in card trace length for **RST#** is between 0.75 inches and 3.0 inches, inclusive.		
	Trace spacing, geometries, and materials limit cumulative crosstalk to 5% of the amplitude of the aggressor signal.		
	PCI Clock Trace length for **P_CLK** is between 2.4 inches and 2.6 inches, inclusive and routes only to one load for add-in card. (Same as conventional PCI.) Total length for non-add-in card is < 8” .		
	PCI Clock Buffer: **P_CLK**s lengths matched to .1” Design Guide, section 6.3.1. • PCI Clock Buffer: use low skew clock buffer [2] . • PCI Clock Buffer: **P_CLK** lines at least 25mils from each other and themselves.		
	PCI Address Bus AD: wiring lengths follow recommendations in Design Guide, section 6.4 dependent on speed and number of slots.		

Table 2. Checklist (Sheet 2 of 5)

Category	Guideline	Compliance	
		Yes	No
DDR Constraints: Design Guide Chapter 7			
DDR Source Synchronous Design Guide, section 7.4.1	Series Resistor **DQ/DQS/DM/CB** Series resistors = 10 Ω.		
	Parallel term resistor **DQ/DQS/DM/CB** = 60 Ω.		
	Trace Length 80321 BGA pin to series resistor 1.8 to 4.9”.		
	Trace Length series resistor to DIMM < 0.5”.		
	Trace Length to parallel resistor 0.1” to 0.8”.		
	Length Matching within group 0.025” – nine signals.		
	Length Matching over all signals to clock longest x-1” to shortest x-2”, x= clock length.		
DDR Clocked Signals Group Design Guide, section 7.4.2.1	Trace width 5 mils, trace spacing 7 mils and 20 mils between next closest trace.		
	Series resistors **M_CK/M_CK#** = 27 Ω.		
	Parallel term resistors **M_CK/M_CK#** = 120 Ω – ONLY for non-DIMM.		
	Trace Length 80321 BGA pin to series resistor not specified (closer to 80321).		
	Trace Length 1” to 7”.		
	Length Matching **M_CK/M_CK#** = 2 mils.		
	Length Matching between clock groups +/-25 mils.		
	M_CK polarity alternated (not two **M_CK#**s next to each other).		
	M_CK minimize layer changes (two vias or less).		
DDR Source Clocked Signals Termination (control) Design Guide, section 7.4.2.2	Series Resistor **RAS**, **CAS**, **WE**, **MA[12:0]**, **BA[1:0]** = 15 Ω.		
	Parallel term resistor **RAS**, **CAS**, **WE**, **MA[12:0]**, **BA[1:0]** = 60 Ω.. Resistor Packs are acceptable for the parallel control termination resistors but control signals can NOT be placed within the same RPACK as data, strobe, or command signals. Termination resistor: Rp 56 Ω +/- 1%.		
	Trace Length 80321 BGA pin to series resistor not specified (closer to 80321).		
	Trace Length 2” to 5”.		
	Trace Length to parallel resistor 0.1” to 0.8”.		
	Length Matching within group 0.025” – nine signals.		
DDR CS, CKE Design Guide, section 7.4.3	Series Resistor **CS**, **CKE** = 10 Ω.		
	Parallel term resistor **CS**, **CKE** = 60 Ω.		
	Trace Length 80321 BGA pin to series resistor not specified (closer to 80321).		
	Trace Length 2” to 5”.		
	Trace Length to parallel resistor 0.1” to 0.8”.		
	Length Matching over all signals to clock longest x-1” to shortest 2”, x= clock length.		
	Route on same layer as **M_CK**s.		
	Minimize layer changes (two vias or less).		
	Rp is needed for non-DIMM application 120 Ω +/- 1%.		
	Length Matching over all signals to clock longest x-1” to shortest 2”, x= clock length.		
DDR Voltages Design Guide, section 7.4.4	All Parallel termination Resistors pulled to **VTT_DDR** = +1.25V.		

Table 2. Checklist (Sheet 3 of 5)

Category	Guideline	Compliance	
		Yes	No
DDR Constraints: Design Guide Chapter 7 (Continued)			
V_{TT}	**V_{TT}** island at least 50 mils wide.		
	V_{TT} Decouple plane with 0.1 µF cap per two termination resistors.		
	V_{TT} Decouple plane with large 10uF or larger at each end of the termination island.		
	V_{TT} electrically isolated from the core voltage.		
	V_{TT} able to source/sink significant switching current for **DDR**s.		
V_{REF}	**DDR_VREF** = + 1.25 V and Electrically separate from **VTT_DDR.**		
	V_{REF} is generated with a resistor divider circuit off the 2.5 V voltage to create a stable 1.25 V reference. R1 and R2 are 49.9 Ω +/- 1%. Design Guide, Section 8, Figure 46.		
VCC_SPD	For DIMM design connect DIMM EPROM voltage: **VCC_SPD** = serial presence detect +2.3 V to +3.6 V, electrically isolated from the **V_{DD}/V_{DDQ}** plane.		
	Connect **DDR_RESET*** to **80321_M_RST***.		
Peripheral Local Bus Design Guide 7.8			
Length Constraints	All lengths less 8”.		
	Address demultiplexor lengths short as possible.		
	Peripheral **PB_CLK**s matched in length.		
	Series Termination resistor may be necessary if bus is running > 66 MHz.		
Other Signals			
Non Battery Backup	**DDR_SCKE** lines - 1.5 K pull-up.		
	SCKE on 80321 no connects.		
	PWRDELAY pin low through 1.5 K pull-down.		
Voltages	**V_{CC}** = +2.5 V and V_{CCQ} = +2.5 V electrically isolated.		
	VCC_PLL1, **VCC_PLL2** circuit recommendation ( ) use low ESR caps - electrically isolated from 2.5 V supply. Design Guide, section 8.0		
General Decoupling	The decoupling must average at least 0.01 µF (high-speed) per V_{CC} pin.		
	The trace length from pin pad to capacitor pad no greater than 0.25 inches using a trace width of at least 0.02 inches.		
	Add one high frequency decoupling capacitor per power pin where possible. To minimize inductance, use 0805 or 1206 style surface-mount 0.01 µF or 0.1 µF capacitors.		
	RCVENI# and **RCVENO#** tied directly together and trace length matched to average memory clock length plus average length of the **DQS** signals. (pg 103) There is no need for series termination or load capacitor. From Design Guide, Section 7.3.		
	BE[3:0]# - if not used, no connect.		
	PB_CLK - no action needed.		
	DEN# - no action needed.		
	BLAST# - no action needed.		
	RDYRCV# - no action needed.		
	HOLD - 4.7 K pull-down.		
	HOLDA - no connect.		
	POR# terminated as shown in the Design Guide, Figure 53.		

Table 2. Checklist (Sheet 4 of 5)

Category	Guideline	Compliance	
		Yes	No
PCE[5:0]	**PCE[5:0]** Configuration Pins are latched at the de-asserting edge of **P_RST**. **PCE[5:4]** PBI Bus speed: 11= 33 MHz default 10 = 66 MHz 4.7 K on **PCE[4]** 01 = 100 MHz 4.7 K on **PCE[5]** 00 = Undefined		
	PCE[3]/P_BOOT16# : Peripheral Bus Boot Width 16 Enable: Specifies the width of the peripheral bus for flash accesses during boot up. 0 = 16-bit bus width - 4.7 K pull down. 1 = 8-bit bus width default.		
	PCE[2]/32BITPCI#: 32-bit PCI is latched at the deasserting edge of **P_RST#** and it indicates the width of the PCI-X bus to the PCI-X Status Register (bit 16 of the PCI-X Status Register). 0 = 32-Bit PCI-X Bus - Requires pull-down resistor of 4.7 K. 1 = 64-Bit PCI-X Bus - Default mode.		
	PCE[1]/RETRY: is latched at the **deasserting edge of P_RST# and it determines if the** primary PCI Interface disables PCI Configuration Cycles by signaling a Retry until the Configuration Cycle Retry bit Is cleared in the PCI Configuration and Status Register. 0 = Configuration Cycles enabled - Requires pull-down resistor of 4.7 K. 1 = Retry enabled - Default mode.		
	PCE[0]#/RST_MODE#: RESET MODE is latched at the deasserting edge of **P_RST#** and it determines the Intel® 80321 I/O processor is held in reset until the Intel® XScale™ core process or Reset bit is cleared in the PCI Configuration and Status Register. 0 = Hold in reset - Requires pull-down resistor of 4.7 K. 1 = Don't hold in reset -Default mode.		
	P_ACK64# - 4.7 K pull-up only when not already pulled up on PCI bus. An add-in card may rely on the motherboard to pull-up these values.		
	P_CLK - 4.7 K pull-up only when not already pulled up on PCI bus. An add-in card may rely on the motherboard to pull-up these values.		
	P_INT[A:D]# - 4.7 K pull-up only when not already pulled up on PCI bus. An add-in card may rely on the motherboard to pull-up these values.		
	P_M66EN - 4.7 K pull-up only when not already pulled up on PCI bus. An add-in card may rely on the motherboard to pull-up these values.		
	TXD – no connect.		
	RXD - 1.5 K pull-down when unused.		
	XINT[3:0]# - 4.7 K pull-up when unused.		
	HPI# High Priority Interrupt - 4.7 K pull-up when unused.		

Table 2. Checklist (Sheet 5 of 5)

Category	Guideline	Compliance	
		Yes	No
GPIO	**GPIO[3:0]** When **GPIO** is not used then pin can be no connect **NC**s. When **GPIO[3:0]** is used: and **GPIO** pins need to be outputs after reset - 1.5 K pull-down is required.		
	GPIO[4]/SDA1 1. When **GPIO[4]** is used: • When **GPIO[4]** pin needs to be an output after reset - 1.5 K pull-down is required. • When **GPIO[4]**/I^2C is not used then the pin can be no connect **NC**. 2. When I^2C port 1 is used: • 2.7 K pull-up is required on **GPIO[4]/SDA1**		
	GPIO[5]/SCL1 1. When **GPIO[5]** is used: • When **GPIO[5]** pin needs to be an output after reset - 1.5 K pull-down is required. • When **GPIO[5]**/I^2C is not used then the pin can be no connect **NC**. 2. When I^2C port 1 is used: • 2.7 K pull-up is required on **GPIO[5]/SCL1**		
	GPIO[6]/SDA0 1. When **GPIO[6]** is used: • When **GPIO[6]** pin needs to be an output after reset - 1.5 K pull-down is required. • When **GPIO[6]**/I2C is not used then the pin can be no connect NC. 2. When I^2C port 0 is used: • 2.7 K pull-up is required on **GPIO[6]/SDA0**		
	GPIO[7]/SCL0 1. When **GPIO[7]** is used: • When **GPIO[7]** pin needs to be an output after reset - 1.5 K pull-down is required. 2. When I^2C port 0 is used both conditions need to be met: • 2.7 K pull-up is required on either **GPIO[7]/SCL0.**		
	TRST# - 1.5 K pull-down, when not used this signal tied to GND.		
	RCOMP must have a 30.1 Ω 1% 1/4 W resister pulled to ground.		
	PWRDELAY: For non-battery back up systems, must have 1.5 K Pull-down.		
	NC[2:0] No connect - do not connect to any signal, power, or ground.		
	V_{CCPLL1}: Low-pass filter as described in Design Guide, Section 8.		
	PCI-X: Follow PCI-X Layout Guidelines as described in the Design Guide, Section 6: Single-Slot at 133 MHz, Dual-Slot at 100 MHz, Quad-Slots at 66 MHz.		
	For the following signals: **P_ACK64#, P_AD[63:32], P_C/BE[7:4]#, P_DEVSEL#, P_FRAME#, P_INTA#, P_INTB#, P_INTC#, P_INTD#, P_IRDY#, P_M66EN, P_PAR64, P_PERR#, P_REQ64#, P_SERR#, P_STOP#, P_TRDY#,** use a 4.7 KΩ pull-up only when not already pulled up on PCI bus. An add-in card may rely on the motherboard to pull-up these values.		