



# **Intel<sup>®</sup> 80321 I/O Processor**

## **Design Review Checklist**

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*June 2002*





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No figures used at this time

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## **Revision History**

| <b>Date</b> | <b>Revision</b> | <b>Description</b> |
|-------------|-----------------|--------------------|
| June 2002   | 001             | Initial Release.   |

## 1.0 Introduction

This checklist is a compilation of key signals and strap options. It is not meant to be a complete signal list or a substitute for proper study of available design guides or reference schematics. Designers use this guide in conjunction with the *Intel® 80321 I/O Processor Design Guide*, built on Intel® XScale™ microarchitecture (ARM architecture compliant) and the Intel® IQ80321 evaluation platform board schematics. References are in [Table 1](#) below.

## 1.1 List of References

**Table 1. List of References**

| Document  | Document Number/Reference   |
|---|---|
| <i>Intel® 80321 I/O Processor Datasheet</i>                             | 273518  |
| <i>Intel® 80321 I/O Processor Developer's Manual</i>                    | 273517  |
| <i>Intel® 80321 I/O Processor Specification Update</i>                  | 273519  |
| <i>Intel® 80321 I/O Processor Design Guide</i>                          | 273520  |
| <i>PCI Local Bus Specification, Revision 2.2</i>                        | <a href="http://www.pcisig.com/specifications/conventional_pci">http://www.pcisig.com/specifications/conventional_pci</a>                             |
| <i>PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a</i> | <a href="http://www.pcisig.com/specifications/pci_x">http://www.pcisig.com/specifications/pci_x</a>   |
| <i>PCI-X Compliance Checklist</i>                                       | <a href="http://www.pcisig.com/data/specifications/pci_x_checklist_1_0_a.doc">http://www.pcisig.com/data/specifications/pci_x_checklist_1_0_a.doc</a> |
| <i>PCI 2.2 Compliance Checklist</i>                                     | <a href="http://www.pcisig.com/data/specifications/2_2_checklist.doc">http://www.pcisig.com/data/specifications/2_2_checklist.doc</a>                 |

## 1.2 Intel® 80321 I/O Processor Checklist

Table 2. Checklist (Sheet 1 of 5)

| Category   | Guideline  | Compliance |    |
|--|--|------------|----|
|  |  | Yes        | No |
| PCI-X  | Characteristic impedance of signal traces is 60 ±10% Ω.  |            |    |
|  | Signal propagation delay of traces is between 150 and 190 ps/inch, inclusive. (Same as conventional PCI.)  |            |    |
|  | Source bridge requires <b>IDSEL</b> inputs to be resistively coupled to <b>AD</b> bits, those resistors have a value of a least 2 KΩ.  |            |    |
|  | Source bridge requires <b>IDSEL</b> inputs to be resistively coupled to <b>AD</b> bits, devices 1-4 connect to <b>AD[17]</b> through <b>AD[20]</b> respectively.   |            |    |
|  | System includes slots for add-in cards, the system provides a circuit for sensing the connection of the <b>PCIXCAP</b> pin of all add-in cards.  |            |    |
|  | <b>PCIXCAP</b> pin is connected to ground through a 0.01 ±10% μF capacitor for PCI-X 133, or through a 10 K ±5% resistor in parallel with a 0.01 ±10% mF capacitor for PCI-X 66.   |            |    |
|  | <b>PCIXCAP</b> <ul style="list-style-type: none"> <li>• maximum length between the resistor (if installed), cap and the connector is 0.25".</li> <li>• maximum length between resistor (if installed), cap and ground is 0.1".</li> <li>• this connector pin not connected to any other device pins or voltages.</li> </ul>                                      |            |    |
|  | <b>PRSNT[1:2]#</b> are connected to show correct power consumption.  |            |    |
|  | All <b>GND</b> fingers are provided and are bussed together.   |            |    |
|  | All bussed signals contain no more than ONE 10pF (max) load.   |            |    |
|  | <b>M66EN</b> finger (pin 49, side B) is either an input or a no-connect. It is advisable to connect <b>P_M66EN</b> to a 0.01 μF capacitor located with-in 0.25 inches of the <b>M66EN</b> pin on a add-in connector.   |            |    |
|  | PCI connector pins: Ensure 3.3 V pins (even if they are not actually delivering power), and any unused 5 V and V <sub>IO</sub> pins on the PCI edge connector provide an ac return path. These pins must have plated edge fingers and be decoupled to the ground plane on the add-in board to ensure they continue to function as efficient ac reference points. |            |    |
|  | All <b>RESERVED</b> fingers are no-connect and are NOT bussed together.  |            |    |
|  | Add-in card protection circuitry on <b>INTA/B/C/D</b> to prevent damage to chip. Design Guide, section 6.2.3   |            |    |
|  | Add-in card trace length for <b>AD[31::0]</b> is between 0.75 inches and 1.5 inches, inclusive.  |            |    |
|  | Add-in card trace length for <b>AD[63::32]</b> is between 1.75 inches and 2.75 inches, inclusive.  |            |    |
|  | Add-in card trace length for <b>RST#</b> is between 0.75 inches and 3.0 inches, inclusive.   |            |    |
|  | Trace spacing, geometries, and materials limit cumulative crosstalk to 5% of the amplitude of the aggressor signal.  |            |    |
|  | PCI Clock Trace length for <b>P_CLK</b> is between 2.4 inches and 2.6 inches, inclusive and routes only to one load for add-in card. (Same as conventional PCI.) Total length for non-add-in card is < 8" .  |            |    |
|  | PCI Clock Buffer: <b>P_CLKs</b> lengths matched to .1" Design Guide, section 6.3.1. <ul style="list-style-type: none"> <li>• PCI Clock Buffer: use low skew clock buffer <sup>2</sup> .</li> <li>• PCI Clock Buffer: <b>P_CLK</b> lines at least 25mils from each other and themselves.</li> </ul>   |            |    |
| PCI Address Bus <b>AD</b> : wiring lengths follow recommendations in Design Guide, section 6.4 dependent on speed and number of slots. |  |            |    |

Table 2. Checklist (Sheet 2 of 5)

| Category  | Guideline  | Compliance |    |
|---|--|------------|----|
|   |  | Yes        | No |
| <b>DDR Constraints: Design Guide Chapter 7</b>  |  |            |    |
| DDR Source Synchronous<br>Design Guide,<br>section 7.4.1                                | Series Resistor <b>DQ/DQS/DM/CB</b> Series resistors = 10 Ω.   |            |    |
|   | Parallel term resistor <b>DQ/DQS/DM/CB</b> = 60 Ω.   |            |    |
|   | Trace Length 80321 BGA pin to series resistor 1.8 to 4.9".   |            |    |
|   | Trace Length series resistor to DIMM < 0.5".   |            |    |
|   | Trace Length to parallel resistor 0.1" to 0.8".  |            |    |
|   | Length Matching within group 0.025" – nine signals.  |            |    |
|   | Length Matching over all signals to clock longest x-1" to shortest x-2", x= clock length.  |            |    |
| DDR Clocked Signals Group<br>Design Guide,<br>section 7.4.2.1                           | Trace width 5 mils, trace spacing 7 mils and 20 mils between next closest trace.   |            |    |
|   | Series resistors <b>M_CK/M_CK#</b> = 27 Ω.   |            |    |
|   | Parallel term resistors <b>M_CK/M_CK#</b> = 120 Ω – ONLY for non-DIMM.   |            |    |
|   | Trace Length 80321 BGA pin to series resistor not specified (closer to 80321).   |            |    |
|   | Trace Length 1" to 7".   |            |    |
|   | Length Matching <b>M_CK/M_CK#</b> = 2 mils.  |            |    |
|   | Length Matching between clock groups +/-25 mils.   |            |    |
|   | <b>M_CK</b> polarity alternated (not two <b>M_CK#</b> s next to each other).   |            |    |
|   | <b>M_CK</b> minimize layer changes (two vias or less).   |            |    |
| DDR Source Clocked<br>Signals Termination (control)<br>Design Guide,<br>section 7.4.2.2 | Series Resistor <b>RAS, CAS, WE, MA[12:0], BA[1:0]</b> = 15 Ω.   |            |    |
|   | Parallel term resistor <b>RAS, CAS, WE, MA[12:0], BA[1:0]</b> = 60 Ω.<br>Resistor Packs are acceptable for the parallel control termination resistors but control signals can NOT be placed within the same RPACK as data, strobe, or command signals. Termination resistor: Rp 56 Ω +/- 1%. |            |    |
|   | Trace Length 80321 BGA pin to series resistor not specified (closer to 80321).   |            |    |
|   | Trace Length 2" to 5".   |            |    |
|   | Trace Length to parallel resistor 0.1" to 0.8".  |            |    |
|   | Length Matching within group 0.025" – nine signals.  |            |    |
|   |  |            |    |
| DDR CS, CKE<br>Design Guide,<br>section 7.4.3   | Series Resistor <b>CS, CKE</b> = 10 Ω.   |            |    |
|   | Parallel term resistor <b>CS, CKE</b> = 60 Ω.  |            |    |
|   | Trace Length 80321 BGA pin to series resistor not specified (closer to 80321).   |            |    |
|   | Trace Length 2" to 5".   |            |    |
|   | Trace Length to parallel resistor 0.1" to 0.8".  |            |    |
|   | Length Matching over all signals to clock longest x-1" to shortest 2", x= clock length.  |            |    |
|   | Route on same layer as <b>M_CK</b> s.  |            |    |
|   | Minimize layer changes (two vias or less).   |            |    |
|   | Rp is needed for non-DIMM application 120 Ω +/- 1%.  |            |    |
| Length Matching over all signals to clock longest x-1" to shortest 2", x= clock length. |  |            |    |
| DDR Voltages<br>Design Guide,<br>section 7.4.4  | All Parallel termination Resistors pulled to <b>VTT_DDR</b> = +1.25V.  |            |    |

**Table 2. Checklist (Sheet 3 of 5)**

| Category   | Guideline   | Compliance |    |
|--|---|------------|----|
|  |   | Yes        | No |
| <b>DDR Constraints: Design Guide Chapter 7 (Continued)</b> |   |            |    |
| <b>V<sub>TT</sub></b>                                      | <b>V<sub>TT</sub></b> island at least 50 mils wide.   |            |    |
|  | <b>V<sub>TT</sub></b> Decouple plane with 0.1 μF cap per two termination resistors.   |            |    |
|  | <b>V<sub>TT</sub></b> Decouple plane with large 10uF or larger at each end of the termination island.   |            |    |
|  | <b>V<sub>TT</sub></b> electrically isolated from the core voltage.  |            |    |
|  | <b>V<sub>TT</sub></b> able to source/sink significant switching current for <b>DDRs</b> .   |            |    |
| <b>V<sub>REF</sub></b>                                     | <b>DDR_VREF</b> = + 1.25 V and Electrically separate from <b>VTT_DDR</b> .  |            |    |
|  | <b>V<sub>REF</sub></b> is generated with a resistor divider circuit off the 2.5 V voltage to create a stable 1.25 V reference. R1 and R2 are 49.9 Ω +/- 1%. Design Guide, Section 8, Figure 46.   |            |    |
| <b>VCC_SPD</b>   | For DIMM design connect DIMM EPROM voltage: <b>VCC_SPD</b> = serial presence detect +2.3 V to +3.6 V, electrically isolated from the <b>V<sub>DD</sub>/V<sub>DDQ</sub></b> plane.   |            |    |
|  | Connect <b>DDR_RESET*</b> to <b>80321_M_RST*</b> .  |            |    |
| <b>Peripheral Local Bus Design Guide 7.8</b>               |   |            |    |
| <b>Length Constraints</b>                                  | All lengths less 8".  |            |    |
|  | Address demultiplexor lengths short as possible.  |            |    |
|  | Peripheral <b>PB_CLKs</b> matched in length.  |            |    |
|  | Series Termination resistor may be necessary if bus is running > 66 MHz.  |            |    |
| <b>Other Signals</b>                                       |   |            |    |
| <b>Non Battery Backup</b>                                  | <b>DDR_SCKE</b> lines - 1.5 K pull-up.  |            |    |
|  | <b>SCKE</b> on 80321 no connects.   |            |    |
|  | <b>PWRDELAY</b> pin low through 1.5 K pull-down.  |            |    |
| <b>Voltages</b>  | <b>V<sub>CC</sub></b> = +2.5 V and <b>V<sub>CCQ</sub></b> = +2.5 V electrically isolated.   |            |    |
|  | <b>VCC_PLL1</b> , <b>VCC_PLL2</b> circuit recommendation ( ) use low ESR caps - electrically isolated from 2.5 V supply. Design Guide, section 8.0  |            |    |
| <b>General Decoupling</b>                                  | The decoupling must average at least 0.01 μF (high-speed) per <b>V<sub>CC</sub></b> pin.  |            |    |
|  | The trace length from pin pad to capacitor pad no greater than 0.25 inches using a trace width of at least 0.02 inches.   |            |    |
|  | Add one high frequency decoupling capacitor per power pin where possible. To minimize inductance, use 0805 or 1206 style surface-mount 0.01 μF or 0.1 μF capacitors.  |            |    |
|  | <b>RCVENI#</b> and <b>RCVENO#</b> tied directly together and trace length matched to average memory clock length plus average length of the <b>DQS</b> signals. (pg 103) There is no need for series termination or load capacitor. From Design Guide, Section 7.3. |            |    |
|  | <b>BE[3:0]#</b> - if not used, no connect.  |            |    |
|  | <b>PB_CLK</b> - no action needed.   |            |    |
|  | <b>DEN#</b> - no action needed.   |            |    |
|  | <b>BLAST#</b> - no action needed.   |            |    |
|  | <b>RDYRCV#</b> - no action needed.  |            |    |
|  | <b>HOLD</b> - 4.7 K pull-down.  |            |    |
|  | <b>HOLDA</b> - no connect.  |            |    |
|  | <b>POR#</b> terminated as shown in the Design Guide, Figure 53.   |            |    |



Table 2. Checklist (Sheet 4 of 5)

| Category | Guideline   | Compliance |    |
|----------|---|------------|----|
|          |   | Yes        | No |
| PCE[5:0] | <p><b>PCE[5:0]</b> Configuration Pins are latched at the de-asserting edge of <b>P_RST</b>.</p> <p><b>PCE[5:4]</b> PBI Bus speed:<br/>           11 = 33 MHz default<br/>           10 = 66 MHz 4.7 K on <b>PCE[4]</b><br/>           01 = 100 MHz 4.7 K on <b>PCE[5]</b><br/>           00 = Undefined</p>   |            |    |
|          | <p><b>PCE[3]/P_BOOT16#</b> : Peripheral Bus Boot Width 16 Enable:<br/>           Specifies the width of the peripheral bus for flash accesses during boot up.<br/>           0 = 16-bit bus width - 4.7 K pull down.<br/>           1 = 8-bit bus width default.</p>  |            |    |
|          | <p><b>PCE[2]/32BITPCI#</b>: <b>32-bit PCI</b> is latched at the deasserting edge of <b>P_RST#</b> and it indicates the width of the PCI-X bus to the PCI-X Status Register (bit 16 of the PCI-X Status Register).<br/>           0 = 32-Bit PCI-X Bus - Requires pull-down resistor of 4.7 K.<br/>           1 = 64-Bit PCI-X Bus - Default mode.</p>   |            |    |
|          | <p><b>PCE[1]/RETRY</b>: is latched at the <b>deasserting edge of P_RST#</b> and it determines if the primary PCI Interface disables PCI Configuration Cycles by signaling a Retry until the Configuration Cycle Retry bit is cleared in the PCI Configuration and Status Register.<br/>           0 = Configuration Cycles enabled - Requires pull-down resistor of 4.7 K.<br/>           1 = Retry enabled - Default mode.</p> |            |    |
|          | <p><b>PCE[0]/RST_MODE#</b>: <b>RESET MODE</b> is latched at the deasserting edge of <b>P_RST#</b> and it determines the Intel® 80321 I/O processor is held in reset until the Intel® XScale™ core process or Reset bit is cleared in the PCI Configuration and Status Register.<br/>           0 = Hold in reset - Requires pull-down resistor of 4.7 K.<br/>           1 = Don't hold in reset -Default mode.</p>              |            |    |
|          | <b>P_ACK64#</b> - 4.7 K pull-up only when not already pulled up on PCI bus. An add-in card may rely on the motherboard to pull-up these values.   |            |    |
|          | <b>P_CLK</b> - 4.7 K pull-up only when not already pulled up on PCI bus. An add-in card may rely on the motherboard to pull-up these values.  |            |    |
|          | <b>P_INT[A:D]#</b> - 4.7 K pull-up only when not already pulled up on PCI bus. An add-in card may rely on the motherboard to pull-up these values.  |            |    |
|          | <b>P_M66EN</b> - 4.7 K pull-up only when not already pulled up on PCI bus. An add-in card may rely on the motherboard to pull-up these values.  |            |    |
|          | <b>TXD</b> – no connect.  |            |    |
|          | <b>RXD</b> - 1.5 K pull-down when unused.   |            |    |
|          | <b>XINT[3:0]#</b> - 4.7 K pull-up when unused.  |            |    |
|          | <b>HPI#</b> High Priority Interrupt - 4.7 K pull-up when unused.  |            |    |

Table 2. Checklist (Sheet 5 of 5)

| Category | Guideline  | Compliance |    |
|----------|--|------------|----|
|          |  | Yes        | No |
| GPIO     | <b>GPIO[3:0]</b><br>When <b>GPIO</b> is not used then pin can be no connect <b>NCs</b> .<br>When <b>GPIO[3:0]</b> is used:<br>and <b>GPIO</b> pins need to be outputs after reset - 1.5 K pull-down is required.   |            |    |
|          | <b>GPIO[4]/SDA1</b><br>1. When <b>GPIO[4]</b> is used: <ul style="list-style-type: none"> <li>• When <b>GPIO[4]</b> pin needs to be an output after reset - 1.5 K pull-down is required.</li> <li>• When <b>GPIO[4]/I<sup>2</sup>C</b> is not used then the pin can be no connect <b>NC</b>.</li> </ul> 2. When I <sup>2</sup> C port 1 is used: <ul style="list-style-type: none"> <li>• 2.7 K pull-up is required on <b>GPIO[4]/SDA1</b></li> </ul>                          |            |    |
|          | <b>GPIO[5]/SCL1</b><br>1. When <b>GPIO[5]</b> is used: <ul style="list-style-type: none"> <li>• When <b>GPIO[5]</b> pin needs to be an output after reset - 1.5 K pull-down is required.</li> <li>• When <b>GPIO[5]/I<sup>2</sup>C</b> is not used then the pin can be no connect <b>NC</b>.</li> </ul> 2. When I <sup>2</sup> C port 1 is used: <ul style="list-style-type: none"> <li>• 2.7 K pull-up is required on <b>GPIO[5]/SCL1</b></li> </ul>                          |            |    |
|          | <b>GPIO[6]/SDA0</b><br>1. When <b>GPIO[6]</b> is used: <ul style="list-style-type: none"> <li>• When <b>GPIO[6]</b> pin needs to be an output after reset - 1.5 K pull-down is required.</li> <li>• When <b>GPIO[6]/I<sup>2</sup>C</b> is not used then the pin can be no connect <b>NC</b>.</li> </ul> 2. When I <sup>2</sup> C port 0 is used: <ul style="list-style-type: none"> <li>• 2.7 K pull-up is required on <b>GPIO[6]/SDA0</b></li> </ul>                          |            |    |
|          | <b>GPIO[7]/SCL0</b><br>1. When <b>GPIO[7]</b> is used: <ul style="list-style-type: none"> <li>• When <b>GPIO[7]</b> pin needs to be an output after reset - 1.5 K pull-down is required.</li> </ul> 2. When I <sup>2</sup> C port 0 is used both conditions need to be met: <ul style="list-style-type: none"> <li>• 2.7 K pull-up is required on either <b>GPIO[7]/SCL0</b>.</li> </ul>   |            |    |
|          | <b>TRST#</b> - 1.5 K pull-down, when not used this signal tied to GND.   |            |    |
|          | <b>RCOMP</b> must have a 30.1 Ω 1% 1/4 W resistor pulled to ground.  |            |    |
|          | <b>PWRDELAY</b> : For non-battery back up systems, must have 1.5 K Pull-down.  |            |    |
|          | <b>NC[2:0]</b> No connect - do not connect to any signal, power, or ground.  |            |    |
|          | <b>V<sub>CCPLL1</sub></b> : Low-pass filter as described in Design Guide, Section 8.   |            |    |
|          | PCI-X: Follow PCI-X Layout Guidelines as described in the Design Guide, Section 6: Single-Slot at 133 MHz, Dual-Slot at 100 MHz, Quad-Slots at 66 MHz.   |            |    |
|          | For the following signals: <b>P_ACK64#</b> , <b>P_AD[63:32]</b> , <b>P_C/BE[7:4]#</b> , <b>P_DEVSEL#</b> , <b>P_FRAME#</b> , <b>P_INTA#</b> , <b>P_INTB#</b> , <b>P_INTC#</b> , <b>P_INTD#</b> , <b>P_IRDY#</b> , <b>P_M66EN</b> , <b>P_PAR64</b> , <b>P_PERR#</b> , <b>P_REQ64#</b> , <b>P_SERR#</b> , <b>P_STOP#</b> , <b>P_TRDY#</b> , use a 4.7 KΩ pull-up only when not already pulled up on PCI bus. An add-in card may rely on the motherboard to pull-up these values. |            |    |