

The GAL®16VP8 and GAL20VP8

Introduction

Lattice Semiconductor's two high-drive "VP" series devices, the GAL16VP8 and GAL20VP8, are based upon the industry standard GAL16V8 and GAL20V8 architectures, adding programmable output configuration for higher drive capability. The "VP" series has programmable output buffers that can be configured to either open-drain or totem-pole outputs. Their output buffers can be independently programmed by setting the appropriate control bits in the architectural array. Additionally, their input buffers contain Schmitt trigger inputs for greater noise immunity and active pull-up resistors on all inputs and I/Os.

The GAL "VP" high drive adds value to the popular GAL16V8 and GAL20V8 product line. The advantages of the "VP" series include:

- Higher Output Drive Current Low-Level Output Current -lol = 64 mA vs. 24mA High Level Output Current -loh = -32 mA vs. -3.2mA
- Schmitt Trigger Input Buffers Schmitt trigger input buffers with 200mV of hysteresis between positive and negative input transitions. The Schmitt trigger inputs offer improved noise immunity during switching transitions, especially on the clock input. Hysteresis prevents double clocking when nonmonotonic rise and fall times are present.
- **Programmable Output Buffers** Two independent types of output buffers can be programmed for each OLMC (Output Logic Macro Cell). A combination of open-drain and totem-pole outputs can be used. For example, four totem-pole outputs for interfacing I/O functions and four open-drain outputs for bus interfacing with pull-up resistors. Any mixed combination of output buffers can be used since each output macrocell contains a dedicated fuse to assign the configuration of the output buffer.
 - Totem-pole output for standard high-drive interfacing to external logic systems with heavy capacitive loading. This configuration has Vol and Voh levels that are standard TTL-level data sheet values, Vol=0.5 V max., Voh=2.4 V min.

- Open-drain output for bus interfacing and arbitration circuits. Low logic level Vol has the standard TTL-level data sheet value, Vol = .5 V max. High logic level Voh is set from external pull-up resistors and is a function of the external loading.

These advantages allow the designer greater flexibility when interfacing to bus and memory logic.

The series offers 64mA lol output drive for driving heavy capacitive loads associated with memory elements, such as those on data buses and back plane type systems.

One of the advantages of using high drive programmable logic for interfacing is that it eliminates the need for 74XX240 type drivers that are used in conjunction with decoding logic as a multiple device solution. In many microprocessor applications, decoding logic is used to decode address space for I/O or memory, then these signals are fed to bus driver components, such as the 74XX240 series, to drive heavy loads on busses or back planes.

Using the Lattice "VP" high drive series allows the designer to accomplish this with a single chip solution. The GAL20VP8 or GAL20VP8 devices are used to decode the address space needed and the appropriate output configuration is chosen to supply the drive capability needed to interface with the system.

Programming the 16/20VP8

Development systems such as ABEL and Synario from Data I/O or CUPL from Logical Devices support both the GAL16VP8 and the GAL20VP8 with compiler support. Logic equations and syntax remain the same as with standard GAL16V8 and GAL20V8 devices. There are three possible modes that are used for different OLMC configurations along with the output drive configuration mode: Registered, Complex and Simple. Each of these modes is set according to the logic functions implemented in the source or design file. The only additional information needed in the source file is the configuration of the output buffers. The output buffer configuration is set with a dedicated architecture fuse for each OLMC, architecture fuse AC2.

- AC2 = 1 Defines totem-pole output.
- AC2 = 0 Defines open-drain output.

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Each OLMC has an associated set of architecture fuses; the fuses SYN, AC1, AC0 will be set by the compiler software for the appropriate OLMC mode (Registered, Complex or Simple).

Each output also contains an AC2 fuse. The following is a list of AC2 fuse locations:

GAI 20VP8

GAI 16VP8

These fuses must be set using the compiler software. The following statements for ABEL and CUPL compilers show how to implement the programmable output buffers.

Technical Support Assistance

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F U	GALZUVFO
(AC2 = 2194)	Output 22 (AC2 = 2706)
()	Output 21 (AC2 = 2707)
()	Output 20 (AC2 = 2708)
()	Output 19 (AC2 = 2709)
(AC2 = 2198)	Output 17 (AC2 = 2710)
(AC2 = 2199)	Output 16 (AC2 = 2711)
(AC2 = 2200)	Output 15 (AC2 = 2712)
(AC2 = 2201)	Output 14 (AC2 = 2713)
	(AC2 = 2194) (AC2 = 2195) (AC2 = 2196) (AC2 = 2196) (AC2 = 2197) (AC2 = 2198) (AC2 = 2199) (AC2 = 2200)

Example 1. ABEL Example for the GAL16VP8-15LP (Setting the Output Driver Fuses) Module TEST1 TITLE 'This is an example for the GAL16VP8-15LP that sets the output driver fuses'; TEST1 Device 'P16VP8'; " Note: The GAL16VP8-15LP is a center-pin device. Ground = Pin 15 , Vcc = Pin 5 " Pin Assignments IN1, IN2, IN3, IN4, IN6, IN7, IN8, IN9 Pin 1,2,3,4,6,7,8,9; Pin 11,12,13,14; OUT11, OUT12, OUT13, OUT14 OUT16, OUT17, OUT18, OUT19 Pin 16,17,18,19; " Use the FUSES statement to individually set AC2 fuses for output configurations. FUSES [2194..2197] = [1,1,1,1]; "Set output pins 19,18,17,16 to totem-pole FUSES [2198..2201] = [0,0,0,0]; "Set output pins 14,13,12,11 to open-drain EQUATIONS OUT19 = IN1 & !IN2 & !IN4;" Pin 19 configured as totem-pole. OUT18 = !IN1 & !IN2 & !IN3; " Pin 18 configured as totem-pole. " Pin 17 configured as totem-pole. OUT17 = IN4 & IN6 & !IN8; OUT16 = IN6 & IN7 & !IN8; " Pin 16 configured as totem-pole. OUT14 = !IN3 & !IN8;" Pin 14 configured as open-drain. OUT13 = IN2 & IN7;" Pin 13 configured as open-drain. OUT12 = !IN2 & !IN4 & IN7; " Pin 12 configured as open-drain. OUT11 = !IN4 & IN6 & IN8; " Pin 11 configured as open-drain. end