ispPAC20 Thermoelectric Temperature Controller Evaluation Board PAC20EV-PWMTEC

October 2002 Application Note AN6039

Introduction

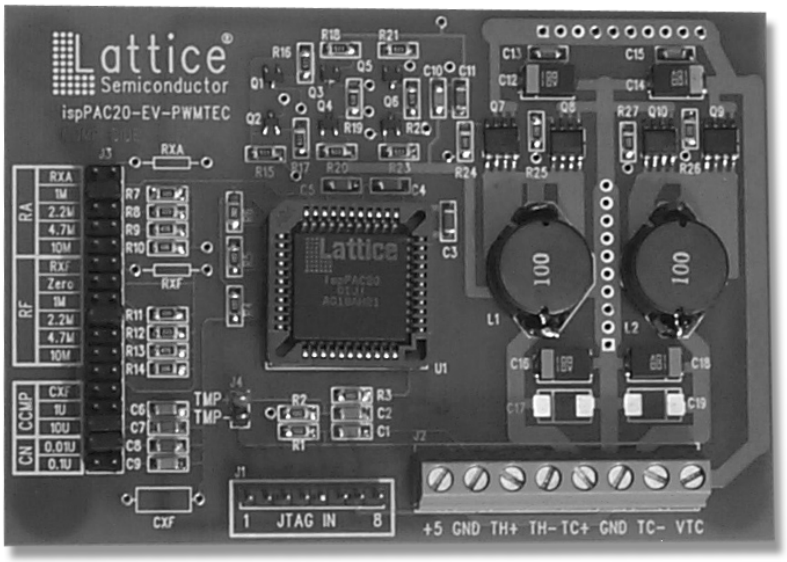
The Lattice Semiconductor ispPAC®20 In-System-Programmable (ISP™) Analog Circuit allows designers to quickly implement analog circuits such as amplifiers and active filters, with circuit descriptions stored in the ispPAC20's non-volatile E^2CMOS® memory. This technology brings in-system programmability to the analog world. Device functionality as well as parameters such as gain and frequency response can be set by the user and changed on-the-fly by reprogramming the device. A standard JTAG IEEE 1149.1 interface allows the user to reconfigure the ispPAC20 while in-system using on-chip non-volatile E^2CMOS technology.

PAC20-EV-PWMTEC Evaluation Board

The ispPAC20-EV-PWMTEC Evaluation Board (Figure 1) allows the user to quickly configure and evaluate the ispPAC20 for thermoelectric temperature control applications. The evaluation board includes an ispPAC20 in a 44-pin PLCC package and the external circuitry necessary to measure temperature with an external 10k thermistor, drive up to a 3A thermoelectric cooler module (TEC), and set control loop compensation. Power, and connections to the external TEC and thermistor are provided through screw terminals for greater ease in prototyping. This evaluation board uses pulse-width modulation (PWM) drive techniques to enable it to drive TEC modules requiring up to 3 A of operating current.

For controlling lower-current TECs (< 1A), it is also practical to use linear-output driver circuitry. For a description of a linear-output ispPAC20-based TEC controller please refer to application note AN6034, *ispPAC20 Thermoelectric Temperature Controller Evaluation Board PAC20EV-TEC*.

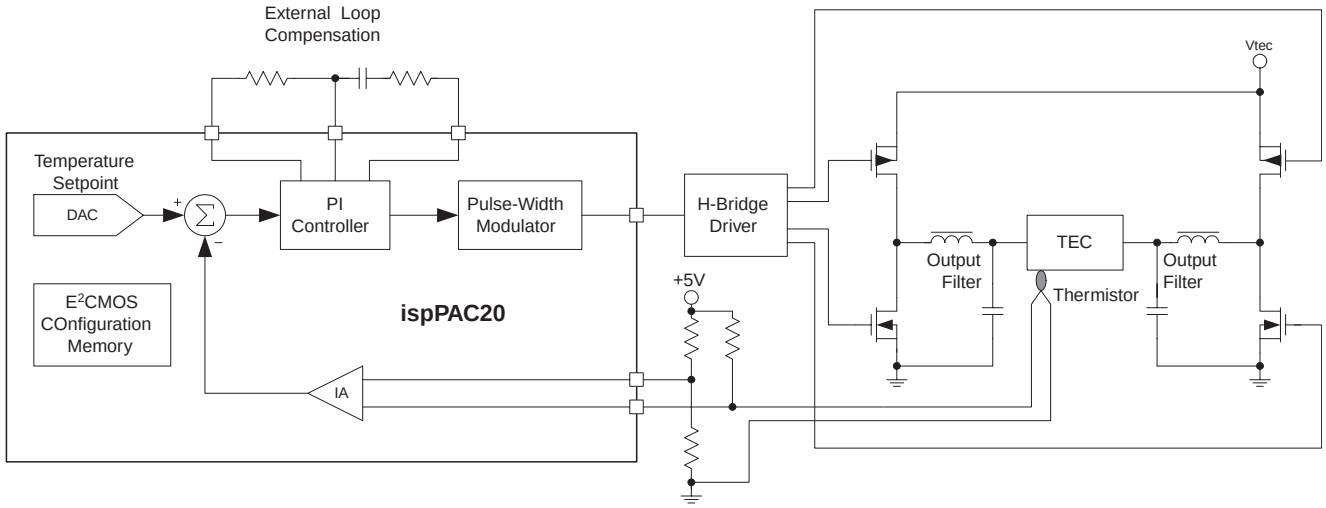
Figure 1. ispPAC20-EV-PWMTEC Evaluation Board



Circuit Description

Figure 2 shows a simplified schematic overview of the ispPAC20-EV-PWMTEC evaluation board. A single ispPAC20 performs all of the major control functions required to drive a TEC to, and maintain it at a given temperature. External on-board components implement an H-bridge power driver for the TEC, an interface to an external thermistor for monitoring TEC temperature, and a control-loop compensation network. A detailed schematic for this evaluation board is shown in Figure 8 of this application note.

Figure 2. ispPAC20-EV-PWMTEC - Simplified Schematic



The ispPAC20 allows a user to program a desired temperature setpoint through its on-chip DAC. In addition to being able to program a desired DAC setting into non-volatile E^2CMOS memory, it is also possible to dynamically change the setpoint by loading the DAC through either the ispPAC20's parallel interface or Serial Peripheral Interface (SPI).

The ispPAC20 is also used to implement a proportional-integral (PI) loop controller. Because the time constants needed to stabilize a thermal system typically range from hundreds of milliseconds to tens of seconds, an external capacitor and one or more resistors are needed to realize the control function.

The output of the loop controller is then used as the control signal for a pulse-width modulator (PWM). The PWM converts the linear output provided by the loop controller into a digital control signal with a duty cycle proportional to the control voltage. In this particular implementation, a control signal of zero volts to the PWM results in a 50% duty cycle on its output, which corresponds to zero power being applied to the TEC. Negative TEC drive levels are represented by duty cycles less than 50%, while positive TEC drive levels are represented by duty cycles greater than 50%. A simple interface circuit then takes the output of the PWM and generates control signals for the gates of each of four MOSFETs forming an H-bridge power driver.

TEC modules are optimally driven with a constant DC source. For this reason LC output filters are placed between the outputs of the H-bridge's power MOSFETs and the TEC. These filters converts the duty-cycled ON-OFF output of the H-bridge into a continuous and proportional DC signal. A small ripple (~100mV) voltage at the PWM frequency will also appear superimposed on these DC signals. The amount of ripple is a function of the TEC load, and can be modified by changing the values of the inductors and capacitors used in the output filter.

The ispPAC20-EV-PWMTEC also provides an interface to measure temperature using an external 10kΩ thermistor. This interface works by including the thermistor as one of the legs in a balanced bridge circuit, where the remaining bridge legs are fixed 10kΩ precision resistors (R1, R2, R3 in Figure 8). This configuration provides a differential signal of approximately 50mV/°C when used with a thermistor with a 'beta' of 3900 (~ -4%/°C tempco). Note that because of this balanced-bridge arrangement, a zero-voltage differential signal will result when the thermistor is 10kΩ (typically at 25°C). It is also possible to use the ispPAC20-EV-PWMTEC board with other thermistors by making appropriate substitutions for R1, R2, and R3.

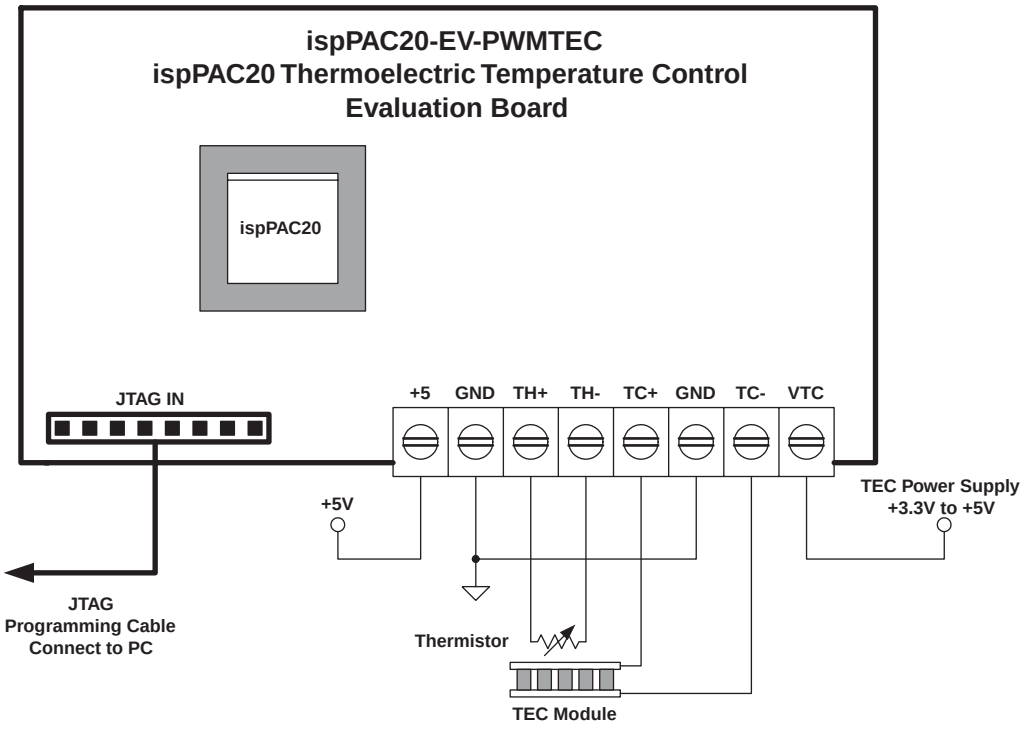
External Connections

The ispPAC20-EV-PWMTEC evaluation board has two external connectors, an 8-position screw-terminal (J2) for power, sensor, and TEC connections, and an 8-position header (J1) to accommodate the JTAG serial programming interface. Figure 3 shows how the thermistor, TEC module, and external power supplies are connected to the evaluation board. Note that a separate supply terminal (VTC) is provided for powering the TEC module. This allows the

user to use TEC modules with different voltage ratings. In general, one will want to select the VTC power supply to be slightly higher than the maximum operating voltage of the TEC being used. Setting the VTC power supply much higher than necessary may result in excessive heating of the output driver transistors.

While the polarity of the connection to the external thermistor is not important, that of the connection to the TEC is critical. If the TEC connection is reversed, this will reverse the feedback sense of the control loop from negative to positive. This will result in the driver moving into a saturated state, and remaining there indefinitely. If the TEC '+' and '-' leads are defined such that applying a positive voltage across them results in heating the thermistor, then the TEC's '+' lead should be connected to the TC+ terminal, and the TEC's - lead should be connected to the TC- terminal.

Figure 3. External Connections for Evaluation Board



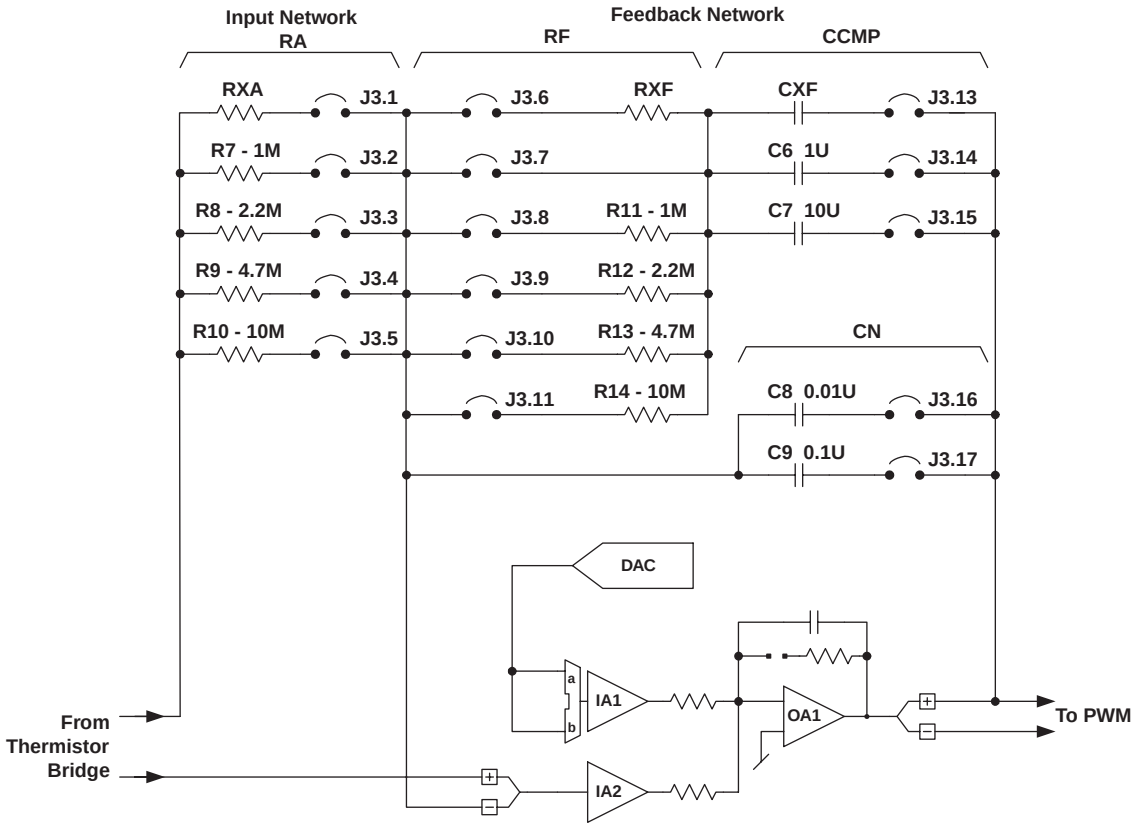
An 8-pin 0.100" (2.54mm) pitch header is provided for the connection of an ispDOWNLOAD® cable for JTAG programming of the on-board ispPAC20. This is the same cable as is used to program ispPAC devices on other evaluation boards, and is included in ispPAC system design kits. This cable may also be purchased as a separate item by part number pDS4102-DL2.

In addition to the screw-terminal connector and 8-pin header, on-board test points are provided to allow for the measurement of thermistor temperature. Temperature is measured as a voltage across the points labeled TMP+ and TMP- (J4). For the most common types of thermistors, one can expect to see ~50mV/°C across these terminals. Note that this voltage measurement is differential, and has a significant (~2.5V) common-mode component.

Compensation Network

Because extremely long time constants (0.1 - 10 seconds) may be needed by a temperature controller, these time constants must be generated by the use of external resistors and capacitors. The ispPAC20-EV-PWMTEC board provides a proportional-integral (PI) compensation network on-board. Because the exact values of loop compensation needed to ensure a stable, fast settling control loop are dependent on the characteristics of the system being controlled, it is usually necessary to 'tune' a given control loop for optimal performance. The ispPAC20-EV-PWMTEC board provides the ability to tune a control loop through the provision of several values of resistance and capacitance which can be selected through jumpers. Figure 4 shows a detail of this compensation network.

Figure 4. Detail of Compensation Network



All jumpers are located on the common dual-row header J3. Jumpers J3.1 through J3.5 control the selection of RA, which controls both integral time constant, and proportional gain. J3.1 selects a user-definable resistor RXA (not installed on board).

Jumpers J3.6 through J3.11 select a feedback resistance RF, which controls proportional gain. J3.6 selects a user-definable resistor. Note that in cases where minimal proportional gain is required, one can select zero ohms with J3.7.

J3.13 through J3.15 select the integration capacitor CCMP. Again, a provision exists for selecting a user-defined capacitor (CXF).

The capacitors selected by J3.13 and J3.14 (C8, C9; the 'CN' group on the board) are used to bypass the feedback resistor bank and reduce high-frequency gain. The inclusion of one of these capacitors is often helpful in reducing the effects of higher-frequency external interference such as 60 Hz power-line hum and RF pickup.

The proportional (K_P) and integral (K_I) gains of the compensation network and error amplifier are given by

$$K_P = \frac{R_F}{R_A} \quad (1)$$

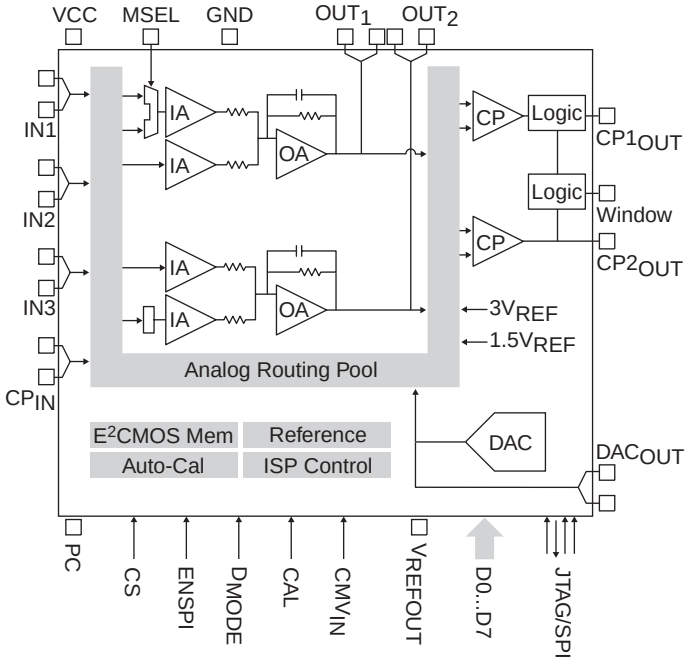
$$K_I(f) = \frac{1}{2\pi f C_F R_A} \quad (2)$$

For further material on implementing control loop compensation networks with the ispPAC20, please refer to application note AN6029, *Thermoelectric Temperature Control Using the ispPAC20.*

ispPAC20 Overview and Configuration

The ispPAC20 is a general-purpose programmable analog IC, providing a variety of functions including gain, filtering, comparison, and D/A conversion, as well as a user-configurable switching network to interconnect the available functions. Figure 5 shows the major user-visible components of the ispPAC20.

Figure 5. ispPAC20 Block Diagram

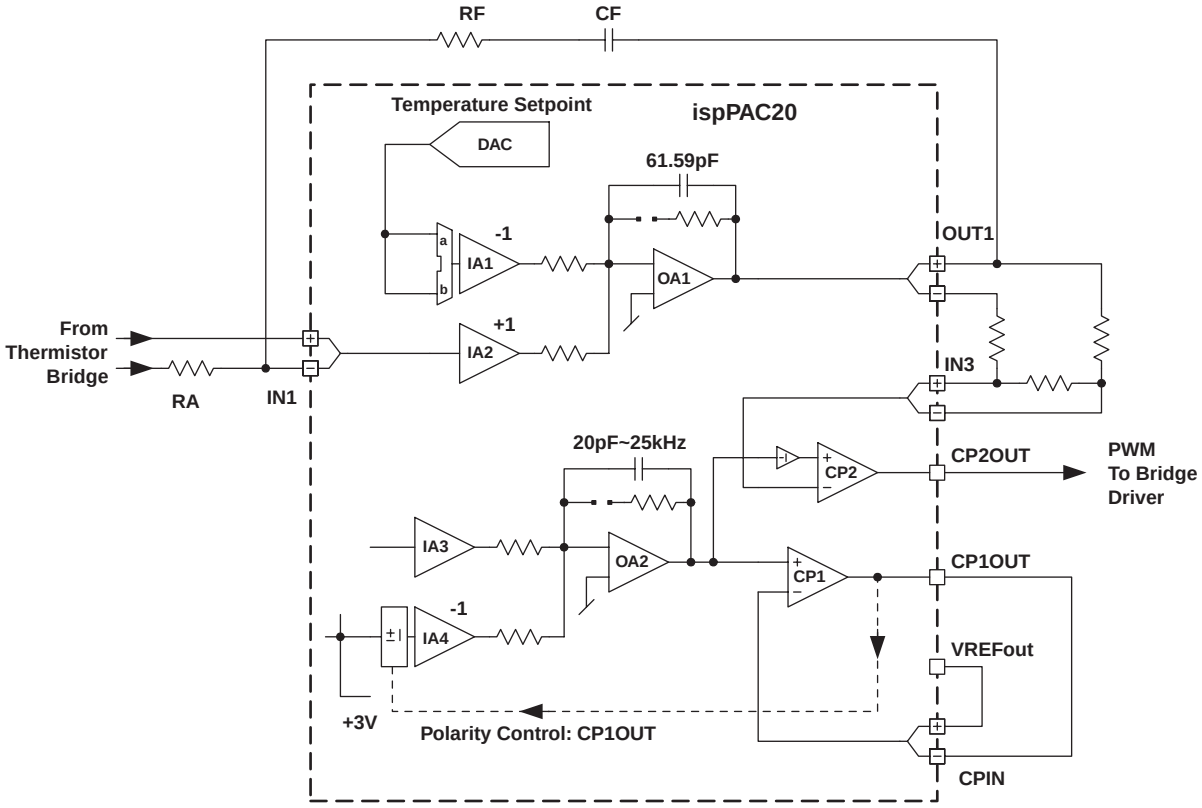


Nearly all of the ispPAC20's on-chip resources are utilized when implementing a PWM-drive temperature control system. The primary functions provided by the ispPAC20 are:

- DAC for establishing temperature setpoint
- Error amplifier and control loop compensation
- Pulse-width modulator

Figure 6 shows an ispPAC20 internal configuration that is compatible with the external circuitry provided on the ispPAC20-EV-PWMTEC board. The compensation loop is implemented externally to the ispPAC20 using discrete components. The temperature signal from the thermistor and the temperature setpoint from the DAC are summed together by OA1, resulting in a PI-compensated error signal at output OUT1.

Figure 6. Internal Configuration of ispPAC20



The pulse-width modulator is implemented by OA2, IA4, CP1 and CP2. The combination of OA2 and IA4 form a voltage ramp generator, with the ramp voltage appearing at the output of OA2. The direction of the ramp is controlled by the state of CP1OUT. Providing external feedback from the CP1OUT pin to the CPIN pin adds +/-2.5V of hysteresis to the CP1 comparator. When this wide-hysteresis comparator is combined with the ramp generator circuit, a triangle wave results at the output of OA2. This voltage is then compared to that at input IN3 to develop a PWM output with a duty cycle proportional to the IN3 voltage. Note that a resistive divider is placed between the output of the loop controller (OUT1) and the input of the PWM. This is to prevent the PWM from being driven outside of a preset range of duty cycles, and can be used to program the maximum effective output voltage to be applied to the TEC.

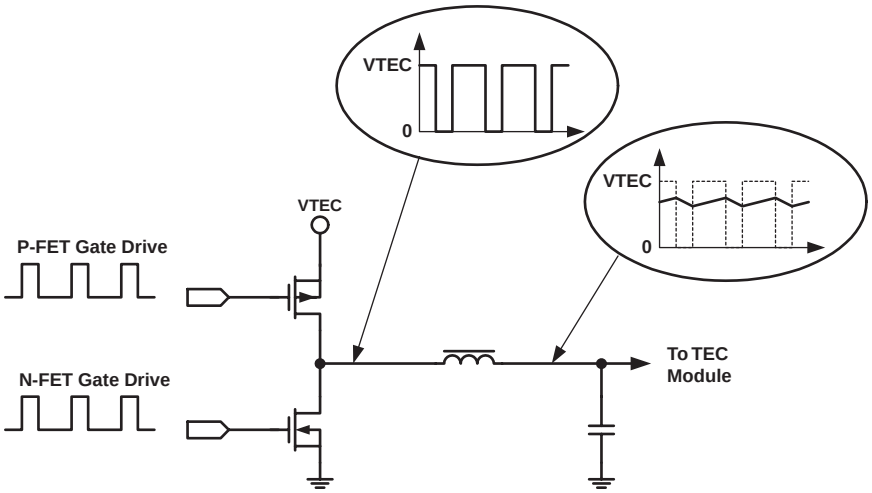
Power Output Driver

The PWM output developed by the ispPAC20 is phase split into true and inverted signals by a discrete FET driver circuit connected to the ispPAC20's CP2OUT output (see Figure 8). The resulting complementary signals are sent to opposite sides of the H-bridge driver. This has the effect of providing a duty cycle of DutyCycle% to one side of the H-bridge, and one of 100-DutyCycle% to the other side. The case where the duty cycle is 50% on both sides of the H-bridge corresponds to zero power applied to the TEC. The total voltage applied to the TEC (VDRV) by both sides of the H-bridge is proportional to

$$V_{DRV} \approx VTEC \times \left(\frac{DutyCycle\% - 50}{50} \right) \quad (3)$$

Figure 7 shows a simplified version of one side of the evaluation board's power driver.

Figure 7. Output Driver, One Side of Bridge

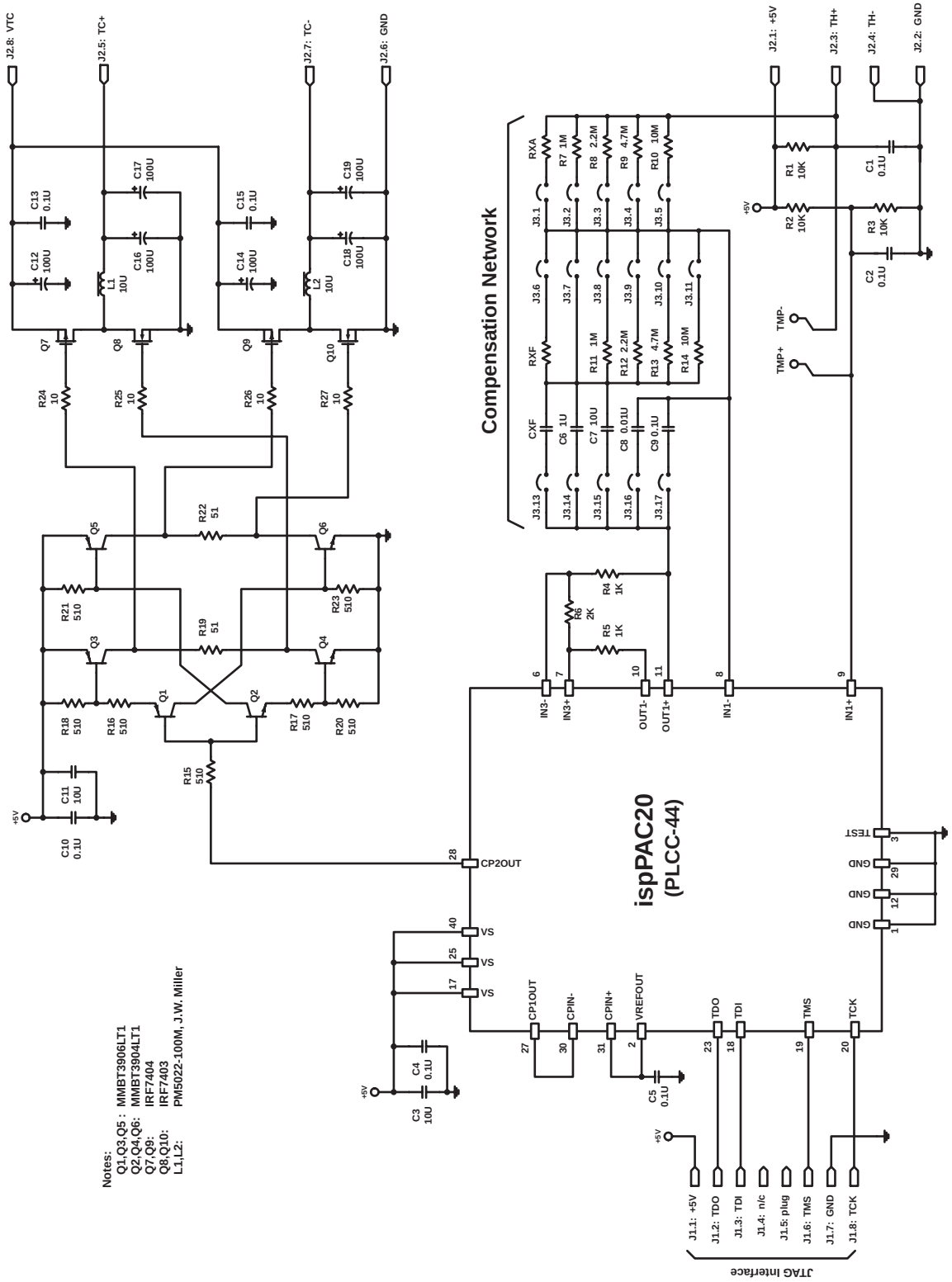


Each side of the H-bridge driver consists of an N-channel and a P-channel power MOSFET, connected to form a digital inverter. Because of the high currents conducted by these transistors in their respective ON states, the evaluation board's FET driver circuitry (Q1-Q6 and associated resistors, see Figure 8) is designed to ensure that there is a brief dead-zone between when one MOSFET turns OFF and the other turns ON, preventing crossover current from flowing directly from the VTEC supply to ground.

The LC filter placed at the output of each MOSFET pair converts the digital PWM signal present at their drains into a continuous DC voltage. In addition to a DC output, there is also a small amount of AC ripple superimposed on the output at the switching frequency. The exact amount of ripple is dependent on the PWM frequency, the choice of L and C, and the characteristics of the load. When the evaluation board is operated at 100kHz with the default component values, and a 1 Ω load, one can expect <100mV of ripple. Output ripple can be reduced to arbitrarily low levels by appropriate selection of output filter components. Because the time constant of the output filter is orders of magnitude faster than those of either the TEC or loop controller, it has negligible effect on either the accuracy or stability of the control system as a whole.

Detailed Schematic

Figure 8. ispPAC20-EVAL- PWMTEC Schematic



Board Artwork

Figure 9. Top side Silkscreen and Component Identification Drawing

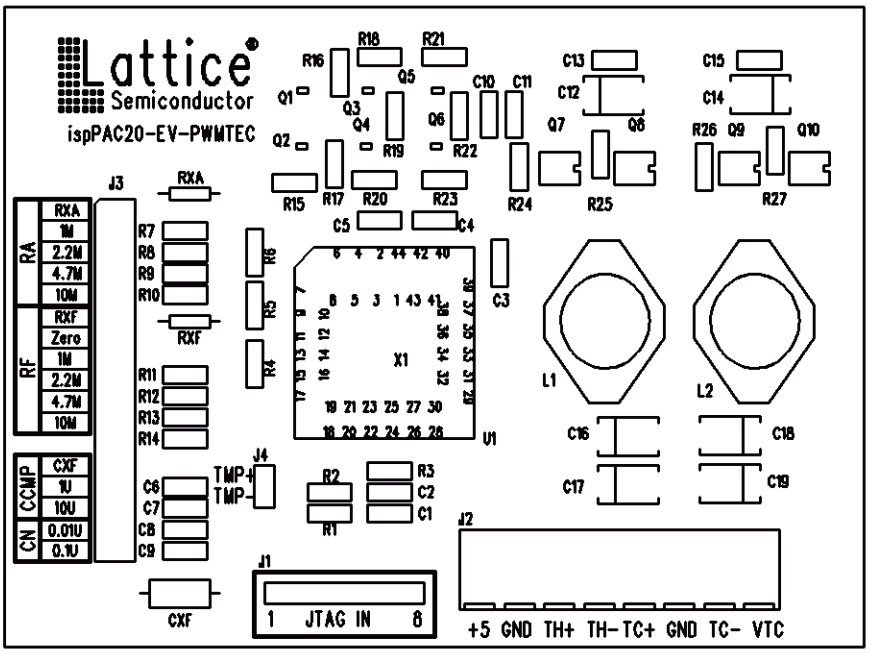


Figure 10. Top Side Foil Pattern

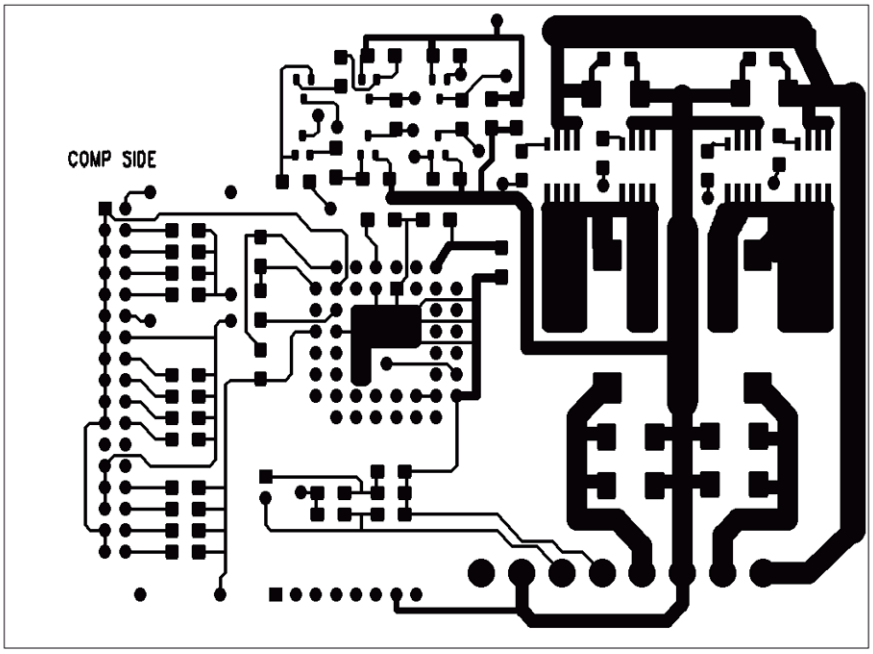
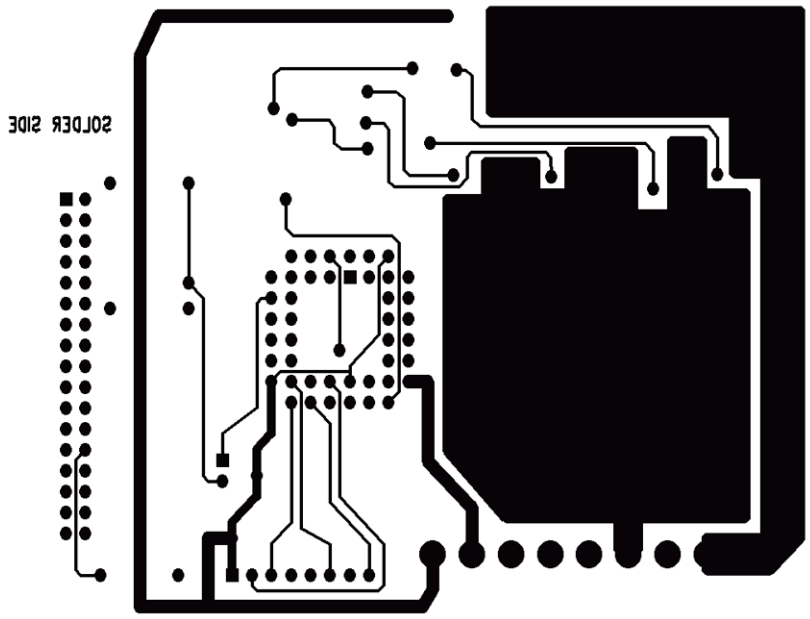


Figure 11. Bottom Side Foil Pattern



Components List

Quantity	Reference	Description
1	ispPAC20-EV-PWMTEC	ispPAC20-EV-PWMTEC Circuit Board
1	U1S	44 Pin PLCC Socket - Mill-Max
1	J1	8x1 0.100” spacing 0.025” header, single row
1	J2	8-position screw terminal block, Phoenix Contact 1729186
1	J3	17x2 0.100” spacing 0.025” header, dual row
1	J4.1	Test Point - Red (Keystone 5000)
1	J4.2	Test Point - Black (Keystone 5001)
4	FEET	Adhesive Rubber Feet
4	JUMPER	0.1” Shorting Blocks
1	U1	ispPAC20-PLCC44
3	Q1,Q3,Q5	MMBT3906LT1 PNP Transistor, SOT-23
3	Q2,Q4,Q6	MMBT3904LT1 NPN Transistor, SOT23
2	Q7,Q9	IRF7404 P-Channel Power MOSFET
2	Q8,Q10	IRF7403 N-Channel Power MOSFET
8	C1,C2,C4,C5,C9,C10, C13,C15	0.1uF 25V 10% X7R monolithic capacitor, SMD1206
2	C3,C11	10uF 10V Y5V multilayer chip capacitor, SMD1206
1	C6	1uF 16V 10% X7R monolithic capacitor, SMD1206
1	C7	10uF 6.3V 10% X7R monolithic capacitor, SMD1206
1	C8	0.01uF 50V 10% X7R monolithic capacitor, SMD1206
6	C12,C14,C16,C17, C18,C19	100uF 10V low-ESR tantalum capacitor, SMD7343
2	L1,L2	10uH Inductor, J.W. Miller PM5022-100M
3	R1,R2,R3	10.0 K, 1% resistor, SMD1206
2	R4,R5	1K, 5% resistor, SMD1206
1	R6	2K, 5% resistor, SMD1206
2	R7,R11	1 Meg 5% resistor, SMD1206
2	R8,R12	2.2 Meg, 5% resistor, SMD1206
2	R9,R13	4.7 Meg, 5% resistor, SMD1206
2	R10,R14	10 Meg, 5% resistor, SMD1206
7	R15,R16,R17,R18,R20, R21,R23	510 Ohm, 5% resistor, SMD1206
2	R19,R22	51 Ohm 5% resistor, SMD1206
4	R24,R25,R26,R27	10 Ohm 5% resistor, SMD1206
A/R		Solder
	RXA,RXF,CXC	Leave Unpopulated - User Installable

Technical Support Assistance

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