DesignCon 2008

A Reset Control Apparatus for PLL Power-Up Sequence and Auto-Synchronization

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CP-01037-1.0
February 2008

Abstract

A phase-locked loop (PLL) reset control apparatus is designed for a proper PLL power-up sequence and auto-synchronization. A very specific PLL power-up sequence during normal mode of operation as well as during reset mode is essential for PLL functionality and performance. This reset control apparatus ensures PLL components “wake up” in an orderly manner for proper operation when user presses RESET in order to resynchronize the PLL. This reset control machine takes two signals as input (user reset pulse and clock signal) and generates internal reset signals for each PLL comprising blocks.

Author Biographies

Kazi Asaduzzaman is a senior member of technical staff at Altera Corporation. He has over 11 years of experience in digital and mixed-signal circuit design. Kazi has worked on SERDES design in the Altera Mercury®, Stratix® GX, and Stratix II GX product lines, as well as PLL design in the Altera Cyclone® II, Cyclone III, and Stratix III product lines. Kazi holds a BSEE degree from University of California at Berkeley and MS degree from Santa Clara University. His areas of interest are in high-speed analog.

Kang-Wei Lai received a BS degree in electronic engineering from the National Chiao-Tung University, Taiwan, in 1990 and the MS degree in electrical and computer engineering from State University of New York, Buffalo, in 1996. He was a circuit designer at Sharp Technology Co., Taipei, from 1992 to 1996, and from 1996 to 2001, he was a circuit designer at Winbond Electronic Co., San Jose, CA. In 2001, he joined Altera Corporation and is currently a senior member of technical staff. Kang-Wei has worked on SERDES, phase-locked loops, and clock networking design in the Altera Stratix, Stratix II, Stratix III, and Cyclone III product lines. His area of interest is high-performance analog and mixed-signal integrated circuit design.

Wanli Chang is a senior member of technical staff at Altera Corporation. He has over 18 years of experience in digital and mixed signal circuit design. His experience includes Altera EAB circuit in Flex 10K® and APEX™ product lines, and clock generator PLL circuits in Flex 10K, APEX II, Stratix, Stratix II, and Stratix III product lines. Prior to joining Altera, he worked on FIFO and transceiver circuits at Cypress Semiconductor. Wanli holds a MSEE degree from Rensselaer Polytechnic Institute in New York.

Leon Zheng is a design engineer at Altera Corporation. He has over six years of experience in digital design and development. Leon has worked on DSP and PLL design in the Altera Stratix, Stratix II, Stratix III, and Cyclone III product lines. Leon holds a bachelors degree in electrical engineering from the University of Waterloo. His areas of interest are in high-speed design.

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Tim Hoang is a design manager at Altera Corporation. He has over 13 years of experience in digital and analog design and development. Tim has worked on SERDES and DPA design in the Altera Stratix GX and Stratix II GX product lines. Tim holds a BS degree in electrical engineering from University of California at Berkeley. His areas of interest are in high-speed analog.

Introduction

The phase-locked loop (PLL) circuit has become an essential part of many electronic components used in telecommunications and in timing synchronization.
Typical PLL applications can be found in analog modulators and demodulators, frequency synthesizers, and clock synchronizations. PLLs are widely used in a variety of applications and system configurations. PLLs are used not only for clock synthesis and for removing clock skew, but also for supporting many new features and a wide variety of applications.

When a PLL is used in a system configuration, it must wake up in an orderly manner for proper operation and functionality. Any change in system configuration or environment could force a user to reset the PLL. Any change in desired input and output frequency, phase requirements, input jitter variations, and many other system requirements could force a different PLL configuration and require resetting the PLL. After the reset event, the PLL must maintain its output to input phase and frequency relationship. When the PLL generates multiple phases, the proper relationship among those multiple phases must also be maintained. This paper describes a PLL reset control apparatus for a proper power-up sequence and auto resynchronization.

PLL Block's Power-Up Requirement

PLL is comprised of a number of critical blocks such as phase frequency detector (PFD), voltage-controlled oscillator (VCO), charge pump (CP), loop filter (LF), counter, and many other digital blocks, as shown in Figure 1. The voltage regulator (VR) has also become an essential building block for PLL design. The VR provides PLL internal voltage regulation and filtering for superior noise performance without the requirement of external power supply regulators. This PLL architecture uses a VR. When a PLL is used in system operation, proper synchronization among its comprising blocks is essential for functionality and performance. Each PLL critical block has its own power-up time, and a specific power-up sequence is necessary for proper PLL operation. Some of the restrictions on the power-up sequence of PLL building blocks during user reset operation are described below.

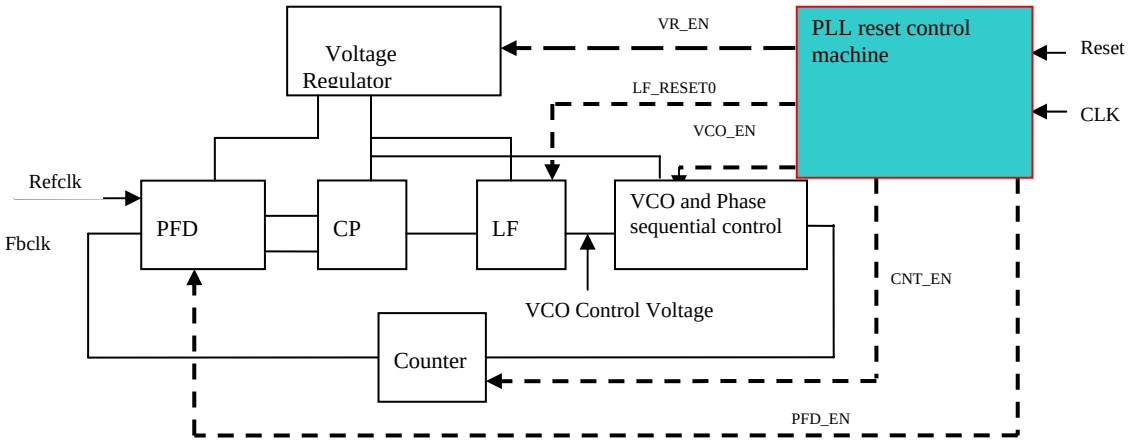


Figure 1. PLL Block Diagram With Reset Control Machine

First, the VR that provides supply voltage to the PLL critical blocks should be ready with stable output voltage before any of the PLL critical blocks wake up. This particular VR generates two different power supplies: one for PFD and one for other PLL analog blocks. Without a properly regulated power supply, the PLL blocks can't go through the power-up initialization. A VR usually comprises a significant area of PLL because it requires a large compensation capacitance and large decoupling cap for noise filtering. As a result, it needs a significant amount of time to generate a stable output.

Second, when the VCO starts toggling, the feedback counter should be ready to take the high-speed clock and be able to divide it without skipping cycles. This implies that counter must be enabled much earlier than the VCO.

Third, the VCO, which is generated from the LF, must charge up from zero voltage to 0.5 V_{CC} once the reset signal is released. This particular PLL used in the FPGA requires a very large LF (in the order of hundreds of pF) in order to maintain its loop stability in a large number of configurations where the size of the feedback counter value could be very large. The LF requires different stable output voltages during the reset event and after the reset event. For this PLL integrated in FPGA, the VCO must be grounded during the reset operation. This restriction originates from the power requirement during the reset event, as the designer may decide to keep the system in a state where the PLL sits idle mode for a long time. During the reset condition, the PLL should burn a negligible amount of current. Forcing the VCO to ground stops the VCO oscillation altogether and draws minimum amount of current. Once the reset signal is released, an LF with a large cap should also be given ample time to raise its voltage from zero voltage to 0.5 V_{CC}, which defines its center frequency. After the reset event, the LF is powered up with 0.5 V_{CC} in order to reduce the PLL lock time and to ensure that when the VCO wakes up it has a large enough input voltage to guarantee oscillation and to generate proper phases.

Finally, VCO phases must be enabled sequentially. With a four-stage delay cell, the VCO has eight phases which are 45° apart (0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°). For example, if the 45° VCO phase is enabled earlier than the 0° phase, then the PLL input clock and output clock phase alignment could be lost after the reset signal is released.

Design of PLL Reset Control Machine

This paper describes a PLL reset control state machine that ensures the PLL components wake up in orderly manner for the proper operation of the PLL when the user resets the PLL and then releases it. Figure 1 shows the general PLL architecture block diagram. A PFD compares the reference clock and feedback clock and generates UP and DN pulses to control CP. More UP pulses indicate the reference clock is faster than the feedback clock, while more DN pulses indicate the feedback clock is faster than the reference clock. These UP and DN signals drive the CP input, which is low pass filtered by the LF block. The output LF block acts as an input control voltage to VCO. The output of the VCO blocks feedbacks to the PFD through the feedback M counter. The output clock frequency of the VCO increases and decreases (more up pulses and down pulses

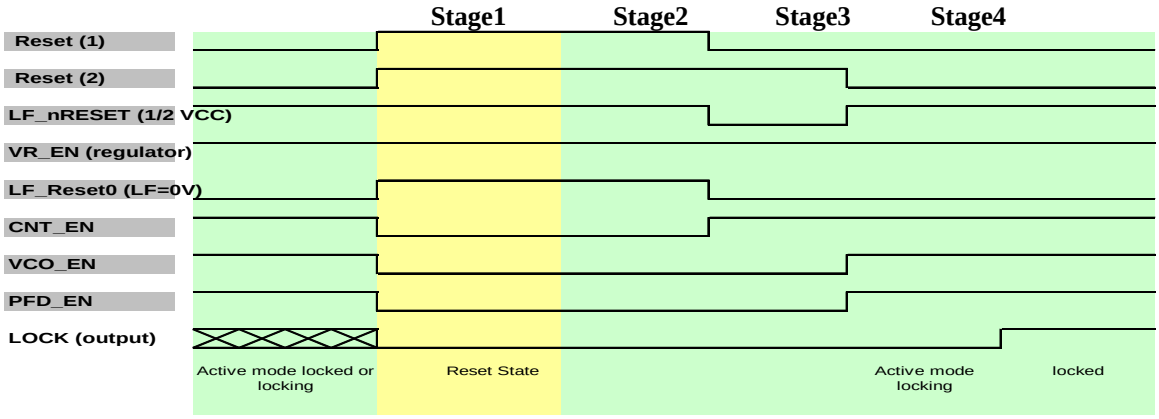
respectively) until the reference clock and feedback clock are frequency and phase aligned.

The PLL comprising blocks (PFD, CP, LF, and VCO) and the phase sequential control, counter, and VR, are controlled by an enable signal that controls each block's wake-up sequence. Figure 1 also shows the PLL reset control engine that generates all the enable signals for each PLL comprising block. This control block takes two signals (user reset pulse and clock signal) as input and generates control outputs that drive each of the PLL building blocks. This diagram also shows the VCO phase sequential control block, which ensures that all VCO phases are enabled sequentially.

PLL Control State Machine's Timing Specification

The PLL control engine is fed by a user reset pulse, the duration of which could be very small or long depending upon the system requirements. The PLL control engine generates two intermediate outputs, Reset(1) and Reset(2). The falling edge of Reset(1) is a delayed version of the falling edge of the user reset signal, and the falling edge of Reset(2) is a larger delayed version of the falling edge of the user reset signal. All of the PLL enable signals can be generated using these Reset(1) and Reset(2) signals along with user reset.

The PLL power-up sequence can be divided into four stages, as shown in Figure 2.



Bias Sources	on	on	on	on	on	on
PFD	enabled	**disabled**	disabled	disabled	**enabled**	enabled
$V_{CONTROL}$	free	**0V**	0V	1/2 VCCREG	free	free
VCO Frequency	locked(ing)	**N/A**	N/A	**F_{SYNCH}**	**locking**	**locked**
C & M Counters	synchronized	preset	preset	**enabled**	**synchronized**	synchronized
VCO phase output	enabled	**disabled**	disabled	**disabled**	enabled	enabled

Figure 2. PLL Control State Machine's Timing Specification

Stage1

Once the reset signal is triggered (go high), all the enable signals that control PLL comprising blocks become disabled (except the VR enable signal) and remain disabled for the duration of reset pulse. The VR that provides supply voltage to the PLL critical analog blocks such as CP, PFD, LF, and VCO should always be ready with stable output voltage. Without a properly regulated power supply, the PLL blocks can't go through the power-up initialization. During the reset process, the VR is the only block that is kept

active. Disabling the VR during the reset operation would increase PLL lock time substantially. During the reset operation, the VCO is set to ground. As a result, the VCO doesn't toggle, and it draws a very negligible amount of current from the VR. CNT_EN goes low, disabling the counter. PFD_EN and VCO_EN go low, which disables those blocks as well. The VCO phase-release sequential circuit also is disabled, at the same time disabling all eight phases of the VCO. LF_Reset0 goes high (active), which forces the VCO to ground and stopping oscillation. It must remain active for the duration of the user reset pulse. During reset, all the current and bias sources are turned off and the PLL burns a negligible amount of current.

Stage2

After reset is released (go low), a certain amount of time (as a function of the reference clock frequency) is provided so that the VCO can discharge to ground. Considering the fact that the user reset pulse could be very narrow and the VCO may need a long time to discharge from a specific voltage (determined by PLL input and output frequency before the reset signal is applied) to ground voltage, additional time was given at this stage. If the reset pulse is very narrow, there would not be a sufficient amount of time for the VCO to discharge to ground in Stage1. The PFD, CP, counter, and VCO phase output remains disabled at this stage.

Stage3

At this stage, the counter is enabled. Before the VCO starts toggling, the feedback counter should be ready to take the high-speed clock and be able to divide it without skipping cycles. If the feedback path is cut off because of the non-readiness of the counter, it could cause the PLL to stick in a state from which it can't recover. This implies that the counter must be enabled much earlier than VCO. At this stage, the enable signal (LF_Reset0) that forces the VCO to ground in Stage1 becomes inactive. Another enable signal (LF_nRESET) forces the VCO, which is generated from LF, to charge from zero voltage to 0.5 V_{CC}. Once the reset is released, the LF with a large cap should also be given ample time to raise its voltage from zero voltage to 0.5 V_{CC}. The VCO with 0.5 V_{CC} defines the PLL center frequency that usually lies between the VCO minimum and maximum frequencies. Once the reset is released, the VCO starts toggling at this known center frequency. This ensures that when the VCO phases are released in next stage, the VCO already has a defined and detectable output for the counter and other blocks to use. Centering the PLL frequency during the release of reset also reduces the PLL lock time.

Stage4

Finally, the VCO and PFD are enabled at the falling edge of the Reset(2) signal, which starts the PLL locking process. The enable signal (LF_nRESET) that forces the VCO to 0.5 V_{CC} becomes inactive at this stage and the VCO becomes free running. The VCO phases also need to be enabled sequentially at this stage. With a four-stage delay cell, the VCO has eight phases which are 45° apart (0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°). In a PLL loop, there are multiple counters—some of them are in the feedback path and others are in the output path. Each of the counters uses the VCO output as its input. If the VCO phases are not enabled sequentially, they can generate glitches that can easily be transferred to the input of the counter. A narrow glitch could cause the counter to

malfunction. If the VCO phases are not released sequentially, it could also disrupt the PLL input and output phase relationship. For example, if the 45° VCO phase is enabled earlier than the 0° phase, then the PLL input clock and output clock phase alignment could be lost after the reset signal is released. In Stage4, the VCO phases are enabled sequentially (0° first, 45° second, 90° third, etc.)

Simple Implementation of PLL Reset Control

Figure 3 shows the simple implementation of the PLL reset control state machine. The digital "counter" takes two inputs—the PLL reference clock (CLK) and the user reset signal. It starts counting at the falling edge of reset (when reset is released) and generates two outputs, CNT_X and CNT_Y. These two outputs drive two DFFs with preset and CLR and generate output Reset(1) and Reset(2). All the PLL block enable signals can be generated using these two outputs and the user reset using simple logics (not shown in the above block diagram).

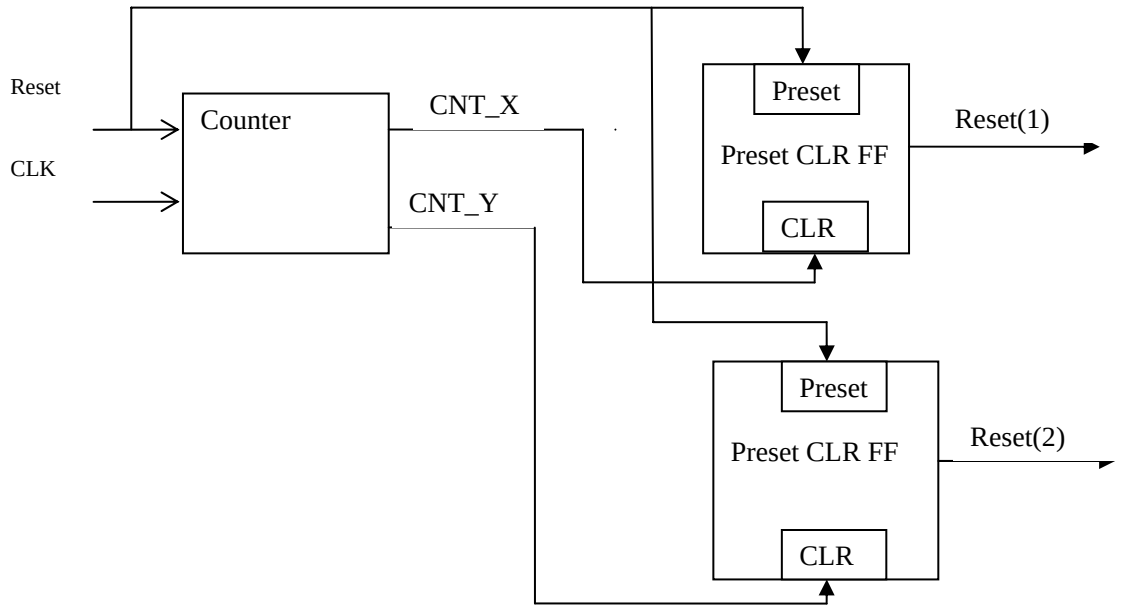


Figure 3. PLL Reset Control Machine's Block Diagram

The amount of time allowed for the VCO to discharge to 0 from a specific voltage is the difference of falling edges between the user reset and Reset(1) signal, in this case X PLL reference clock cycles. The amount of time allowed for the VCO control node to reach from 0V to 0.5 V_{CC} is the difference of falling edges between the user reset and Reset(2) signals, in this case (Y-X) cycles of reference clock. The charge and discharge time requirements are calculated based on the highest reference frequency. Figure 4 illustrates these timing requirements.

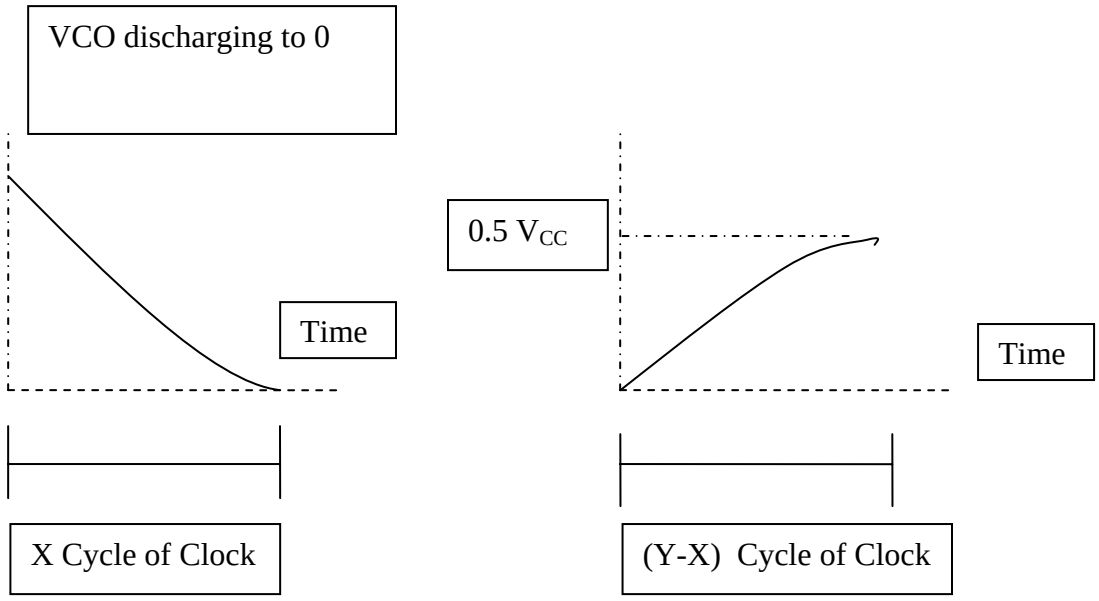


Figure 4. VCO Charging Up and Down

Conclusion

The above described invention ensures that the PLL comprising blocks—PFD, CP, LF, VCO, counter, and others—wake up in proper sequence when the user presses the reset signal and then releases. This proper sequence of PLL enable signals is needed not only for correct synchronization and timing, but is essential also for PLL functionality. For example, if the counter in the feedback path isn't enabled before the VCO, it could result in a malfunction of the PLL. If the VR output is not stable when the reset signal is released, it could also drive the PLL to an unknown state from which it could never recover. The above invention ensures that the PLL consumes a negligible amount of current (µA range) during the whole reset operation. This is essential because in many applications that use a PLL, the user may keep the PLL in idle mode by asserting the reset signal, thus saving significant power. The synchronization control engine also ensures that the PLL input and outputs are properly phase aligned once the reset signal is released and the PLL locks. For example, if the counter isn't enabled before the VCO, it could miss few a VCO cycles and the PLL input-output phase relationship may not be restored.

The described PLL with a reset control state machine was fabricated in TSMC's 65-nm process with fully functional results. During the normal power-up sequence, the PLL woke up properly and the PLL phase input and output phase relationship looked as expected. The PLL maintained its phase relationship between input and outputs (clock network, core register, LVDS network, output pin, etc.) before and after the user reset event.

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