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FPGA I/O Timing Variations Due to Simultaneous Switching Outputs

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Abstract

Voltage noise and timing variations due to simultaneous switching outputs (SSO) impact the performance of modern nano-technology devices. There is a lack of research of I/O timing variations due to SSO; the frequency relationships between the victim and aggressors I/Os have not been revealed. In this paper, we study signal timing variations of two parts: output driver and pre-drive stages. We show that output driver signal timing is affected by crosstalk and power distribution network (PDN) noise. Pre-drive signal timing is affected by PDN noise. This study determined that maximum pre-drive timing variation happens when aggressors switch at half of the PDN resonance frequency. This differs from the well studied logic-level variations at SSO which peak at the PDN resonance frequency. We developed measurement techniques to separate the various noise sources, taking into consideration both synchronous and asynchronous cases. This paper provides simple, scalable models that can be used to evaluate timing variations in the presence of power supply and crosstalk noise.

Author Biographies

Zhe Li is a senior product engineer at Altera Corporation. He received his MSEE from the University of Missouri-Rolla. His interests include signal integrity and power integrity analysis. Currently, he is working on characterization, modeling, and correlation of FPGA high-speed I/O interfaces.

Iliya Zamek has over 20 years of experience with high-speed analog and digital circuits, memory, system design, project management and product development. He is a member of the technical staff at Altera Corporation. Besides developing testers and measurement methodology for FPGA characterization, he leads R&D projects on modeling and prediction jitter in FPGAs and noise in power distribution networks. Prior to joining Altera, he worked for U.S.-based crystal oscillator manufacturers Q-Tech and Statek Corp., and, earlier, for the leading Russian instrumentation corporation, Quartz. He received BS and MS degrees in physics and electronics from Gorky University, and a PhD in measurement techniques. He has published more than 50 papers, and has earned 12 patents, with six more pending.

Peter Boyle received his bachelor's degree in computer engineering from the Georgia Institute of Technology in 1999. He currently works for Altera Corporation as a manager in the product engineering characterization group, which is responsible for measurement of I/Os, phase-locked loops (PLL), external memory interface, and simultaneous switching noise (SSN). His interests include system-level measurement techniques and modeling. He has several inventions pending.

Bozidar Krsnik received his MSEE from the University of Zagreb. He developed extensive experience in test and characterization of ICs in various engineering and management positions with Siemens and Teradyne. Krsnik strengthened his multicultural background while working in Austria, Singapore, France, and the U.S. He managed the characterization group for a 220-nm joint process development project with IBM/Toshiba in East Fishkill, New York. Krsnik is the author of three patents in the design for test field. He has published over 10 papers and a tutorial at IEEE conferences. Currently, he characterizes FPGAs, focusing on signal integrity, at Altera Corporation in San Jose.

TABLE OF CONTENTS

I. Introduction

The higher speed and power consumption of modern nano-technology ICs has brought some new issues. One of them is timing variations due to simultaneous switching inputs and outputs (I/Os). A number of studies have been done on FPGA simultaneously switching noise (SSN) [1-3], when toggling I/Os affect logic levels of a victim channel. In contrast, the research of timing variations due to I/O switching noise is just at the beginning.

Importance of timing analysis in nano-technology devices has increased with increasing devices speed and degree of the integrations. Recent deployments of high-speed memory interfaces like DDR3 and QDR II+ raise the requirements on timing closure. Tens of picoseconds become significant for closing the timing budget. This creates a substantial challenge for the FPGA designer to manage system performance and meet critical timing constraints.

Timing analysis under SSN conditions has some principal distinctions compared to the impact of SSN on logic levels. In SSN analysis, noise affects victim's logic levels which are in a "static" condition, in contrast to the timing variations effects, where the victim itself is dynamically switching. This analysis requires monitoring of the timing and frequency relationship between the victim and aggressors. The frequency relationships were introduced in [4, 5] for the jitter measurements of a periodic signal with one sine wave component in jitter spectrum only. The MIN/MAX effects and complex jitter behavior were demonstrated in [4, 5] even in such simple jitter spectrum case. The jitter spectrum of a victim due to switching I/O aggressors inside integrated circuit has much more complex character than considered in [4, 5]. However, the frequency relationship for main MINs and MAXs are the same, which helped use these frequency relationships for the FPGA jitter measurements due to switching core components and I/Os in [6].

This paper tackles the problems of timing variations due to SSN that includes induced crosstalk, delta-I noise, as well as the power supply resonance analysis on power distribution networks (PDN). Delta-I noise and power supply resonance at pre-drive stages will be analyzed separately as they have distinct timing impacts on I/O buffer delay variations. The PDN model used for the simulation allows the identification of the dominant power supply noise and yields the time response for the on-chip power rails.

The paper is organized as follows. Section II introduces the FPGA system and I/O buffer with pre-drive stages and output off-chip driver. In Section III, we discuss our timing analysis methodology on off-chip signal which includes the effects of crosstalk and power supply noise. In Section IV, we introduce the PDN lumped circuit model for the pre-drive power supply. Measurements in conjunction with simulations were implemented to analyze the impacts on timing variations in both time and frequency domains. We examine the proposed timing analysis by applying it to accumulated timing variation analysis in Section V. Finally, a conclusion is drawn in section VI.

II. FPGA System and I/O Buffer Circuits

1. FPGA System

All the findings presented in this paper are based on the study of Altera® Stratix® family I/Os on a flip-chip package with BGA footprints. Figure 1 provides us with an overview of the FPGA system with Die-Package-PCB structures. Input/Output signals will travel through package transmission line, package vias and solder balls and then get to the PCB level through the PCB vias. Also shown are the power supply connections, with power/ground planes and power/ground vias through package substrates, power/ground pins, solder balls, PCB vias and PCB power/ground planes.

From Figure 1, we see there are two major ways how switching aggressor I/Os might affect the timing of an I/O victim. One way is through direct impact of the aggressor magnetic flux to the victim path. This impact happens along the whole victim path including package and PCB vias. The other way for the aggressor to change the I/O victim edge's delay is through the power supplies. Simultaneously switching aggressors consume significant current. When consumption current peak happens, it causes the power sags, ground bounces, and power supply resonances, which affect the signal delay through I/O circuits.

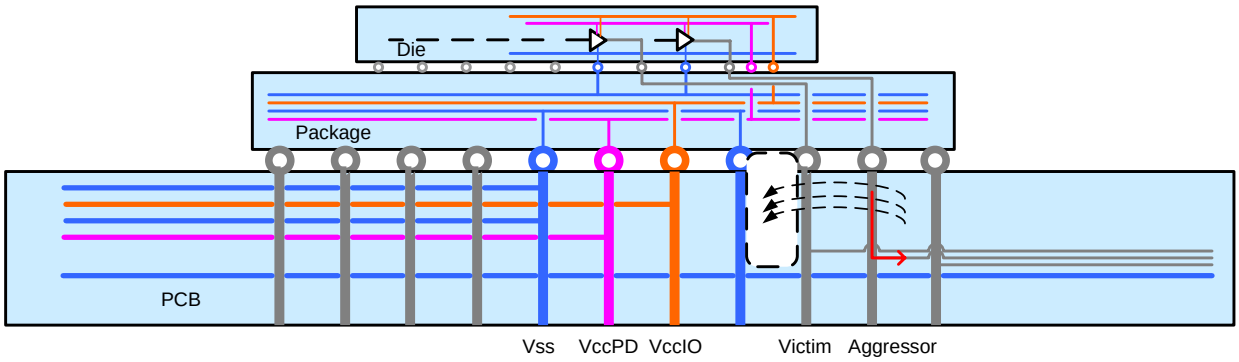

Figure 1. System Overview of Simultaneous Switching Noise

2. I/O Buffer

Stratix family devices were developed to support high-speed memory interfaces and provide high-performance I/Os with programming capabilities for different drive strengths, slew rates, and delay controls. With increasing speed and ability to integrate more functions in the I/O cells, the I/O buffer itself is becoming increasingly complicated.

Figure 2 shows the block diagram of the output buffer in an I/O cell. The main components in the I/O cell are:

- Fast output register with fast timing control from clock to output data
- Output control block, which enables delay adjustment and splits up output signal into P and N branches.
- Level shifter, which is a high-gain differential amplifier converting signals from 1.2V core logic to 3.3V I/O logic
- Pre-drive on-chip driver stage, which contains a chain of thick oxide inverters providing fast signal transitions and strong current drive
- Output driver, which is the last stage of the output buffer to drive off-chip signal and interface with package and PCB environment. The output driver is a typical CMOS driver with pull-up and pull-down MOSFET.

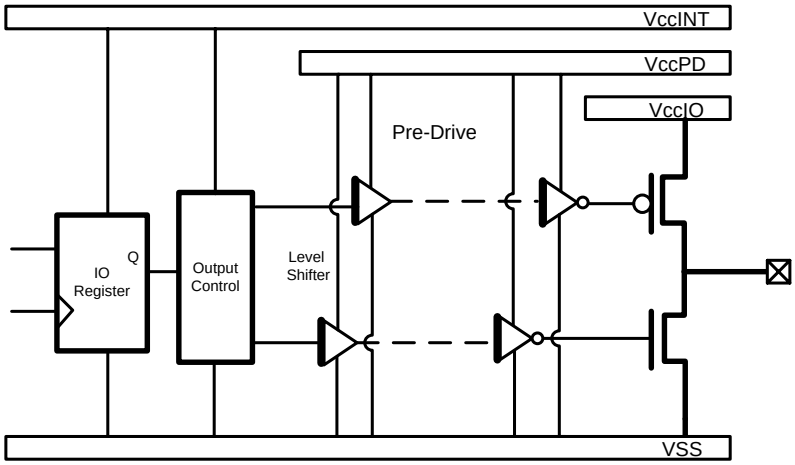

Figure 2. Stratix Family Device Output Driver Block Diagram

The diagram above explains the output buffer circuits and their power supply networks. As the victim signal passes through each stage, its timing will be affected by power supply voltage fluctuations. For best speed and power optimization, the output buffer consists of multiple stages through different power domains. Typical SSN analysis would focus on predicting the voltage noise on V_{CCIO} and analyze signal logic-level degradation on its path through the output driver to the PCB traces and to the receiver. While logic-level degradation due to SSN practically does not depend on the pre-drive stages, timing variations are affected by both pre-drive stages and output driver noise. Moreover, pre-drive stages consume relatively high currents and produce significant power supply noise on V_{CCPD} [7].

In this paper, we develop our timing analysis in two parts: output off-chip driver signal timing variations and signal timing variations through pre-drive on-chip buffers. Off-chip signal timing is affected by crosstalk and power supply network (PDN) noise. On-chip pre-drive signal timing is affected by PDN noise including Delta-I noise and power supply resonances.

III. Output Driver Signal Timing Variations

1. Package and PCB Pin-Field Crosstalk and Its Impact on Timing Variations

1.1 Voltage Noise Due to Inductive Crosstalk

Inductive crosstalk is a dominant noise source at the package and PCB pin-field region. From package solder balls to PCB via structures, signals become inductively coupled to each other as they share the current return path from the same group of power and ground pins. Package and PCB pin-field crosstalk is a function of the mutual inductance between victim and aggressors, which is a function of the proximity of aggressor pin locations to the victim signal pin. Aggressor pins that are further away from the victim pin will generate less and less noise.

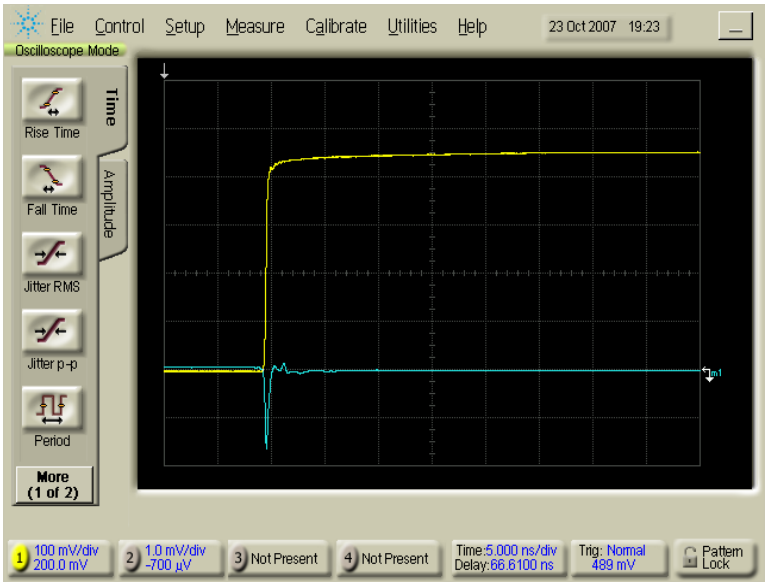

Figure 3. Crosstalk noise measured on the quiet-low victim signal in sync with the aggressor outputs, switching from low to high

One way to quantify the crosstalk noise in the package and PCB pin-field region is through the spiral pattern analysis. The aggressors start to switch on from the I/Os close to the victim and spiral out in a binary sequence until it reaches the maximum number of I/Os available in an I/O bank. The crosstalk noise is measured on the quiet low signal against its quiet low level. As opposed to the quiet high measurements, the quiet low signal is not affected by the power supply noise that might be present on V_{CCIO}. The measurement is performed on the victim signal with all the I/Os setup with SSTL18 Class I topology, 50Ω series on-chip Termination, and no load capacitors. As shown in Figure 3, the crosstalk noise from the pin-field region can be captured on the quiet low victim signal at its far-end termination.

U1	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
AA	GND	GND	AA8	AA9	AA10	AA11	AA12	VCC	GND	VCC	GND	VCC	GND	VCC	GND	VCC
AB	GND	GND	AB8	GND	GND	GND	GND	GND	GND	GND	**AB16**	AB17	AB18	GND	AB20	AB21
AC	GND	GND	GND	AC9	GND	AC11	GND	**AC13**	**AC14**	**AC15**	**AC16**	**AC17**	AC18	AC19	AC20	AC21
AD	GND	GND	GND	GND	GND	GND	GND	**AD13**	**AD14**	GND	VCCPD	VCCPD	GND	VCCPD	VCCPD	GND
AE	GND	AE7	AE8	AE9	AE10	AE11	VCCN	**AE13**	AE14	VCCN	VCC		VCC	VCCN	VCCN	VCCN
AF	GND	AF7	AF8	AF9	**AF10**	AF11	VCCN	**AF13**	AF14	VCCN	VCC	GND	GND	GND	VCC	VCCN
AG	GND	GND	**AG8**	GND	**AG10**	**AG11**	GND	**AG13**	**AG14**	GND	VCCN	GND	GND	VCCN		GND
AH	GND	**AH7**	**AH8**	**AH9**	**AH10**	**AH11**	**AH12**	**AH13**	**AH14**	**AH15**	**AH16**	**AH17**	AH18	AH19	AH20	AH21
AJ	GND	**AJ7**	**AJ8**	**AJ9**	**AJ10**	**AJ11**	**AJ12**	**AJ13**	**AJ14**	**AJ15**	**AJ16**	**AJ17**	AJ18	AJ19	AJ20	AJ21
AK	GND	GND	**AK8**	GND	VREF	**AK11**	GND	VREF	**AK14**	GND	**AK16**	VREF	GND	**AK19**	AK20	GND
AL	GND	**AL7**	**AL8**	**AL9**	**AL10**	**AL11**	**AL12**	**AL13**	**AL14**	**AL15**	**AL16**	**AL17**	**AL18**	**AL19**	AL20	AL21
AM	GND	**AM7**	**AM8**	**AM9**	**AM10**	**AM11**	AM12	AM13	AM14	**AM15**	AM16	**AM17**	**AM18**	AM19	AM20	AM21
AN	GND	GND	**AN8**	GND	**AN10**	**AN11**	GND	**AN13**	**AN14**	GND	**AN16**	**AN17**	GND	AN19	AN20	GND
AP	GND	**AP7**	**AP8**	**AP9**	**AP10**	**AP11**	**AP12**	**AP13**	**AP14**	**AP15**	**AP16**	**AP17**	**AP18**	**AP19**	AP20	AP21

victim
∑ Aggressors = 1
∑ Aggressors = 2
∑ Aggressors = 4
∑ Aggressors = 8
∑ Aggressors = 16
∑ Aggressors = 32
∑ Aggressors = 48
∑ Aggressors = 64
∑ Aggressors = 87 (All)

Figure 4. Aggressor Spiral Pattern. Total 87 aggressors are available. Victim signal is located at pin AL13.

As aggressor I/Os spiral out, the crosstalk-induced noise will saturate after certain numbers of I/Os, Figure 5. Saturation curve from the victim quiet low waveform can clearly show the proximity effect of the inductive crosstalk. Similar crosstalk noise effects have been reported for SSN voltage noise margin analysis in [1].

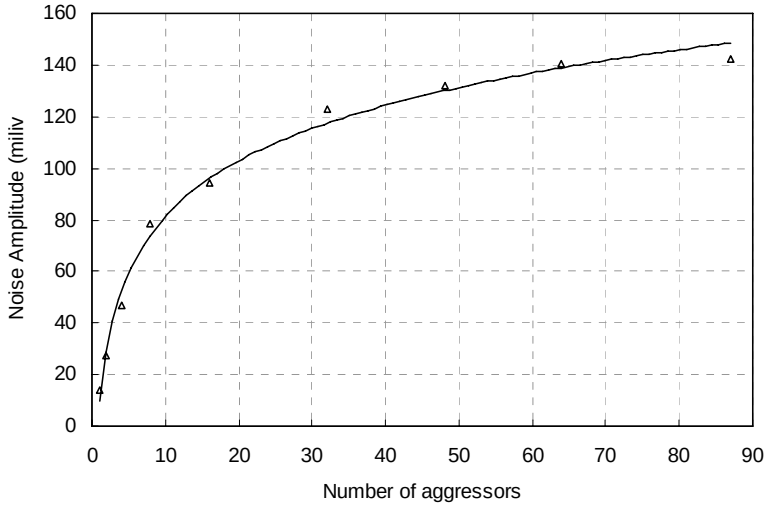

Figure 5. Crosstalk noise saturation effect due to aggressor spatial distribution

1.2. Timing Variations Due to Inductive Crosstalk

Inductive crosstalk affects the signals at the package and PCB pin field, which is a linear, passive region. Superposition rule can be applied for evaluating the timing impacts of the crosstalk noise. When there is no transition, coupled noise simply changes the signal level. When the noise coupling happens at the signal transition, signal edge will be shifted earlier or later. If a negative crosstalk induced pulse is coupled, the victim rising edge will arrive later than the distortion-free edge, which is a timing push-out case. On the other hand, if the crosstalk-induced pulse goes positive, the distorted victim rising edge arrives earlier, a timing pull-in case. Crosstalk induced pulse effects on victim falling edge can also be explained through the same mechanism.

To simplify the process for calculating the victim timing pull-in/push-out, here are some facts about the pulse waveform induced by the inductive crosstalk:

- Timing pull-in and push-out due to inductive crosstalk occur during transitions of the aggressor signals, as shown in Figure 3 (rise time). Pulse width of the crosstalk noise is bounded by the signal transition time.
- Noise amplitude from crosstalk is relatively small compared to the signal amplitude.

Maximum pulse amplitude is 150mV as is observed on the saturation curve. Typical signal swing on SSTL1.8 Class I I/Os is about 900mV. So maximum noise amplitude induced by inductive crosstalk is about 17 percent of the total signal swing. With relatively small noise amplitude, the linear model can be used for timing variation calculations.

As shown in Figure 6, when the crosstalk-induced pulse is superimposed on the rising edge of the victim signal, the victim signal edge is pushed out and the time delay is linearly proportional to the crosstalk

induced pulse amplitude. Assuming that the signal at the middle point ramps up with a constant rate, signal timing variations can be calculated as:

$$\Delta t_{crosstalk,t=T1} = \frac{V_{crosstalk}}{Edge\,Rate}$$

Signal timing as well as the crosstalk noise waveform is influenced by the loading conditions on the signal line. Loading effects are not in the interest of this paper. For the sake of simplicity, we keep 50Ω terminations throughout the simulations and measurements so the signal timing variations are consistent at both far-end and near-end observations.

Figure 6. Crosstalk-induced timing variations. This is a timing push-out case on the victim rising edge. Negative pulse in blue is the inductively coupled noise on the victim quiet low signal when aggressors switching from low to high. Yellow is distortion-free victim signal edge. Green is distorted victim edge by the crosstalk noise.

2. Output Driver PDN Noise and Its Timing Impacts

2.1. Output Driver PDN Noise

Power supply noise on V_{CCIO} will impact the output drivers and reflect on the output signals. This provides us with a method to measure the power supply noise presented on V_{CCIO}. As shown in Figure 7, subtraction from quiet high to quiet low will remove the crosstalk and reveal the V_{CCIO} power supply noise.

The power supply voltage on V_{CCIO} is influenced by the switching currents drawn by aggressors and oscillates with the PDN die-package parallel resonances. The power supply noise on V_{CCIO} is a relatively slow effect compared to the signal transition time and crosstalk-induced pulse. Also as opposed to the crosstalk noise, power supply noise will increase linearly with the number of aggressors and no location dependence is associated with each aggressor.

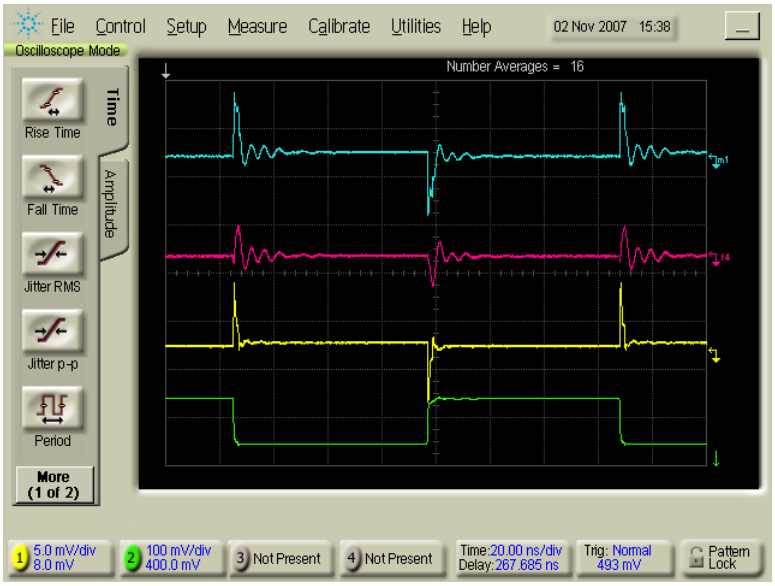

Figure 7. Power Supply Noise on V_{CCIO}. Upper blue curve is the quiet-high victim signal with SSO. The lower Yellow curve is the quiet-low victim signal. The middle Magenta one is subtraction from quiet-high to quiet-low to get the power supply noise on V_{CCIO}

2.2. Static Timing Variations Calculation with Dynamic Power Supply Noise

Output driver delay depends on the power supply voltage. When dealing with power supply resonances, Static Time Analysis (STA) approach can be applied as the buffer switches with a much faster transition rate. At the moment of transitions, the driver sees almost a constant voltage on its power supply. Figure 8 shows the SPICE simulations and measurements for the propagation delay through output driver at the different V_{CCIO} voltage levels. Output driver delay does not follow a linear scale with the voltage variations. Low V_{CCIO} voltage produces larger propagation delays. Buffer delay variations with the presence of power supply oscillations can be calculated as:

$$\Delta t_{off-chip,t} = -k(V) \times \Delta V_{off-chip}(t)$$

Where the timing variations coefficient is extracted with linear interpolations within a certain voltage range. Based on the voltage variation at the corresponding timing location, the output driver delays the variation of the output buffer.

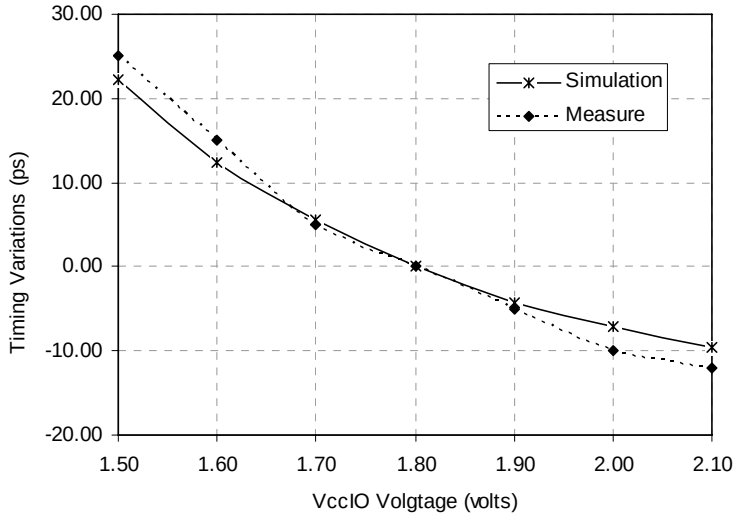

Figure 8. Static timing analysis with voltage level variations on V_{CCIO}

IV. Pre-Drive Signal Timing Variations

Pre-drive stages include the level shifter and pre-drive on-chip buffer chain, which are all tied onto the V_{CCPD} power supply. On-chip and off-chip drivers create different transient stimulus to the PDN and produce different power supply noise. As shown in Figure 9, power supply noise on V_{CCPD} includes two major components, Delta-I noise and power supply resonances, at both the rising and falling edge of the aggressor signal. Delta-I noise is developed at the time when a surge of transient current is applied on the power supply network. A slow varying power supply resonance is shown after the drivers complete their transitions.

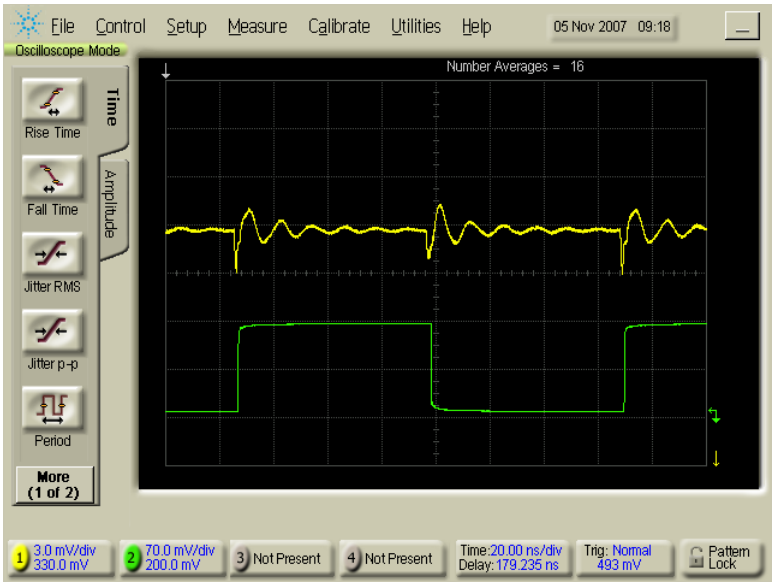

Figure 9. Power supply noise on V_{CCPD} in sync with the aggressor signal. Delta-I noise and power supply resonances at both rising and falling edge. The power supply noise is measured with 10:1 7.5GHz passive probe, probing on the DUT pins under the PCB. Real-time waveforms are captured on an equivalent-time oscilloscope for its high bandwidth and high sampling rates.

1. PDN Lumped Circuit Model and PDN Resonance

PDN in the FPGA system can be represented with an equivalent circuit model, as shown in Figure 10. The on-die decoupling capacitance is implemented as a charge reservoir providing transient currents for the switching I/Os. The power/ground pins through die, package and PCB are typically resistive and inductive in nature, which in many cases can be lumped into effective circuit elements. Although kept small with flipchip and BGA package, the package/PCB parasitic inductance still poses as a primary detrimental effect in the power supply networks. The initial voltage drop on the power/ground terminals is proportional to $L_{effective}\frac{di}{dt}$, Figure 9. With the on-chip decoupling capacitance, it also forms a parallel resonant circuit with its resonance frequency at $f_c = \frac{1}{2\pi\sqrt{L_{effective}C_{on-die}}}$.

A common way for evaluating PDN performance is to measure the PDN impedance as a function of frequency. Based on the lumped circuit model, the PDN input impedance can be determined through an AC sweep at the die location where the on-chip drivers are replaced with an AC current source. The resulting voltage at the die power/ground terminals is proportional to the PDN impedance. As shown in Figure 11, PDN impedance peaks at the parallel resonance frequency.

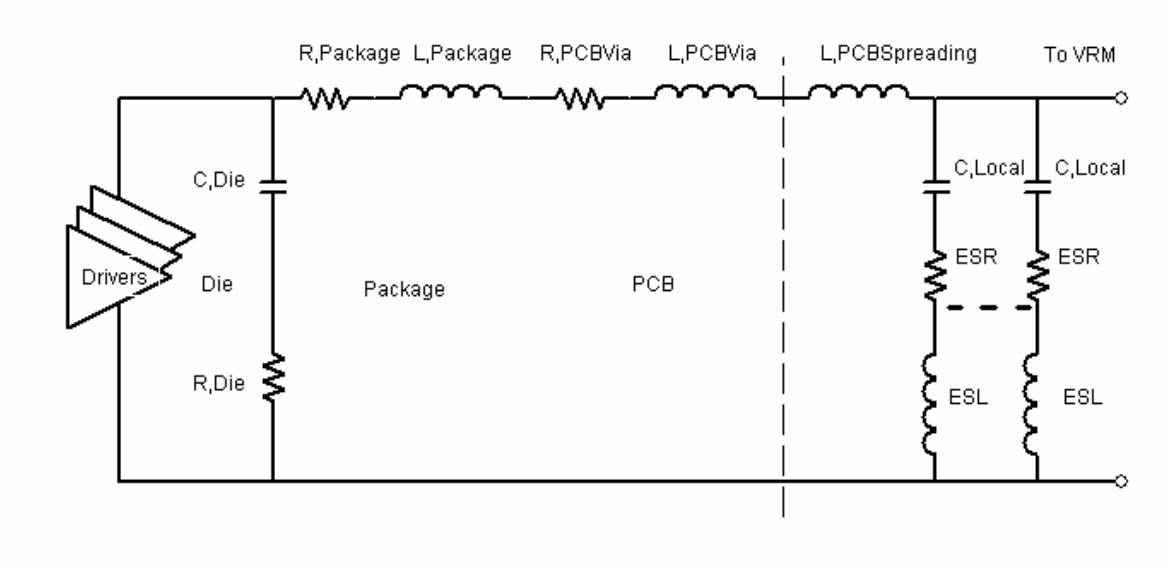

Figure 10. Lumped circuit model for typical power supply networks

It is widely adopted that power supply networks can be simplified to an RLC lumped circuit model and be accurate to simulate the actual performance up to a few hundred MHz. The reduction in computation cost to generate this simplified model versus full-wave electromagnetic (EM) simulations allows more complicated analysis with actual driver circuits to capture the timing effects.

Another assumption made in PDN circuit model is that V_{SS} connections contribute little to the effective inductance in the current loop. This is relatively true for flipchip package where the inductance associated with C4 bump is much smaller compared to the wire bonds in low cost packages. Also, V_{SS}, as the common voltage reference and current return path, is shared for all the signals and power supplies in the package and PCB. V_{SS} is distributed with solid metal layers and enriched with much higher pin count than the power connections.

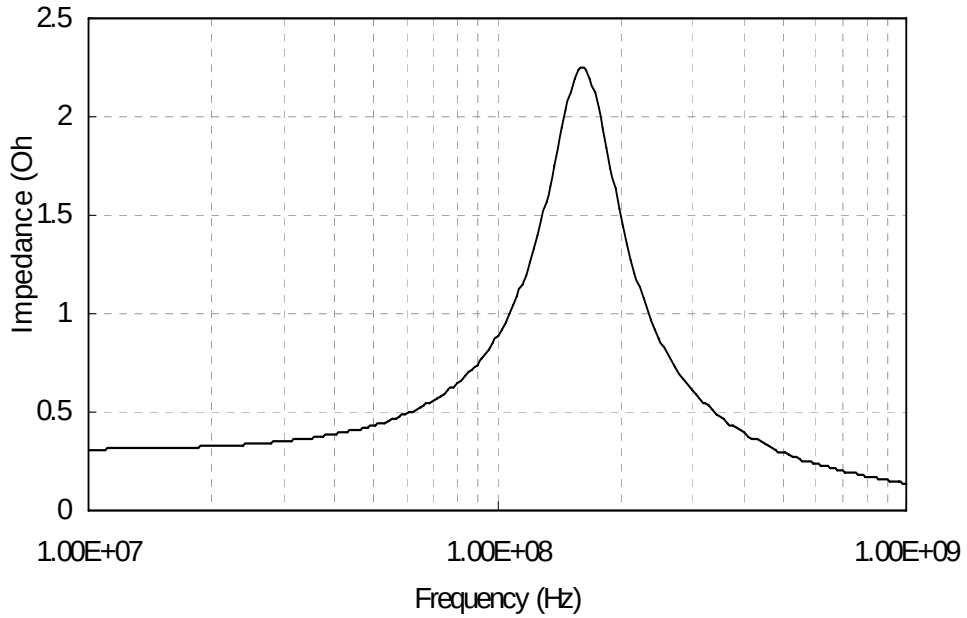

Figure 11. Power supply network impedance on V_{CCPD}. System resonance frequency is at about 160 MHz

Simulation and measurement results for time-domain power supply noise on V_{CCPD} are presented in Figure 12. Because of the highly resonant behavior of the power supply network, it is often possible to capture the noise waveform in time domain. The probing location will be at the DUT pins under the PCB. A total of 87 I/O buffers are switching. The same testing conditions are applied in the simulations. Combined with the PDN, the I/O buffers are simulated with the HSPICE scaled transistor model. Simulation waveforms are extracted at the equivalent terminals (across the dotted line in Figure 10) before the PCB spreading inductance. Good matching is found between the simulation and measurement results for both the voltage drop with the Delta-I noise and the resonant frequency with the power supply ringing.

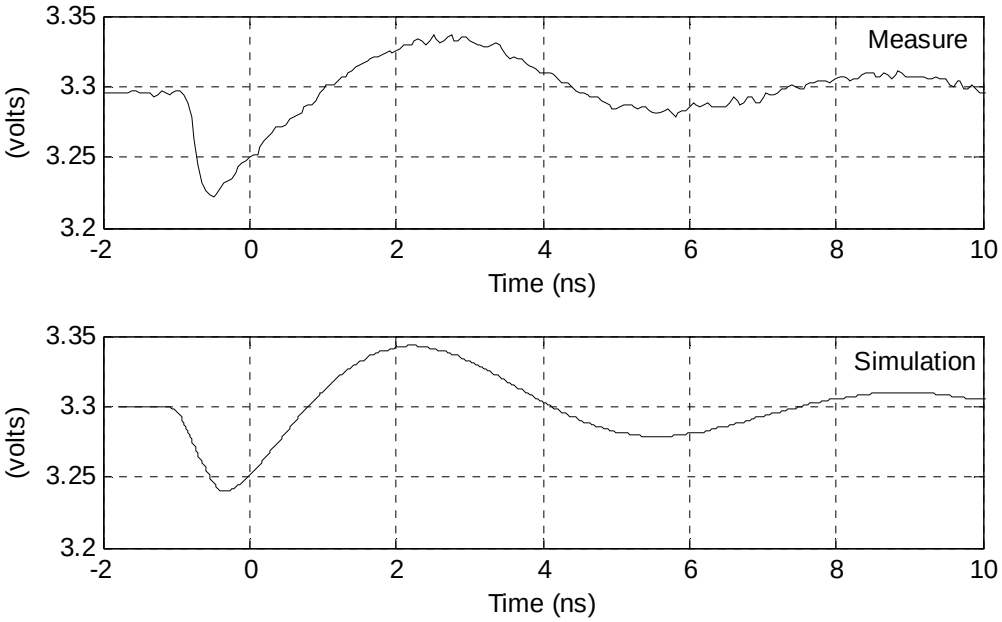

Figure 12. Simulated and measured V_{CCPD} power supply noise at DUT pins under PCB with 87 I/Os switching

2. Pre-Drive Power Supply Dynamic Current and Voltage

2.1. PDN Current and Voltage Waveform in Time Domain

With the established PDN and I/O buffer circuit model, Figure 13 shows the simulation results for pre-drive power supply noise correlated to switching currents and the aggressor signal. Large transient current occurs at both the aggressor rising and falling edge. When the transient current applied, PDN is stimulated first with a deep voltage drop, Delta-I noise, followed by slow varying oscillations. As expected, the voltage drop at the die location is much larger than the voltage captured on the PCB. The difference is determined by the ratio of total loop inductance to the PCB power plane spreading inductance. The total loop inductance is dominant by the inductance from package/PCB vias.

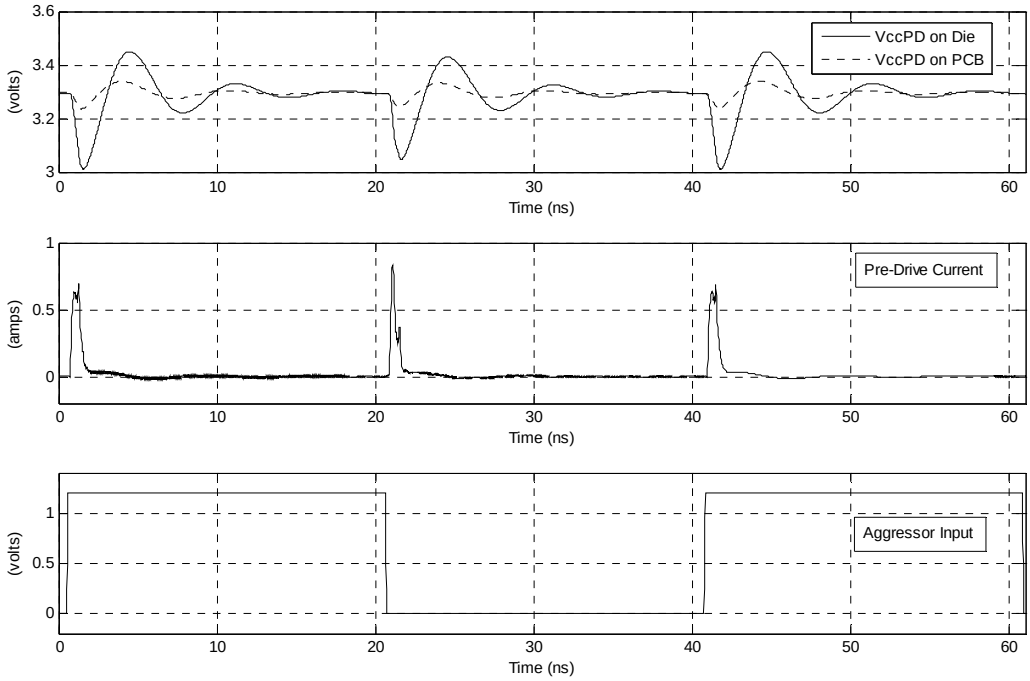

Figure 13. V_{CCPD} noise correlated to the switching current through pre-drive stages and aggressor signals in HSPICE simulations

2.2. PDN Current and Voltage in Frequency Domain

PDN impedance is a measure of the power supply noise on PDN stimulated with single-tone AC currents. The actual switching currents injected into the power supply network are full of frequency components in its spectrum. Given the switching current spectrum and PDN impedance, power supply noise can be calculated as:

$$V(f)=I(f)\cdot Z(f)$$

The actual power supply noise can be simulated with true I/O buffer models and PDN attachments. The above equation is helpful for evaluating the power supply noise with the switching currents at different aggressor frequencies. Figure 14 shows the frequency spectrum of the switching current in the same graph with the power supply impedance. The frequency spectrum of the switching currents is obtained through the Fast Fourier Transform on the currents captured from the simulation with toggling aggressor I/Os. Their switching frequency in the above simulation is at 25 MHz, with a 40 ns time period. The switching current happens at both the rising and falling edge of the aggressor, with a double rate at 50 MHz. This effect of the doubling aggressor frequency is also noted in our paper [8].

The main harmonic of the switching current is located at 50 MHz. The asymmetry of the current waveform at the rising and falling edge creates a weak sub-harmonic at 25 MHz.

Power supply noise is observed to peak at multiple aggressor switching frequencies. As the aggressor changing its switching frequency, the product of the switching current spectrum and PDN impedance will produce power supply noise with the spectrum signatures from both the current source and PDN impedance. The power supply noise will peak when the switching current spectrum carries the harmonic at its resonance frequency. Figure 15 shows the peak noise amplitude captured in time domain simulations at different aggressor switching frequencies. Maximum power supply noise happens when

aggressors switching at 80 MHz, which creates the currents repeating at the PDN resonance frequency, $F_{res}^{PDN} = 160MHz$. This differs significantly in the case of level variations at SSN, which has a peak exactly at the PDN resonance. There are also several local maximum points. The one at 160 MHz, aggressor switching frequency, is created by the weak sub-harmonic of the switching currents. The other ones at lower frequencies are created by the harmonics of aggressor whenever they crossover with the PDN resonance frequency.

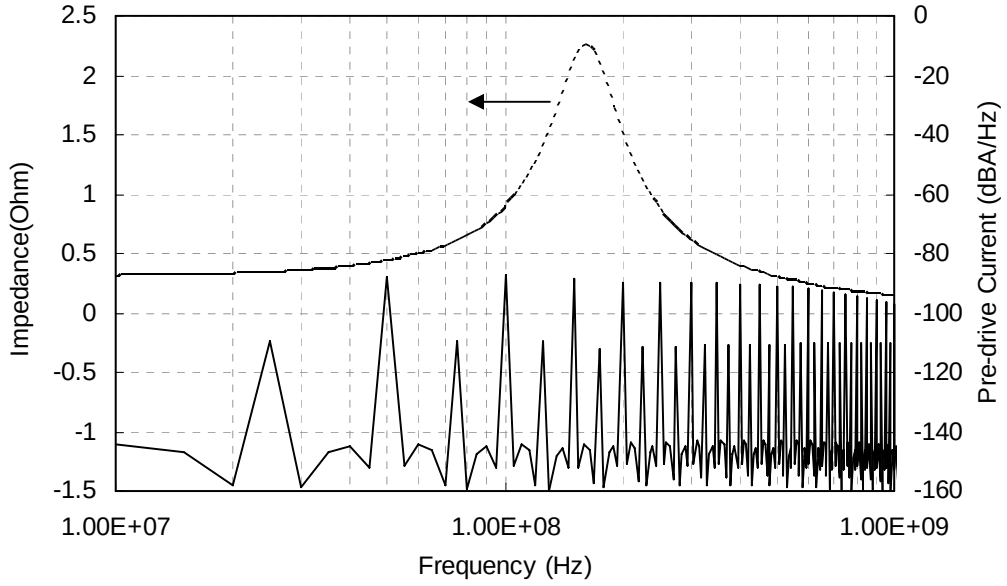

Figure 14. Switching current spectrum relative to PDN impedance

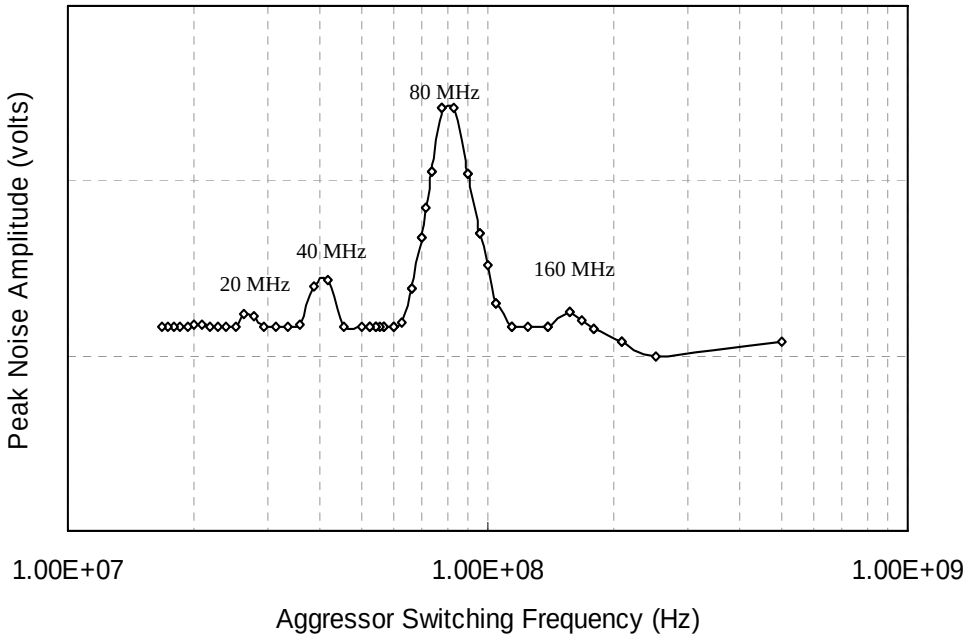

Figure 15. Power supply noise on V_{CCPD} versus the aggressor switching frequencies

3. Pre-Drive Timing Variations

To validate the impacts of the power supply noise, timing measurement and analysis techniques had to be developed to capture the pre-drive on-chip driver timing variations in both time and frequency domains. Without loss of generality, we define a signal ideal timing as the time its voltage reaching 50% of the power supply level at quiet condition with no other aggressors toggling. Timing pull-in and push-out is signal delay variations on the signal edges with the presence of power supply noise.

Buffer delay variations at pre-drive stages can be observed by disabling the output drivers on the aggressor pins. In this way, no aggressor signals will pass through the output drivers. Therefore, no power supply noise will be present on V_{CCIO}. Also, there will be no inductive crosstalk affecting the signal timing at the package and PCB pin field. Meanwhile, pre-drive on-chip buffers of aggressor I/Os are still toggling. Power supply noise on V_{CCPD} will impact the signal timing at the pre-drive stages.

In this paper, we developed measurement techniques to research maximum timing variations for both synchronous and asynchronous cases. The synchronous case analyzes the impact of aggressors while we control and monitor their phase relationship. Asynchronous measurements provide results at different aggressor frequencies and simulate the case when one I/O interface affects another inside one chip.

3.1. Asynchronous Aggressors and Victim

Power supply noise varies with different aggressor frequencies. Following the power supply noise, buffer delay variation is also a function of the aggressor frequencies. In the experiment, we vary the aggressor frequency with the victim frequency fixed and we measured the victim timing variations. Measured timing variations versus aggressor frequencies are plotted in Figure 16. Maximum power supply noise happens when aggressors switch at half of the PDN resonance frequency, Figure 15. The timing variations, corresponding to the power supply noise, confirm the same frequency dependencies on the power supply resonance.

When we have two I/O groups operating at different frequencies while sharing the same power supply, one I/O group will affect the timing of other I/O groups. In this case, timing variations for each of I/O groups will depend on their frequency relationship. These frequency relationships were introduced in [4, 5] for the measurements of a periodic signal timing variations with one sine wave component in jitter spectrum only; numerous MIN/MAX were noted [4, 5] in jitter behavior even in such simple jitter spectrum case. The jitter spectrum of a victim pin due to the switching components inside the integrated circuit has much more complex character compared to one sine wave harmonic. However, the frequency relationship for main MINs and MAXs are the same. We studied timing variations of a victim due to switching device core components and I/Os in paper [6]. In [6] it was shown that, in spite of different physical phenomena, the main frequencies relationships for MIN and MAX are the same as obtained in [4, 5]. In particular, the maximum jitter observed when aggressor frequency chosen is close to the half of the PDN resonance frequency F_{res}^{PDN} :

$$F_{aggressor} = \frac{F_{res}^{PDN}}{2}$$

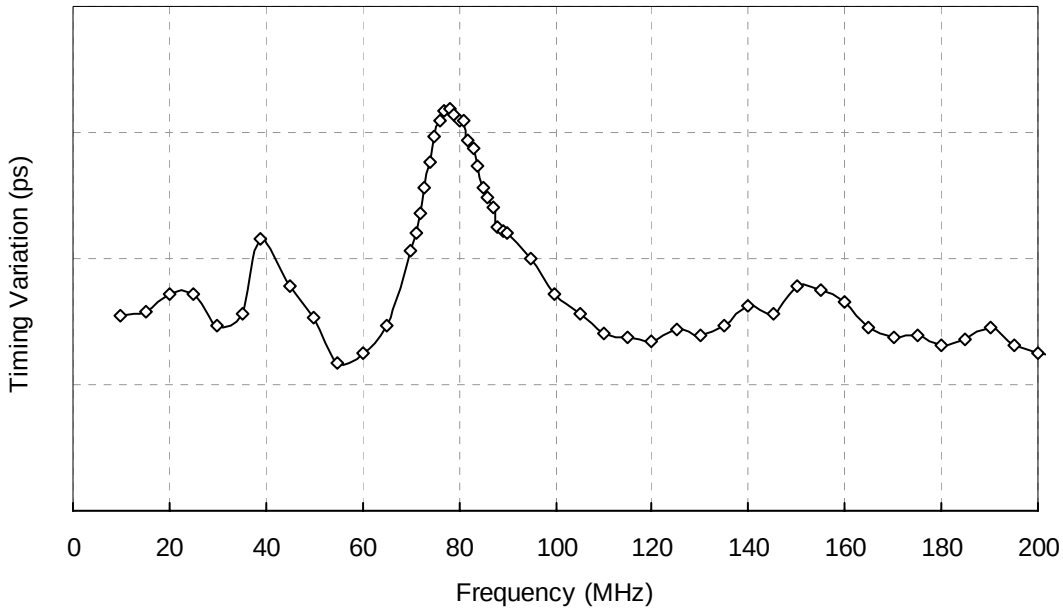

Figure 16. Timing variations at pre-drive stages versus aggressor switching frequencies

3.2. Synchronous Aggressors and Victim

Buffer delay variations are proportional to power supply changes. Over time, signal timing should follow the power supply variations. As shown in Figure 17, through phase sweeping, victim signal variations can be observed. Victim and aggressor signals are synchronized and both running at very low frequencies. The first delay increase (timing push-out) is caused by the sharp voltage drop, Delta-I noise, when all the on-chip drivers are simultaneously switching. As victim edge sweeps into the power supply resonance region, the victim signal phase is modulated by the power supply variations. Timing variations oscillate with a frequency equal to pre-drive PDN resonance frequency (about 160 MHz). For power supply resonance, STA can be applied for the dynamic timing variations.

$$\Delta t_{pre-drive-resonance,t} = -k\ (V) \times \Delta V_{pre-drive}(t)$$

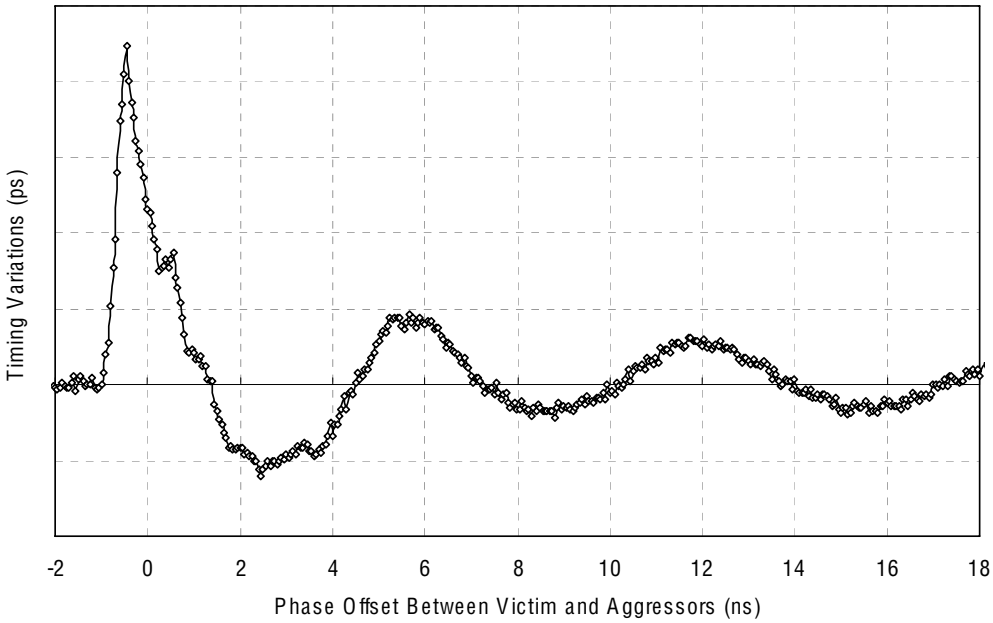

Figure 17. Timing variations at different phase offsets. 87 I/Os are switching. Delay variations is isolated at the pre-driver stages by disable the off-chip drivers of the aggressor I/Os.

Timing variation increase rapidly at the time location where the victim signal is affected by the Delta-I noise. The STA approach does not apply as the Delta-I pulse is comparable to the signal transition time. However, buffer delay variations due to Delta-I noise can be measured with a different number of switching aggressors. As shown in Figure 18, buffer delay variations scale almost linearly to the number of aggressors. Buffer delay variations at the time location where Delta-I noise is dominant can be calculated as:

$$\Delta t_{pre-drive-Delta-I,t=T1} = k \times N$$

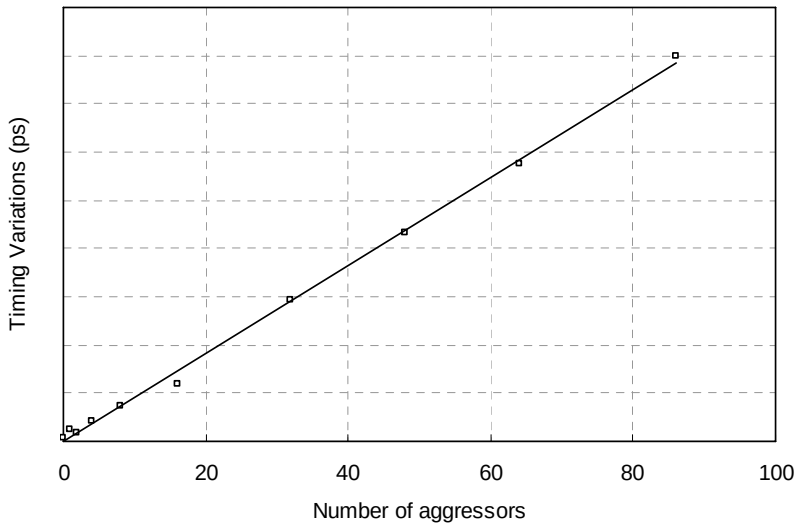

Figure 18. Delay variation versus the number of aggressors. Timing variations were measured at the timing location where Delta-I noise occurs.

V. Accumulated Timing Variations

Timing variations are accumulated through the I/O buffer and package/PCB pin field where each noise source has its impact on the signal timing. Three of the major noise sources are:

- Inductive crosstalk at the package and PCB pin-field region
- V_{CCIO} power supply resonances
- V_{CCPD} pre-driver power supply noise including Delta-I noise and power supply resonance

Timing variation contribution for each of the noise sources is a function of time and phase relation to the victim pin. Delta-I noise and crosstalk are evaluated on a worst-case basis at fixed time locations. Timing variations due to power supply resonance on V_{CCIO} and V_{CCPD} have long lasting effects. Accumulated timing variations can be expressed as:

$$\Delta t_{total,t} = \Delta t_{crosstalk,t=T1} + \Delta t_{off-chip,t} + \Delta t_{pre-drive-resonance,t} + \Delta t_{pre-drive-delta-I,t=T1}$$

To validate the timing analysis process, Figure 19 shows the accumulated timing variations measured at the victim signal rising edge in correlation to the V_{CCPD} noise, V_{CCIO} noise and inductive crosstalks in reference to the aggressors rising edge. The first peak on the accumulated timing variations is mainly due to V_{CCPD} Delta-I noise and by crosstalk noise. After the initial peak, the rest of the waveform shows the modulation effects driven from both V_{CCPD} and V_{CCIO} power supply resonances.

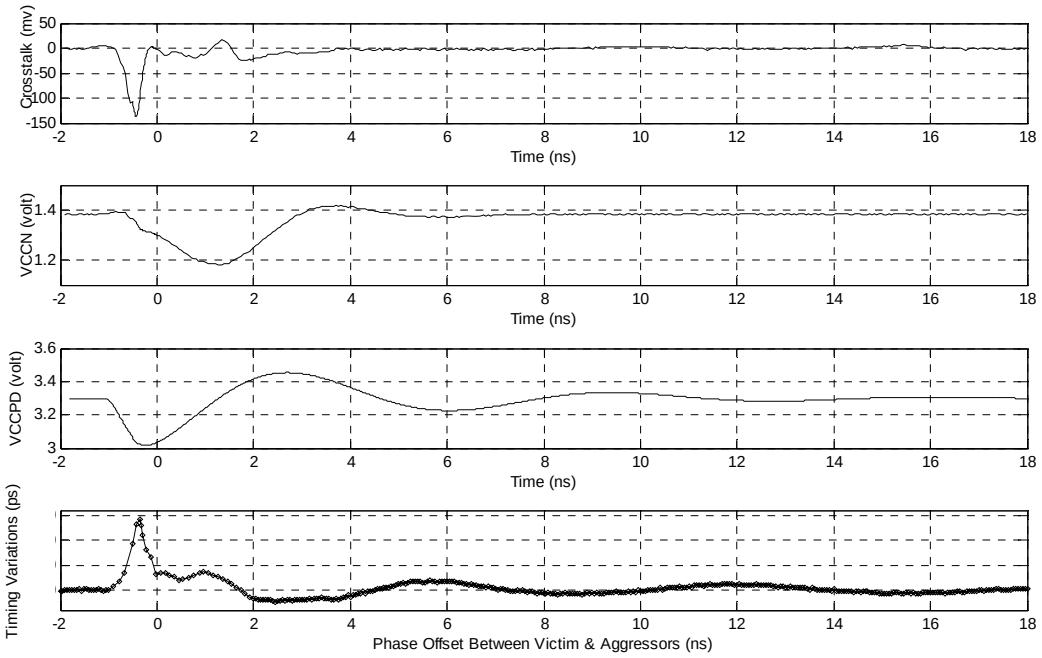

Figure 19. Accumulated timing variations correlated in time to the Crosstalk, V_{CCPD} noise, V_{CCIO} noise

VI. Conclusions

In summary, the paper describes the analysis and measurement techniques that are used for evaluating amplitude noise and timing variations due to SSN. Among the key points addressed in this work:

- Signal timing variations hold a linear relationship against crosstalk noise. However, crosstalk noise increases non-linearly with the number of aggressors and the saturation effect is due to the spatial distribution of the aggressor I/Os in a large group.
- Timing variations due to power supply resonances can be evaluated with a static timing analysis approach. Signal timing varies dynamically with the power-supply voltage variations.
- For the synchronous aggressor and victim, timing variations of a victim depend on their phase relationship.
- In the asynchronous case, the maximum timing variation is observed when the aggressor frequency chosen is close to half of the PDN resonance frequency, $F_{aggressor} = F_{res}^{PDN} / 2$.
- Scalar timing analysis model is developed for timing variation estimation, including STA with power supply resonances and worst-case timing variations from Delta-I noise and crosstalk at fixed time locations.

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