Thermal Interface Material (TIM) Design Guidance For Flip Chip BGA Package Thermal Performance

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Abstract

Thermal interface materials (TIM) are studied to identify its design criterion in a flip chip PBGA applications at different power dissipation levels. As there are continuous interests in proper selection of TIM material and design, the thermal performance analysis can offer design guidance for packaging engineers. Computational techniques are used with both computational fluid dynamics software and finite element analysis (FEA). The purpose of the paper is to identify key design parameters for TIM in different applications where power level ranges can be confined. Results and design recommendations were given and discussed.

Keyword: thermal interface material, flip chip, thermal resistance, design guidance, computational fluid dynamic.

Introduction

With increasing level of silicon integration, continuing shrinking of feature size and increasing clock speed, there is a continuous trend in increasing power and heat flux on the silicon. As flip chip package has been considered as the preferred choice for interconnection technology to offer the higher power delivery capability, the increasing in power dissipation rate put significant challenges on packaging technology and must be carefully managed.

For flip chip package, with the chip connected with solder ball interconnection to the substrate on the circuit side, the other side of the chip is flipped and can be used as a thermal conduction path for cooling. As shown in Figure 1, a heat transfer path can be established by selecting the proper thermal interface material (TIM) between silicon die and the conductive heat spreader.

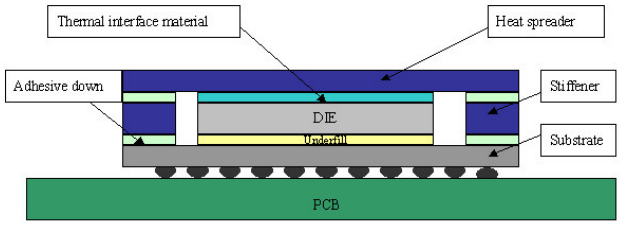


Figure 1. FC-PBGA package without a heat sink.

As the chip power becomes higher, the role of TIM for flip chip package becomes more important. Not only does it affect thermal performance, it also affects mechanical reliability during the stress and manufacturing processes. Kohli et al. (1), Tonapi et al. (2) and Mok (3) have identified suitable TIM material attributes that include low thermal resistance, low stress, good adhesion and good thermal performance after standard stressing testing, in addition to good compatibility with current adhesive dispensing equipment processes.

Rauch (4) studied phase-change type of thermal interface materials for low-power applications. Chiu et al. (5) studied how to control TIM's bond line thickness. The contact surfaces are never perfectly flat due to the manufacturing process-induced warpage on both heat sinks and electronic packages. To accurately address this issue, a simplified numeric approach is proposed for the non-flat surfaces. Dean et al (6) addressed the actual testing parameters, such as surface flatness, surface roughness, and test pressure by an enhanced standardized test method to capture deviations from idealized conditions and show experimental results

which illustrate how material performance changes in response to surface flatness. In order to identify higher thermal conductivity TIM, Marotta et al. (7) conducted an experimental investigation for flexible graphite on thermal joint conductance of an important interstitial material employed in microelectronic components.

For the purpose of this study, we are concerned with the internal thermal resistances of thermal interface material in a challenging thermal environment. With the trends of increasing chip power and decreasing thermal budget, there is great need to manage the packaging internal thermal resistance. This is the motivation of this study. The objective is then to identify the thermal design guidance for thermal interface material that meets the thermal requirement for flip chip package in different thermal and power conditions. In order to accurately study this problem, both FEA and CFD analyses were considered. The purpose of the use of FEA is to utilize its convenience and fastness in generating parametric design analysis. However, the use of computational fluid dynamics technique is to provide the proper boundary conditions and offer the model validation for FEA results. The computational analysis results by CFD were validated by experimental data comparison.

Problem Statement

The problem of interest concerns a flip chip package with thermal enhanced heat spreader as shown in Figure 2. Consider a silicon chip of 17 x 17 x 0.7 mm in size, which is packaged in a flip chip plastic ball grid array package of 33 x 33 x 1 mm in size. The package is then surface mounted on a printed circuit board of 76.2 x 76.2 x 1.6 mm. The printed circuit card, substrate and other components and their dimensions and thermal conductivities are listed in Table 1. A straight fin heat sink is added on the module surface with airflow on both sides.

In this analysis, chip power is classified into three categories as shown in Table 2 with their respective thermal conditions.

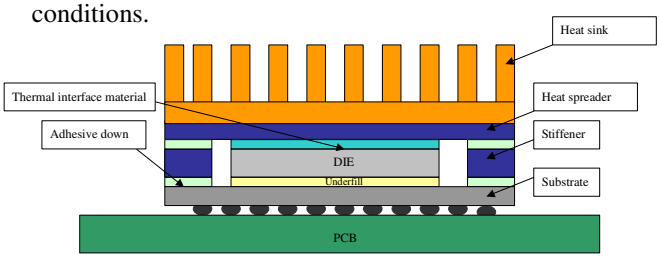


Figure 2. FC-PBGA package with a heat sink

	Size (mm x mm)	Thickness (mm)	Conductivity (W/m*K)
Die size	20*20	0.5	110
Substrate	33*33	1.	17.5
Underfill		0.10	4.3
TIM		0.17	2
Stiffener Adhesive Up		0.07	0.5
Stiffener Adhesive Down		0.1	0.5
Stiffener	3mm wide	0.6	389
Heat Spreader		0.5	389
Solder Ball		0.5	10.05
PCB	76.2*76.2	1.6	13

Table 1. FC-PBGA package dimensions and thermal conductivities.

Case	Model domain size	Fluid	Die power
Low power	600mm * 200mm* 68mm	Air, Ambient temperature50°C	below 10W
Medium power	600mm * 200mm* 68mm	Air, Ambient temperature50°C	10W~30W
High power	600mm * 200mm* 68mm	Air, Ambient temperature50°C	above 30W

Table 2. Thermal modeling conditions.

Mathematical Formulation

Assuming incompressible flow and steady state, the governing conservation equations can be written as follows.

The governing equation for mass conservation is

$$\frac{\partial u_i}{\partial x_i} = 0 \tag{1}$$

The governing equations for momentum is

$$\rho u_j \frac{\partial u_i}{\partial x_i} = -\frac{\partial p}{\partial x_i} + \frac{\partial}{\partial x_i}\left(\mu \frac{\partial u_i}{\partial x_j}\right) \tag{2}$$

And the conservation of energy equation is written as

$$\rho u_j \frac{\partial h}{\partial x_i} = \frac{\partial}{\partial x_i}\left(\frac{k}{C_p}\frac{\partial h}{\partial x_j}\right) \tag{3}$$

Equations together with appropriate boundary conditions constitute the mathematical problem, which is solved by an appropriate numerical solution scheme.

ICEPAK (8), a computational fluid dynamics code, is used to solve the fluid flow and heat transfer problems. The convergence for the flow field solution is obtained as the normalized residuals meet the order of 10E-3, while the convergence of temperature field is satisfied when the normalized residual of temperature is less than 10E-6.

CFD modeling verification

The modeling accuracy is examined with an experimental study of a 13mm x 13mm flip chip ceramic ball grid array package without the heat spreader mounted on a PCB. The testing was performed under a wind tunnel condition with various air speeds from 0.5 m/s to 3 m/s and the air flowed through both sides of the PCB. The maximum variation of R_{JA}, the chip junction to ambient resistance, between the experimental and numerical results is 5.3%, see Figure 3. It has confirmed that the numerical model is accurate.

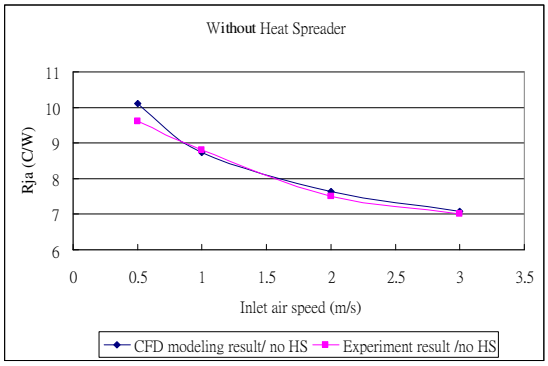


Figure 3. CFD vs. Experimental results under various inlet air speed

CFD and FEM comparison

Finite element analysis (ANSYS (9)) is efficient in conducting thermal parametric analysis. It is conduction based and requires the assignment of empirical external convection boundary conditions. On the other hand, CFD analysis is convection based and does not need assignment of empirical convection boundary conditions. However, it is not as fast as FEM. We have conducted CFD analysis to validate the boundary conditions and prediction accuracy of FEM.

The results of CFD and FEM thermal resistance at different air speed are shown in Figure 4. The overall results shows that R_{JA} values from the CFD results are lower than those from the FEM results. However, the normalized R_{JA} values from the CFD and FEM results are well correlated and their variation is less than 10%.

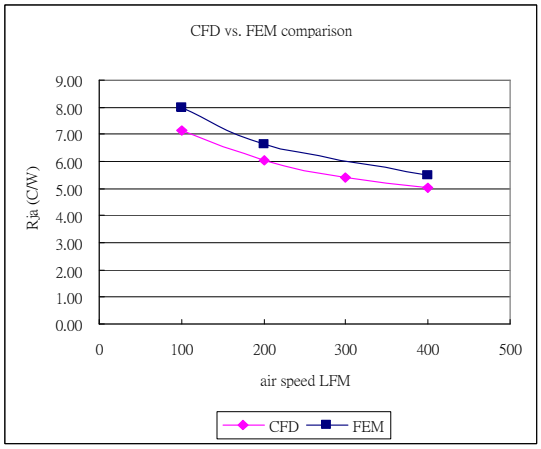


Figure 4. CFD vs. FEM results under various inlet air speed

Results and Discussion

After the model accuracy is validated with both experimental data and companion finite element model (FEM), the modeling using computational fluid dynamics is extended to study the design parameters for thermal interface materials. In this paper, three design parameters are considered to be critical which are the thermal conductivity, the bond line thickness and the % coverage of the thermal interface material. As shown in Table 2, three different chip power ranges: low power, medium power, and high power, are to be evaluated and discussed for thermal design guideline.

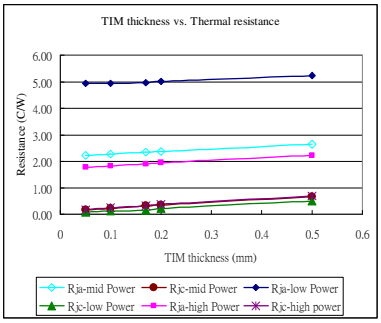
TIM thickness

Figure 5 is showed the simulation results of R_{JA} , junction to ambient resistance, and R_{JC} , junction to case resistance for low power applications, i.e., within 10 watts without the heat sink. TIM thickness does not have significant effect on R_{JA} under the range studied from 50 to 500 microns. Therefore, under low power applications with TIM thickness range from 50 to 500 microns, it is not expected to see significant changes in thermal performance. When the chip power increases up to 25 watts, or in medium power applications, the heat sink is added and TIM thickness becomes more sensitive. In order to study this problem, an external heat sink has to be added. Based on the simulation results, it is shown TIM thickness must be controlled within 200 microns to keep proper junction temperature. For high power case, the TIM thickness must

be controlled within 150 microns to maintain proper junction temperature.

Figure 5. Thermal performance result under various TIM thicknesses

THK mm	low power Rja	Rjc
0.05	4.95	0.06
0.1	4.93	0.11
0.17	4.96	0.15
0.2	5.02	0.21
0.5	5.23	0.48
THK mm	Mid power Rja	Rjc
0.05	2.22	0.16
0.1	2.28	0.23
0.17	2.35	0.31
0.2	2.38	0.35
0.5	2.64	0.67
THK mm	High power Rja	Rjc
0.05	1.78	0.17
0.1	1.83	0.24
0.17	1.91	0.32
0.2	1.94	0.36
0.5	2.23	0.69

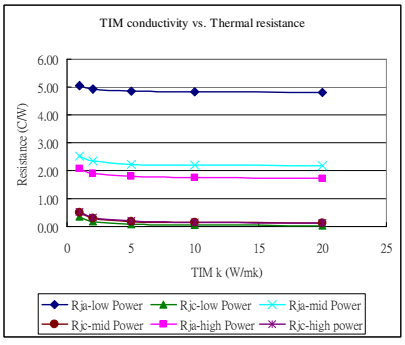


TIM thermal conductivity

As shown in Figure 6, with low power applications TIM thermal conductivity (K) can be lower without affecting thermal performance. With medium power applications where an external heat sink is added, TIM thermal conductivity must be selected in the range of 1 w/mk to 5 w/mk. For example, at power level of 25 watts, the chip junction temperature T_J at TIM K of 1 W/mK can be 4.25 °C higher than T_J at TIM K of 2 W/mK. For high power applications, TIM K should be higher than 2 W/mK to avoid thermal penalty. From the results, it is also confirmed that high conductive TIM with 5 or 20 W/mK will not see significant advantages until power is approaching 100 W.

Figure 6. Thermal performance result under various TIM conductivity

TIM K w/m*k	low power Rja	Rjc
1	5.05	0.35
2	4.93	0.19
5	4.86	0.08
10	4.82	0.05
20	4.79	0.03
TIM K w/m*k	Mid power Rja	Rjc
1	2.52	0.50
2	2.35	0.31
5	2.24	0.19
10	2.20	0.14
20	2.18	0.12
TIM K w/m*k	High power Rja	Rjc
1	2.08	0.52
2	1.91	0.33
5	1.79	0.20
10	1.75	0.15
20	1.73	0.13



TIM coverage

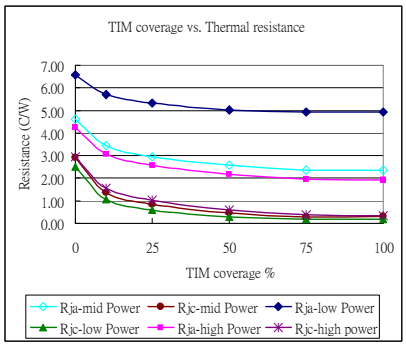
TIM coverage (percentages) was studied from 0% to 100%. TIM 0% coverage means TIM is completed delaminated from the die. At low power applications (≤10 W), 25% coverage is the lowest requirements to maintain thermal performance, as shown in Figure 7. For example, by degrading TIM coverage from 100 % to 25 %, the chip junction temperature T_J will only increase 3 °C for 10 watts chip power. However a further decrease of TIM coverage from 25% to 10 % can cause 4 °C T_J increase for a 10 watts chip.

For medium power application such as 25 watts where external heat sinks is required, the minimal requirements of 50 % TIM coverage is strongly recommended. As noted, TIM coverage changing from 100 % to 50 % will degrade R_{JA} by 0.21 C/W. At 25 watts, it means 5 °C increase in T_J.

For high power applications such as 40 watts with external heat sinks, the minimal requirements of 75 % TIM coverage is strongly recommended. For example, the change of TIM coverage from 100 % to 50 % will degrade R_{JA} by 0.26 °C/W. consequently resulting in 10.4 °C increase in T_J at 40 watts power.

Figure 7. Thermal performance results under various TIM coverage percentages

Coverage %	low power Rja	Rjc
0	6.57	2.51
10	5.69	1.05
25	5.32	0.58
50	5.03	0.28
75	4.93	0.19
100	4.93	0.19
Coverage %	Mid power Rja	Rjc
0	4.62	2.90
10	3.43	1.35
25	2.94	0.83
50	2.56	0.46
75	2.35	0.27
100	2.35	0.32
Coverage %	High power Rja	Rjc
0	4.23	2.95
10	3.07	1.55
25	2.58	1.01
50	2.17	0.59
75	1.95	0.37
100	1.91	0.35



With the above studies, we have obtained the following design guidance:

Low power applications (< 10 watts)

TIM thickness: ≤ 500 microns

TIM Coverage: ≥ 25 % of die area

TIM thermal conductivity: ≥ 1 W/mK after degradation

Medium power applications (10 watt – 30 watts)

TIM thickness: ≤ 200 microns

TIM Coverage: ≥ 50 % of die area

TIM thermal conductivity: ≥ 2 W/mK after degradation

High power applications (> 30 watts)

TIM thickness: ≤ 150 microns

TIM Coverage: ≥ 75 % of die area

TIM thermal conductivity: ≥ 5 W/mK after degradation

Concluding Remarks

TIM design guidelines for flip chip BGA packages have been determined for different power ranges. Following are the summaries:

For power range below 10watts, selection of TIM is less stringent, because thermal performance of packages is not very sensitive to the changes to thermal conductivity, coverage and thickness of TIM.

For power ranges between 10 and 30 watts, where a heat sink is used, TIM must be carefully selected. It is recommended that thermal conductivity be greater than 2 w/mk, the thickness be less than 100 microns and the coverage be greater than 90%, to keep junction temperature to be within manageable limits.

For chip power greater than 30 watts and less than 100 watts, TIM selection becomes critical. They must have very high thermal conductivity (≥ 5 W/mK), a thin bond line thickness and nearly 100% coverage. A slight change in these parameters can affect thermal performance significantly.

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