Translating Yield Learning Into Manufacturable Designs

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Introduction:

Improving semiconductor yield is a multi-dimensional process that must include design, fabrication and test aspects. An integrated approach to yield management that incorporates all these aspects enables companies to rapidly reach higher levels of profitability[1]. Incorporating design-for-manufacturability (DFM) concepts is not always an intuitive process. It needs to include prior and ongoing learning and experience on what worked and what did not.

As feature sizes shrink beyond 130nm, it is possible to identify another class of failures that is more systematic and related not to manufacturing defects but to DFM marginalities related to layout. It will be shown here that DFM can also help reduce design sensitivity to process variations[2]. Examples of these failure modes and the lessons learnt are listed here:

Relaxed Design Rules for Repeated Patterns:

Advanced technology design rules are becoming more complex, especially with the introduction of context dependant design rules i.e. design rules which change depending on the surrounding patterns. Consequently, simple rules in the past like: 'allowed minimum space' on a layer are no longer hard numbers but depends on what patterns are on the layer below or surrounding the minimum space in question. Furthermore, in many cases design rules no longer indicate what is allowed or not allowed but are becoming recommendations and best practices for manufacturability. With these trends in design rules, product layout is not simply an implementation of schematics by an isolated group of layout engineers following simple yes/no rules but rather a cross functional exercise in optimizing performance, area, and yield.

In this new framework, design layout offers many opportunities where good engineering judgment can lead to net gain in cost and performance. Pattern integrity is now a complex function of drawn shape, mask quality, RET (reticle enhancement techniques), proximity effects, scanner lens uniformity, within reticle placement, and process conditions, layout patterns which are repeated often require special DFM cross functional attention to area yield trade offs. For example, use of minimum design rule in repeated patterns may lead to smaller die area but may not be cost effective due to cumulative increased probability of failure.

To illustrate, minimum poly finger spacing to wide poly is difficult to control and repeated use of this minimum spacing leads to a higher failure rate (see Fig.1.)

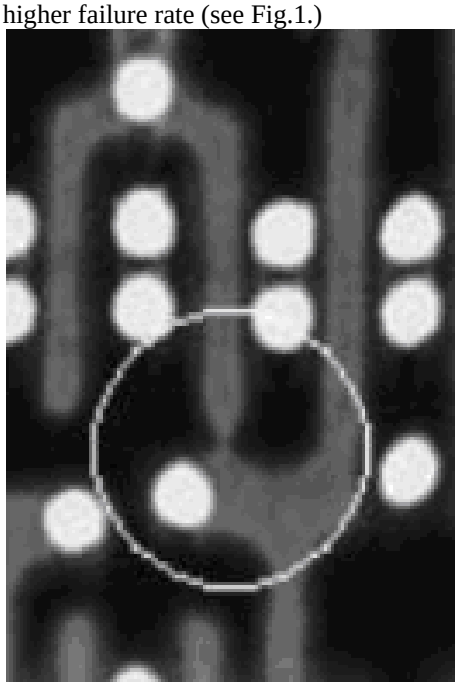

Fig. 1 Example showing poly bridging between a narrow vertical poly structure to a wide horizontal poly with minimum spacing.

Relaxing Design Rules to Reduce Yield Loss:

(a) I/O active with minimum area overlap:
Gates with tight design rules can fall prey to fabrication equipment drifts. An example, of such failures is shown here as I/O leakage failure. Gates with tighter design rules of the thick gate oxide (TGO mask) (Fig. 2) was more susceptible to failures compared to similar gates with a good design margin (Fig. 3). This vulnerability has been shown to be related to the minimum I/O active area to core active area overlap design rule. The physical manifestation of the failure was established to be due to gate oxide thinning at the STI (Shallow trench isolation) edge leading to leakage.

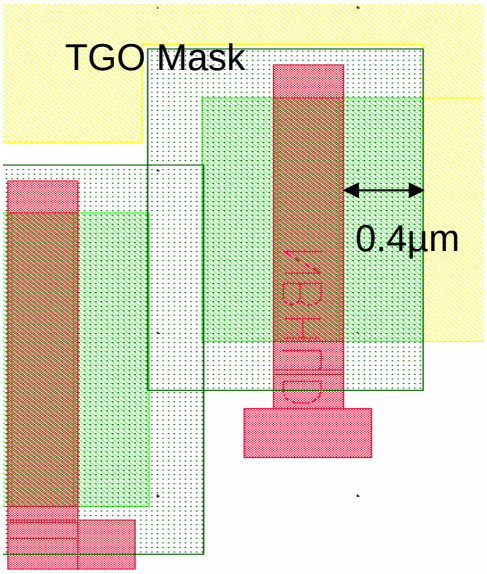

Fig. 2 Poly Gate (Pink) is vulnerable to process drifts. The thick gate oxide mask is missing at the right edge making it vulnerable to process drifts.

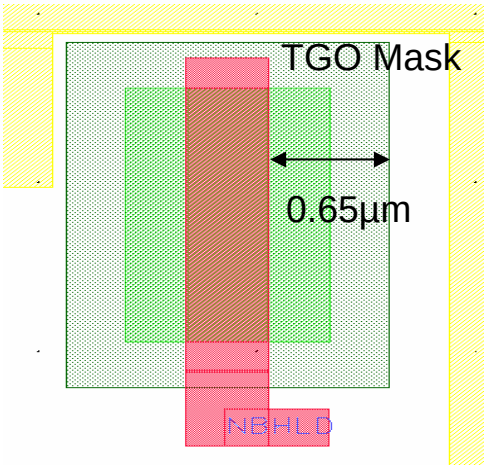

Fig. 3 Poly Gate (Pink) has thick gate all around. This gate never fails because there is enough process margin. The TGO mask wraps around protecting the STI.

A cross sectional transmission electron microscopy (TEM) analysis confirms the damage at the STI corner (see Fig. 4). The cause of this marginality was shown to be due to resist process marginality resulting in slight photo resist lifting which only affected the gates drawn with the minimum design feature. Process drifts aggravate this problem intermittently from lot to lot. Confirmation of this mechanism was obtained when tight diffusion CD controls were implemented in the manufacturing fab that made the problem go away.

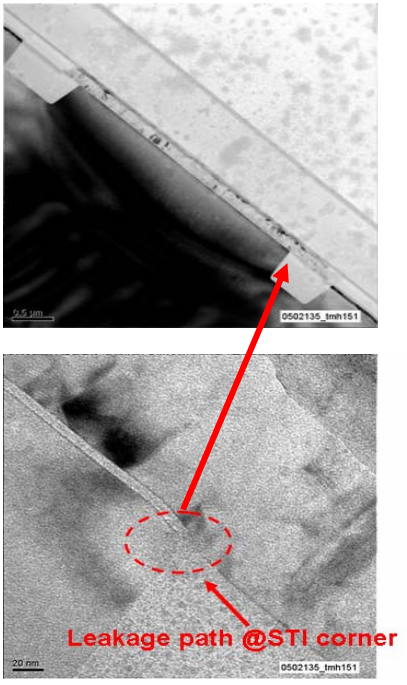

Fig. 4 Cross sectional TEM of the failing gate confirms the leakage path at the STI corner.

(b) Micro Arcing and Plasma Damage:
It is a well known fact that plasma charging effects[3,4] during manufacturing can cause device failures. If the discharge path for the charge build up is not adequate, oxide breakdown can occur. An example is shown in figs. 5 and 6 below.

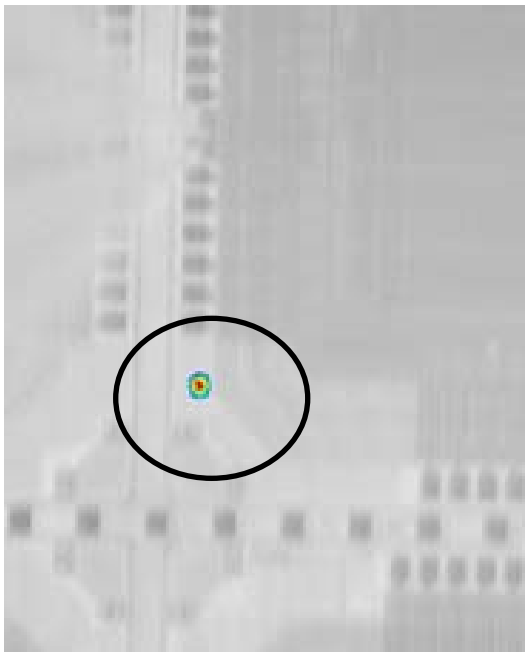

Fig. 5 An Infra red hot spot indicating a gate capacitor failure

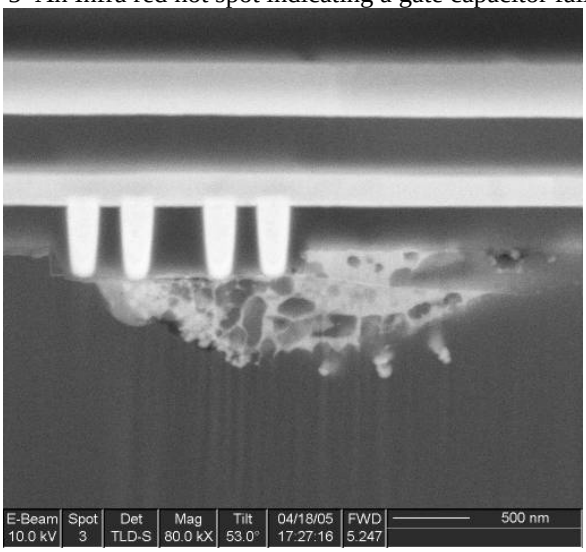

Fig. 6 Cross section at the hot spot indicates the capacitor failure was due to electrical over stress type of failure rooted in the fabrication process

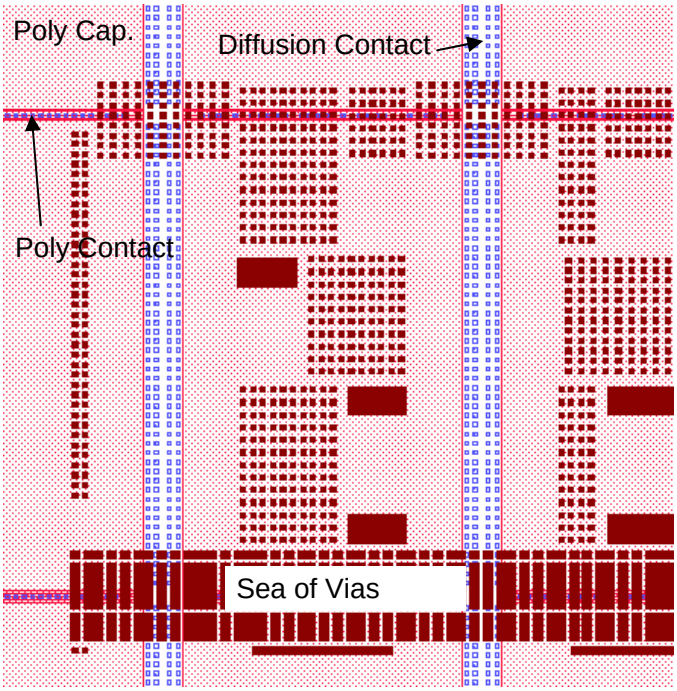

Fig. 7 The layout indicates the failure site to be linked to a sea of vias clustered together Charge build up at these vias was ascribed to an etch-tool

The gate capacitor breakdown always showed a specific layout signature. Problem was intermittent, with some lots not failing at all. A certain manufacturing tool was identified as the cause of this problem. Layout study indicates that the capacitor failures stem from an arcing mechanism during backend via etch process. The damage always coincided with the layout sensitivity due to a cluster of vias accumulating charge that got dissipated through the diffusion and poly contacts (Fig. 7).

The manufacturing tool responsible for this failure was subsequently removed by the fab. However, to resolve the wafer arcing issue completely, plasma instability along with the structure/layout sensitivity has to be understood.

Special Considerations for Analog circuit layout:

Transistor matching is critical for analog circuits. Usually, care is taken to layout the transistor in a common centroid form involving front end layers. However, interconnect also plays an important role in matching V_t and Id_{sat} of transistors. Due to plasma charging and subsequent discharge while processing BEOL (back end of line) layers, the antenna ratio seen by the gates of matched transistors affects the V_t and Id_{sat} of these devices. Standard topological design rules give a maximum antenna ratio to limit V_t shift due to gate discharge. However, if the antenna ratio of the gate interconnect of two transistors is not matched, V_t and Id_{sat} of these two transistors will be shifted by different degrees resulting in systematic mismatch between the transistors. The effect of plasma damage is demonstrated on test structures on 90nm technology by measuring the Id_{sat} of the 3.3V NMOS and PMOS on transistors. Specifically we have two NMOS transistors which are laid out identically except for the addition of a diode to the gate of one of the transistors which reduces its antenna ratio. Figure 8 (a) shows the Id_{sat} data for these two NMOS transistors (3.3V_NMOS_No is without extra diode to gate and 3.3VNMOS_Yes is with extra diode to gate) indicating a systematic shift.

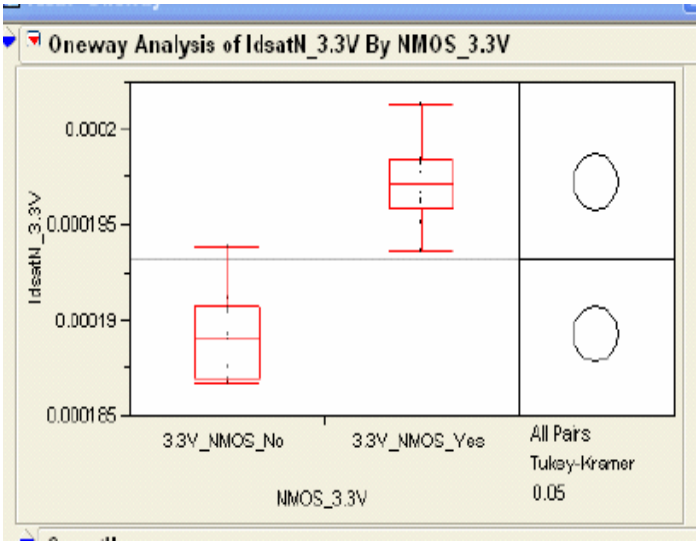

Fig. 8a 3.3VNMOS_Yes has an extra diode to gate and 3.3VNMOS_No is without the diode resulting in larger antenna ratio.

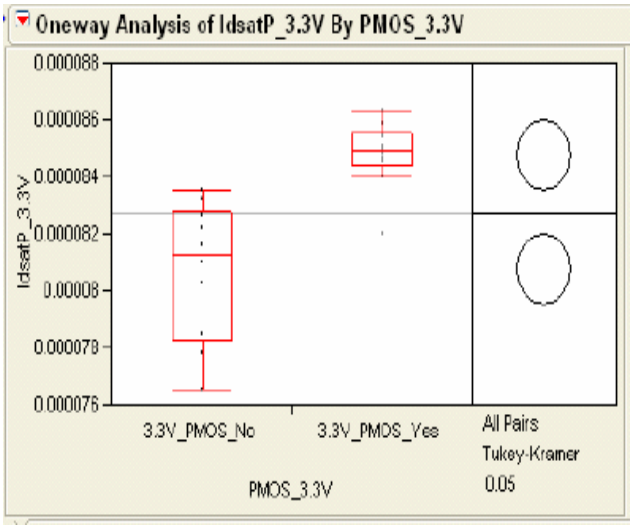

Fig. 8b 3.3VPMOS_No is without extra diode to gate and 3.3VPMOS_Yes has an extra diode to the gate resulting in larger antenna ratio.

Similarly, we have two PMOS transistors which are laid out identically except for the addition of a diode to the gate of one of the transistors which reduces its antenna ratio. Figure 8 (b) shows the Id_{sat} data for these two PMOS transistors (3.3V_PMOS_No is without extra diode to gate and 3.3V_PMOS_Yes is with extra diode to gate) indicating a systematic shift. The above data clearly shows the importance of matching antenna ratios for matched transistors to eliminate systematic device characteristics shifts.

Redundant Via Insertion: Vias are very important components of via-interconnect system in VLSI circuits. Vias may fail partially or completely in a manufacturing process. Misalignments and thermal stress induced voiding are some common causes of failure. Yield loss due to a single via can be avoided by redundant via insertion adjacent to each single via. An additional via also decreases the total via resistance and alleviates the delay penalty that can result from partial via failures (Fig.9). Layout changes on existing designs (Fig. 10a) to accommodate doubling of vias are shown in (Fig. 10b). Advanced via doubling tools were used in an intelligent manner to double the vulnerable vias without a design change.

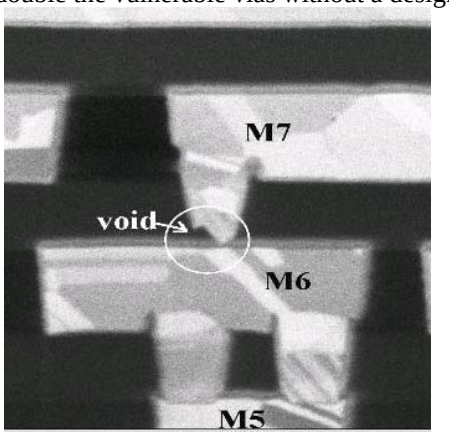

Fig. 9 Single via failure can cause a product to fail functionally.

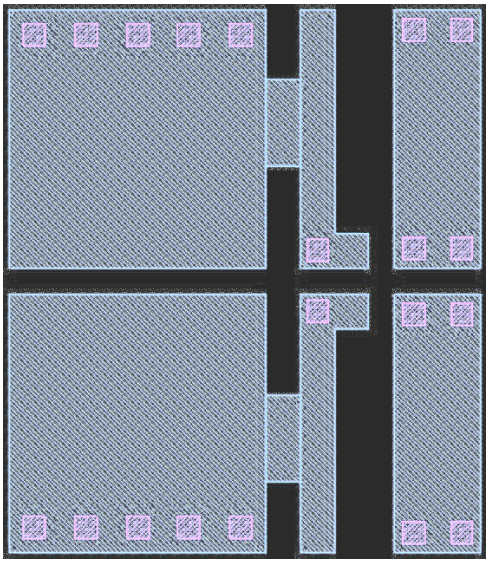

Fig. 10a An example of a single vulnerable via in a circuit leading to high resistance and eventual circuit failure (pink-via;Blue-metal).

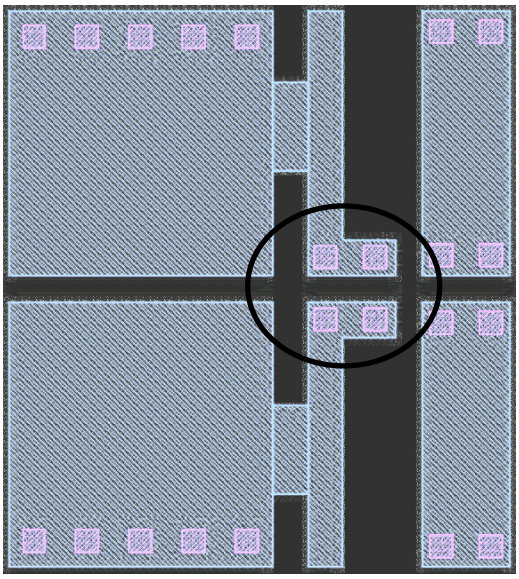

Fig. 10b An example of double via insertion (b) retrofit to meet 90nm DFM rules (pink-via;Blue-metal).

Metal Slots: Wide metal busses without any stress relief slots generate high levels of stress leading to micro cracks in the Intra level Dielectric. These failures get accentuated during reliability testing resulting in qualification failure (Fig.10). The recent study resulted in implementation of metal slots on all power busses >10um to minimize the thermal stress (Fig.11).

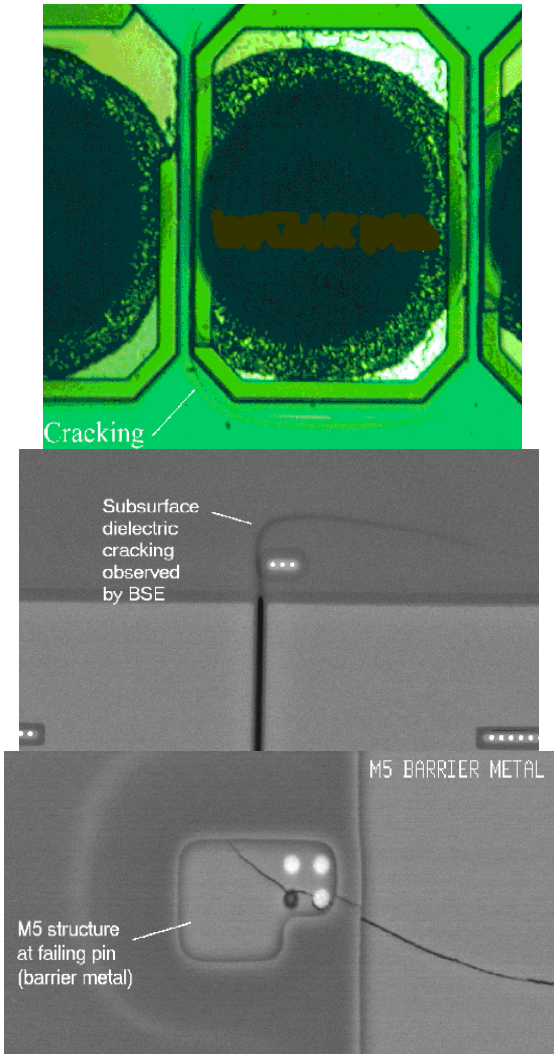

Fig. 11 Images A (top), B and C above show cracks developed in the Intra level metal dielectric during reliability testing. The failures were only seen around the metal busses (>10um wide) with no slots.

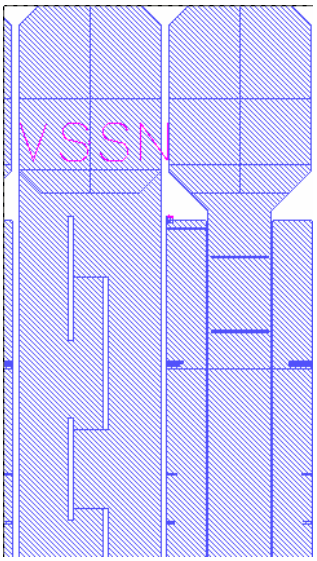

Fig.12 Slotting the wide metal busses prevented stress induced failures.

Conclusion:

Even though manufacturing design rules exist for a production process technology, good manufacturing practice requires that these be constantly reviewed in the light of ongoing learning and experience acquired through failure analysis and yield enhancement efforts. Since these rules are typically too difficult and 'low level' for the designer to get involved in, they need to be implemented in CAD tools.

Traditionally, it is the foundries that have been primarily responsible for managing yield. As technologies advance to finer geometries, yield tends to become product specific. A partnership between back end design, failure analysis, EDA[5] and fabrication engineers will become increasingly important to achieve yield objectives.

Acknowledgement:

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