

# Design Techniques for Radiation-Hardened FPGAs

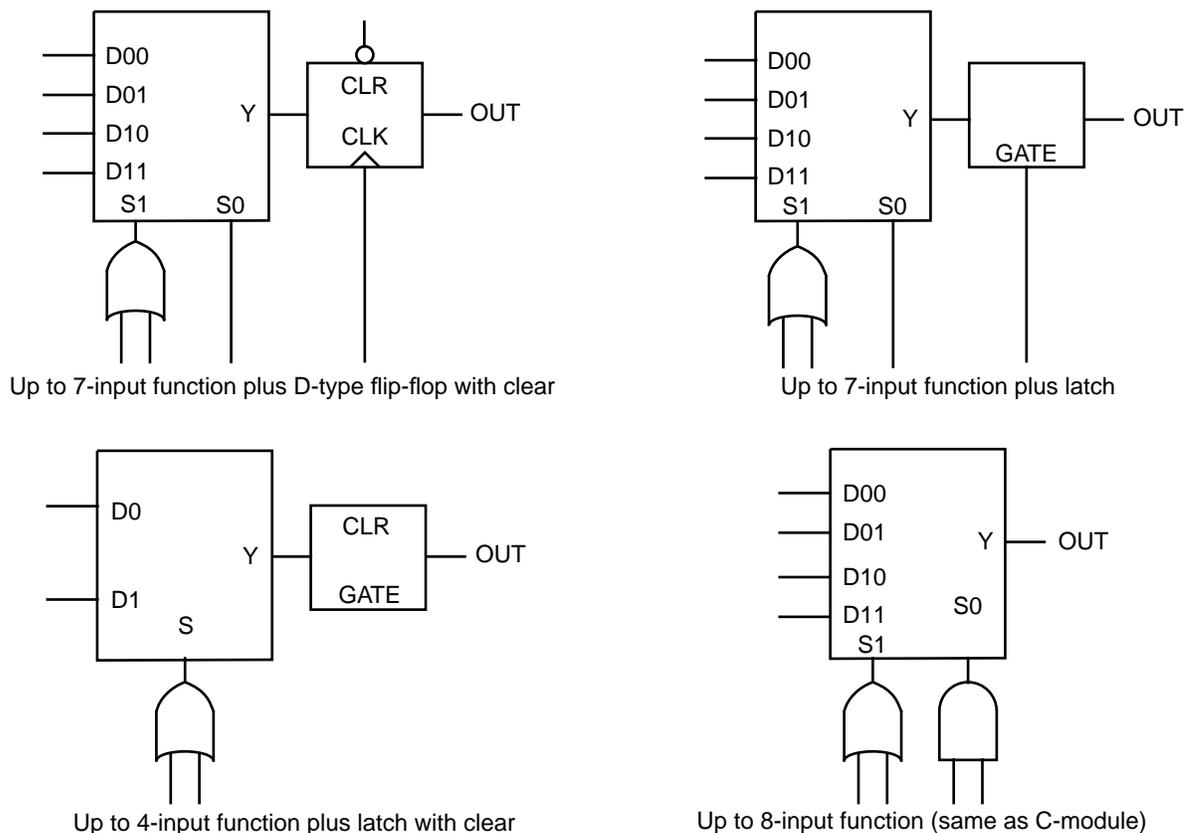
## Introduction

With the RH1280 and RH1020, Actel Corporation introduces radiation-hardened versions of the popular A1280 and A1020 field programmable gate array (FPGA) families with equivalent gate densities of 8,000 and 2,000 gate array gates, respectively. These products are processed to the QML process flow as defined in MIL-PRF-38535. They are manufactured with a 0.8 micron, two-level metal epitaxial bulk CMOS technology, and offer total dose radiation-hardness in excess of 300K rads (Si) with guaranteed latch-up immunity. Because of this high total dose capability, the RH1280 and RH1020 are intended for use in applications including Earth orbiting satellites, deep space probes, and military electronics.

The RH1280 contains a total of 1232 logic modules. There are two types of logic modules: a combinatorial (C-module) and a sequential module (S-module). The S-module can implement the same combinatorial logic as the C-module, and it also contains a flip-flop that can be configured in several different ways. Logic diagrams for the C-module and S-module are shown in Figure 1. The RH1280 contains 608 C-modules and 624 S-modules.

## Single Event Upset (SEU) and Mitigation of Its Effects in the RH1280

SEU data shows that the flip-flop in the S-module, (SFF), is the softest memory bit in the RH1280. The failure rate is



**Figure 1 • S-Module Implementations**

$1 \times 10^{-6}$  upsets per bit-day in a 90% worst case geosynchronous earth orbit, quiet space environment (the default environment for the SEU rate calculation). Also, the SFF has shown a sensitivity to proton-SEU. There are two unique SEU-hardening design techniques described in this Application Note: both can eliminate the proton-SEU sensitivity, and improve the SEU rate to  $1 \times 10^{-7}$  upsets per bit-day, or better. These techniques are summarized in this section and their implementation is described in detail in the following sections.

The first recommended technique for improving SEU and eliminating proton-SEU sensitivity is to avoid using the SFF portion of the S-module. This will make the device immune to proton-SEU effects and improve the SEU rate to  $1 \times 10^{-7}$  upsets per bit-day. Avoiding the use of the SFF forces the memory bit to be constructed using two adjacent modules in order to build flip-flops (flip-flops, the basic test structure, is used as the memory bit in the following discussions). Two-module flip-flops can be constructed in four different ways: C-C; C-S; S-C; and S-S. The S-modules used to create these two-module flip-flops utilize only the combinatorial portion of the S-module. This configuration has been called a “bypassed S-module (BS)” [5] and a “modified S-module (MS)” [6]. When using this technique, I/O latches in the RH1280 can also be used since they are proton-SEU immune and the SEU rate is no worse than  $1 \times 10^{-7}$  upsets per bit-day [4,5].

Triple Modular Redundancy (TMR), a well-known technique for SEU mitigation, is the second recommended technique. The Actel RH1280 FPGA provides an ideal arena to design using TMR at the chip level. This technique can significantly improve the SEU immunity of the device, to a rate less than  $1 \times 10^{-10}$  upsets per bit-day. However, the trade-off to using TMR is that it requires an increased amount of device resources. Additionally, the I/O latch circuitry cannot support TMR, and can therefore not be used in the designs.

### Using Two Module Flip-Flops in the RH1280

Actel’s design software for the RH1280 contains macros for many types of edge-triggered flip-flops and is compatible with the ACT 2 commercial/military family. The Actel Macro Library Guide (1995) describes these macros and indicates if they are implemented with a single S-module (using the SFF), an S-module with a C-module, or two C-modules. When the Macro Guide states that an S-module and C-module are used, it should be assumed by the designer that an SFF will be used for storage and that the macro will have the SEU performance of an SFF. Thus, for designs that need a moderate level of SEU hardness, all macros using an S-module and C-module should be avoided. Only macros using two C-modules should be used. Table 1 lists the names of the edge-triggered flip-flops constructed with two C-modules.

Similarly, one should only use latch macros implemented with C-modules for moderate hardness. Table 2 lists these acceptable latch macros.

**Table 1 • ACT 2 Two-Combinatorial Module Flip-Flop Macros**

DFP1	D-Type Flip-Flop with Active High Preset
DFP1A	D-Type Flip-Flop with Active High Preset and Active Low Clock
DFP1B	D-Type Flip-Flop with Active Low Preset
DFP1D	D-Type Flip-Flop with Active Low Preset and Active Low Clock
DFPC*	D-Type Flip-Flop with Active High Preset, Active Low Clear, and Active High Clock

\* If you are connecting a global clock (Clkbuf, Clkint) on CLR/PRE pins insert a regular buffer (Buf) between the global clock and CLR/PRE.

**Table 2 • ACT 2 Combinatorial Module Data Latch Macros**

DLC1	Data Latch with Active High Clear
DLC1A	Data Latch with Active High Clear and Active Low Clock
DLE2C	Data Latch with Active Low Enable, Active Low Clock, and Active High Clear
DLE3B	Data Latch with Active Low Enable, Active Low Clock, and Active High Preset
DLE3C	Data Latch with Active Low Enable, Active Low Preset, and Active Low Clock
DLP1	Data Latch with Active High Preset and Active High Clock
DLP1A	Data Latch with Active High Preset and Active Low Clock
DLP1B	Data Latch with Active Low Preset and Active High Clock
DLP1C	Data Latch with Active Low Preset and Active Low Clock

Note that when the Macro Guide states a C-module is used it does not exclude the use of the combinatorial portion of the S-module. However, for these macros the SFF portion of the S-module will not be used for storage. If the Macro Guide states that two C-modules are used, it is possible a flip-flop could be implemented as a C-C, C-S, S-C, or S-S combination. The place and route software gives preference to the C-C combination to avoid wasting SFFs. The Chip Edit tool is an excellent way to quickly see how a flip-flop macro is implemented. Chip Edit also easily allows the designer to modify the placement of the flip-flop macro, thus determining which of the C-C, C-S, S-C, or S-S implementations are used. Chip Edit is available in Designer 2.3.x, and Designer 3.1 or later.

## Creating Additional Two Module Flip-Flop Macros

Table 1 lists five two-module flip-flop macros currently available for the RH1280. Additional macros may be offered in future software releases. In addition, it is possible for the user to create one's own flip-flops using the CM8 macro. CM8 is a combinatorial macro that allows full access to the logic of the C-module. Two (or more) CM8 macros can be used to create custom flip-flops. This technique is generally not recommended due to potential problems in calculating accurate timing information. For additional information on using two CM8 macros, please contact Actel Technical Support.

## Avoiding SFFs with VHDL, ACTgen and ABEL

Designers using VHDL methodology can avoid SFFs by creating a VHDL script that excludes all flip-flop and latch macros which can use an SFF. Please contact Actel Technical Support for any assistance required to create this script. For ACTgen and ABEL applications, use a tool such as ViewGen from Viewlogic to create a schematic of the design block, edit the drawing by replacing flip-flop macros as required, and use the schematic to create a new netlist to import into the Designer Series software tools.

## Confirming That No SFFs Are Used

The Compile program in Designer checks for fatal or non-fatal design problems, and creates a report about logic module and routing utilization for the design. Compile will report how many SFFs (if any) have been used; checking this report will allow the designer to be certain that SFFs have been avoided.

## Triple Modular Redundancy

As mentioned above, triple modular redundant (TMR) flip-flops achieve superior SEU performance in the RH1280, even if the SFF is used [2]. TMR has been used in many applications, and is ideal for effectively hardening SEU-soft flip-flops in gate arrays. This section will show how to construct SEU-hardened D-type, register, and J-K flip-flops. The MUX-based architecture of the RH1280 allows an efficient implementation of TMR.

Figure 2 shows an implementation of a D-type flip-flop using TMR. Three D-type flip-flops are connected in parallel to the clock and data inputs. A voter (or majority circuit) is implemented by the top MUX to create a "hardened" output. The outputs of two flip-flops, A and B, go to the selects of the voter MUX. If both A and B read logic zero, MUX input D0 is selected. Since it is tied to GND, the output of the MUX will read logic zero. Similarly, if A and B read logic one, the output of the MUX will read logic one. If A and B disagree due to an

SEU (or for other reasons), the MUX will select flip-flop C. We know C agrees with either A or B, and thus the MUX "voted" to produce data agreed on by two of the three flip-flops.

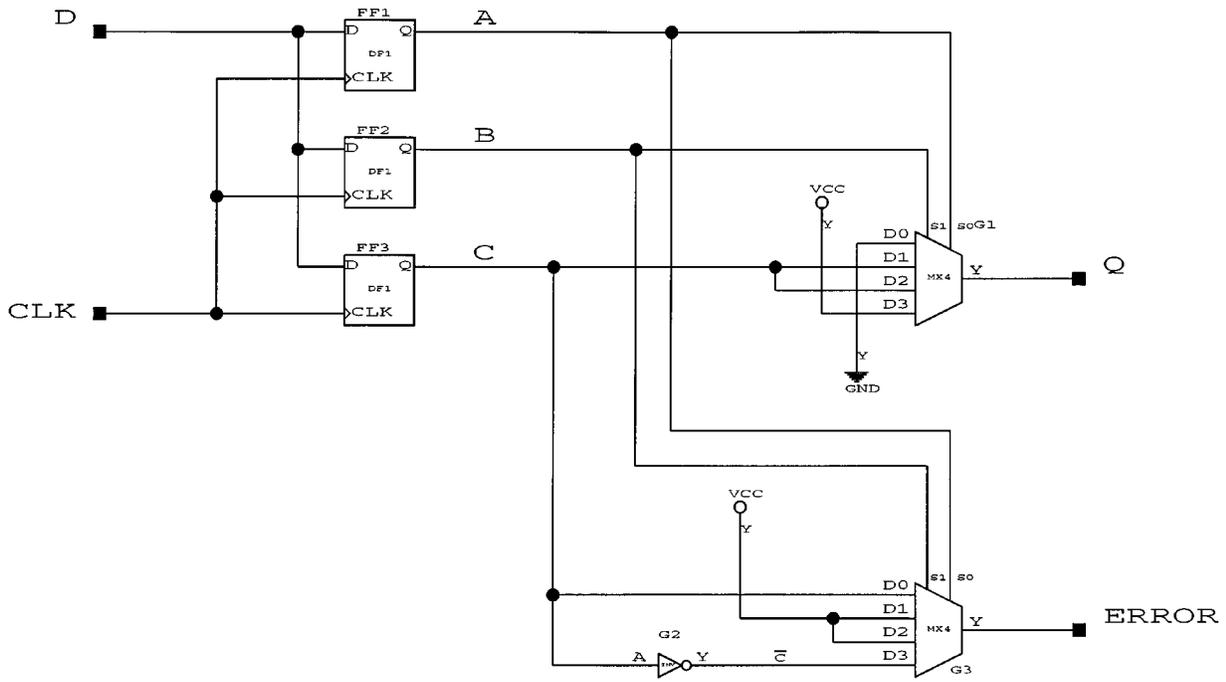
An optional error signal implemented by an inverter and the bottom MUX is also shown in Figure 2. The output of this MUX will be low as long as all three flip-flops agree. If any flip-flop disagrees, the output of the error MUX will go high.

The high degree of data protection using TMR allows the use of SFFs for three parallel flip-flops, while still achieving superior SEU performance. If the D-type TMR circuit shown were to feed another similar circuit, such as in a shift register, then an efficient use of the S-module can be achieved by using three voter MUX's as shown in Figure 3. (Calculating effective SEU hardness is discussed in [2].) Although the number of MUX's has increased, the place and route software will combine each MUX into an S-module and use the SFF for the flip-flop. This allows implementation of the entire TMR circuit into an average of just three S-modules per bit, and the speed penalty of a separate voter module is eliminated. Since the voters are redundant, a combinatorial upset on a voter will affect just one flip-flop and be voted out.

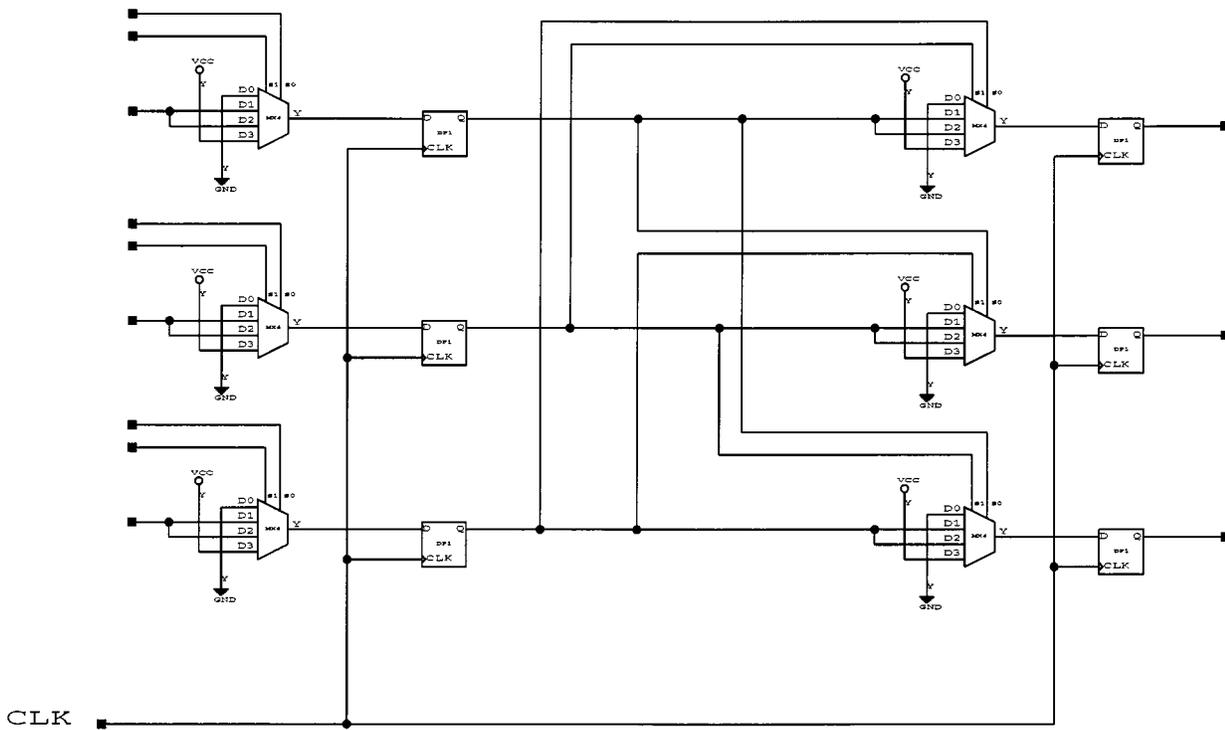
Care is needed when using TMR circuits. First, the output of the voter may be susceptible to a logic hazard "glitch." This is not a problem if the TMR is feeding the input of another synchronous input. However, the TMR output should never feed asynchronous inputs such as flip-flop clocks, clears, sets, read/write inputs, etc.

Second, if gated clocks are used and the flip-flops are not continuously clocked, errors can "accumulate" in the TMR triplets over time. Calculations show that even low to moderate speed clocks will perform well. Ground testing using artificially high SEU rates showed no difference in performance for clock rates ranging from 4 kHz to 10 MHz [2].

Third, the proper operation of parallel flip-flops is not fully testable after the FPGA is programmed because if one flip-flop is not functioning, the TMR circuit will "repair" it. While it is highly unlikely this will occur, 100% fault coverage testing of the TMR circuit's flip-flops in an RH1280 or RH1020 can be achieved in a number of ways. First, the optional error monitoring circuits can be tied into an OR-tree and brought off-chip for monitoring. Other methods use Actel's proprietary ActionProbe test circuit, which allows the output of any internal logic module to be addressed and read by any of two special external pins (PRA and/or PRB). Thus all internal parts of the TMR circuit can be read. This can be done on either the Actel Activator programmer using the debugger interactively, or by applying vectors and comparing data from a file. ActionProbe can also be used during ATE device testing as well. Lastly, all internal modules can be read while the device is on the circuit board using the ActionProbe.



**Figure 2 • D-Type Flip-Flop Implemented with TMR**



**Figure 3 • TMR Shift Register Using Separate Voters. MUX and Flip-Flop Can Combine Into One S-Module.**

## TMR Circuits with Refresh

For memory elements such as loadable registers, a modified TMR circuit (shown in Figure 4) can be used. This circuit will constantly “refresh” itself by feeding corrected data back into the inputs of the flip-flops when the enable (E) input is low, permitting error-free data to be held indefinitely. When enable is high, new data is loaded into the TMR triplet. Again, this circuit very efficiently maps into the RH1280 architecture. Typically, this configuration requires only four logic modules if the SFFs are used.

A J-K flip-flop TMR circuit with refresh is shown in Figure 5. It operates on a similar principle to the circuit shown in Figure 3, with the voter circuit inside the feedback loop. Each of the three 4:1 MUX and flip-flop pairs will map into one S-Module using the SFF. The voter MUX and inverter (for toggling) cannot be combined, resulting in a typical number of five modules per J-K flip-flop.

## Summary

Using the design techniques described in this Application Note, satisfactory SEU performance can be achieved for most space applications. Immunity to many ions can be achieved by selecting flip-flops constructed only from C-modules. Greater SEU performance can be achieved by utilizing TMR techniques. Circuit topologies are shown for all basic flip-flop applications: D-type, register, and J-K. These are readily adapted to variants to satisfy particular requirements (e.g., adding asynchronous clear). The RH1280 architecture is particularly efficient in implementing TMR circuits with minimal effect on system performance. Actel’s ActionProbe allows 100% observability into the operation of all redundant

flip-flops during device test and after installation on a circuit board.

## References:

1. T. Scott and R. Brown, “FPGAs Single Event Effects Test Report”, Loral Internal Report #96-T31-5, February 6, 1996.
2. R. Katz, R. Barto, P. McKerracher, B. Carkhuff, and R. Koga, “SEU Hardening of Field Programmable Gate Arrays for Space Applications and Device Characterization” (unabridged version), IEEE Transactions on Nuclear Science, NS-41, pp. 2179-2186, July 1994.
3. T. Scott and R. Brown, “FPGAs Proton Single Event Effects Test Report”, Loral Internal Report #96-T31-9, February 11, 1996.
4. R. Katz, et al, BNL test data, 1996.
5. Stanley Mattsson and Mikael Wiktorson, “Radiation Pre-Evaluation of Field Programmable Gate Array (FPGA)”, Final Report, ESA Contract No. 11407/95/N2/CN, 1996.
6. J.J. Wang, et al, “Improved SEE Susceptibility of Radiation-Hardened ONO Antifuse FPGA”, 10th SEE Symposium, April 1996.

## Acknowledgment:

We wish to thank Richard Katz of the NASA-Goddard Space Flight Center for developing the TMR design examples and for his invaluable help in producing this Application Note.

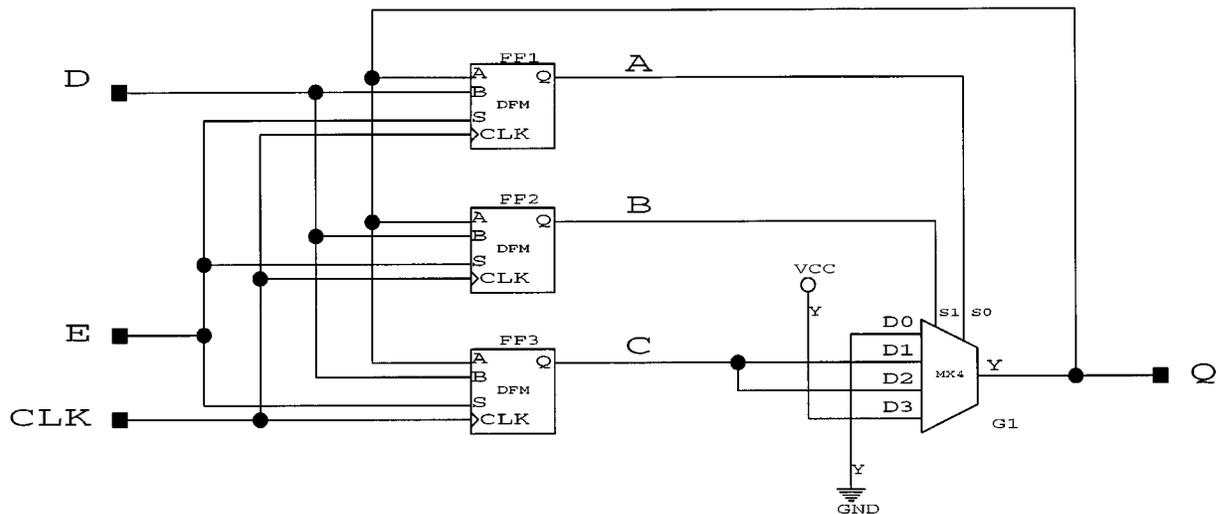
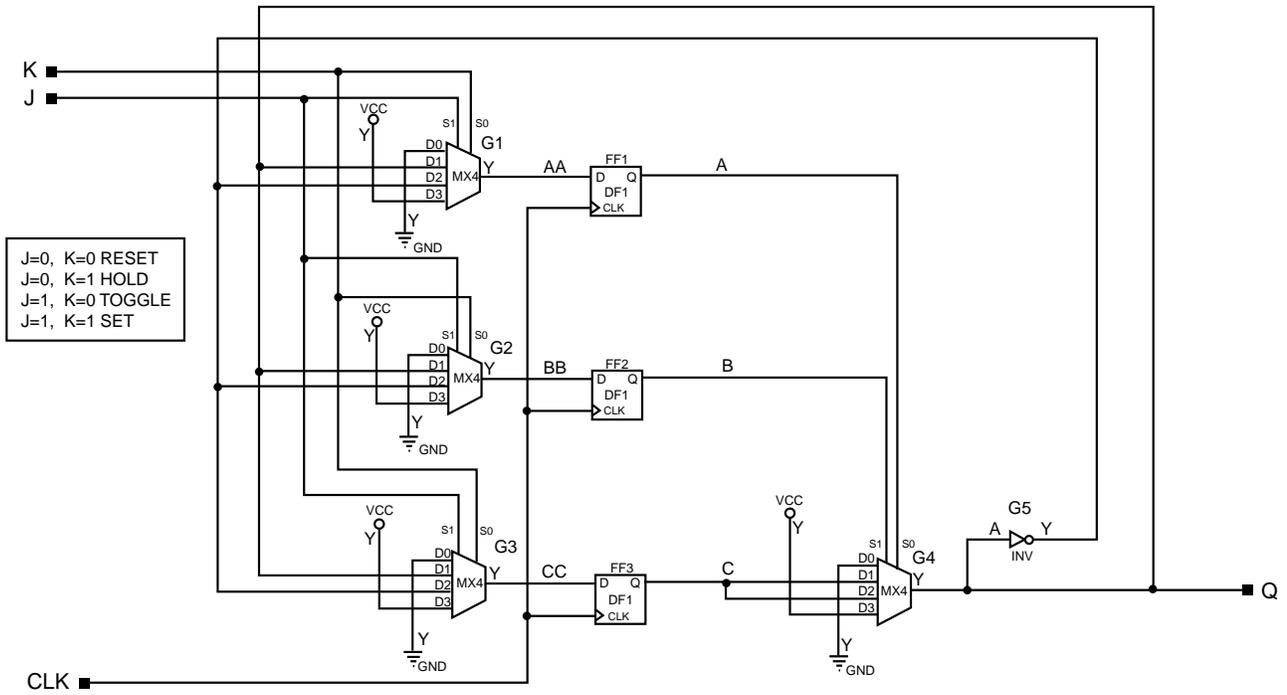


Figure 4 • Register Element with TMR



**Figure 5 • J-K Flip-Flop with TMR**



Actel and the Actel logo are registered trademarks of Actel Corporation.  
All other trademarks are the property of their owners.



**Take it to a higher level.**

<http://www.actel.com>

**Actel Europe Ltd.**

Daneshill House, Lutyens Close  
Basingstoke, Hampshire RG24 8AG  
United Kingdom

**Tel:** +44(0).1256.305600

**Fax:** +44(0).1256.355420

**Actel Corporation**

955 East Arques Avenue  
Sunnyvale, California 94086  
USA

**Tel:** 408.739.1010

**Fax:** 408.739.1540

**Actel Japan**

EXOS Ebisu Bldg. 4F  
1-24-14 Ebisu Shibuya-ka  
Tokyo 150 Japan

**Tel:** +81.(0)3445.7671

**Fax:** +81.(0)3445.7668