# Frequency/Phase Comparator for Phase-Locked Loops

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**Summary**

The phase comparator described in this Application Note permits phase-locked loops to be constructed using LCA devices that only require an external voltage-controlled oscillator and integrating amplifier.

**Xilinx Family**

XC3000
XC4000
XC5000

## Introduction

A Phase-Locked-Loop (PLL) manipulates a local voltage-controlled oscillator (VCO) so that it is in phase with a reference signal. One popular application is a programmable frequency synthesizer for radio communications. Here a crystal oscillator is divided down to a low reference frequency of 5 kHz, for example.

As shown in Figure 1, a programmable divider scales the VCO frequency down to the fixed reference frequency. The counter output is compared to the reference frequency to generate a signal that, when required, modifies the VCO frequency up or down until the comparator inputs are not only of the same frequency, but also have their falling (High-to-Low) edges in phase.

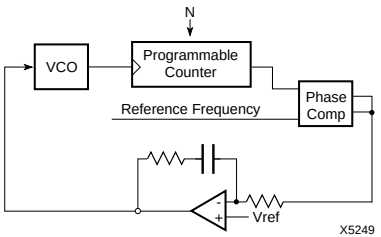


**Figure 1: Typical Digital Phase-Locked Loop**

This frequency/phase comparator must have a wide capture range, i.e. it must generate the appropriate output, not only to pull in a small phase error, but also to correct a large frequency error. It should not generate false outputs when the input is at a multiple or fraction of the desired frequency. The well-known circuit shown in Figure 2, introduced in the early 1970's as the Motorola MC4044, performs this function. It generates pump-up pulses when the VCO frequency is too low, pump-down pulses when its too high. The multiple feedback network assures proper operation even with large frequency errors. Figure 3 and Figure 4 show this circuit implemented in two CLBs plus two IOBs, directly driving the integrator (low pass filter) controlling the VCO.

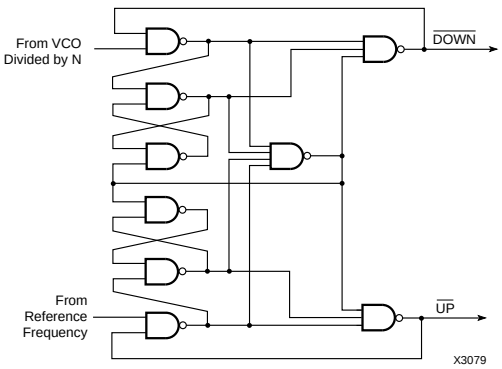


**Figure 2: Digital Frequency/Phase Detector**

Figure 3 and Figure 4 show two slightly different implementations of the frequency/phase detector. Figure 3 generates internal active Low signals, and therefore drives the active Low Output Enable. Figure 4 generates internal active High signals, and therefore drives the active High Output Enable. The two circuits perform exactly the same function. They are both shown here because previous editions of Xilinx documentation, and early macros, had mixed up the internal polarities.

These circuits have been simulated and are known to work.

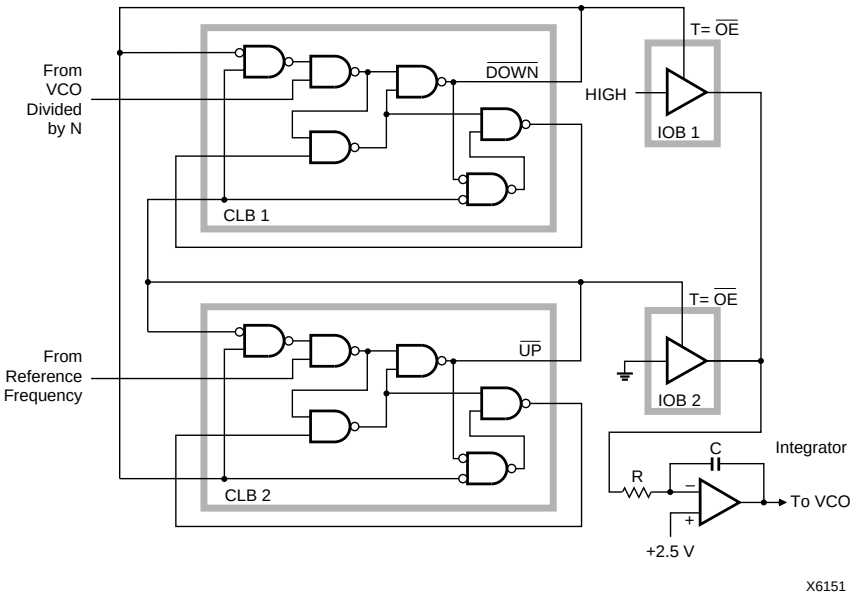


**Figure 3: Frequency/Phase Detector Using Two CLBs and Two IOBs (Active Low)**

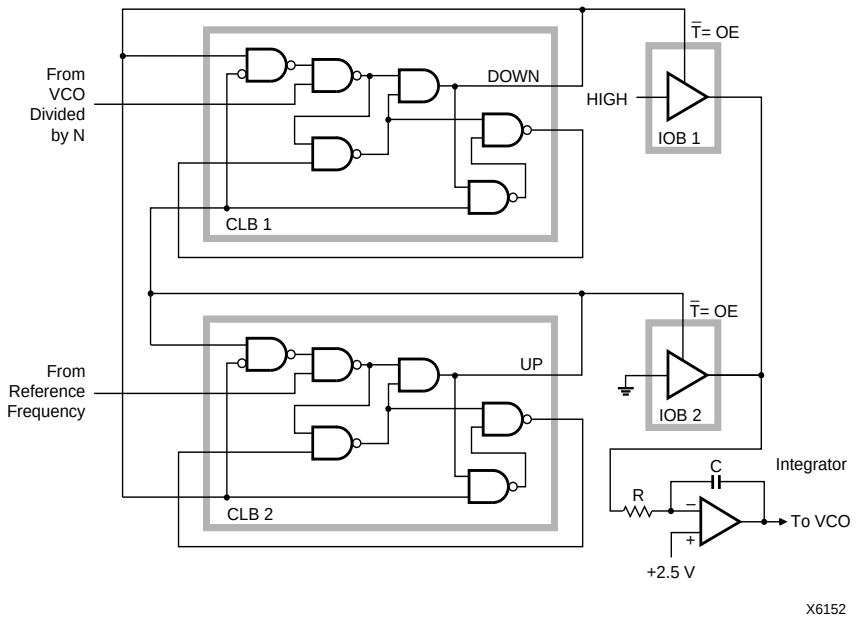


**Figure 4: Frequency/Phase Detector Using Two CLBs and Two IOBs (Active High)**