**TriQuint**
SEMICONDUCTOR®

Robust Bias Option for 0.15 μm pHEMT MMIC Low-Noise Amplifiers

Background: A bias network has been designed for low-noise MMIC amplifiers fabricated using the 0.15 um pHEMT process. This process exhibits a low pinch-off voltage (near zero volts) and the optimum gate-source voltage can be a negative or positive voltage, due to normal process variations.

Method: The circuit shown in Figure 1 below will automatically set the gate voltage (which is equivalently the gate-source voltage because the source is grounded on the MMIC chip) to achieve a desired current target, I_d, as defined by

$$I_d = (V_{pos} - V_d) / R_d$$
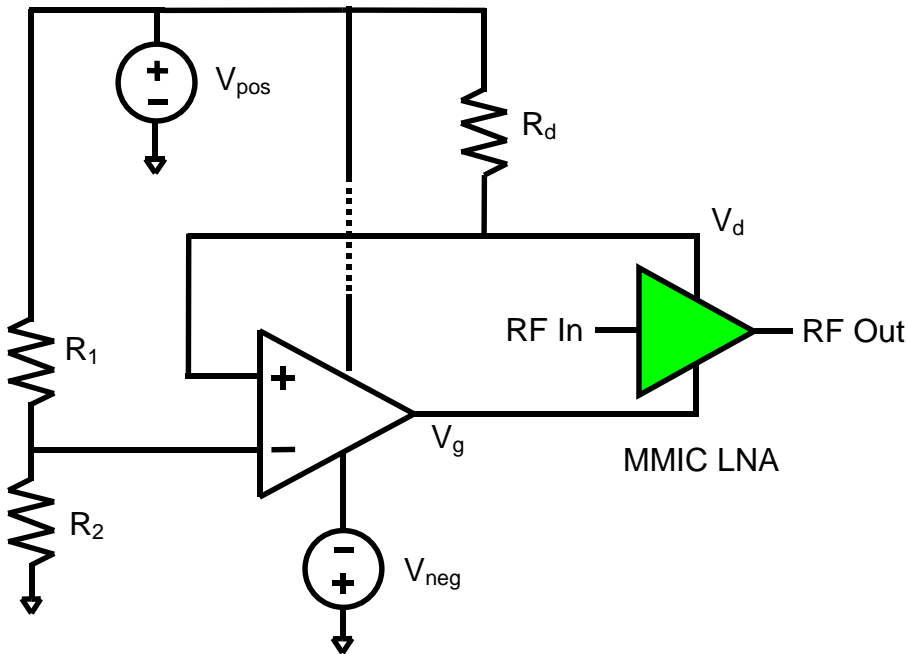
Figure 1

This circuit works well with low noise amplifiers for two reasons:

1) The optimum MMIC drain voltage, V_d, is typically 3 to 4 volts so that a voltage dropping resistor (R_d) is already required to reduce the supply voltage from its typical value of 5 to 8 volts.
2) The level of bias current is modest, usually in the range of 50 to 250 mA. This allows easy placement of a small series resistor (R_d) without thermal issues.

Additionally, the circuit is very inexpensive, requiring only one standard, low cost op amp and three resistors. Typically, the MMIC LNA will already have bypass capacitors on the drain and the gate terminals (not shown). The negative voltage applied to the op amp is not critical; it only needs to be more negative than the pinch-off voltage (this depends somewhat on the choice of op amp). Negative 3 to negative 5 volts (-3V to -5V) will satisfy most applications. Also, the op amp provides a low driving impedance at the gate and will sink the small leakage currents that are common in GaAs FETs and pHEMTs without a change in the drain bias current.

Recommended Approach: If the values of V_{pos}, V_d, I_d are known, the next steps will be to:

1) Solve for R_d $R_d = (V_{pos} - V_d) / I_d$,

2) Solve for resistor ratio $Ratio = R_2 / (R_1 + R_2) = V_d / V_{pos}$,

3) Choose R_2, solve for R_1 $R_1 = R_2 * (1 - ratio) / ratio$.

Example:

The TGA1319A LNA requires a bias quiescent current of 45mA at a drain voltage of 3 volts. The power supply voltage is 5 volts and a negative voltage of -5 volts is available.

Knowns: $V_{pos} = 5$ volts, $V_{neg} = -5$ volts, $V_d = 3$ volts

Target: $I_d = 45$ mA

$R_d = (5 - 3) / 0.045 = 44.44$ ohms   Power Dissipated = $1.5 * 0.045 = 67.5$ mW

Ratio = $3 / 5 = 0.6$

Choose $R_2 = 10$ kohms, then $R_1 = 10 * (1 - 0.6) / 0.6 = 6.67$ kohms

The closest 1% standard resistor values for R_d, R_1, and R_2 are 44.2 ohms, 6.65 kohms and 10.0 kohms which results in a nominal drain current of 45.2 mA instead of 45 mA.

Design Issues: Several other design issues should be considered in development of a bias network for a MMIC LNA. Not all of these issues are relevant for all applications.

    1.) Op amp stability – The design should ensure that the op amp will be stable driving the load presented by the gate terminal of the MMIC. This includes any bypass capacitors (not shown in Figure 1) which might be attached to this terminal. These capacitors are often necessary to ensure the stability of the MMIC at frequencies much lower than their band of operation. Capacitance values below

100pF do not cause most op amps a stability problem, whereas much larger values such as 0.01uF will often cause the op amp to oscillate in the kHz or low MHz region. Special op amps are available that are designed to drive highly capacitive loads. The capacitor on the MMIC drain terminal is usually not a problem, but should be included in any stability analysis.

2.) Transient RF response – Some applications require the MMIC LNA to respond to pulsed or transient RF signals. This op amp bias circuit forms a closed loop feedback network that can have an effect on the LNA if the bias current needs to change during the transient condition. While this is atypical of LNA designs, this is a normal condition for power amplifiers that operate in the gain compression region. The LNA design should be evaluated for any conditions where the bias current might need to change rapidly (such as turning the LNA on and off). Under these conditions the bias network will have an effect on the rate of change and the settling time.

3.) Signal modulation – Unwanted modulation of the RF signal is a potential problem. This network is attached to positive and negative power supplies from which the correct gate voltage for the MMIC is derived. Therefore, any modulation of these DC voltages (from a switching power supply or digital circuitry, etc) can be impressed on the MMIC gate voltage. Since the gate is typically the most sensitive terminal on the MMIC to modulation, attention should be given to the level and frequency of modulation on the positive and negative power supply voltages. Also, the power supply rejection ratio (PSRR) of the op amp should be evaluated at the frequencies of modulation (not the DC value) for sufficient attenuation of the unwanted signals. For very high modulation frequencies or large amplitudes, filtering of the positive and negative terminals of the op amp may be necessary to reduce the magnitude to an acceptable level.

4.) Bias accuracy – The accuracy of this network in achieving the desired drain current target is dependent primarily on two variables: the value of R_d and the value of V_{pos}. The drain current is directly proportional to both of these variables. A 5% change in the supply voltage will cause a 5% change in the drain bias current. Of secondary importance is the ratio of resistors R_1 and R_2 and the non-ideal op amp characteristics such as input offset voltage and offset currents. There are many solutions to improving the accuracy of these variables if warranted by the design requirements.

Other issues will often be included in the complete design study. These can include, but are not limited to, the cost of the bias network versus other alternatives, the amount of board space required by the bias network, the power consumption of the network, the performance over temperature or the radiation hardness of the network.

For additional information, please contact TriQuint Texas Applications Engineering Department at 972-994-3647.