

LAN8700/LAN8700I and LAN8187/LAN8187I Ethernet PHY Layout Guidelines

1 Introduction

The LAN8700/LAN8700I and LAN8187/LAN8187I are highly-integrated devices designed for 10 or 100 Mbps Ethernet systems. They are based on IEEE 10BASE-T and 100BASE-TX standards. The IEEE 802.3-2005 standard for 100BASE-TX defines networking over two pairs of Category 5 unshielded twisted pair cable or Type 1 shielded twisted pair cable.

These devices come in a combination of two package options and support for two temperature ranges. The LAN8700/LAN8700I is available in a 36-pin QFN package and the LAN8187/LAN8187I is available in a 64-pin TQFP package. The (I) designation indicates that the device is industrial temperature (-40°C to 85°C) compatible.

The LAN8700/LAN8700I and LAN8187/LAN8187I comply with the IEEE 802.3-2005 Auto-Negotiation and Full Duplex Flow Control standard. The LAN8700/LAN8700I and LAN8187/LAN8187I also include a PHY interface compliant to either the MII or RMII interface connection standards.

The LAN8700/LAN8700I and LAN8187/LAN8187I feature HP Auto-MDIX, which automatically switches transmit and receive circuitry to correct for cross-over cables.

This application note is intended to assist customers in designing a PCB using SMSC's LAN8700/LAN8700I or LAN8187/LAN8187I to interface with an Ethernet network. This document provides recommendations regarding the PCB layout is a critical component in maintaining signal integrity.

1.1 Audience

This application note is written for a reader that is familiar with Ethernet hardware design.

1.2 Overview

The following recommendations for the PCB layout with SMSC parts are not the only way to layout our QFP/QFN parts. Every board designer will have his/her own preference. Complexity, board space, number and types of devices can dictate routing and placement strategies.

1.3 References

The following documents should be referenced when using this application note:

- SMSC LAN8700/LAN8700I datasheet
- SMSC LAN8187/LAN8187I datasheet
- SMSC EVB LAN8700 users manual
- SMSC EVB LAN8187 users manual

2 Components

The EVB board schematics and gerber files can be found on the SMSC web site. These can be used as a reference for component placement and routing.

2.1 Industrial Temperature

When designing with the industrial temperature version of the PHY, care needs to be given to the temperature range of the supporting components. If the end application requires industrial temperature support, then the System Designer needs to select all pertinent components to be functional in the industrial temperature range.

2.2 General Design Guidelines

Good engineering practices should be followed with respect to unused inputs by terminating them with pull-up or pull-down resistors, unless the datasheet, design guide or reference schematic indicates otherwise. Do not attach pull-up or pull-down resistors to any pins identified as reserved (unless explicitly stated in the datasheet). These devices may have special test modes that could be entered inadvertently.

Component placement can affect signal quality, emissions, and component operating temperature. Careful component placement can decrease potential EMI problems and simplify the task of routing traces.

Differential traces should be designed to a 100 ohm differential impedance value to prevent reflections.

2.3 Placement

The EVB Board and gerbers can be found on the SMSC web site. These can be used as a reference for component placement and routing.

- If the magnetic is a discrete component, then the distance between the magnetic and the RJ-45 needs to have the highest consideration and be kept to under 1 inch of separation. The differential impedance should be 100 Ohms. The traces need to run symmetrically, differential pairs should be routed with consistent separation and with exactly the same lengths and physical dimensions.
- The distance between the PHY and the magnetics needs to be less than two inches and the differential pairs need to maintain symmetry and a target differential impedance of 100 ohms.
- The crystal oscillator and resistors and capacitors on the crystal oscillator must be placed within 0.5 inches to the PHY.
- The power supply decoupling capacitors needs to be placed close to the PHY. The Internal Core power decoupling capacitors also need to be as close as possible to the PHY VDDCORE pin.
- The external bias resistor must be placed close to the PHY EXRES pin.
- Keep the PHY device and the differential transmit pairs at least 1 inch from the edge of the PCB, up to the magnetics, if the magnetics are integrated into the RJ45, then bring the differential pairs up to the back of the integrated magnetics RJ45 connector, away from the board edge.
- If the design has ESD suppression capacitors on the output lines (TXP/TXN and RXP/RXN), then the designer needs to ensure these components are placed close to the PHY device.
- The 49.9 Ohm pullup resistors on the differential lines, TXP/TXN and RXP/RXN, must be close to the PHY device. This ensures the transmit path is identical between the TX and RX.
- The Boot-Strap resistors need to be located close to the PHY to ensure the voltage into the pin at boot-up is at the correct VIH or VIL level. An example of the bootstrap resistor is the address and mode pins.

3 Review of Critical Circuits

This chapter provides guidelines for the sensitive circuits associated with the system application of the LAN8700/LAN8700I and the LAN8187/LAN8187.

3.1 Controlled Impedance for Differential Signals

The 802.3-2005 specifications requires the TX and RX lines to run in differential mode. The TXP and TXN are a differential pair and need to be designed to a 100 ohm differential impedance. The RXP and RXN traces are also a differential pair and need to be designed to a 100 ohm differential impedance target. In the design referenced below, the traces are 8 mils wide with minimum line spacing of 6 mils. These numbers are derived for a 10 mils distance from the ground reference plane. A continuous ground plane is required directly beneath the TX/RX traces to the middle of the magnetics module, and extending at least 5 times the spacing width to either side of differential lines.

The Board Designer must maintain 100 Ohms differential impedance in the layout for all the differential pairs of nets. For different dielectric thickness, copper weight or board stack-up, trace widths and spacings will need to be recalculated.

Differential pair nets must maintain symmetry. TXP and TXN must be equal length and symmetric. RXP and RXN must be equal length and symmetric. Symmetric with regards to shape, length, and via count. For example, if TXP goes through a via at 0.33 inches, then TXN should also go through a via at 0.33 inches.

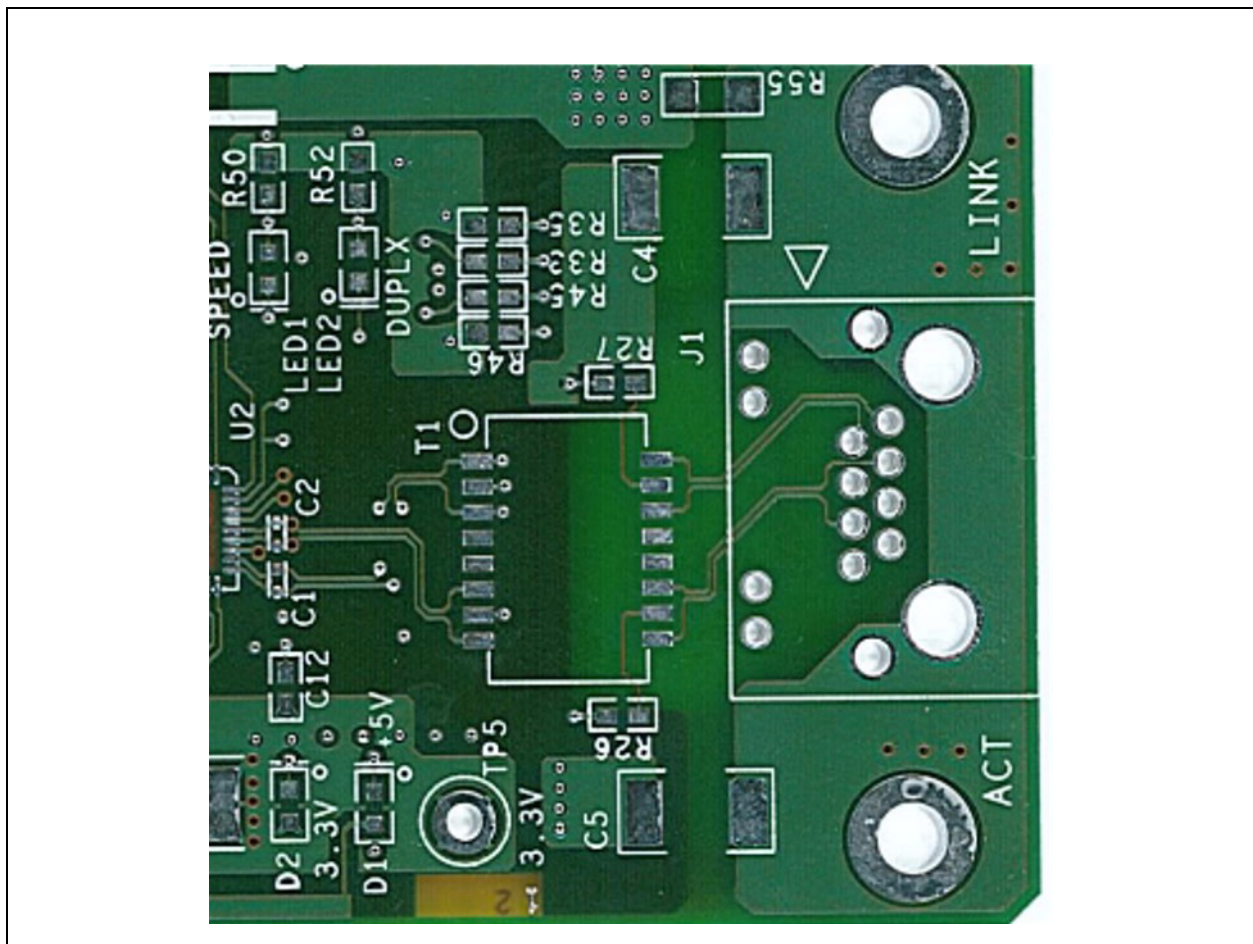


Figure 3.1 Example of Routing TX/RX to RJ-45

Figure 3.1 shows TX/RX traces with approximately equal trace length and symmetry. It is important to maintain width and spacing that provides differential and common mode impedances compliant with the 802.3 specification. Avoid using 90 degree turns to minimize impedance discontinuities.

- Isolation of TX/RX Traces

The TX/RX traces must be isolated from nearby circuitry and signals. Maintain a distance of parts to lines that are greater than or equal to 5 times the distance of the 6 mil spacing between the traces. Do not route differential pairs under parts. Do not cross TX/RX lines with other PCB traces unless the traces are on the opposite side of the ground plane from TX/RX. Route TX/RX traces over a solid ground plane, not over power planes.

- Crystal Oscillator

The crystal oscillator is sensitive to stray capacitances and noise from other signals. It can also disturb other signals and cause EMI noise. The load capacitors, crystal and parallel resistors should be placed close to each other. The ground connection for the load capacitors should be short and out of the way from return currents of power lines.

Figure 3.2 shows a schematic of the crystal oscillator circuit.

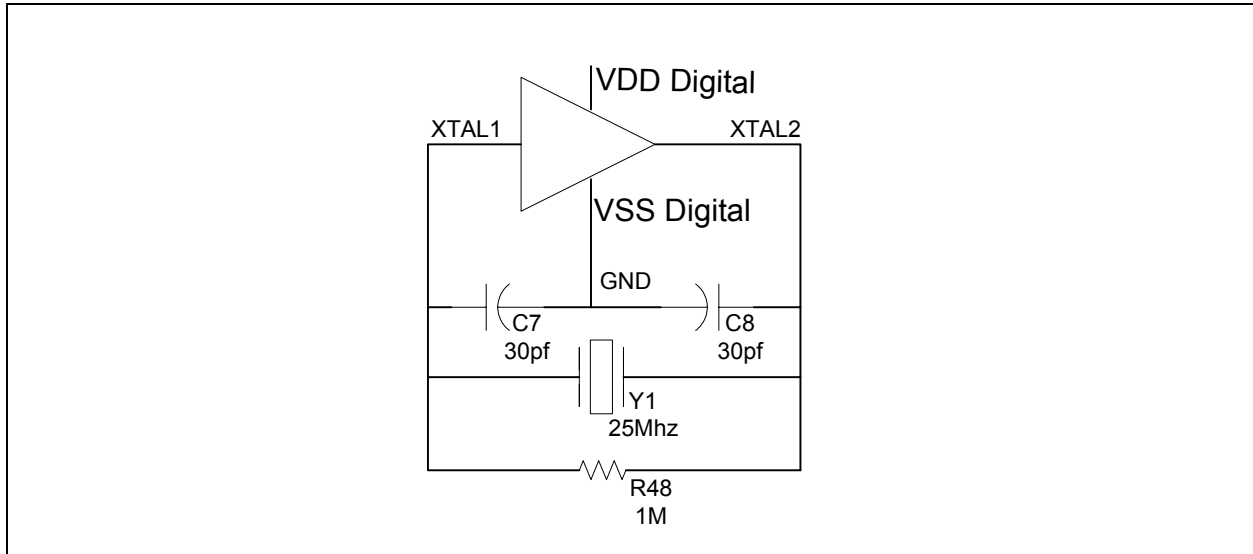


Figure 3.2 Crystal Oscillator Schematic

Figure 3.3 illustrates a suggested PCB layout of the crystal circuit. All components are far removed from TX/RX lines.

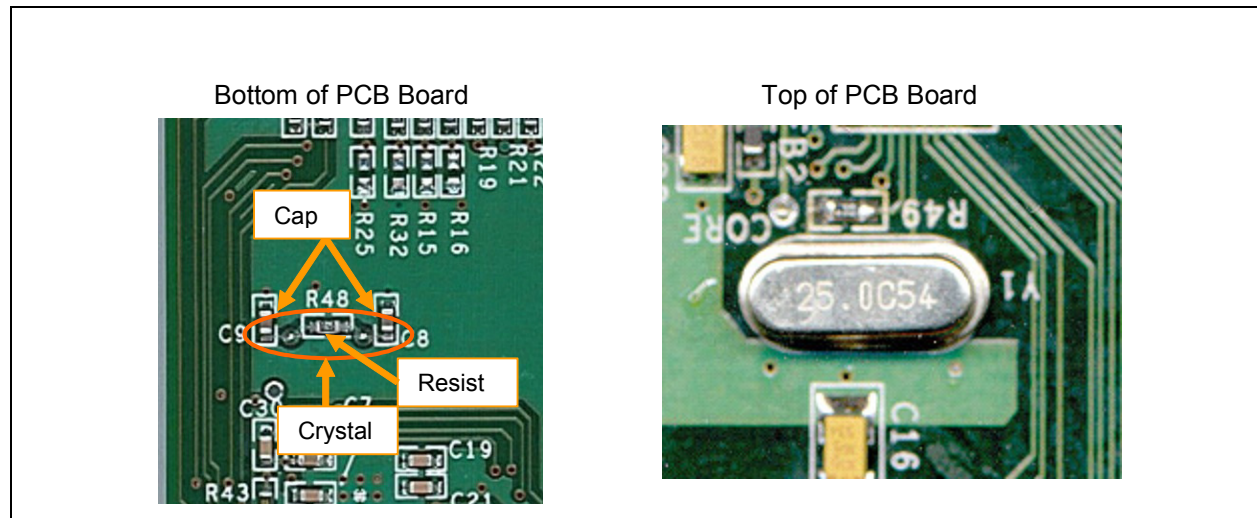


Figure 3.3 Crystal Oscillator PCB Layout

3.2 RBIAS

The external resistor connected to the EXRES pin must have 1% tolerance or better. The resistor must be located close to the EXTRES pin with a good ground return.

The RBIAS resistor sets an internal current source reference. Thus, the RBIAS pin is a high impedance node and so any noise induced on the RBIAS traces will directly impact internal current references and negatively degrade eye-diagram quality. The RBIAS resistor should be placed close to the RBIAS pin and the ground return should be short and direct to VSS with RBIAS placed the same way as bypass capacitors as described in [Section 2.3](#). Resistor traces should be very short and isolated from nearby traces if possible.

3.3 Power Supply Bypass Capacitors

Bypass capacitors should be placed close to the power pins of the PHY and connected with short traces. The LAN8700/LAN8700I evaluation board has bypassing directly under the part, with return current paths tied to the bottom ground plane.

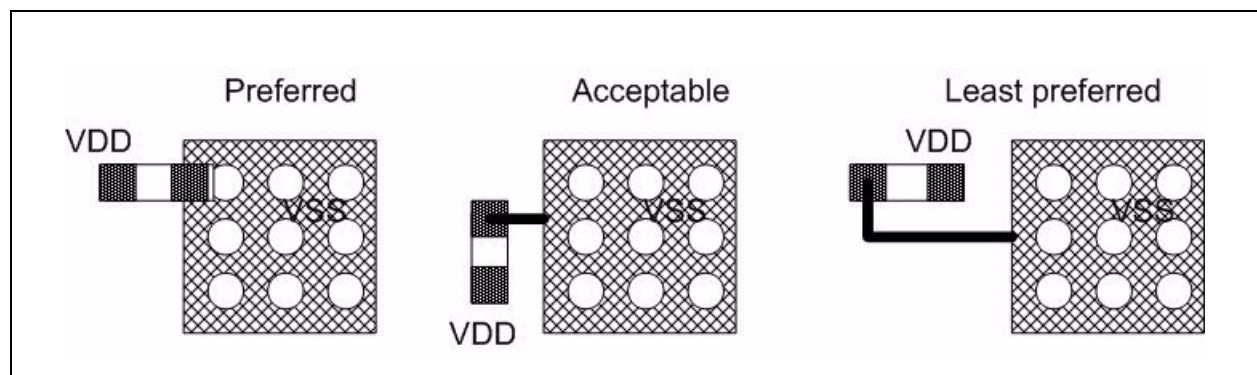


Figure 3.4 Placement of Bypass Capacitors

3.4 VIAS in Ground Flag for QFN Package

The die pad (flag) is approximately 180 mils x 180 mils. A 15 mil via in a pattern of 3 X 3 grid pattern has been used which resulted in excellent signal integrity performance.

3.5 Magnetics Module

The magnetics module has a critical effect on overall IEEE and emissions conformance. The device should meet the performance required for a design with reasonable margin to allow for manufacturing variation. Occasionally, components that meet basic specifications may cause the system to fail IEEE testing because of interactions with other components or the Printed Circuit Board (PCB) itself. Carefully qualifying new magnetics modules can go a long way toward preventing this type of problem.

SMSC provides two levels of Magnetics qualification, Suggested magnetics and Qualified magnetics.

Suggested magnetics have not been tested in order to verify proper operation with the specified SMSC device. This category of magnetic has been evaluated by the contents of the vendor supplied data sheet and legacy performance only. However, the designer can assume with some degree of confidence, that with proper PCB design techniques, the combinations of SMSC devices and magnetics presented as suggested magnetics will perform to high standards.

Qualified magnetics have been tested in order to verify proper operation with the specific SMSC device listed with it. The designer can assume with a high degree of confidence, that with proper PCB design techniques, the combinations of SMSC devices and qualified magnetics will perform to the highest standards.

For more information on magnetics, please refer to the [Application Note 8-13 "Suggested Magnetics"](#).



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