Powerex, Inc., 173 Pavilion Lane, Youngwood, Pennsylvania 15697 (724) 925-7272

DIP-IPM Power Devices

Application Note

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Application Information

1.0 Introduction to the DIP-IPM Family

The use of inverters with small AC motors in appliances, HVAC and low power industrial applications is increasing rapidly. The power stage of these inverters is required to meet the efficiency, reliability, size, and cost constraints of the end application. Presently, many of these small inverters rely on discrete IGBTs, free-wheel diodes and HVICs (High Voltage Integrated Circuits) for their power stage. A common problem with this approach is the high manufacturing cost associated with mounting and isolating multiple high voltage discrete components. Another equally perplexing problem is maintaining consistent performance and reliability when the characteristics of the HVIC drivers, IGBTs and free-wheel diodes are not matched. The DIP-IPM Family presented in this application note is designed to provide a cost effective solution to these problems by combining optimized drive ICs and power devices into a single transfer molded component. The DIP-IPMs simplify mechanical assembly and provide consistent, reliable, performance for a wide range of motor control applications.

1.1 The DIP-IPM Concept

Conventional IPMs (Figure 1.1) with integrated power devices and low voltage ASICs (Application Specific Integrated Circuits) provide gate drive and protection functions and have been widely accepted for general purpose motor drive applications ranging from 200W to more than 150kW. The success of these modules is the direct result of advantages gained through increased integration. Some of these advantages include the following: (1) Reduced design time and improved reliability offered by the factory tested, built-in gate drive and protection functions; (2) Lower losses resulting from optimization of power chips; (3) Smaller size resulting from the use of bare power chips and application specific control ICs; (4) Improved manufacturability resulting from lower external component count.

Unfortunately, in spite of these advantages, the conventional IPM's relatively expensive IMS or DBC ceramic based package design and optically coupled interface circuit is often too expensive and complex to meet the demanding cost and size requirements of low end industrial and consumer appliance inverters. In most of these applications significant cost saving is obtained by utilizing HVICs to provide level shifting thereby eliminating the need for optocouplers. Additional savings are obtained by utilizing bootstrap power supplies for the high-side gate drivers rather than the four isolated supplies required by the conventional IPM.

The key to the DIP-IPM, shown in Figure 1.2, is the integration of custom HVICs to provide level shifting and gate drive for the high-side IGBTs. This results in significant cost savings by allowing direct connection of all six IGBT control signals to the MCU. The HVIC also provides undervoltage lockout protection to allow simplified implementation of the required bootstrap power supplies. With just a few external components the entire three-phase power stage can operate from a single 15V

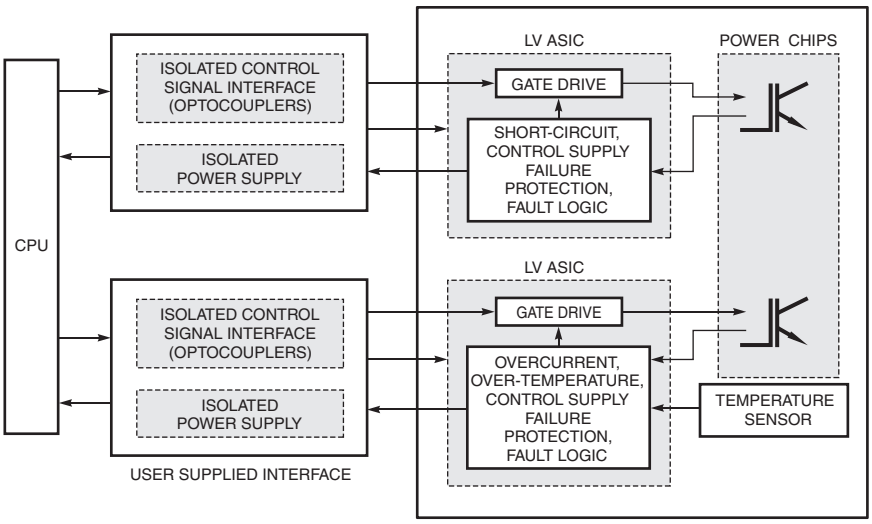


Figure 1.1 Conventional IPM

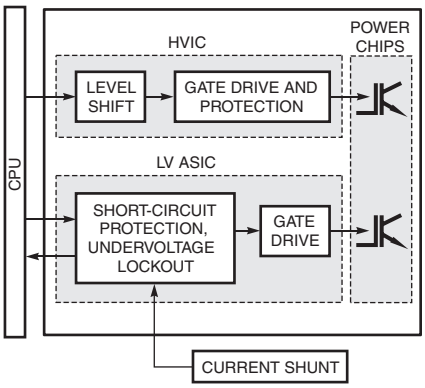


Figure 1.2 DIP-IPM and Mini/ Super-Mini DIP-IPM

control power supply. The DIP-IPM also utilizes a custom low voltage integrated circuit to provide gate drive, short-circuit protection and undervoltage lockout for the low-side IGBTs. Incorporating the level shifting into the DIP-IPM reduces high voltage spacing requirements on the control PCB. This leads to a significant savings in circuit board space. The DIP-IPM package was further reduced to the Mini DIP-IPM and Super-Mini DIP-IPM, each having smaller packages than the former.

1.2 System Advantages

Figure 1.3 shows a comparison of the components required in a typical three-phase motor drive using discrete co-packaged IGBT devices versus a Mini DIP-IPM. Clearly, there are significant manufacturing advantages to the DIP-IPM approach. Each of the discrete devices must be individually mounted and isolated which typically results in a very complex assembly and significant manufacturing time. On the other hand, the DIP-IPM contains all six of the required IGBT/free-wheel diode pairs and is fully isolated. Mounting is accomplished with only two screws and no additional isolation material is required. The reduced manufacturing time and simplified assembly provided by the DIP-IPM will allow improvements in both cost and reliability of the finished system.

Another advantage of the DIP-IPM is that the incorporated IC's gate drive and protection functions are factory tested with the IGBTs as a subsystem. This eliminates uncertainty about the critical coordination of the electrical characteristics of these components. The result is better, more consistent system performance and reliability.

2.0 Product Description

The original transfer molded DIP-IPM was introduced by Mitsubishi in 1998 to address the rapidly growing demand for cost effective motor control in consumer appliance applications. These devices soon became the industry benchmark for performance and reliability in small motor drives. In the years that followed continuous improvements in performance and packaging have led to the industries most advanced line-up of modules for small motor control. Today modules are available for motors rated from 100W to 15kW at line voltages of 120VAC to 480VAC. The following subsections present the module line-up and common features.

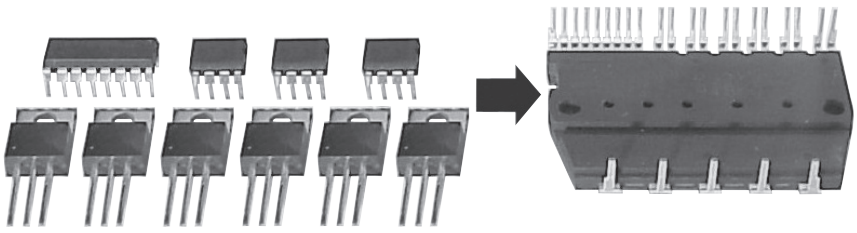


Figure 1.3 Discrete Approach vs DIP-IPM

2.1 Numbering System

(1) Device
PS2 = Transfer Mold Type IPM

(2) Voltage (V_{CES})
1 = 600V
2 = 1200V

(3) Package Style
0 = DIP 2 Package
5 = Mini DIP Package
6 = DIP (Generation 3.5) Package
7 = Mini DIP (Generation 4) Package
8 = DIP (Generation 3) Package
9 = Super-mini DIP Package

(4) Factory Information

(5) Current Rating (I_C)
1 = 3A
2 = 5A
3 = 10A
4 = 15A
5 = 20A
6 = 25A
7 = 30A
9 = 50A

(6) Options
See Table 2.1

Example:

PS2 1 9 6 2 – S
(1) (2) (3) (4) (5) (6)

PS21962-S is a transfer mold IPM rated for 600 Volts and 5 Amperes. It is an open-emitter Super-mini DIP style package with 1500V isolation.

2.2 Line-up and Typical Applications

Figure 2.1 shows photographs of a the available DIP-IPM packages. The Mini and Super-Mini DIP-IPM are available with collector-emitter blocking voltages of 600V. The DIP 2 is available with 600V and 1200V ratings. The Mini DIP-IPM is a smaller version of the original DIP-IPM and the new Super-Mini DIP-IPM is smaller still. They all integrate IGBTs and free-wheel diodes, along with gate drive and protection circuits. The 600V class is suitable for 100VAC to 220VAC motor drives, while the 1200V DIP-IPM class is suitable for low power AC motor drives up to 480VAC. Appliances and low-end industrial drives are the target markets for the DIPs. Typical applications range from refrigerator compressor motors to blower and fan motors in HVAC systems. They can also be used in fitness equipment, power tools and pumps for residential or small commercial applications. Table 2.1 and 2.2 shows the product line-up of DIP-IPMs.

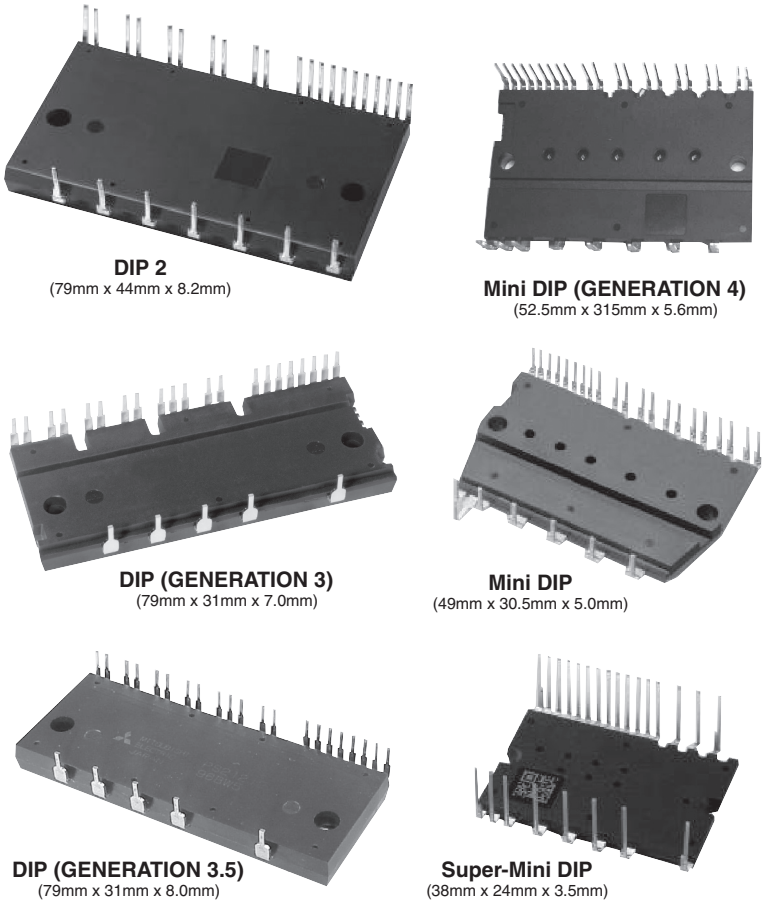


Figure 2.1 DIP-IPM Family

2.3 Product Features

Figure 2.2 shows basic block diagrams of the DIP-IPM integrated features. The key features include:

- Three-phase IGBT bridge including six of the latest generation IGBTs and six optimized shallow-diffused soft-recovery free-wheeling diodes.
- High voltage integrated circuit (HVIC) level shifters for high-side gate drive enables direct connection of all six IGBT gating control signals to the controller

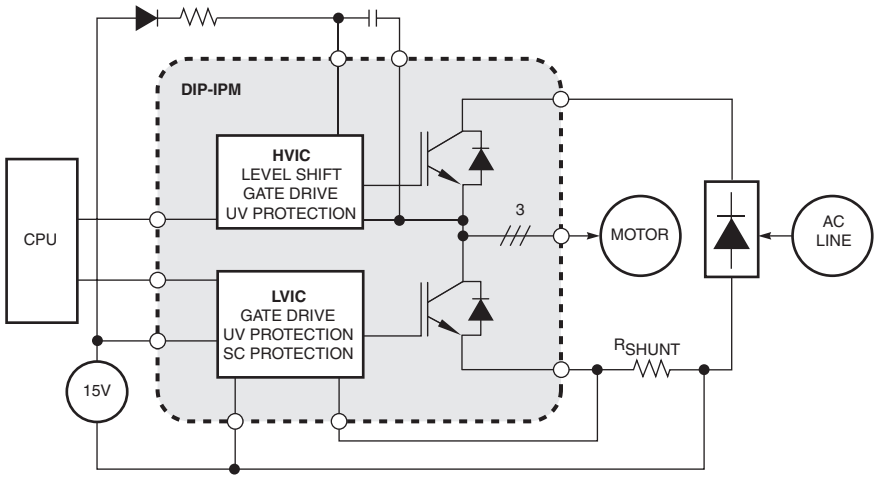


Figure 2.2 DIP-IPM Block Diagram

Table 2.1 600V DIP-IPM Line-up

Package	Nominal / Peak Current IGBT & Free-wheeling Diode		Continuous Sinusoidal Inverter Output Current ($T_{sink} \le 80°C$, $T_j \le 125°C$, $I_{peak} \le 1.7\ I_C$) (ARMS)*		Isolation Voltage (V_{RMS})	Part Number	Options (-Part Number Suffix)
	I_C/I_{CP}	Rated Voltage	f_{sw} = 5kHz	f_{sw} = 15kHz			
Mini DIP	5A / 10A	600V	6.0	5.2	2500	PS21562-P	-SP Open-emitters
	10A / 20A	600V	10.4	7.0	2500	PS21563-P	
	15A / 30A	600V	12.0	7.8	2500	PS21564-P	
Mini DIP *(New Gen. 4)*	20A / 40A	600V	T.B.D.	T.B.D.	2500	PS21765(1)	Over-temperature Protection
	30A / 60A	600V	T.B.D.	T.B.D.	2500	PS21767(1)	
Super-Mini DIP *(New Gen. 4 Technology)*	3A / 6A	600V	T.B.D.	T.B.D.	2500	PS21961(2)	-A Long (16mm) Pins -S Open-emitters -C Zig-zag Lead Form -W Double Zig Zag -T Over-temperature Protection *(New Option Available Summer 2006)*
	5A / 10A	600V	6.0	6.0	1500	PS21962	
	8A / 16A	600V	9.6	7.4	1500	PS21963-E	
	10A / 20A	600V	11.2	8.1	1500	PS21963	
	15A / 30A	600V	14.0	9.6	1500	PS21964	
	20A / 40A	600V	16.2	11.0	1500	PS21965	
	30A / 60A	600V	T.B.D.	T.B.D.	1500	PS21967(3)	
DIP	20A / 40A	600V	20.0	13.5	2500	PS21265-P(4)	-AP Long (16mm) Pins
	30A / 60A	600V	26.0	17.5	2500	PS21267-P(4)	
	50A / 100A	600V	37.4	23.6	2500	PS21869-P	
DIP 2	20A / 40A	600V	20.0	14.0	2500	PS21065	Open-emitters Standard Package Compatible with 1200V DIP-IPM
	30A / 60A	600V	26.0	16.5	2500	PS21067	
	50A / 100A	600V	34.0	21.0	2500	PS21069	

*$T_j \le 125°C$ and $I_{peak} \le 1.7 * I_C$ are selected according to recommended design margins. The actual device limit is $T_j \le 150°C$, $I_{peak} \le I_{CP}$.

(1) NEW – Available Fall, 2006

(2) NEW – Available Summer, 2006

(3) Under Development – Spring, 2007

(4) NEW – Generation 3.5 replaces generation 3 types (PS21865-P and PS21867-P).

Table 2.2 1200V DIP-IPM Line-up

Package	Nominal / Peak Current IGBT & Free-wheeling Diode		Continuous Sinusoidal Inverter Output Current ($T_{sink} \le 80°C$, $T_j \le 125°C$, $I_{peak} \le 1.7\ I_C$) PF = 0.8V, V_{CC} = 300V (ARMS)*		Isolation Voltage (V_{RMS})	Part Number	Options
	I_C/I_{CP}	Rated Voltage	f_{sw} = 5kHz	f_{sw} = 15kHz			
DIP 2	5A / 10A	1200V	6.0	5.5	2500	PS22052	Open-emitters Standard
	10A / 20A	1200V	11.8	7.5	2500	PS22053	
	15A / 30A	1200V	14.1	8.6	2500	PS22054	
	25A / 50A	1200V	19.3	11.5	2500	PS22056	

*$T_j \le 125°C$ and $I_{peak} \le 1.7 * I_C$ are selected according to recommended design margins. The actual device limit is $T_j \le 150°C$, $I_{peak} \le I_{CP}$.

and single control power supply operation using bootstrap supply techniques.

- P-side (high-side driver) floating supply undervoltage (U_V) lockout.
- N-side (low-side driver) control power supply undervoltage (U_V) lockout with fault signal output.
- Short-circuit (SC) protection using an external shunt resistor in the negative DC link with fault signal output.
- Optional over-temperature protection
- Compact low cost transfer mold packaging allows miniaturization of inverter designs.
- High reliability due to factory tested coordination of HVIC and power chips.

3.0 Electrical Characteristics

The basic electrical characteristics and operation of the DIP-IPM family are covered in this section. More detailed design information can be found in later sections.

3.1 Functional Description

Figure 3.1 shows a general functional diagram for a DIP-IPM along with typical user supplied supporting circuits. All modules in the DIP-IPM family consist of a combination of power chips and custom integrated circuits for gate drive configured in a standard three-phase bridge topology. This circuit configuration is suitable for most three-phase induction and brushless DC motor drives. The internal circuit design and pin-out varies slightly over the range of available modules. However, the basic functions, characteristics and external circuit requirements are the same for all modules in the family. This common functionality helps to minimize the engineering time required to develop a complete family of drives for a range of output power ratings. The only noteworthy variation is the "open-emitter" configuration in which the three lower emitters are pinned out separately rather than being connected within the module as shown in Figure 3.1. This configuration allows the use of separate current shunts for each leg which is useful for some control schemes. The open-emitter configuration is standard on some devices and available as an option on others.

Each DIP-IPM contains the six IGBT/free-wheel diode pairs required for a three-phase motor drive. The IGBT chips utilize the latest fine pattern processes to achieve high efficiency with low switching and conduction losses. All free-wheeling diodes used in the DIP-IPMs are super fast/soft recovery shallow diffused types. These diodes have been carefully

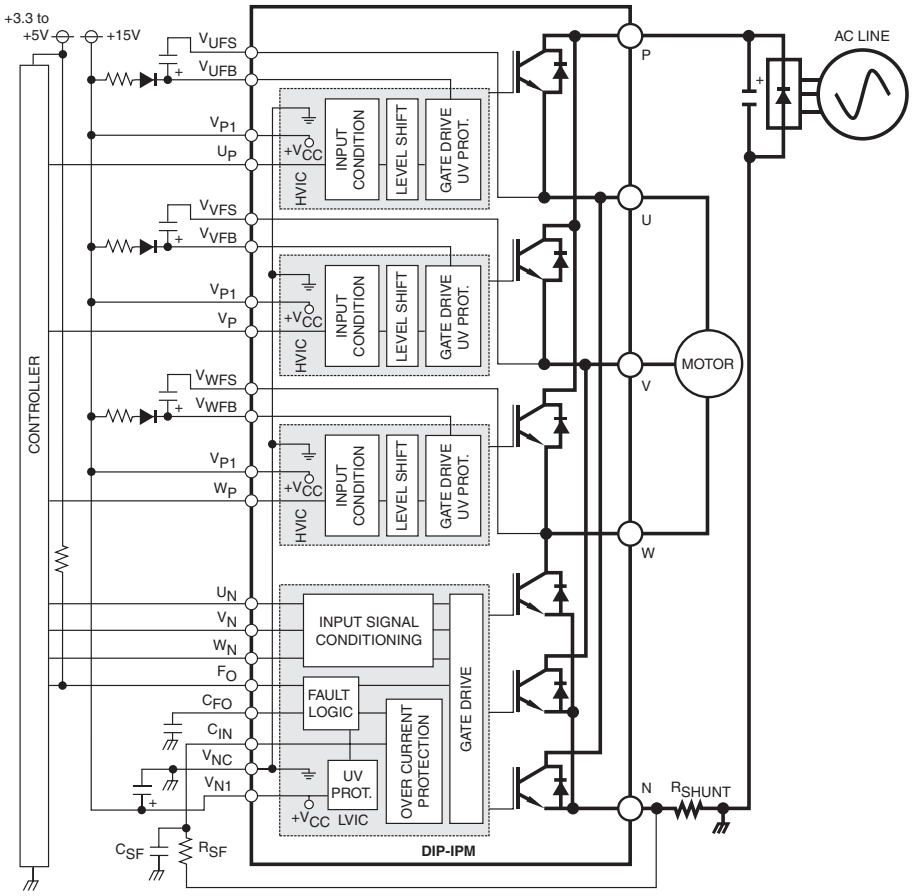


Figure 3.1 DIP-IPM Family Basic Functional Diagram

optimized to have soft recovery characteristics over a wide range of currents in order to minimize EMI/RFI noise. DIP-IPMs are available with blocking voltage ratings of either 600V or 1200V. Normally the 600V devices will be used for applications operating from 100VAC to 240VAC and the 1200V rated devices will be used in applications operating from 360VAC to 480VAC.

The DIP-IPM also includes custom ICs to provide gate drive and protection functions. The built-in gate drive allows direct connection to the logic level signals supplied by the controller. Proprietary HVIC (High Voltage Integrated Circuit) technology is utilized to level shift logic level control signals from the low-side ground reference to the high-side gate drivers.

3.2 High Voltage Level Shift

The DIP-IPMs built-in level shift eliminates the need for optocouplers and allows direct connection of all six control inputs to the CPU/DSP. The detailed operation and timing diagram for the level shift function is shown in Figure 3.2. The falling and rising edges of the P-side control signal (A) activate the one shot pulse logic which generates turn on pulses (B, C) for the high voltage level shifting MOSFETs. Narrow ON pulses are used to minimize the power dissipation within the HVIC. The high voltage MOSFETs pull the input to the high-side driver latch (D, E) low to set and reset the gate drive for the P-side IGBT (F).

3.3 Bootstrap Supply Scheme

Power for the high-side gate drive is normally supplied using external bootstrap circuits. The bootstrap circuit typically consists of a low current fast recovery diode that has a blocking voltage equivalent to the V_{CES} rating of the DIP with a small series resistor to limit the peak charging current and a floating supply reservoir capacitor. In order to avoid transient voltages and oscillations on the floating power supplies it is often desirable to add a low impedance film or ceramic type capacitor in parallel with each floating supply reservoir capacitor. The operation of the bootstrap supply is outlined in Figure 3.3.

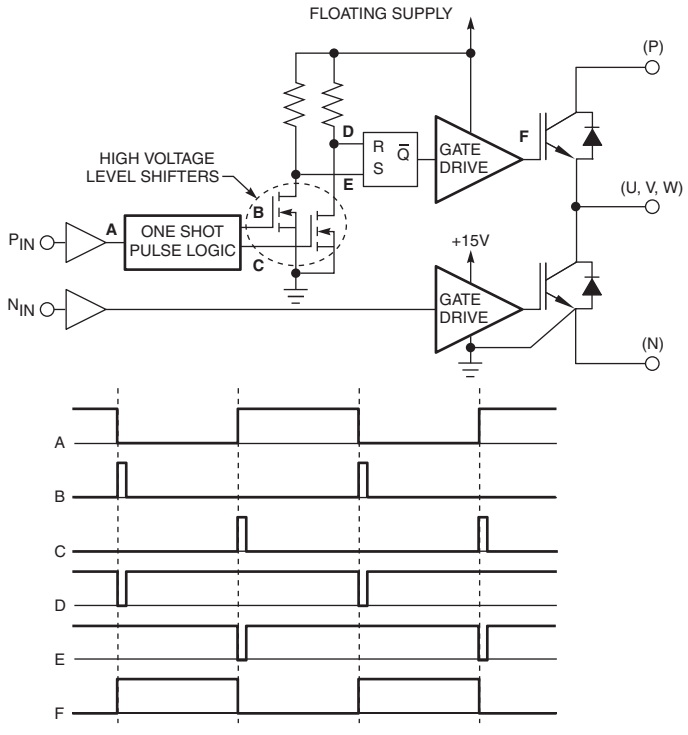


Figure 3.2 High Voltage Level Shift

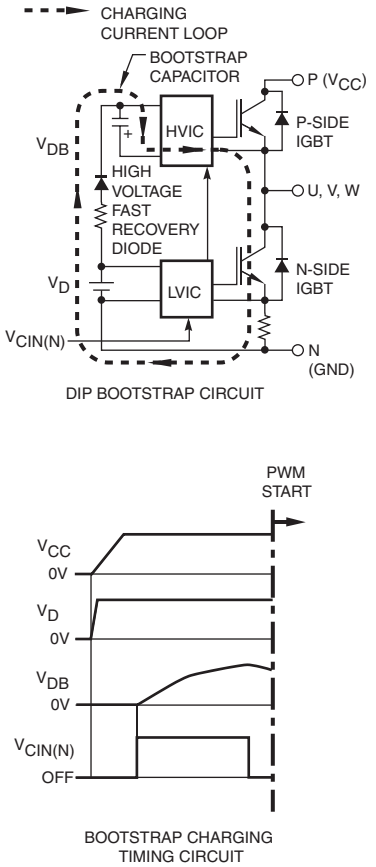


Figure 3.3 Bootstrap Supply Operation

When the lower IGBT is turned on, the floating supply capacitor is charged through the bootstrap diode. When the lower IGBT is off, the energy stored in the capacitor provides power for the high-side gate drive. Using this technique it is possible to operate all six IGBT gate drivers from a single 15V supply. The bootstrap circuit is a very low cost method of providing power for the high-side IGBT gate drive. However, care must be exercised to maintain the high-side supplies when the inverter is idle and during fault handling conditions. This usually means that the low-side IGBTs must be pulsed on periodically even when the inverter is not running. At power up, the bootstrap supplies must be charged before the PWM is started. Normally, this is accomplished by turning on the low-side IGBTs for a period long enough to fully charge the floating supply reservoir capacitor as shown in Figure 3.3. For reference, the charge time is 15ms for a 100uF bootstrap capacitor with a 50Ω resistor.

3.4 Undervoltage Lockout

The DIP-IPM is protected from failure of the 15V control power supply by a built-in undervoltage lockout circuit. If the voltage of the control supply falls below the UV level specified on the data sheet, the low-side IGBTs are turned off and a fault signal is asserted. In addition, the P-side HVIC gate drive circuits have independent undervoltage lockout circuits that turn off the IGBT to protect against failure if the voltage of the floating power supply becomes too low. If the high-side undervoltage lockout protection is activated, then the respective IGBT will be turned off, but a fault signal is not supplied.

3.5 Short-circuit Protection

The DIP-IPM uses the voltage across an external shunt resistor (R_{SHUNT}) inserted in the negative DC bus to monitor the current and provide protection against overload and short-circuit conditions. When the voltage at the C_{IN} pin exceeds the V_{SC} reference level specified on the device data sheet the lower arm IGBTs are turned off and a fault signal is asserted at the FO pin. When an overcurrent or short-circuit condition is detected, the IGBTs remain off until the fault time (t_{FO}) has expired and the input signal has cycled to its OFF state. The duration of t_{FO} for the DIP-IPM is set by an external timing capacitor C_{FO}.

The short-circuit protection function will be discussed in detail in the applications section for DIP-IPMs, specifically in Sections 5.4.2 through 5.4.4. Table 3.1 shows a summary of protection functions.

3.6 Over-temperature Protection

Over-temperature protection is available in the latest generation Mini DIP-IPM and Super-Mini DIP-IPMs. A temperature detection circuit located on the LVIC forces all of the low-side IGBTs off when the OT trip temperature is reached. The low-side IGBTs remain off until the LVIC detects a temperature that has fallen below the OT reset temperature which is typically 10°C below the OT trip temperature. (See Figure 3.4.)

3.7 Fault Output

The DIP-IPMs have a fault signal output for the N-side IGBTs. The fault signal is used to inform the system controller if the protection functions have been activated.

The fault signal output is in an active low open collector configuration. It is normally pulled up to the logic power supply voltage via a pull-up resistor. The resistor should be selected so that the maximum I_{FO} specified on the data sheet is not exceeded. Figure 3.5 shows the voltage at FO as a function of sink current for the DIP and Mini/Super-Mini DIP.

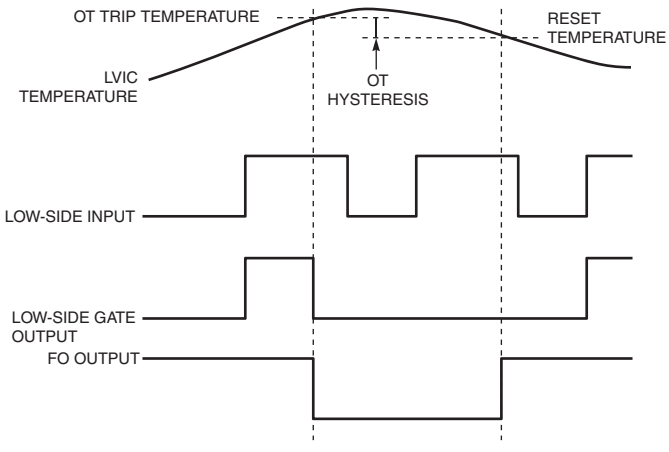


Figure 3.4 Timing Chart for Over-temperature Protection

Table 3.1 Conventional IPM

Function	Symbol	Description
Normal Drive	–	• The control inputs are active high. • $V_{CIN} < V_{th(off)}$ turns the respective IGBT off, and $V_{CIN} > V_{th(on)}$ turns the respective IGBT on.
Short-circuit Protection	SC	• The external shunt resistance detects current in the DC link. When the current exceeds a preset SC trip level, a short-circuit is detected and the N-side IGBTs are turned off immediately. • A fault signal is asserted from the FO terminal. Its duration is specified on the data sheet as t_{FO}. After the FO time expires, normal operation will resume at the next input turn-on signal.
Control Circuit Undervoltage Protection (UV)	UV_D	• Internal logic monitors the N-side control supply voltage. If the voltage falls below the UV_{Dt} trip level, input signals to the N-side IGBTs are blocked and an FO signal is generated. • The fault signal output period is specified on the data sheet as t_{FO}. After the FO time expires and the control supply is above the UV_{Dr} reset level, normal operation will resume at the next on pulse.
	UV_{DB}	• Internal logic monitors the P-side floating voltage supplies. If the voltage level drops below the UV_{DB} trip level, input signals to the P-side IGBTs are blocked. • The UV_{DB} protection is reset when the voltage exceeds the UV_{DBr} reset level. • A fault signal is not generated for the P-side UV state.

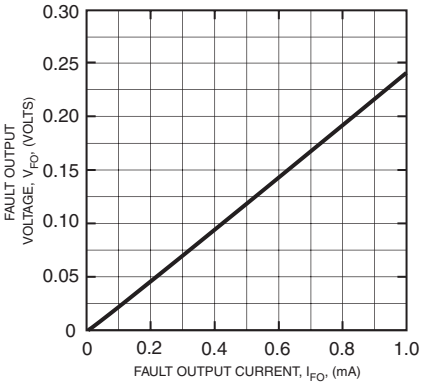


Figure 3.5 1200V DIP, 600V DIP and Mini/Super-Mini DIP Voltage Current Characteristics of F_O Terminal

If the FO terminal is exposed to excessive noise the control IC may trigger a false fault condition. To prevent this, it is recommended to use as low of a pull-up resistor as possible and connect it as close as possible to the DIP-IPM's pins.

When a fault occurs the fault line pulls low and all the gates of the N-side IGBTs are interrupted. If the fault is caused by an N-side SC condition, the output asserts a pulse (t_{FO} specified on the data sheets) and is then automatically reset. In the case of an N-side control supply UV lockout fault, the signal is maintained until the control supply returns to normal.

The internal short-circuit protection function is designed to protect the DIP from non-repetitive abnormal current. Operation of a DIP is guaranteed only within its maximum published ratings. Therefore, the device should not be continuously stressed above its maximum ratings. As soon as a fault output (FO) is given from the module, the system operation should immediately shift to a proper fault clearance mode stopping all operations of the DIP.

3.8 Static Characteristics

Tables 3.2 and 3.3 list the most important static characteristics for 1200V DIP and 600V DIP example types. For the other products, please refer to the individual data sheets.

3.9 Dynamic Characteristics

Tables 3.4 and 3.5 list the key dynamic characteristics for the same examples of the 1200V and 600V DIP. Once again, refer to the data sheets for the other types.

The switching times given on the data sheets as electrical characteristics are for half-bridge inductive load. This reflects the fact that inductive loads are the most prevalent application for DIP-IPMs. Figure 3.6 shows the standard half-bridge test circuits for the DIPs. The switching waveform in Figure 3.7 illustrates how the data sheet parameters are defined.

Figures 3.8, 3.9, and 3.10 are turn-on and turn-off waveforms for the DIP, Mini DIP and Super-Mini DIP. They were measured under the specified conditions and are typical of the devices listed.

Table 3.2 25A/1200V DIP-IPM (PS22056)

Symbol	Parameter	Condition	Rating
V_{CES}	Collector-Emitter Voltage	—	1200V (Max.)
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$V_D = V_{DB} = 15V$, $V_{CIN} = 5V$, $I_C = 25A$, $T_j = 25°C$	3.0V (Typ.)
V_{EC}	FWD Forward Voltage	$-I_C = 25A$, $V_{IN} = 0V$, $T_j = 25°C$	2.0V (Typ.)

Table 3.3 10A/600V Super-Mini DIP-IPM (PS21963)

Symbol	Parameter	Condition	Rating
V_{CES}	Collector-Emitter Voltage	—	600V (Max.)
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$V_D = V_{DB} = 15V$, $V_{CIN} = 5V$, $I_C = 10A$, $T_j = 25°C$	1.7V (Typ.)
V_{EC}	FWD Forward Voltage	$-I_C = 10A$, $V_{CIN} = 0V$, $T_j = 25°C$	1.7V (Typ.)

Table 3.4 25A/1200V DIP-IPM (PS22056)

Symbol	Parameter	Condition	Rating
t_{on}/t_{off}	Switching Times	$V_{CC} = 600V$, $V_D = 15V$, $I_C = 25A$, $T_j = 125°C$, $V_{CIN} = 0 \leftrightarrow 5V$	1.5/2.0μs (Typ.)
$t_{c(on)}/t_{c(off)}$	Switching Times	$V_{CC} = 600V$, $V_D = 15V$, $I_C = 25A$, $T_j = 125°C$, $V_{CIN} = 0 \leftrightarrow 5V$	0.4/0.4μs (Typ.)
$E_{sw(on)}/E_{sw(off)}$	Switching Losses	$V_{CC} = 600V$, $V_D = 15V$, $I_C = 25A$, $T_j = 125°C$, $V_{CIN} = 0 \leftrightarrow 5V$	3.75/2.75 mJ/pulse (Typ.)

Table 3.5 10A/600V Super-Mini DIP-IPM (PS21963)

Symbol	Parameter	Condition	Rating
t_{on}/t_{off}	Switching Times	$V_{CC} = 300V$, $V_D = 15V$, $I_C = 10A$, $T_j = 125°C$, $V_{CIN} = 0 \leftrightarrow 5V$	1.1/1.5 μs (Typ.)
$t_{c(on)}/t_{c(off)}$	Switching Times	$V_{CC} = 300V$, $V_D = 15V$, $I_C = 10A$, $T_j = 125°C$, $V_{CIN} = 0 \leftrightarrow 5V$	0.4/0.5 μs (Typ.)
$E_{sw(on)}/E_{sw(off)}$	Switching Losses	$V_{CC} = 300V$, $V_D = 15V$, $I_C = 10A$, $T_j = 125°C$, $V_{CIN} = 0 \leftrightarrow 5V$	0.63/0.58 mJ/pulse (Typ.)

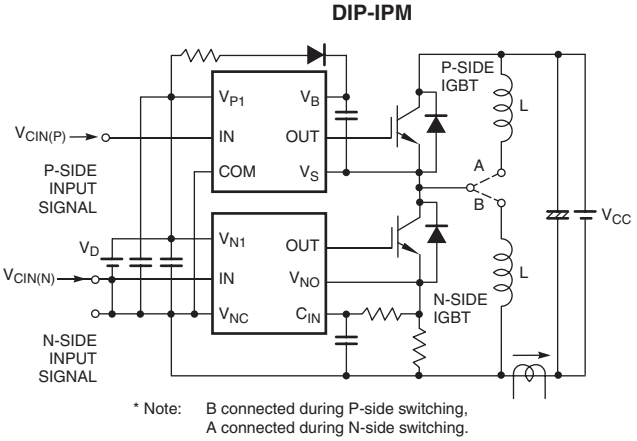


Figure 3.6 Half-bridge Evaluation Circuit Diagrams (Inductive Load)

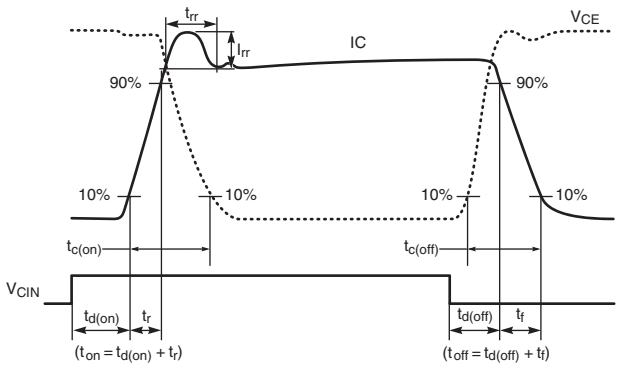


Figure 3.7 Switching Test Time Waveforms

3.10 Voltage Ratings

Recommended maximum operating voltages for the DIP-IPMs are specified on the device data sheets. V_{CC} is the maximum P-N voltage in the static (not switching) state. A braking circuit should be activated if the P-N voltage exceeds this specification. $V_{CC(surge)}$ is the maximum P-N surge voltage in the static state. A snubber circuit is necessary if the P-N voltage exceeds $V_{CC(surge)}$. V_{CES} is the maximum sustainable collector-emitter voltage of the IGBT. $V_{CC(prot)}$ is the maximum DC bus voltage for which the IGBT is guaranteed to turn off safely in the case of a short-circuit. The IGBT may be damaged if the bus voltage exceeds this specification.

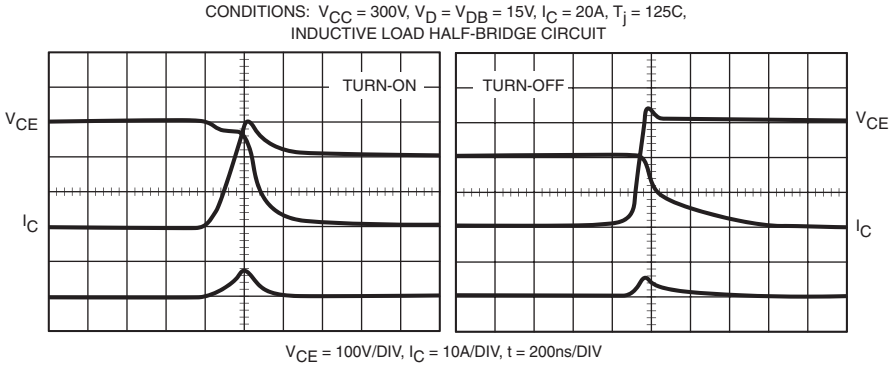


Figure 3.8 Typical Switching Waveform of DIP PS21865 (20A/600V) N-side

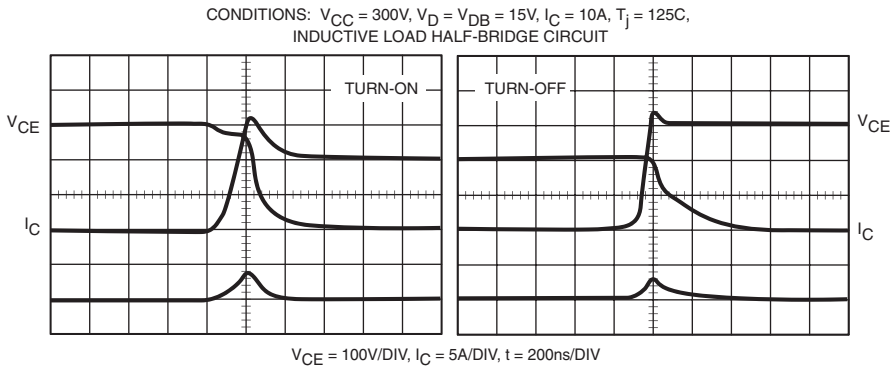


Figure 3.9 Typical Switching Waveform of Mini DIP PS215635 (10A/600V) N-side

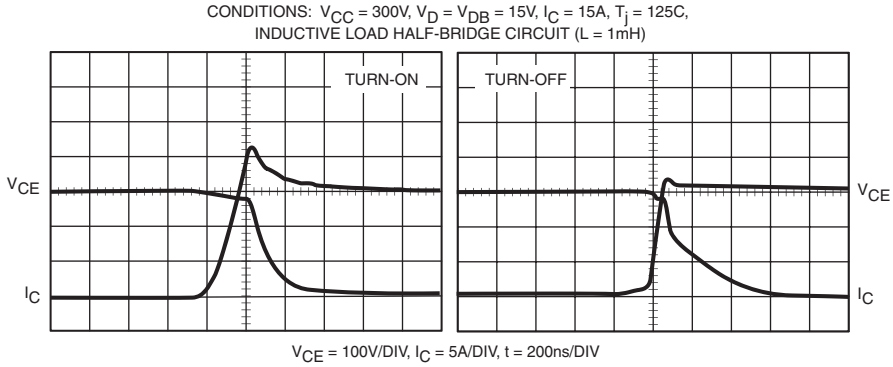


Figure 3.10 Typical Switching Waveform of Super-Mini DIP PS21964 (15A/600V)

4.0 Package

The DIP-IPMs employ a revolutionary, low cost, rugged, transfer molded package developed by Mitsubishi for small motor control applications. The packages have been optimized for small size and highly automated mass production.

4.1 DIP 2 and DIP Generation 3.5 Cross-section

A cross-section diagram of the DIP 2 and DIP Generation 3.5 package is shown in Figure 4.1. First, bare power chips are assembled on a lead frame along with custom HVIC and LVIC die. Ultrasonic bonding of large diameter aluminum wires makes electrical connections between the power chips and lead frame. Small diameter gold wires are bonded to make the signal level connections between the IC die and lead frame. The lead frame along with the connected power chips, ICs and bond wires are then encapsulated in the first of the injection mold process. Then an Al heatsink is joined to the epoxy

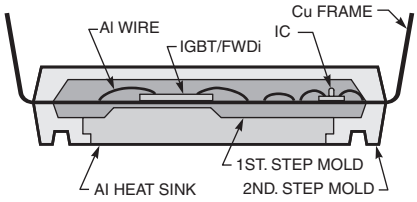


Figure 4.1 DIP 2 and DIP Generation 3.5 Cross-section

mold, with a thin separation so that it is close to the power chips, to provide good heat transfer. A second injection mold process is then made to encapsulate the entire device along with the heatsink.

4.2 DIP Generation 3 Cross-section

A cross-section diagram of the DIP Generation 3 package is shown in Figure 4.2. The device is fabricated using a transfer mold process like a large integrated circuit. First, bare power chips are assembled on a lead frame along with custom HVIC and LVIC die. Ultrasonic bonding of large diameter aluminum wires makes electrical connections between the power chips and lead frame. Small diameter gold wires are bonded to make the signal level connections between the IC die and lead frame. The device is then encapsulated using a single step injection mold process. A copper block is attached to the lead frame underneath the power chips for heat spreading. A thin layer of thermally conductive epoxy is formed between the copper block and heatsink mounting surface. It allows good heat transfer and provides 2500VRMS electrical isolation. The injection mold process encapsulates the entire lead frame assembly to achieve the final form. Compared to conventional hybrid modules this process eliminates the IMS (Insulated Metal Substrate) or ceramic substrate and plastic shell package thereby substantially reducing cost. The transfer mold process is also well suited for high volume, automated mass production. The superior thermal performance achieved using this process allows fabrication of modules with IGBT ratings of 20A or more at elevated case temperatures. This performance is comparable to assemblies utilizing discrete TO-247 style co packaged (containing both IGBT and free-wheel diode chips) devices.

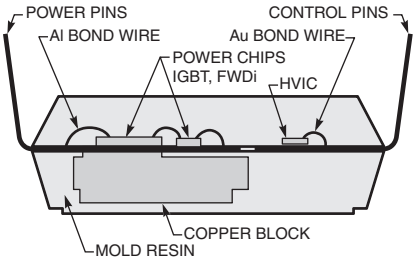


Figure 4.2 DIP Generation 3 Cross-section

4.3 Mini DIP-IPM Cross-section

The Mini DIP-IPM was developed to provide reduced cost and smaller size for low power applications that would normally utilize TO-220 style discrete co packaged IGBTs. A cross-sectional diagram of the Mini DIP-IPM is shown in Figure 4.3. Like the larger DIP-IPM, the Mini DIP-IPM is fabricated using a transfer mold process like large integrated circuits. First, bare power chips are assembled on a lead frame along with custom IC die. Ultrasonic bonding using large diameter aluminum wires makes electrical connections between the power chips and the lead frame. Small diameter gold wires are bonded to make the signal level connections between the IC die and lead frame. The device is then encapsulated using a single step injection mold process. The lead frame is formed to produce a thin, flat, layer of thermally conductive epoxy at the heatsink mounting surface of the device. This thin layer of epoxy allows good heat transfer and provides 2500VRMS electrical isolation. This process encapsulates the entire lead frame assembly to achieve the final form. Compared to conventional hybrid modules this process eliminates the IMS (Insulated Metal Substrate) or ceramic substrate and plastic shell package thereby substantially reducing cost. The single step transfer mold process allows simplified, high volume, automated mass production. The packages shown have been utilized to fabricate modules with IGBT ratings of 5A to 15A at elevated case temperatures. This performance is comparable to assemblies utilizing discrete TO-220 style co packaged devices.

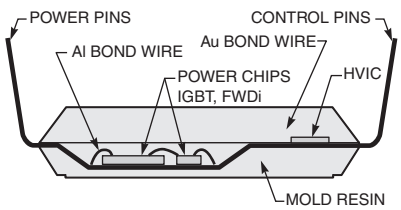


Figure 4.3 Mini DIP-IPM Cross-section

4.4 Super-Mini DIP-IPM Cross-section

The Super-Mini DIP-IPM was developed to provide an ultra-small size with enhanced thermal transfer for low power applications. A cross-sectional diagram of the Super-Mini DIP-IPM is shown in Figure 4.4. First, bare power chips are assembled on a lead frame along with custom IC die. Ultrasonic bonding using large diameter aluminum wires makes electrical connections between the power chips and the lead frame. Small diameter gold wires are bonded to make the signal level connections between the IC die and lead frame. A thermal conductive, electrical isolating sheet is then placed be-

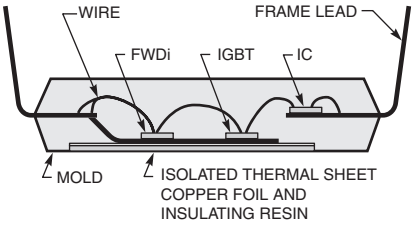


Figure 4.4 Super-Mini DIP-IPM Cross-section

tween the lead frame and a panel of copper foil. The device is then encapsulated using a single step injection mold process leaving the copper foil exposed. This copper foil provides excellent thermal dissipation and the thin layer of isolation material provides 1500VRMS electrical isolation. This process encapsulates the entire lead frame assembly to achieve the final form. The Super-Mini DIP has ratings of 3A to 30A at elevated case temperatures. This performance is comparable to assemblies utilizing discrete TO-220 style co packaged devices.

4.5 Pin Names and Functions

The pin names and functions for the line of DIP-IPMs are described in Table 4.1.

Table 4.1 Detailed Description of the DIP-IPM Input and Output Pin Functions

Item	Symbol	Description
P-side Drive Supply Terminal P-side Drive Supply GND Terminal	V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS} or U(V_{UFB})-V_{UFS}, V(V_{VFB})-V_{VFS}, W(V_{WFB})-V_{WFS}	• These are the drive supply terminals for the P-side IGBTs. • By using bootstrap circuits, no external power supplies are required for the DIP-IPM P-side IGBTs. • Each bootstrap capacitor is charged from the N-side V_D supply during ON state of the corresponding N-IGBT in the loop. • Abnormal operation may result if this supply is not properly filtered or has insufficient current capability. In order to prevent malfunction, this supply should be well filtered with a low impedance electrolytic capacitor and a good high frequency decoupling capacitor connected right at the DIP-IPMs pins. • Insert a zener diode (24V/1W) between each pair of control supply terminals to help prevent surge destruction.
Control Supply Terminals	V_{P1}* V_{N1}	• These are the control supply terminals for the built-in ICs. * V_{P1} is only on the 1200V DIP, 600V DIP and Mini DIP. • All V_{P1} and V_{N1} terminals should be connected to the external 15V supply. • In order to prevent malfunction caused by noise and ripple in the supply voltage, this supply should be well filtered with a good high frequency decoupling capacitor connected right at the DIP's pins. • Insert a zener diode (24V/1W) between each pair of control supply terminals to help prevent surge destruction.
P-side Control GND Terminal * N-side control GND Terminal	V_{PC}* V_{NC}	• These are control grounds for the built-in ICs. • V_{PC} and V_{NC} should be connected externally. * The V_{PC} pin is only on the 1200V and 600V DIP-IPM. The Mini/Super-Mini DIP-IPM P-side grounds are connected internally.
Control Input Terminal	U_P, V_P, W_P U_N, V_N, W_N	• Input terminals for controlling the DIP switching operation. • Operate by voltage input signals. These terminals are internally connected to a Schmitt trigger circuit composed of 5V class CMOS. • Each DIP-IPM signal line is pulled down to GND inside the device, therefore an external resistor is not needed. • The wiring of each input should be as short as possible (~2cm) to protect the DIP against noise. • An RC filter is recommended to prevent signal oscillations.
Short-circuit Trip Voltage Sensing Terminal	C_{IN}	• The signal from the current sensing resistance should be connected between this terminal and V_{NC} to detect short circuit. • Impedance for C_{IN} terminal is approximately 600kW. • An RC filter should be connected in order to eliminate noise.

Table 4.1 Detailed Description of the DIP-IPM Input and Output Pin Functions (Continued)

Item	Symbol	Description
Fault Output Terminal	FO	• This is the fault output terminal. A fault condition produces an active low output at this terminal (SC and UV operation at N-side). • This output is open collector. The FO signal line should be pulled up to the power supply with a resistor.
Fault Pulse Output Time Setting Terminal	C_{FO}	• This is the terminal for setting the fault output duration. • An external capacitor should be connected between this terminal and V_{NC} to set the fault pulse output time on the DIP and Mini DIP.
Inverter Positive Power Supply Terminal	P	• DC link positive power supply terminal of the inverter. • Internally connected to the collectors of the P-side IGBTs. • In order to suppress surge voltage caused by DC link wiring or PCB pattern inductance, connect the main filter capacitor as close as possible to the P and N terminals. It is also effective to add a small film capacitor with good high frequency characteristics.
Inverter GND Terminal	N*	• DC link negative power supply terminal of the inverter. • This terminal is connected to the emitters of the N-side IGBTs. *N_U, N_V and N_W are used with open emitter type DIPs
Inverter Power Output Terminal	U, V, W	• Inverter output terminals for connection to inverter load (AC motor) • Each terminal is internally connected to the center point of the corresponding IGBT half-bridge arm.
Low Side Output Stage Common	V_{NO}*	• It should be connected to the N terminal externally for these devices. * The V_{NO} pin is only used on Mini DIPs PS21562 and PS21563.

4.6 Installation Guidelines

When mounting a module to a heatsink, it is essential to avoid uneven mounting stress that may cause the device to be damaged or degraded. The mounting stress, heatsink flatness and thermal interface must therefore be considered carefully.

It is important to avoid uneven or excessive tightening stress. Figure 4.5 shows the recommended torque order for mounting screws. Use a torque wrench to tighten the screws. The maximum torque specifications are provided in Tables 4.2, 4.3 and 4.4.

When selecting a heatsink for the 1200V DIP-IPM it is important to ensure that the required creepage and strike distance, outlined

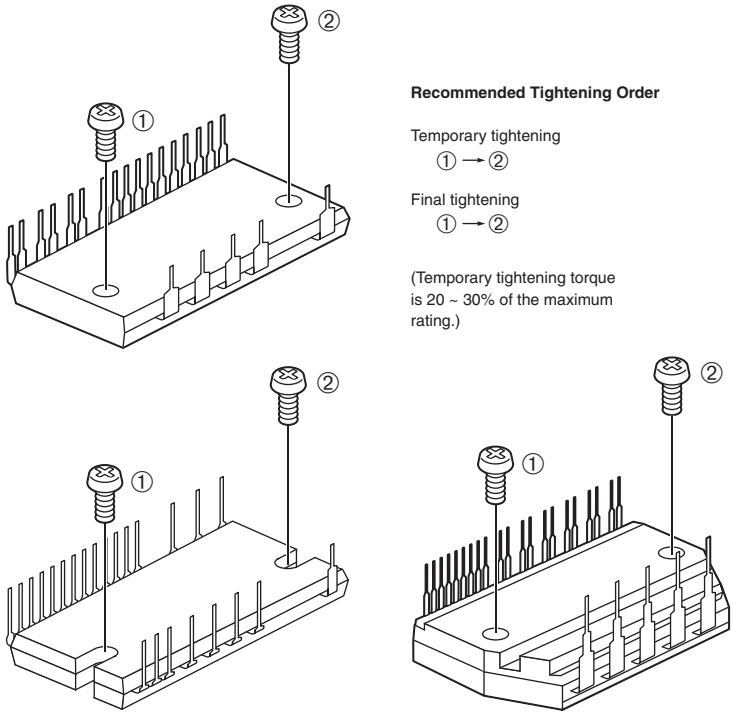


Figure 4.5 Recommended Torque Order for Mounting Screws

in Table 4.5, between the DIP-IPM terminals and the heatsink are met. This is done by mounting the heatsink to the DIP-IPM along the uniquely designed slot as shown in Figure 4.6. The data shown in Table 4.5 are appropriate when the DIP-IPM is mounted to a 6.8mm stepped heatsink similar to what is shown in the figure.

Heatsink flatness requirements are also listed in these tables. The flatness is measured as prescribed in Figure 4.7, which depicts the devices' footprint on the heatsink. The flatness of the heatsink underneath the module should be measured along the line shown in the figure.

The heatsink should have a surface finish of 64 micro-inches or less. Use a uniform 4 mil to 8 mil coating of thermal interface compound. Select a compound that has stable characteristics over the whole operating temperature range and does not change its properties over the life of the equipment. See Table 4.6 for suggested types.

Table 4.2 Mounting Torque and Heatsink Flatness Specification for 1200V and 600V DIP-IPM

Item	Condition		Ratings			
			Min.	Typ.	Max.	Unit
Mounting Torque	Mounting Screw: M4	Recommended 10.4 in-lb	8.67	10.4	13	in-lb
		Recommended 1.18 N•m	0.98	1.18	1.47	N•m
Heatsink Flatness	—		-0.50	—	+100	µm

Table 4.3 Mounting Torque and Heatsink Flatness Specification for Mini DIP-IPM

Item	Condition		Ratings			
			Min.	Typ.	Max.	Unit
Mounting Torque	Mounting Screw: M3	Recommended 6.9 in-lb	5.22	6.9	8.7	in-lb
		Recommended 0.78 N•m	0.59	0.78	0.98	N•m
Heatsink Flatness	—		-0.50	—	+100	µm

Table 4.4 Mounting Torque and Heatsink Flatness Specification for Super-Mini DIP-IPM

Item	Condition		Ratings			
			Min.	Typ.	Max.	Unit
Mounting Torque	Mounting Screw: M3	Recommended 6.0 in-lb	5.2	6.1	6.9	in-lb
		Recommended 0.69 N•m	0.59	0.69	0.78	N•m
Heatsink Flatness	—		-0.50	—	+100	µm

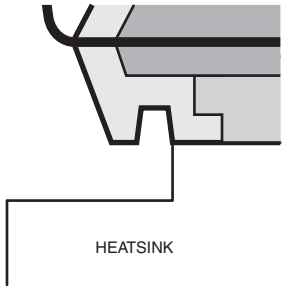


Figure 4.6 Standard Satisfaction Mounting Method for Meeting Clearance Standards

Table 4.5 Isolation Distance of DIP-IPM

Standard	Clearance (mm)		Creepage Distance (mm)	
UL 508 Table 34.1-A Rating Voltage: 301V ~ 600V	9.5		12.7	
	DIP-IPM		DIP-IPM	
	Between Power Terminals	7.16	Between Power Terminals	7.16
	Between Control Terminals	5.16	Between Control Terminals	5.16
	Between Terminals and Fin	4 (10.8)	Between Terminals and Fin	(12.7)

Table 4.6 Heatsink Compounds

Manufacturer	Type
Shinetsu Silicon	G746
Dow Corning	DC340

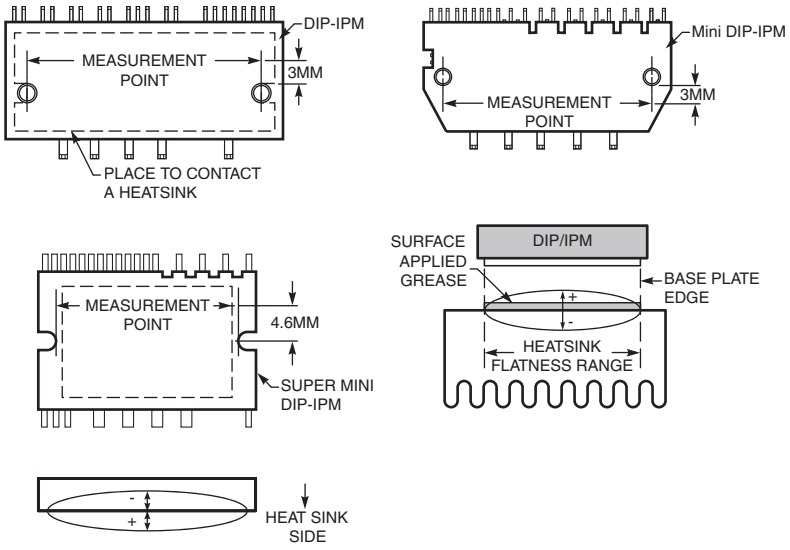


Figure 4.7 Measurement Point for Heatsink

5.0 Application Guidelines

DIP-IPMs and Mini/Super-Mini DIP-IPMs are based on advanced low loss IGBT and free-wheel diode technologies. The application issues and general guidelines are essentially the same for all product groups. The information presented in this section is intended to help users of DIP-IPMs apply the devices effectively and reliably.

5.1 System Connection Diagram

Figure 5.1 shows a typical system connection diagram for a DIP-IPM and Mini/Super-Mini DIP. Component selection information and relevant notes are included in Figure 5.1.

5.2 Control Power Supplies Design

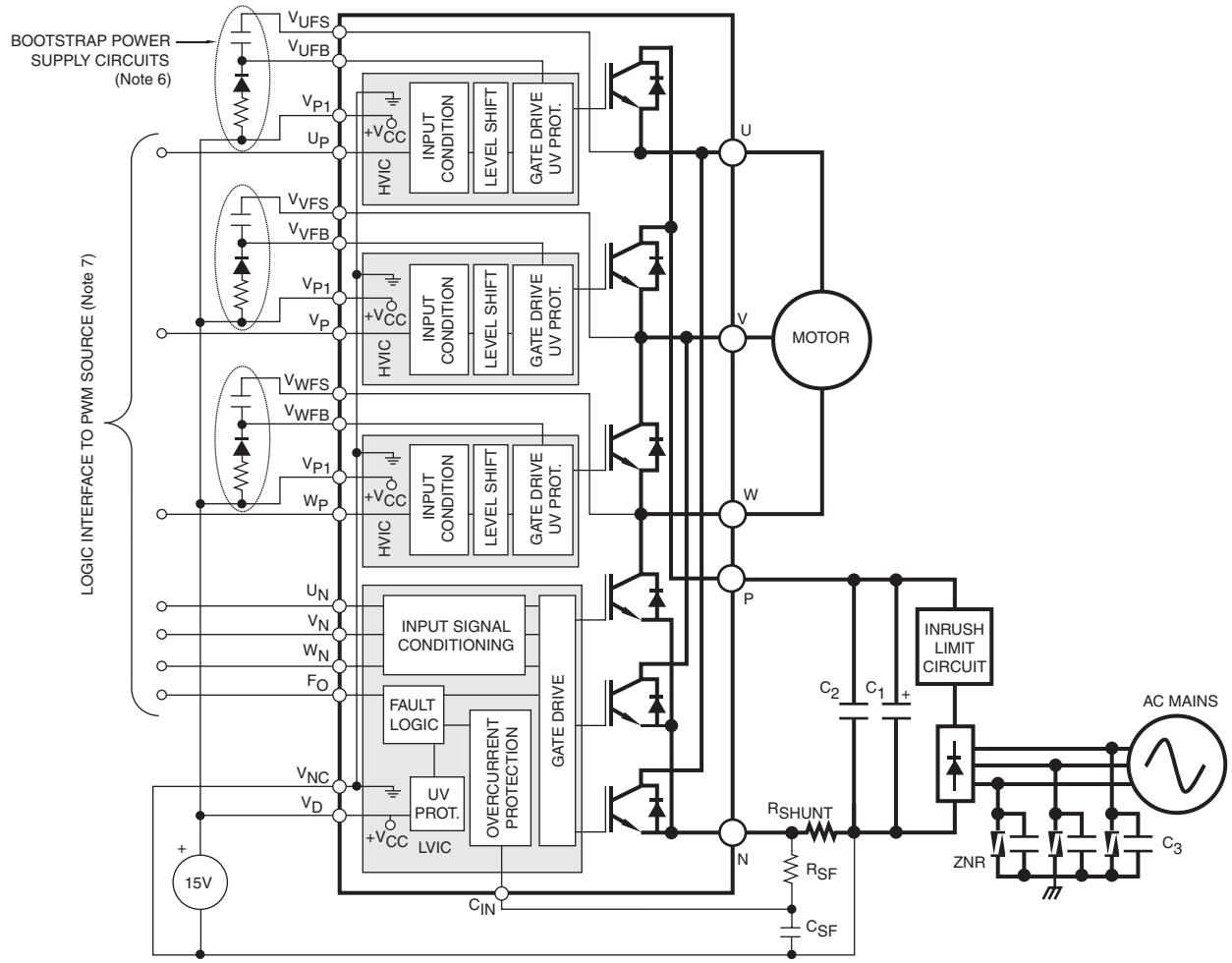
In most applications the DIP-IPMs built-in gate drive, level shifting and protection functions will be powered from a single 15V source. To do this, four additional low voltage control power supplies must be created. The main 15V source (V_D) supplies power directly to the low-side IGBT gate drivers and protection circuits. The common reference of the V_D supply is essentially at the negative DC bus. This is also the common reference for all of the DIP-IPM's logic level control input signals. A 3.3V or 5V logic power supply is used to provide power for the PWM controller. In the case of the 1200V DIP-IPM 5V or 15V logic must be used. Three floating 15V power supplies (V_{DB}) for the high-side gate drivers can be developed using external bootstrap circuits. The following sub-sections describe the detailed operation and timing requirements for all of these control power supplies.

5.2.1 Main Control Power Supply (V_D)

Control and gate drive power for the DIP-IPM is normally provided by a single 15VDC supply that is connected at the modules V_{N1} and V_{NC} terminals. For proper operation this voltage should be regulated to 15V ±10%. Table 5.1 describes the behavior of the DIP-IPM for various control supply voltages. This control supply should be well filtered with a low impedance electrolytic capacitor and a high frequency decoupling capacitor connected as close as possible to the DIP-IPM's pins. High frequency noise on the supply may cause the internal control IC to malfunction and generate erroneous fault signals. To avoid these problems, the maximum ripple on the supply should be less than 2V peak-to-peak and the maximum dV/dt should be less than ±1V/µs. In addition, it may be necessary to connect a 24V, 1W zener diode across the supply to prevent surge destruction.

The positive side of the main control supply is also connected to the DIP and Mini DIP modules three V_{P1} terminals to provide power for the low voltage side of the HVICs. On the DIP-IPM package another connection is required from the negative side of the control power supply to module's V_{PC} terminal. This connection provides the ground reference for the low voltage side of the three internal HVICs. In the Mini DIP and Super-Mini DIP packages this connection is not required because it is made internally.

The control circuit ground reference is normally established at the upstream side of the current sensing resistor in the negative DC bus. This means that the voltage at the module's V_{PC} terminal is



Component Selection:

Dsgn.	Typ. Value	Description
R_{SHUNT}	5-100m ohm	Current sensing resistor – Non-inductive, temperature stable, tight tolerance (Note 3)
R_{SF}	1.8k ohm	Short-circuit detection filter resistor (Note 4, note 5)
C_{SF}	1000pF	Short-circuit detection filter capacitor – Multilayer ceramic (Note 4, Note 5)
C_1	200-2000µF, 450V	Main DC bus filter capacitor – Electrolytic, long life, high ripple current, 105°C
C_2	0.1-0.22µF, 450V	Surge voltage suppression capacitor – Polyester/polypropylene film (Note 1)
C_3	2.2-6.5nF	Common mode noise suppression filter – Polyester/polypropylene film (Note 2)
ZNR	Line Voltage	Transient voltage suppressor – MOV (Metal Oxide Varistor)

Notes:

1) The length of the DC link wiring between C1, C2, the DIP's P-terminal and the shunt must be minimized to prevent excessive transient voltages. In particular, C2 should be mounted as close to the DIP as possible.
2) Common mode noise (dV/dt) suppression capacitors are recommended to prevent malfunction of DIP's internal circuits.
3) Use high quality, tight tolerance current sensing resistor. Connect resistor as close as possible to the DIP's N-terminal. Be careful to check for proper power rating. See text for calculation of resistance value.
4) Wiring length associated with R_{SHUNT}, R_{SF}, C_{SF} and the C_{IN} terminal of the DIP must be minimized to avoid improper operation of the SC function.
5) R_{SF}, C_{SF} set short-circuit protection trip time. Recommended time constraints is 1.5µs-2.0 s. See text for details.
6) Bootstrap circuits provide floating power supplies for high side gate drivers. Component values must be adjusted depending on the PWM frequency and technique. See text and interface circuit diagrams for details.
7) Logic level control signal interface to PWM controller. See interface circuit diagram and text for details.

Figure 5.1 DIP-IPM System Connection Diagram

Table 5.1 DIP-IPM Functions vs Control Power Supply Voltage

Main Control Power Supply Voltage (V_D)	DIP-IPM State
0V ~ 4V	Control IC does not function. Undervoltage lockout and fault output do not operate. dV/dt noise on the main P-N supply may trigger the IGBTs.
4V ~ 12.5V	Control IC starts to function. Undervoltage lockout activates, control input signals are blocked and a fault signal is generated.
12.5V ~ 13.5V	Undervoltage lockout is reset. IGBTs will turn on when control inputs are pulled low. Driving voltage is below the recommended range so $V_{CE(sat)}$ and switching losses will be larger than normal.
13.5V ~ 16.5V	**Normal Operation. This is the recommended operating range.**
16.5 ~ 20V	IGBT switching remains enabled. Driving voltage is above the recommended range. Faster switching of the IGBTs will cause increased system noise. Peak short-circuit current may be too large for proper operation of the overcurrent protection.
20V+	Control circuit in DIP-IPM may be damaged.

different from that at the N power terminal by the drop across the sensing resistor. It is very important that all control circuits and power supplies be referenced to this point and not to the N terminal. If circuits are improperly connected the additional current flowing through the sense resistor may cause improper operation of the short-circuit protection function. In general, it is best practice to make the common reference at V_{NC} a ground plane in the printed circuit layout.

The main control power supply is also connected to the bootstrap circuits that are used to establish the floating supplies for the high-side gate drivers. The bootstrap supply operation will be discussed in more detail in Sections 5.2.4 through 5.2.7.

5.2.2 The Logic Power Supply

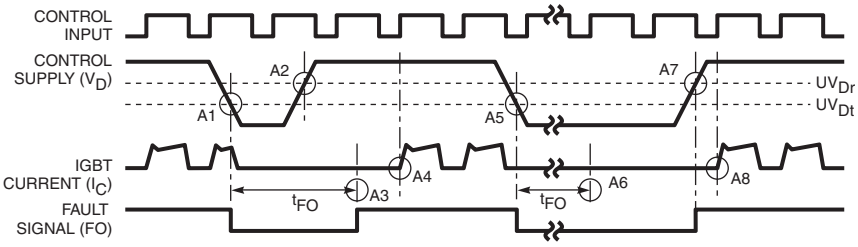
The 600V DIP-IPM's active high control inputs require 3.3V or 5V logic level signals to provide ON and OFF commands for the six internal IGBTs. The 1200V DIP-IPMs can only accept 5V active high logic for control signals. The configuration of these inputs is described in more detail in Section 5.3. The inputs are even suitable for operation at 15V. A logic power supply referenced to the same common as the main control power supply is required to provide power for the controller in applications where the inputs are directly connected. In optically coupled interface applications the supply is still required to provide logic level signals for the control inputs.

5.2.3 Main Control Power Supply Undervoltage Lockout

The ICs that provide short-circuit protection and gate drive for the three low-side IGBTs in the DIP-IPM have an undervoltage lockout function to protect the IGBTs from insufficient driving voltage if the main control power supply voltage is too low. A timing diagram for this protection is shown in Figure 5.2. If the main control power supply (V_D) drops below the undervoltage trip level (UV_{Dt}) specified on the DIP-IPM's data sheet, gate drive for the three low-side IGBTs is inhibited and a fault output signal is asserted. The minimum duration of the fault signal is specified on the device's data sheet. The undervoltage lockout includes hysteresis and a 10µs trip delay to prevent oscillations and nuisance tripping. In order to clear the fault, V_D must exceed the undervoltage reset level (UV_{Dr}) specified on the data sheet and the fault timer must expire. Once the fault is cleared normal switching will resume at the next on-going transition of the control input signal.

5.2.4 Bootstrap Power Supplies (V_{DB})

In most applications floating power supplies for the high-side gate drivers will be generated from the main control power supply using external bootstrap circuits. A typical bootstrap circuit is shown in Figure 5.3. When the low-side IGBT (IGBT2) is turned on, current flows from the low-side control power supply (V_D) through the diode D and inrush-limiting resistor (R_{BS}) to charge the high-side reservoir capacitor (C_{BS}). C_{BS} then supplies power



A1: Control supply falls below UV_{Dt} level, IGBT switching is stopped, fault signal is asserted.
A2: Control supply exceeds UV_{Dr} level but no action is initiated because t_{FO} has not expired.
A3: t_{FO} timer expires and fault signal is cleared.
A4: Switching of IGBT resumes at the first on going transition after the fault signal is cleared.
A5: Control supply falls below UV_{Dt}, the IGBT switching is stopped and a fault signal is asserted.
A6: t_{FO} timer expires but no action is initiated because the control supply is still below the UV_{Dr} level.
A7: The control supply exceeds the UV_{Dr} level and the fault signal is cleared.
A8: Switching of the IGBT resumes at the first on going transition after the fault signal is cleared.

Figure 5.2 Main Control Power Supply (V_D) Undervoltage Lockout Timing Diagram

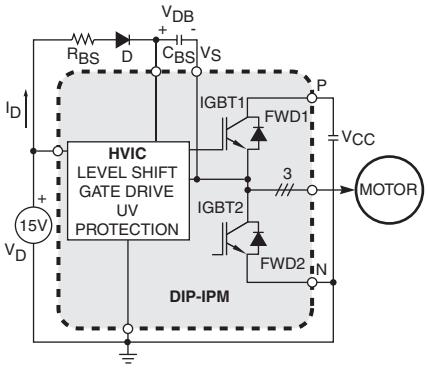


Figure 5.3 Bootstrap Circuit

for the high-side gate drive while IGBT2 is off. The inrush-limiting resistor is included to prevent the bootstrap charging current pulses from producing excessive ripple on the control power supply. The bootstrap diode is required to block the full DC bus voltage when IGBT2 is off. To do this, a device with a reverse blocking voltage rating (V_{rrm}) equal to or greater than the IGBT's V_{CES} rating should be used. The diode (D) must also be an ultra fast recovery type in order to prevent reverse recovery surge voltages and noise on the control power supply. The bootstrap supply reservoir capacitor must be sized so that sufficient voltage is maintained on the high-side gate driver during the OFF time of IGBT2. Some guidelines for selecting this capacitor will be provided in the following sections.

High frequency noise on the supply may cause the internal control IC to malfunction. To avoid these problems, the maximum ripple on the supply should be less than 2V peak-to-peak and the maximum dV/dt should be less than ±1V/µs.

In addition, it may be necessary to connect a 24V, 1W zener diode across the supply to prevent surge destruction.

5.2.5 Bootstrap Power Supply Timing Diagrams

There are two conditions under which the bootstrap reservoir capacitor will charge. The first condition (Case 1) is when the low-side IGBT (IGBT 2) is on. When IGBT2 first turns on, the voltage ON C_{BS} (V_{DB}) is given by:

$$V_{DB(1)} = V_D - V_F - V_{CE(sat)2} - I_D \times R_{BS}$$
(Dynamic Condition)

where:
$V_{DB(1)}$ = bootstrap supply voltage (Case 1)
V_D = main control supply voltage
V_F = forward voltage drop across D at I_D
$V_{CE(sat)2}$ = saturation voltage of IGBT2
I_D = bootstrap supply charging current
R_{BS} = inrush limiting resistor

As the voltage on the bootstrap reservoir capacitor increases the charging current decreases and the steady state voltage V_{DB} becomes nearly equal to the main control supply voltage V_D.

$$V_{DB} = V_D \text{ (Steady State)}$$

When IGBT2 is first turned off there will be a dead time during which neither IGBT1 or IGBT2 is on. The inductive load (motor) will force forward current through FWD1 bringing the voltage at V_S to nearly the positive DC bus voltage (V_{CC}). The bootstrap diode D becomes reverse biased cutting off the flow of bootstrap charging current (I_D). This sequence of events is shown in the timing diagram Figure 5.4. During the ON time of IGBT1 the bootstrap supply voltage (V_{DB}) gradually declines as the current consumed in the HVIC gate drive circuit discharges the reservoir capacitor.

The second condition under which the bootstrap supply capacitor will charge is when FWD2 is conducting (Case 2). This mode is illustrated in the timing diagram shown in Figure 5.5. In this case IGBT1 is being turned on and off while IGBT2 is always off. During the time when both IGBT1 and IGBT2

are off the inductive load (motor) current will circulate through FWD2. When this happens the voltage at V_S becomes nearly equal to the negative bus voltage and D becomes forward biased allowing bootstrap charging current I_D to flow from the main control power supply. The I_D will begin recharging the bootstrap supply reservoir capacitor C. For this case the bootstrap supply voltage ($V_{DB(2)}$) is specified by:

$$V_{DB(2)} = V_D - V_F + V_{EC2}$$

where:

$V_{DB(2)}$ = bootstrap supply voltage (Case 2)

V_D = main control supply voltage

V_F = forward voltage drop across D at I_D

V_{EC2} = forward voltage drop across FWD2

When IGBT1 is on, the voltage at V_S becomes nearly equal to the positive DC link voltage thereby reverse biasing D and stopping the flow of charging current (I_D). The bootstrap supply voltage (V_{DB}) then begins to gradually decline as the current consumed by the HVIC gate drive circuit discharges the reservoir capacitor.

5.2.6 Selecting the Bootstrap Reservoir Capacitor, Resistor and Diode

For the charging sequence shown in Case 1 the required bootstrap reservoir capacitance depends on the operating frequency, the maximum ON time of IGBT1 and the quiescent current consumption of the HVIC gate driver. In order to have a stable bootstrap supply voltage the charge lost during the ON time of IGBT1 must be replaced during the ON time of IGBT2. By assuming conservation of charge

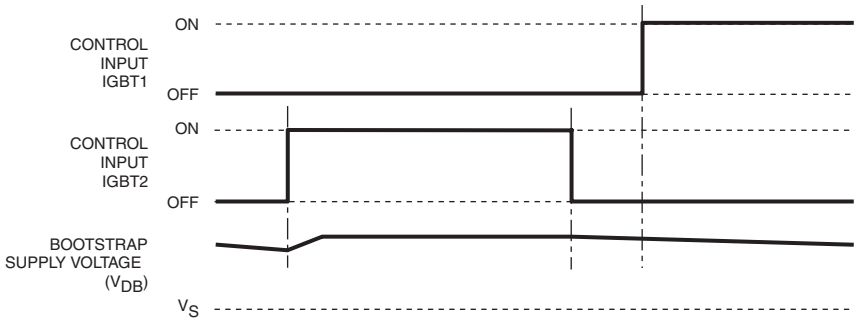


Figure 5.4 Bootstrap Supply Charging (Case 1)

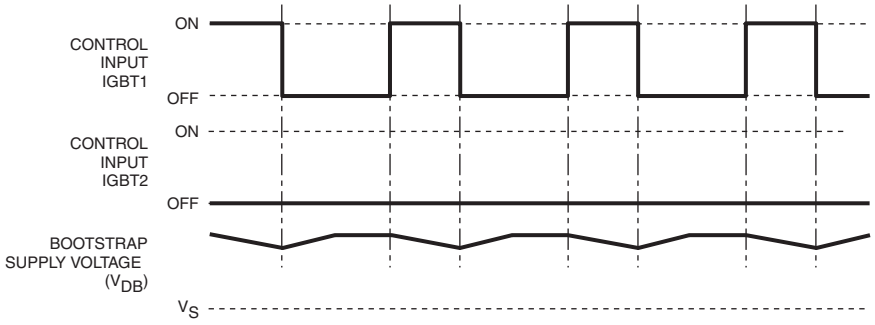


Figure 5.5 Bootstrap Supply Charging (Case 2)

in C_{BS} the bootstrap capacitor can be approximated as follows:

From $Q = C \times \Delta V = I \times t$

$$Q_{discharge} = I_{BS} \times t_1$$

where:

t_1 = maximum ON time of IGBT1

I_{BS} = current consumption of the HVIC gate driver

$$Q_{charge} = CBS \times \Delta V$$

where:

C_{BS} = bootstrap capacitance

ΔV = maximum allowable discharge of V_{DB}

Setting $Q_{discharge} = Q_{charge}$ and solving for C_{BS} yields:

$$\Rightarrow C_{BS} = I_{BS} \times t_1/\Delta V$$

If the PWM technique being used has times when only IGBT1 is switching with IGBT2 always off (Case 2 above), C_{BS} will be charged only when FWD2 is conducting. In this case C_{BS} is discharged during the ON time of IGBT1 just like it was in Case 1. Therefore, the equation shown for C_{BS} above applies to the case as well.

The equation above gives the minimum capacitance needed to avoid discharging the bootstrap supply (V_{DB}) by more than ΔV. However, in most applications a larger capacitor is required to provide design margin, improve stability and prevent power circuit surge voltages from overcharging the bootstrap supply. In addition, C_{BS} may need to be adjusted for start-up, shutdown, and fault handling conditions.

The inrush limiting resistance (R_{BS}) should be selected large enough to prevent excessive bootstrap charging currents (I_D) from

disturbing the main control power supply (V_D). It should also be small enough to completely recharge the bootstrap reservoir capacitor (C_{BS}) during the minimum on time of IGBT2 for charging Case 1 or the minimum off time of IGBT1 for Case 2. This requires that R_{BS} be selected so that when combined with C_{BS} the time constant will enable proper recharging.

The bootstrap diode for the 600V rated DIP-IPMs should have a withstanding voltage of more than 600V. In the DIP-IPM, the maximum rating of the power supply is 450V. This voltage is usually imposed by a surge voltage of about 50V; therefore the actual voltage applied on the diode is 500V. Furthermore, by considering 100V for the margin, then a 600V class diode is necessary. It is also highly recommended for the diode to have high speed recovery characteristics (recovery time is less than 100ns).

The 1200V DIP-IPM's maximum power supply voltage rating is 800V. In order to allow for surge voltages and margin a bootstrap diode is recommended with at least 1200V blocking capability and high speed recovery characteristics.

After the bootstrap voltage has been fully charged it is necessary to apply an input pulse to reset the P-side input signal before starting PWM. In some control algorithms such as those for BLDCM (Brushless DC) or 2-phase modulation of an induction motor the high-side IGBT may have a large ON time. This must be considered when selecting the bootstrap components. In some cases, very large bootstrap capacitors along with zener diodes may be required to maintain acceptable regulation of the floating supplies. Alternately, separate isolated power supplies or charge pumping schemes may be used instead of the bootstrap circuit.

The following example shows a typical calculation for the bootstrap capacitor and resistor. The actual values required in a given application may need to be adjusted considering the control PWM pattern.

Example:
Bootstrap Circuit Design

Selecting bootstrap capacitor:
Conditions:
ΔV_{DB} =1V, maximum ON pulse width t_1 of IGBT1 is 5ms,
I_{DB} = 0.35mA(max)
Therefore:
$C_{BS} = I_{DB} \times t_1/\Delta V_{DB} = 1.75 \times 10^{-6} = 1.75\mu F$

But, taking into consideration the characteristic distribution and reliability, the capacitance is generally selected to be 2~3 times of the calculated one. Therefore, C_{BS} is set to 5μF.

Selecting bootstrap resistor:
Conditions:
From above, C_{BS} = 5μF,
V_D =15V, V_{DB} =14V.

If the minimum ON pulse width t_0 of IGBT2, or the minimum OFF pulse width t_0 of IGBT2 is 20μs, then the bootstrap capacitor needs to be charged ΔV_{DB} =1V during this period.

Therefore:
$R_{BS} = \{(V_D - V_{DB}) \times t_0\}/(C_{BS} \times \Delta V_{DB}) = 4\Omega$.

Table 5.2 Typical Circuit Current (mA) for 1200V DIP PS22056

T_j (°C)	PWM Frequency F_C (kHz)	Duty (%)				
		10	30	50	70	90
25	3	0.94	0.94	0.94	0.94	0.94
	5	1.19	1.19	1.19	1.19	1.19
	7	1.44	1.44	1.44	1.44	1.44
	10	1.82	1.82	1.82	1.82	1.81
	15	2.44	2.44	2.44	2.44	2.44
	20	3.05	3.05	3.05	3.05	3.05
125	3	0.85	0.85	0.85	0.85	0.85
	5	1.11	1.11	1.11	1.11	1.11
	7	1.37	1.37	1.37	1.36	1.36
	10	1.74	1.74	1.74	1.74	1.73
	15	2.38	2.38	2.37	2.36	2.36
	20	3.00	3.00	3.00	2.99	2.97
-20	3	0.98	0.98	0.98	0.98	0.98
	5	1.23	1.23	1.23	1.23	1.23
	7	1.48	1.48	1.48	1.48	1.48
	10	1.85	1.85	1.85	1.85	1.85
	15	2.46	2.46	2.46	2.46	2.46
	20	3.08	3.08	3.08	3.08	3.08

As previously mentioned, the current consumed by the HVIC gate driver (IBS) inside the DIP-IPM depends on operating frequency, temperature and switching duty. Typical characteristics are shown in Tables 5.2 and 5.3 and Figures 5.6 through 5.8.

Table 5.3 Typical Circuit Current (μA) for 600V DIP PS21869

T_j (°C)	PWM Frequency F_C (kHz)	Duty (%)				
		10	30	50	70	90
25	3	266	244	221	199	176
	5	280	263	241	218	196
	7	296	281	259	236	214
	10	316	310	288	265	242
	15	351	350	336	312	291
	20	387	389	385	364	340
125	3	295	273	250	226	204
	5	311	290	268	246	222
	7	324	309	286	263	240
	10	342	338	313	290	266
	15	373	372	361	335	314
	20	400	403	400	379	355
-20	3	248	225	203	181	159
	5	266	245	223	200	179
	7	281	265	243	220	198
	10	302	294	272	250	228
	15	338	339	322	300	277
	20	373	377	371	350	326

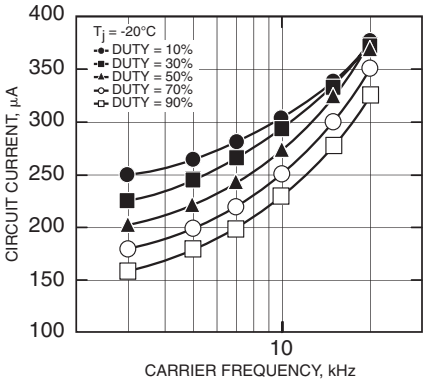


Figure 5.6 Characteristics Under the Condition of T_j = -20°C (Typical for DIP PS21869)

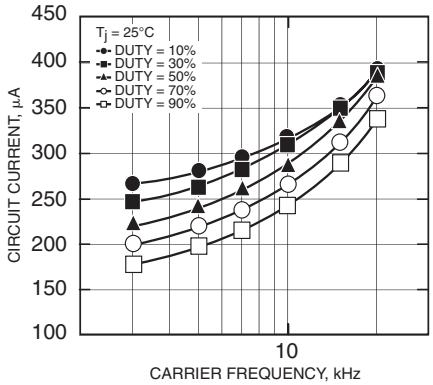


Figure 5.7 Characteristics Under the Condition of T_j = 25°C (Typical for DIP PS21869)

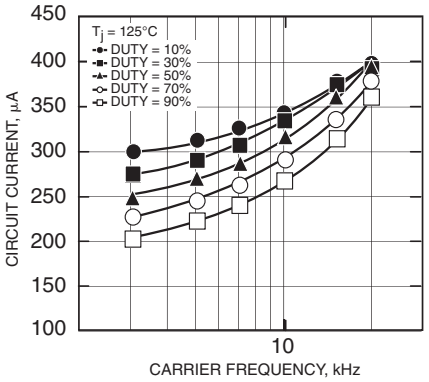


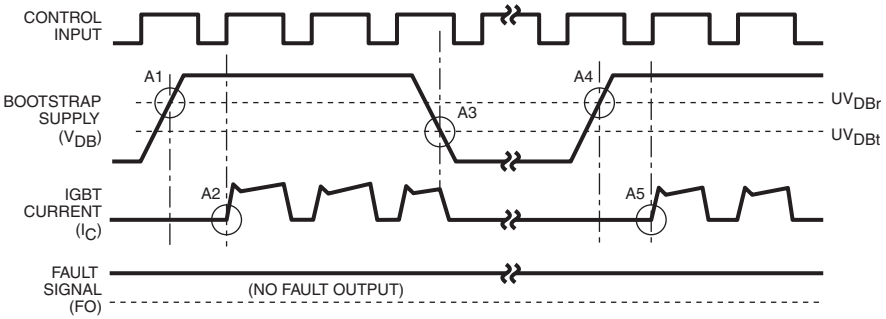
Figure 5.8 Characteristics Under the Condition of T_j = 125°C (Typical for DIP PS21869)

5.2.7 Bootstrap Power Supply Undervoltage Lockout

The HVIC drivers in the DIP-IPM provide an undervoltage lockout function to protect the high-side IGBTs from insufficient gate driving voltage. If the voltage on any of the bootstrap power supplies drops below the data sheet specified undervoltage trip level (UV_{DBt}) the respective high-side IGBT will be turned off and input control signals will be ignored. In order to prevent oscillation of the undervoltage protection function hysteresis has been provided. For normal operation to resume the bootstrap supply voltage must exceed the data sheet specified undervoltage reset level (UV_{DBr}). Switching will resume at the next on command after the supply has reached UV_{DBr}. A timing diagram showing the operation of the HVIC undervoltage lockout is shown in Figure 5.9.

5.2.8 Hybrid Circuits for Control Power Supplies

Powerex has developed two hybrid DC-DC converters to simplify control power supply design. The M57182N-315 and M57184N-715 are high input voltage, non-isolated, step-down, DC-DC converters designed to derive low voltage control power directly from the main DC bus. These converters accept input voltages of 140VDC to 380VDC allowing them to operate directly from rectified AC line voltages of 100VAC to 240VAC. The M57182N-315 provides a 200mA regulated 15VDC output. The M57184N-715 supplies a 350mA, 15VDC output and a 200mA, 5VDC output. Each circuit is configured in a compact SIP (Single In-line Package) to allow efficient layout with minimum printed circuit board space. The Powerex M57184N-715 hybrid DC-DC converter is ideal for creating the 15V control power supply and the 5V logic supply directly from the DC bus. Figure 5.10 shows an example application circuit using the M57184N-715. The figure shows how the required power supplies are derived directly from the main DC link voltage (V_{CC}). For more detailed information on the hybrid DC-DC converters see the individual device data sheets and Powerex application note “Product Information: M57182N-315 and M57184N-715 Hybrid DC-DC Converters”.



A1: The control supply exceeds the UV_{DBr} level. Undervoltage protection is reset.
A2: Normal operation. Switching starts at next on going transition of control input.
A3: Bootstrap supply falls below UV_{DBt}. IGBT switching is stopped.
A4: The control supply exceeds the UV_{DBr} level. Undervoltage protection is reset.
A5: Normal operation resumes. Switching starts at next on going transition of control input.

Figure 5.9 HVIC Undervoltage Lockout Timing Diagram

5.2.9 Control Power for Multiple Devices

The circuit in Figure 5.11 shows the parallel connection of the control power supply for two DIP-IPMs. Such an application is likely to require long wiring. Route 1 and 2 indicate the gate charging path of low-side IGBT in DIP-IPM No.2. If the route is too long, the gate voltage might drop due to large voltage drop from the wiring impedance, which will negatively affect the operation of the second IPM. Charging of the bootstrap capacitor for the high-side will be insufficient also. In addition, noise might be easily imposed on the wiring impedance. If there are many DIP-IPMs connected in parallel, the GND pattern becomes long. The fluctuation of GND potential may influence other circuits (power supply, protection circuit etc.). Therefore, parallel connection of the control power supply is not recommended. For an application with more than one motor, it is recommend to use individual control supplies for the each DIP-IPM. Sharing the common DC bus among multiple DIP-IPMs is generally not a problem.

5.2.10 Ground Terminal Voltage Limits and Precautions

The DIP-IPM performs short-circuit protection by detecting DC link current with an external shunt resistor. For this method, wiring inductance may have influence on the DIP operation if it is too large.

When the high-side IGBT turns off, motor currents will flow continuously through the low-side free-wheel diode. The positive terminal voltage of high-side floating supply (V_{FB}) may drop below the N terminal volt-

age. This phenomenon is common for the case of switching a large current. Generally, for HVICs using a junction-isolated process, if the V_{FB} voltage becomes too negative with respect to the N terminal voltage, then the IPM may malfunction. Table 5.4 shows the recommended range of the N terminal voltage with respect to common (V_{NC}).

When a short-circuit is detected the IPM's SC protection activates and interrupts the current through the device. This abrupt turn-off of high current may cause a surge voltage. If the wiring length of the external shunt resistor is too long, the voltage drop may cause the voltage applied to the DIP-IPM supply terminals to exceed allowable levels.

The internal IC may malfunction or be destroyed by such voltages. To avoid this it is necessary to minimize the shunt wiring length. See Section 5.4.1 for more details. In addition, inserting a zener diode (24V, 1W) between V_{N1} and GND will improve the surge voltage withstand capability of the device.

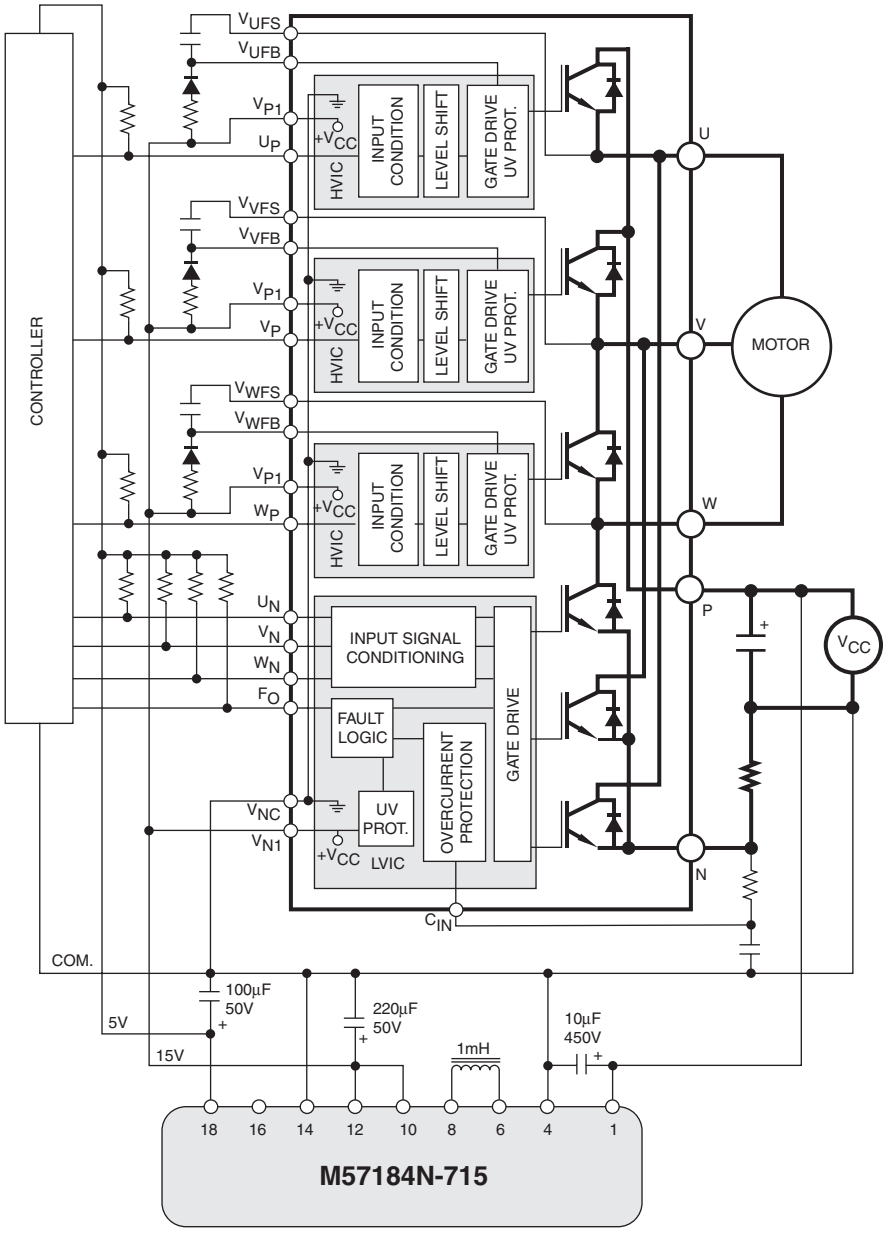


Figure 5.10 Power Supply for DIP-IPM

5.3 Interface Circuits

The DIP-IPM has six microprocessor compatible inputs in addition to a fault output signal. The built in HVIC level shifters allow all signals to be referenced to the common ground of the 15V control power supply. The signals for 600V DIP are 3.3V and 5V TTL/CMOS compatible in order to permit direct connection to a PWM controller. The 1200V DIP demands the user to use a 5V logic interface but a 15V logic interface can be used. The interface circuit between the PWM controller and the DIP-IPM can be made by either direct connections or optocouplers depending on the requirements of the application. This section presents the electrical characteristics of the DIP-IPM's control signal inputs and outputs, and provides detailed descriptions of typical interface circuits.

5.3.1 General Requirements

Figure 5.12 shows the internal structure of the DIP-IPM's control signals and a simplified schematic of a typical external interface circuit. ON and OFF operations for all six of the DIP-IPM's IGBTs are controlled by the active high control inputs U_P, V_P, W_P, U_N, V_N, W_N. These inputs are pulled low with an internal resistor. No external pull-up or pull-down resistors are required. The controller commands the respective IGBT to turn on by pulling the input high. Approximately 1V of hysteresis is provided on all control inputs to help prevent oscillations and enhance noise immunity. The optional capacitor (C) and resistor (R), shown dashed in the figure, can be added to further improve noise filtering. These components may be required in some applications depending on the circuit layout and length of connections to the controller. If these filters are added it is important to check that proper dead time is being maintained. In addition, a minimum ON time is necessary for proper IGBT turn-off operation. The required minimum ON time is given in Table 5.5. The control inputs should be pulled down to between 0V and 0.8V in the OFF state.

Table 5.4 Recommended Range of N Terminal Voltage

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
N Terminal Voltage	V_{NO}	Voltage between V_{NC} - N including surge voltage	-5	—	+5	V

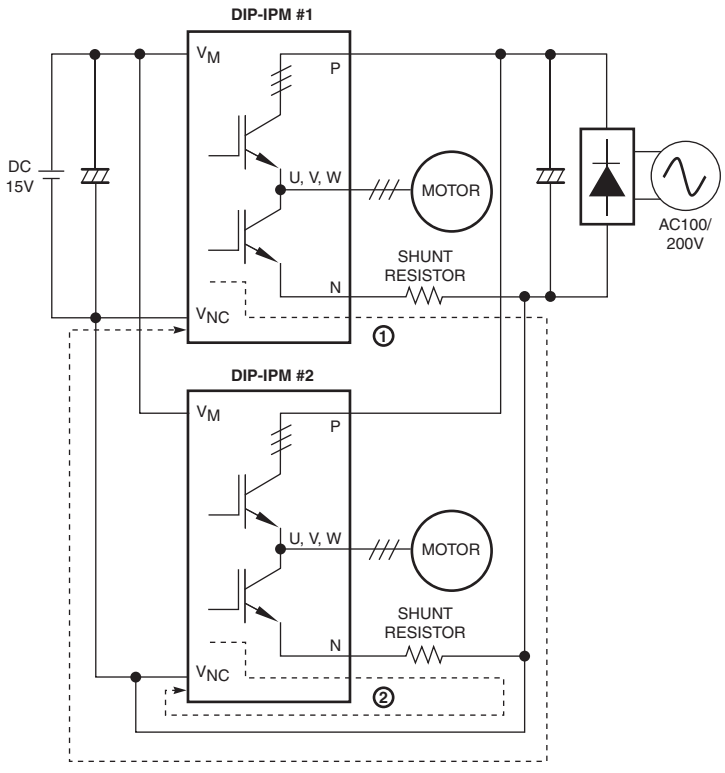


Figure 5.11 Parallel Connection

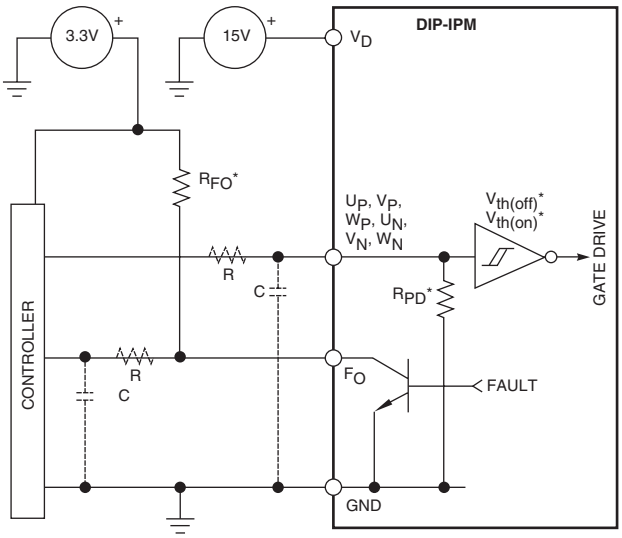
The fault signal output (FO) is in an open collector configuration. Normally, the fault signal line is pulled high to the logic supply voltage with a resistor as shown in Figure 5.12. When a short-circuit condition or improper control power supply voltage is detected the DIP-IPM turns on the internal open collector device and pulls the fault line low. The maximum allowable sink current at the FO pin is specified on the device's data sheets. The fault output pull-up voltage can be up to V_D+0.5V (typically 15.5V) so connection of the pull-up resistor to the 15V control power supply is allowable. However, in most applications it is desirable to use the logic supply so that the fault signal voltage is the same as the control input signals.

5.3.2 Interface Circuit Examples

Figure 5.13 shows a typical interface circuit for direct connection of the DIP and Mini/Super-Mini DIP to the PWM controller. Figure 5.14 shows a typical high speed opto-coupled interface circuit for the DIP and Mini/Super-Mini DIP. Component selection information and relevant notes are included below each figure.

Table 5.5 Minimum ON Time for DIPs

Device	DIP-IPM	Mini DIP-IPM	Super-Mini DIP-IPM
Minimum ON Time	300ns	300ns	500ns

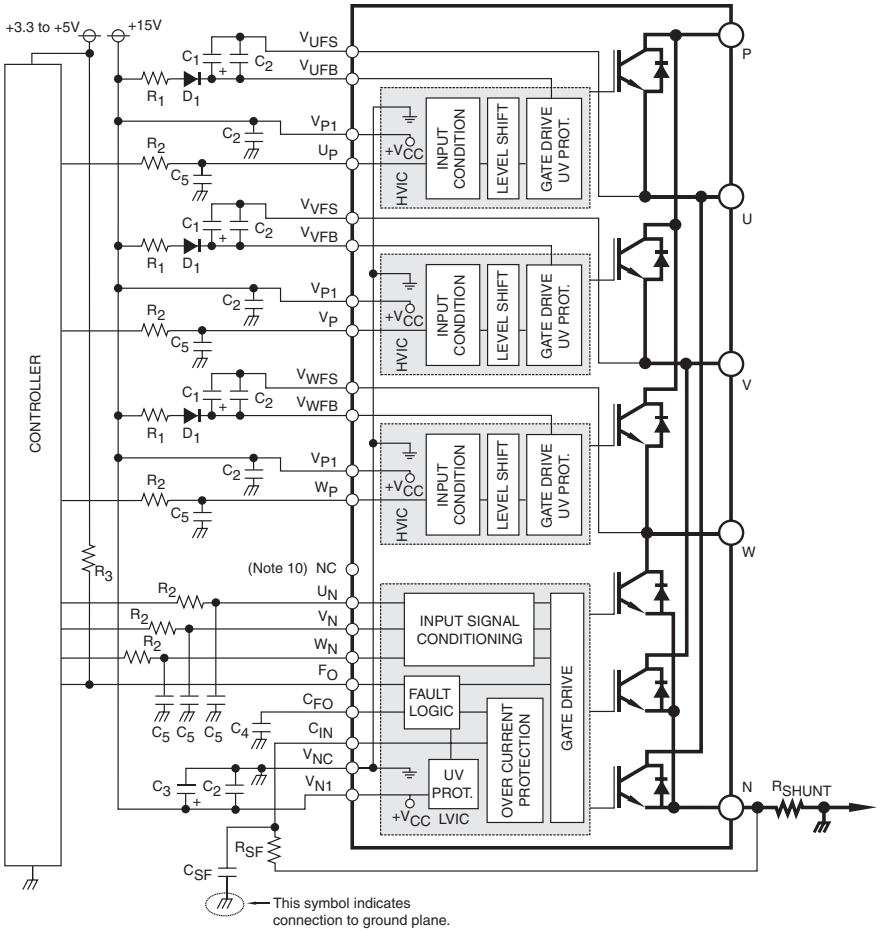


*Values for figure above. V_D = 15V, T_j = 25°C

Device	PS21562	PS21563	PS21564	PS21865	PS21867	PS21869
R_{FO} Typ.	10k ohm	10k ohm	10k ohm	10k ohm	10k ohm	10k ohm
R_{PD} Typ.	2.5k ohm	2.5k ohm	2.5k ohm	2.5k ohm	2.5k ohm	2.5k ohm
$V_{th(off)}$ Min.	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V
$V_{th(on)}$ Max.	2.6V	2.6V	2.6V	2.6V	2.6V	2.6V

Device	PS21962	PS21963	PS21964	PS22052	PS22053	PS22054	PS22056
R_{FO} Typ.	10k ohm	10k ohm	10k ohm	10k ohm	10k ohm	10k ohm	10k ohm
R_{PD} Typ.	3.3k ohm	3.3k ohm	3.3k ohm	2.5k ohm	2.5k ohm	2.5k ohm	2.5k ohm
$V_{th(off)}$ Min.	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V
$V_{th(on)}$ Max.	2.6V	2.6V	2.6V	4.2V	4.2V	4.2V	4.2V

Figure 5.12 DIP-IPM Interface Circuit



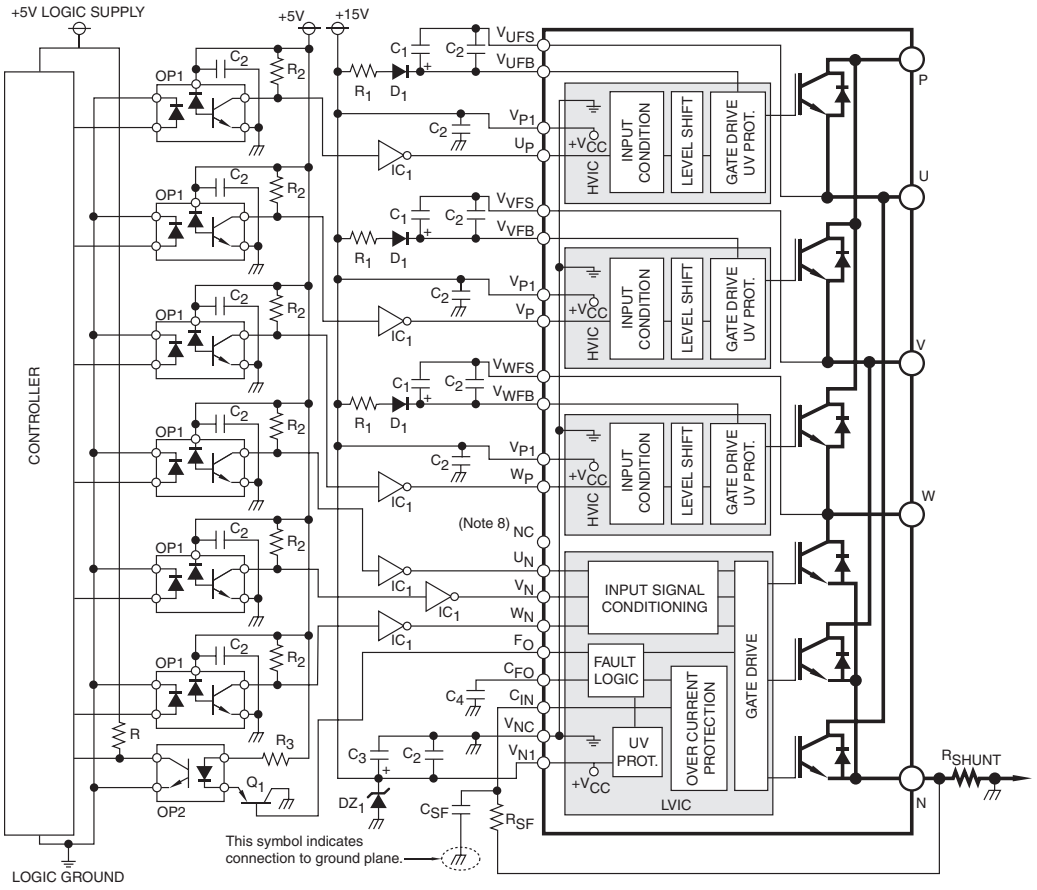
Component Selection:

Dsgn.	Typ. Value	Description
D_1	1A, 600V	Boot strap supply diode – Ultra fast recovery
C_1	10-100µF, 50V	Boot strap supply reservoir – Electrolytic, long life, low Impedance, 105°C (Note 5)
C_2	0.22-2.0µF, 50V	Local decoupling/high frequency noise filters – Multilayer ceramic (Note 8)
C_3	10-100µF, 50V	Control power supply filter – Electrolytic, long life, low Impedance, 105°C
C_4	22nF, 50V	Fault lock-out timing capacitor – Multilayer ceramic (Note 4)
C_5	100pF, 50V	Optional input signal noise filter – Multilayer ceramic (Note 1)
C_{SF}	1000pF, 50V	Short-circuit detection filter capacitor – Multilayer ceramic (Note 6, Note 7)
R_{SF}	1.8k ohm	Short-circuit detection filter resistor (Note 6, Note 7)
R_{SHUNT}	5-100m ohm	Current sensing resistor – Non-inductive, temperature stable, tight tolerance (Note 9)
R_1	10 ohm	Bootstrap supply inrush limiting resistor (Note 5)
R_2	330 ohm	Optional control input resistor (Note 1, Note 2)
R_3	10k ohm	Fault output signal pull-up resistor (Note 3)

Notes:

1) To prevent input signal oscillations, minimize wiring length to controller (~2cm). Additional RC filtering (C5 etc.) may be required. If filtering is added, be careful to maintain proper dead time and voltage levels. See application notes for details.
2) Internal HVIC provides high voltage level shifting allowing direct connection of all six driving signals to the controller.
3) F_O output is an open collector type. Pull-up resistor (R3) should be adjusted to current sink capability of the module.
4) C4 sets the fault output duration and lock-out time. C4 ≈ $12.2E^{-6}$ x t_{FO}, 22nF gives ~1.8ms
5) Bootstrap supply component values must be adjusted depending on the PWM frequency and technique.
6) Wiring length associated with R_{SHUNT}, R_{SF}, C_{SF} must be minimized to avoid improper operation of the SC function.
7) R_{SF}, C_{SF} set overcurrent protection trip time. Recommend time constant is 1.5µs-2.0us. See application notes.
8) Local decoupling/high frequency filter capacitors must be connected as close as possible to the modules pins.
9) Use high quality, tight tolerance current sensing resistor. Connect resistor as close as possible to the DIP's N terminal. Be careful to check for proper power rating. See application notes for calculation of resistance value.
10) This pin is connected internally. It must not be connected to any external circuits.

Figure 5.13 Typical Direct Connection Interface Circuit (Shown Pins Up)



Component Selection:

Dsgn.	Typ. Value	Description
D_1	1A, 600V	Bootstrap supply diode – Ultra fast recovery
DZ_1	28V, 1W	Zener diode for Transient Voltage Suppression
C_1	10-100µF	Bootstrap supply reservoir – Electrolytic, long life, low Impedance, 105°C (Note 4)
C_2	0.22-2.0µF	Local decoupling/High frequency noise filters - Multilayer ceramic (Note 7)
C_3	10-100µF	Control power supply filter – Electrolytic, long life, low Impedance, 105°C
C_4	22nF	Fault lock-out timing capacitor – Multilayer ceramic (Note 3)
C_{SF}	1000pF	Short circuit detection filter capacitor – Multilayer ceramic (Note 5, Note 6)
R_{SF}	1.8k ohm	Short circuit detection filter resistor (Note 5, note 6)
R_1	10 ohm	Bootstrap supply inrush limiting resistor (Note 4)
R_2	4.7k ohm	Control input pull-up resistor (Note 1)
R_3	10k ohm	Fault output current limiting resistor (Note 2)
Q_1	PNP	Buffer transistor for fault output
IC_1	**HC04	CMOS hex inverter
OP1	Fast Optocoupler	High common mode noise immunity type. Example: HCPL4504
OP2	Slow Optocoupler	CTR 100-200% examples: Sharp PC817, NEC PS2501

Notes:

1) To prevent input signal oscillations, minimize wiring length between opto and controller (~2cm). Additional RC filtering may be required. If filtering is added be careful to maintain proper dead time. See text for details.
2) F_O output is an open collector type. R3 should be set considering the CTR of the opto and the DIP I_{FO} limit. A buffer (Q_1) may be needed.
3) C4 sets the fault output duration and lock-out time. C4 $12.2E^{-6} \times t_{FO}$, 22nF gives ~1.8ms
4) Bootstrap supply components must be adjusted depending on the PWM frequency and technique.
5) Wiring length associated with R_{SHUNT}, R_{SF}, C_{SF} must be minimized to avoid improper operation of the SC function.
6) R_{SF}, C_{SF} set short-circuit protection trip time. Recommend time constant is 1.5µs-2.0µs. See text for details.
7) Local decoupling/high frequency filter capacitors must be connected as close as possible to the modules pins.
8) This pin is connected internally. It must not be connected to any external circuits.

Figure 5.14 Typical High-speed Optocoupler Interface Circuit

5.3.3 Decoupling Capacitor

Decoupling capacitors are usually used to control turn-off and free-wheel diode recovery surge voltages. There are two positions to mount a decoupling capacitor to the DIP-IPM as shown in Figure 5.15. The capacitor should be installed in position 2 in order to remove surge voltage most effectively. However, the charging and discharging currents generated by the wiring inductance and the decoupling capacitance will flow on the shunt resistor. This might trigger the protection if the current is large enough to reach the SC trip level on the shunt resistor. In order to remove the surge voltage maximally and prevent a fault, the decoupling capacitor should be located in position 1 just outside the shunt resistor. The wiring at part A should be as short as possible. The recommended wiring is shown by location 3 in the figure.

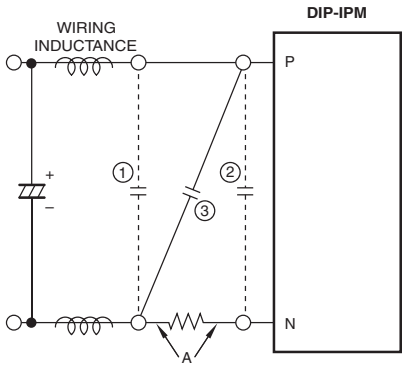


Figure 5.15 Decoupling Capacitor Location

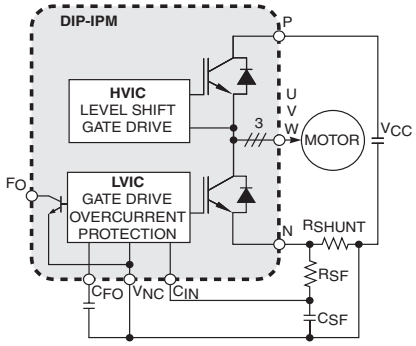


Figure 5.16 DIP-IPM Current Sensing Circuit

5.4 Short-circuit Protection Function

The DIP-IPMs have an integrated short-circuit protection function. The IC monitors the voltage across an external shunt resistor (R_{SHUNT}) to detect excessive current in the DC link and provide protection against short-circuits. Figure 5.16 illustrates the typical external components used for sensing current. The voltage across R_{SHUNT} is filtered by an RC circuit (R_{SF}, C_{SF}) and connected to the C_{IN} pin. If the voltage at the C_{IN} pin exceeds $V_{SC(ref)}$, which is specified on the devices data sheets, then a fault signal is asserted and the lower arm IGBTs are turned off. The following sections will provide a detailed description of the short-circuit protection function and external component selection.

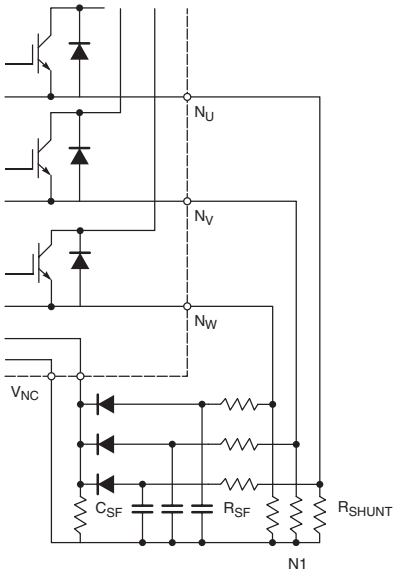


Figure 5.17 Shunt Wiring for Open Emitter DIPs

The 1200V and -S are open-emitter type IPMs which allows the user to access the terminals of each of the low-side IGBT emitters. In order to utilize the short-circuit protection features on the open-emitter DIPs the user can connect the N_U, N_V and N_W terminals together and proceed to use the connection circuit shown in Figure 5.16. Alternatively the user can have separate shunt resistors for each low-side IGBT as shown in Figure 5.17. Each shunt resistor should be followed by the appropriate RC noise filter. The three shunt voltages are then diode OR'd gated so that the highest voltage across the shunt resistors will be fed into the C_{IN} pin. For this circuit it is best to use Schottky diodes to minimize losses in the shunt resistors. It is also possible to disable the short-circuit protection provided by the DIP by pulling the voltage at the C_{IN} pin low through a resistor. Shunt resistors can still be used from the N-side emitters to the V_{NC} pin. This gives the user the possibility of designing their own current monitoring and protection scheme for the devices.

5.4.1 Recommended Wiring of Shunt Resistor

An external current sensing resistor is used to detect short-circuit conditions. A long wiring pattern between the shunt resistor and DIP-IPM could cause a surge voltage that might damage the built-in IC. To decrease the pattern inductance, the wiring between the shunt and DIP-IPM should be made as short as possible. Figures 5.18 and 5.19 present some wiring recommendations.

5.4.2 Timing Diagram of SC Protection

Figure 5.20 is a timing diagram showing the operation of the short-circuit protection. When current flows in the negative DC bus a voltage is developed across R_{SHUNT}. The voltage across R_{SHUNT} is filtered using an RC circuit consisting of R_{SF} and C_{SF} and connected to the C_{IN} input on the DIP-IPM. If the collector current exceeds the I_{SC} level for long enough to charge the shunt filter capacitor (C_{SF}) to a voltage greater than $V_{SC(ref)}$ the protection is activated. The I_{SC} level is set by the external shunt resistor (R_{SHUNT}). The filter (C_{SF}, R_{SF}) adds a time delay to prevent erroneous operation of the protection due to free-wheeling diode recovery currents and voltage surges caused by stray inductance in the sensing circuit. Selection of the shunt resistor and filter components will be covered in Sections 5.4.3 and 5.4.4. When the protection is activated all three low-side IGBTs are turned off and the open collector fault output is pulled low. The IGBTs remain in the OFF state and the fault signal remains low for the duration of the fault timer (t_{FO}). The length of t_{FO} is specified on the device's data sheets. During this time the low-side control input signals (U_N, V_N, W_N) are ignored. Normal operation resumes at the first OFF-to-ON transition following the end of the fault timer.

5.4.3 Selecting the Current Sensing Shunt Resistor

The external shunt resistor (R_{SHUNT}) shown in Figures 5.18 and 5.19 is used to detect the current in the negative DC bus and provide a proportional voltage to the C_{IN} pin to activate the short-circuit protection. For reliable and stable operation the shunt resistor should be a high quality, non-inductive, tight tolerance type. The shunt resistor must have an appropriate power rating. In some applications it will need to dissipate several watts. Stray inductance in the circuit that includes the shunt resistor and filtering components (C_{SF} and R_{SF}) must be minimized to prevent erroneous short-circuit detection caused by L x di/dt surge voltages. In general, this means that the wiring between R_{SHUNT}, R_{SF}, C_{SF} and the modules N, V_{NC}, C_{IN} pins must be made as short as possible.

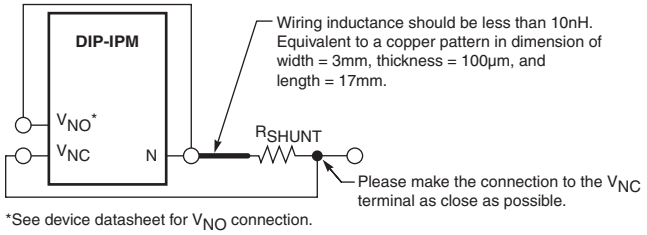


Figure 5.18 Typical Wiring of Shunt Resistor

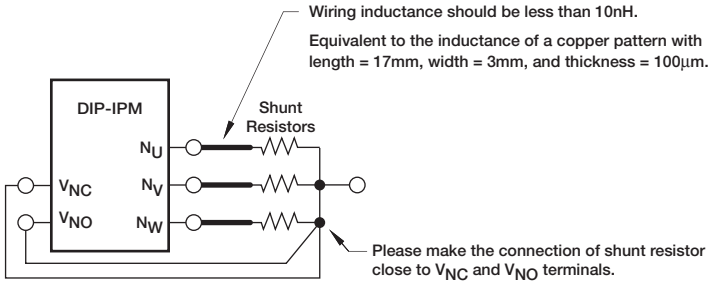
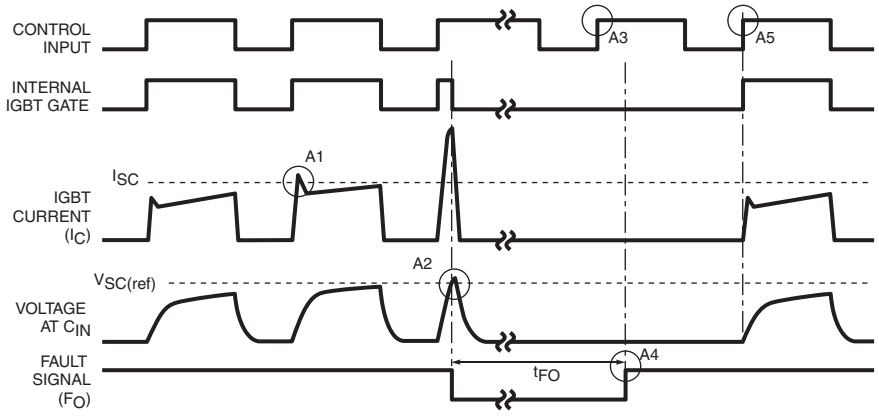


Figure 5.19 Typical Wiring of Shunt Resistor



A1: Free-wheel diode recovery current pulse ignored due to R_{SF}, C_{SF} filter.
A2: Short-circuit event: C_{IN} voltage exceeds $V_{SC(ref)}$. Low side IGBTs are turned off. fault signal is set.
A3: Input ON commands are ignored during t_{FO}.
A4: t_{FO} expires and fault signal is cleared.
A5: Switching of IGBT resumes at the first on going transition after the fault signal is cleared.

Figure 5.20 Timing Diagram for Short-circuit Protection

Table 5.6 Specification for $V_{SC(ref)}$

Device	Conditions	Min.	Typ.	Max.
DIP-IPM	-20°C ≤ T_j ≤ 125°C	0.43V	0.48V	0.53V
Mini DIP-IPM	-20°C ≤ T_j ≤ 125°C	0.43V	0.48V	0.53V
Super-Mini DIP-IPM	-20°C ≤ T_j ≤ 125°C	0.43V	0.48V	0.53V

The short-circuit protection current trip level is set by selecting the appropriate value for the external shunt resistor. The process for selecting R_{SHUNT} is basically the same for all DIP-IPMs. The current sensing shunt resistor value is calculated using the expression $R_{SHUNT} = V_{SC(ref)}/I_{SC}$, where $V_{SC(ref)}$ is the SC reference voltage (trip level) of the DIP-IPM's control IC, and I_{SC} is the current value to be interrupted.

The DIP-IPM's short-circuit detection reference voltage ($V_{SC(ref)}$), depends on control IC manufacturing tolerances, control supply voltage and operating temperature. Table 5.6 shows the range of $V_{SC(ref)}$ that must be considered when selecting R_{SHUNT}.

The maximum allowable short-circuit trip current (minimum shunt resistance) for a given DIP-IPM type depends on the IGBTs short-circuit saturation current. The short-circuit saturation current is the maximum self-limited current that the IGBT will conduct under short-circuit conditions. If the shunt is selected so that I_{SC} is larger than the IGBT's short-circuit saturation current, the IGBT will desaturate and limit the current to a level below I_{SC}. Thus, if R_{SHUNT} is made too small the SC protection function is effectively disabled. The short-circuit saturation current depends on the IGBT's transconductance (input voltage to output current gain) and the applied gate voltage. Figure 5.21 shows a typical saturation current characteristic versus control supply voltage for a DIP-IPM. In order to avoid potential problems it is generally a good idea to design for a maximum short-circuit trip current of less than 1.7 times the nominal rated collector current (I_C).

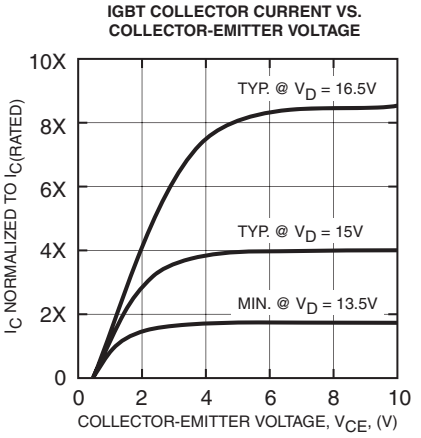


Figure 5.21 IGBT Collector Current vs Collector-emitter Voltage

The following example shows a typical calculation for the current sensing shunt resistance value and the resulting range of short-circuit protection trip level (I_{SC}) for a Super-Mini DIP-IPM. The method is essentially the same for all DIP-IPMs.

Example: PS21962 (5A/600V)

The maximum recommended short-circuit trip current is 1.7 times the nominal I_C rating of the module:

$$I_{SC(max)} = I_{C(rated)} \times 1.7 = 5 \times 1.7 = 8.5A$$

The minimum allowable shunt resistance is determined by requiring that the protection must operate at I_C = 8.5A even if the modules short-circuit detection reference level ($V_{SC(ref)}$) is at its maximum. Referring to Table 5.6 for $V_{SC(ref)}$ the minimum shunt resistance is:

$$R_{SHUNT(min)} = \frac{V_{SC(ref)max}}{I_{SC(max)}} = \frac{0.53}{8.5} = 62m\Omega$$

If the tolerance of the shunt resistor is 5% then the possible range is:

R_{min} = 59mΩ, R_{typ} = 62mΩ and R_{max} = 65mΩ

The typical short-circuit trip current is:

$$I_{SC(typ)} = \frac{V_{SC(ref)typ}}{R_{(typ)}} = \frac{0.48V}{62m\Omega} = 7.7A$$

The minimum short-circuit trip current is:

$$I_{SC(min)} = \frac{V_{SC(ref)min}}{R_{max}} = \frac{0.43V}{65m\Omega} = 6.6A$$

Therefore, the range for short-circuit trip current is from 6.6A to 8.5A.

This example uses the maximum recommended I_{SC} as the upper limit. In many applications it will be desirable to set the maximum I_{SC} to a lower level to provide additional safety margin or limit dissipation in the DIP-IPM to a level compatible with the available heatsink. It is possible that the actual SC protective level is less than the calculated one. This is due to oscillations caused mainly by parasitic inductance and parasitic capacitance. It is recommended to verify the shunt resistance by prototype experiment.

5.4.4 Selecting the RC Filter

An RC filter (R_{SF}, C_{SF}) must be inserted between the current sensing resistor and the DIP-IPMs C_{IN} pin as shown in Figures 5.16 and 5.17. The RC filter helps prevent erroneous fault detection due to di/dt noise on the shunt resistor and free-wheel diode recovery current pulses. The RC filter also has the added advantage of producing a time dependent short-circuit trip level that responds quickly to severe low impedance short-circuits and slowly to less dangerous overloads conditions. This characteristic is illustrated in Figure 5.22. The RC filter causes a delay in the short-circuit detection that must be coordinated with the short-circuit withstanding capability of the IGBTs. A detailed description of the IGBT SOA and short-circuit withstanding capability is given in Section 5.5. It is also important to consider the propagation delay of the control IC. The delay for the IGBT gate drive to be interrupted after the voltage on C_{IN} exceeds $V_{SC(ref)}$ is shown in Table 5.7. This delay must be added to the delay caused by the time constant of the R_{SF}, C_{SF} filter. For the DIP-IPMs an RC time constant ($\tau = R_{SF} \times C_{SF}$) of 2µs or less will normally provide safe operation.

5.5 SOA

The DIP-IPMs built-in gate drive, undervoltage lockout and short-circuit protection guard them from many of the operating modes that would violate the Safe Operation Area (SOA) of discrete IGBTs. A conventional SOA definition that characterizes all possible combinations of voltage, current and time that would cause power device failure is not required. In order to define the SOA for DIP-IPMs, the power device capability and control circuit operation must both be considered. The resulting easy to apply switching and short-circuit SOA definitions for the DIP-IPMs are summarized in this section.

5.5.1 Switching SOA

Switching or turn-off SOA, as shown in Figure 5.23, is normally defined in terms of the maximum allowable simultaneous voltage and current during repetitive turn-off switching operations. In the case of the DIP-IPMs, the built-in gate drive eliminates many of the dangerous combinations of voltage and current that are caused by improper gate drive. In addition, the maximum operating current is normally limited by the short-circuit protection. Given these constraints the switching SOA can be defined using the waveform shown in Figure 5.24. This waveform shows that the device will operate safely as long as the DC bus voltage is below the data sheet $V_{CC(prot)}$ specification, the turn-off transient voltage across the collector and emitter of each IGBT switch is maintained below the V_{CES} specification and T_j is less than 125°C. In this waveform I_C is the current that the DIP-IPM will allow for safe switching.

Table 5.7 DIP-IPMs Internal Time Delay of IC

Min.	Typ.	Max.	Unit
0.3	0.5	1.0	µs

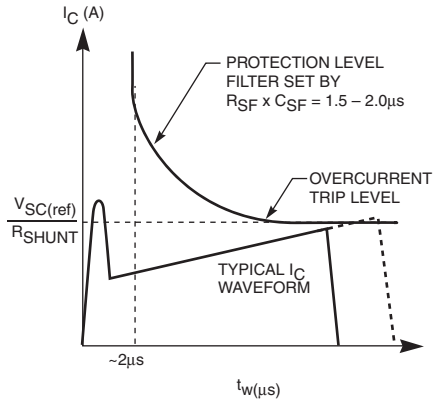
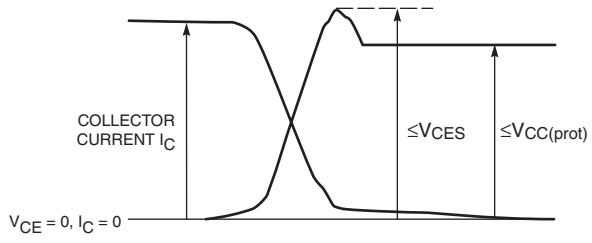


Figure 5.22 Short-circuit Protection Characteristics



WHERE:

V_{CES} IS THE MAXIMUM IGBT COLLECTOR-EMITTER BLOCKING VOLTAGE RATING

$V_{CC(prot)}$ IS THE MAXIMUM DC BUS VOLTAGE FOR SAFE OPERATION OF PROTECTION CIRCUITS

I_C IS 2 x I_{RATED}

Figure 5.23 Turn-off Waveform

5.5.2 Short-circuit SOA

The waveform in Figure 5.24 depicts typical short-circuit operation. The standard test condition uses a minimum impedance short-circuit, which causes the maximum short-circuit current to flow in the device. In this test, the short-circuit current (I_{SC}) is limited only by the device characteristics. The DIP-IPMs are guaranteed to survive non-repetitive short-circuit conditions as long as the initial DC bus voltage is less than the $V_{CC(prot)}$ specification, all transient voltages across C-E of each switch are maintained less than the V_{CES} specification, the starting junction temperature (T_j) is less than 125°C and t_W is less than 2µs.

The typical short-circuit capability of the IGBTs inside the DIP-IPM is shown in Figure 5.25. This figure shows that the maximum worst case short-circuit current may reach thirteen times the nominal device rating when V_D = 16.5V. Even a device with a short-circuit current this high will survive for 4µs when V_{CC} = 400V and the starting junction temperature is less than 125°C. This capability must be taken into consideration when selecting the R_{SF}, C_{SF} filter circuit. Considering the 4µs capability an RC time constant of less than 2µs will normally yield adequate safety margin.

5.5.3 Active Region SOA

Like most IGBTs, the IGBTs used in the DIPs Mini DIPs and Super-Mini DIPs are not suitable for linear or active region operation. Normally device capabilities in this mode of operation are described in terms of FBSOA (Forward Biased Safe Operating Area). The devices' internal gate drive forces the IGBT to operate with a gate voltage of either zero for the OFF state or the control supply voltage (V_D) for the ON state. The DIP-IPM has built in undervoltage lockout protection for all six IGBT to prevent any possibility of active or linear operation by automatically turning the power device off if the driving voltage becomes too low.

5.6 Thermal Considerations

When operating, the power devices contained in DIP-IPMs will have conduction and switching power losses. The heat generated as a result of these losses must be conducted away from the power chips and into the environment using a heatsink. If an appropriate thermal system is not used, then the power devices will overheat, which could result in failure. In many applications the maximum usable power output of the module will be limited by the systems thermal design.

5.6.1 Power Losses

The first step in thermal design is the estimation of total power loss. In power electronic circuits using IGBTs, the two most important sources of power dissipation that must be considered are conduction losses and switching losses.

Conduction Losses

Conduction losses are the losses that occur while the IGBT is on and conducting current. The total power dissipation during conduction is computed by multiplying the ON state saturation voltage by the ON state current. In PWM applications the conduction loss should be multiplied by the duty factor to obtain the average power dissipated. A first approximation of conduction losses can be obtained by multiplying the IGBT's rated $V_{CE(SAT)}$ by the expected average device current. In most applications the

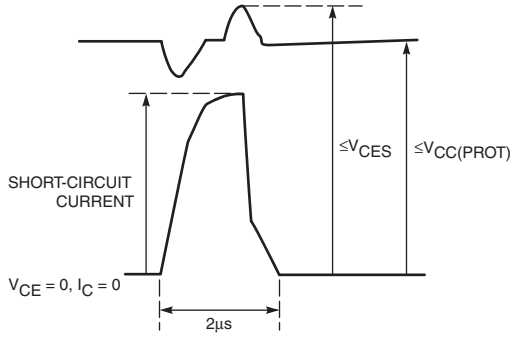
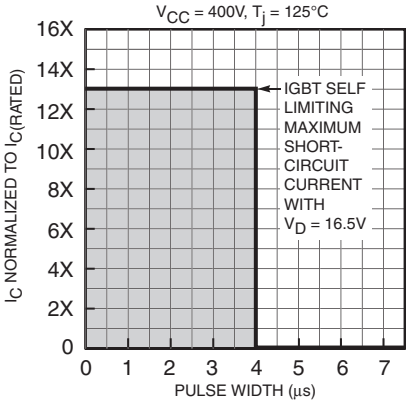


Figure 5.24 Short-circuit Operation



NOTE: At turn off V_{CE} surge must be less than V_{CES} rating of IGBT. V_{P-N} surge must be less than $V_{CC(surge)}$ rating.

Figure 5.25 Typical Short-circuit Capability

actual losses will be less because $V_{CE(SAT)}$ is lower than the data sheet value at currents less than rated I_C. When switching inductive loads the conduction losses for the free-wheel diode must be considered. Free-wheel diode losses can be approximated by multiplying the data sheet V_{EC} by the expected average diode current.

Switching Losses

Switching loss is the power dissipated during the turn-on and turn-off switching transitions. In high frequency PWM switching losses can be substantial and must be considered in thermal design.

The most accurate method of determining switching losses is to plot the I_C and V_{CE} waveforms during the switching transition. Multiply the waveforms point by point to get an instantaneous power waveform. The area under the power waveform is the switching energy expressed in Watt-seconds/pulse or J/pulse. The area is usually computed by graphic integration.

Digital oscilloscopes with waveform processing capability will greatly simplify switching loss calculations.

The standard definitions of turn-on ($E_{SW(on)}$) and turn-off ($E_{SW(off)}$) switching energy is given in Figure 5.26. The waveform shown is typical of hard switched inductive load applications such as motor drives. From Figure 5.26 it can be observed that there are pulses of power loss at turn-on and turn-off of the IGBT.

The instantaneous junction temperature rise due to these pulses is not normally a concern because of their extremely short duration. However, the sum of these power losses in an application where the device is repetitively switching on and off can be significant. In cases where the operating current and applied DC bus voltage are constant and, therefore, $E_{SW(on)}$ and $E_{SW(off)}$ are the same for every turn-on and turn-off event, the average switching power loss can be computed by taking the sum of $E_{SW(on)}$ and $E_{SW(off)}$ and dividing by the switching period T. Noting that dividing by the switching period is the same as multiplying by the frequency results in the most basic equation for average switching power loss:

$$P_{SW} = f_{SW} \times (E_{SW(on)} + E_{SW(off)})$$

where:

f_{SW} = switching frequency

$E_{SW(on)}$ = turn-on switching energy

$E_{SW(off)}$ = turn-off switching energy

The turn-on loss includes the losses caused by the hard recovery of the opposite free-wheel diode. The critical conditions including junction temperature (T_j), DC bus voltage (V_{CC}), and control supply voltage (V_D) are given on the curves. Switching energy curves like these are available for all DIP-IPMs. Switching energy curves are very useful for initial loss estimation. In applications where the operating current and applied DC bus voltage are constant the average switching power loss can be computed by reading $E_{SW(on)}$ and $E_{SW(off)}$ from the curves at the operating current and using the equation given above. In applications where the current is changing such as in a sinusoidal output inverter the loss computation becomes more complex. In these cases it is necessary to consider the change in switching energy at each switching event over a fundamental cycle.

A method for loss estimation in a sinusoidal output PWM inverter is given in Section 5.6.2. Final switching loss analysis should always be done with actual waveforms taken under worst case operating conditions. The main use of the

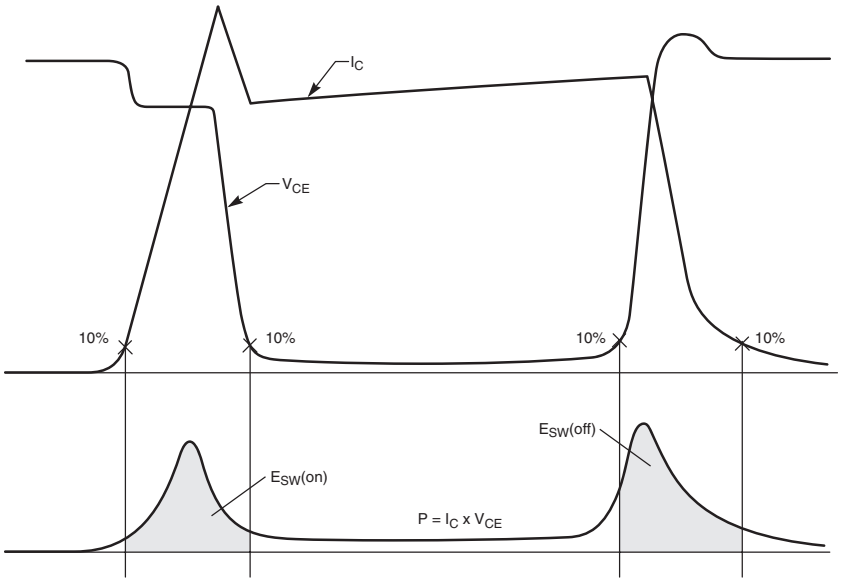


Figure 5.26 Switching Losses

estimated power loss calculation is to provide a starting point for preliminary device selection. The final selection must be based on rigorous power and temperature rise calculations.

5.6.2 VVVF Inverter Loss Calculation

The most common application of DIP-IPMs is the variable voltage variable frequency (VVVF) inverter. In VVVF inverters, PWM modulation is used to synthesize sinusoidal output currents. Figure 5.27 is a typical VVVF inverter circuit and output waveform. In this application the IGBT current and duty cycle are constantly changing making loss estimation very difficult.

The Powerex IGBT application note provides a general description of the methodology for loss estimation and thermal system design. The Mitsubishi Average Loss Simulation Software is also a very powerful tool for estimating power loss.

The following steps take you through an example calculation estimating losses with a PS21964 using the simulator:

1) Start the simulation software.
2) Click on the (IGBT icon) in the tool bar.
3) Select IPM from the division pull down menu.
4) Select IPM L-series from the series pull down menu.
5) Select PS21964 from the module pull down menu.
6) Click the OK button
7) Enter the application conditions. (Typical application conditions for the device will be entered as a default.)

Application conditions are as follows:

Icp: Peak collector current
Vcc: Bus Voltage
Fsw: Switching Frequency
Tf: Heatsink Temperature
Rg: Resistivity of Gate Resistor
PF: Power Factor

8) Click the (equal icon) in the tool bar.

Simulator results for the PS21964 are shown in Figure 5.28.

The initial results displayed by the simulator are a steady state approximation and are as follows:

Tj (IGBT) Chip junction temperature for the IGBT
Tj (Diode) Chip junction temperature for the free-wheeling diode
P(IGBT) Power loss by each IGBT
P(Diode) Power loss by each diode
P(Total) Sum of power loss from all diode and IGBTs in the module

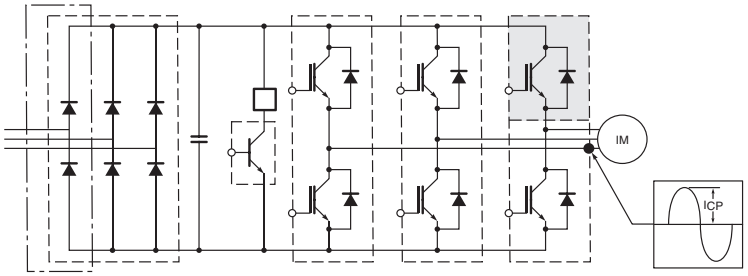


Figure 5.27 Typical VVVF Inverter Circuit and Output Waveform

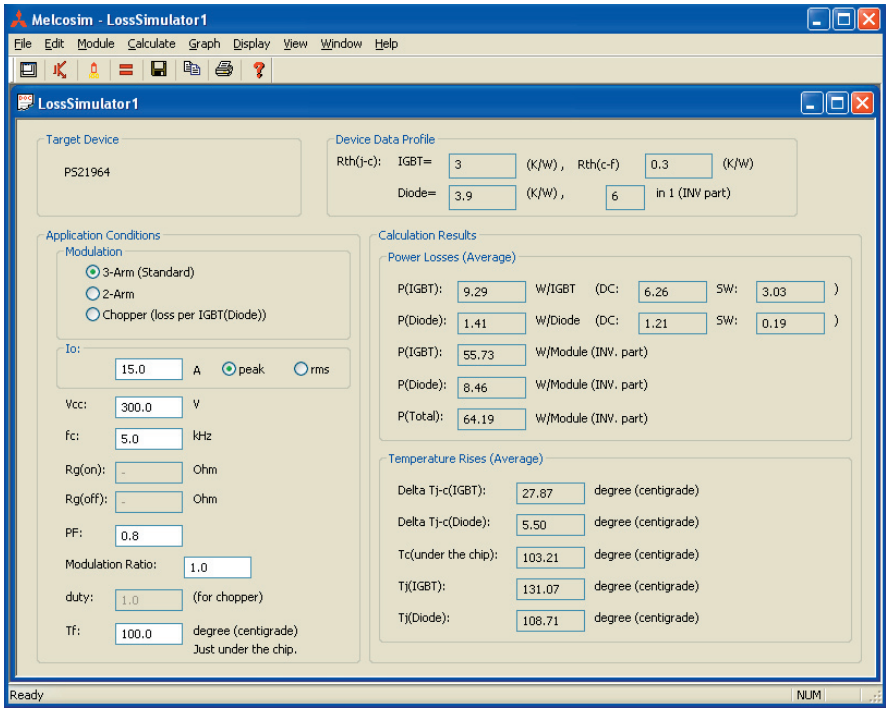


Figure 5.28 PS21964 Power Loss Simulation

Once the simulator has made power loss calculations, you can choose a variety of power loss curves from the Graph menu in the tool bar as shown in Figure 5.29.

Figure 5.30 shows total power dissipation versus switching frequency while Figure 5.31 shows total power dissipation versus collector current for the PS21964. Both graphs have separate curves for IGBT and diode losses.

Table 5.8 shows a comparison of the effective output current at a 5kHz and 15kHz switching frequency for several Super-Mini DIP-IPMs. These values were obtained by entering the values given above the table into Melcosim. It is important to notice the differences in the available output current shown on this table versus what is shown in Table 2.1. The variations rise from the differing heatsink temperature (T_f). Maintaining a low heatsink temperature allows the DIP-IPM user to operate at higher currents without exceeding the maximum junction temperature (T_j) rating of the DIP-IPM.

It is pertinent not to exceed any of the DIP-IPMs maximum ratings. When using Melcosim or other methods of loss estimation it is recommended to not construct a design that would cause there to be a current in excess of 1.7 times the devices current rating and to maintain a junction temperature of less than 125°C. These recommendations are reflected in the effective output currents shown on Tables 2.1 and 5.8.

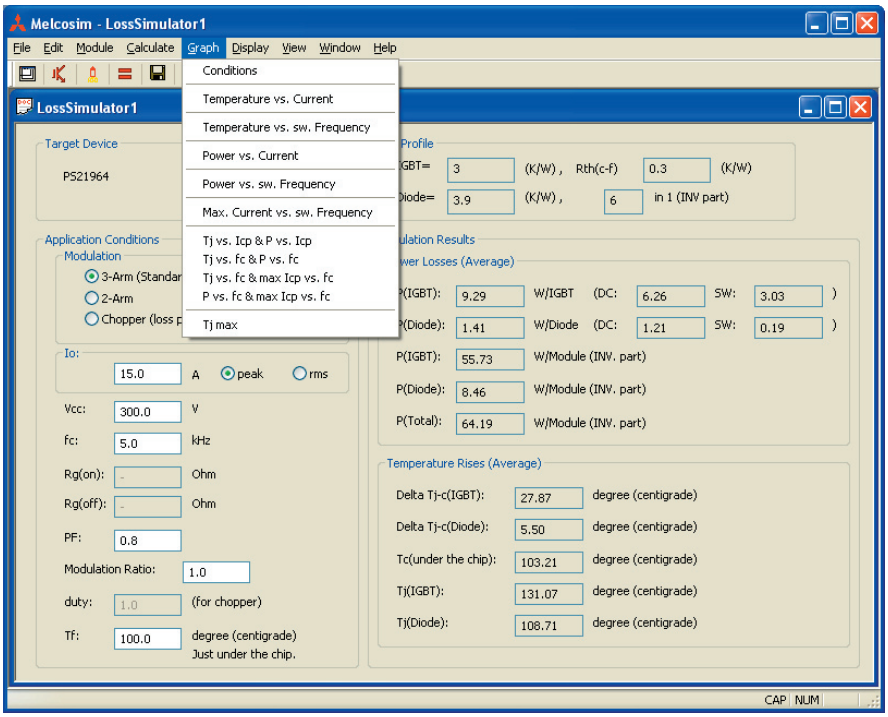


Figure 5.29 Graph Menu Options

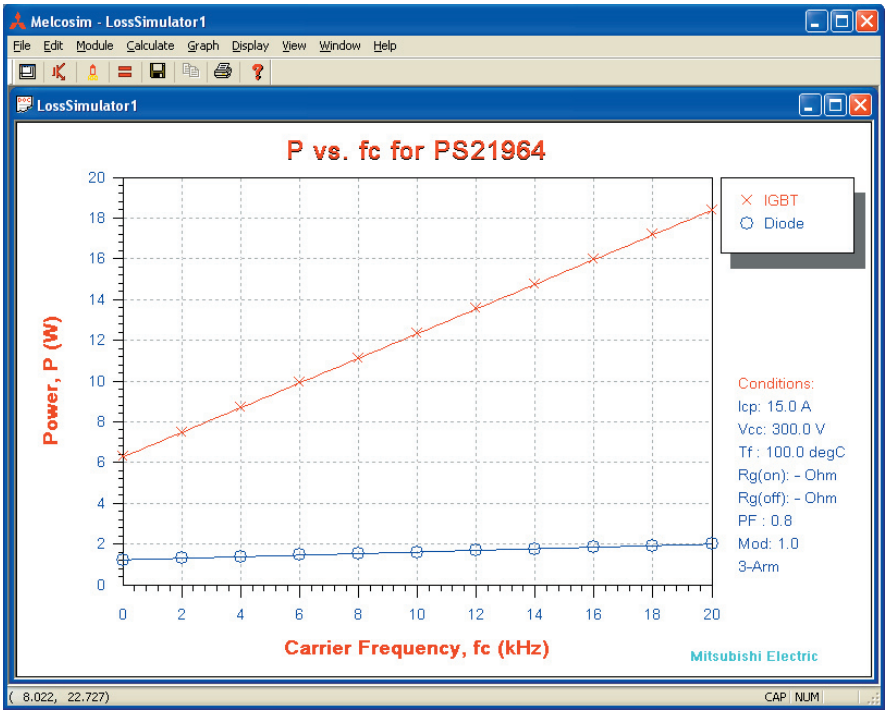


Figure 5.30 PS21964 Total Power Loss vs Switching Frequency

5.6.3 Power Cycling Life

A final thermal design consideration is the temperature range, ΔT_j, through which the junction will cycle as the equipment operates in actual application. The concern here is what is called thermal fatigue. That is, as the component parts of the module heat and cool due to collector power dissipation there are mechanical stresses caused by the different coefficients of expansion of the various component materials. This differential expansion puts the intermediate layers under bending and shear stress. With the accumulation of these stress cycles the assembly structure can deteriorate causing eventual failure. Studies of this phenomenon involve tests at multiple operating points to create curves that indicate cycling life as a function of the ΔT_j excursion. These curves are specific to particular temperature, time, and operating ranges, so that a general curve cannot be generated. Figure 5.48 is an example curve taken for modules using the test setup shown in Figure 5.33. All available information has indicated that thermal fatigue is not an issue when ΔT_j is kept below 30°C. Repetitive operation of short-circuit protection will result a repeated large temperature change of the IGBT (ΔT_j), and therefore shorten the device life-cycle expectancy. The SC protection function designed to protect the DIP-IPM from non-repetitive short-circuit conditions. Therefore, it is best practice to stop operation of the device when there is a fault. For applications involving a large number of power cycles in conjunction with junction temperature excursions greater than 30°C the application should be reviewed in detail with Powerex application engineers.

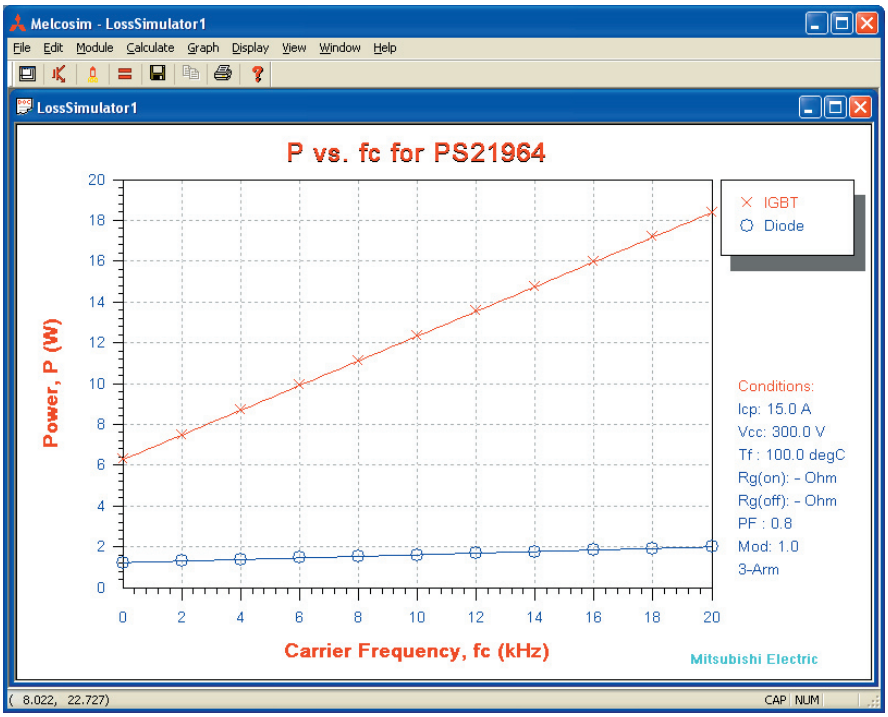


Figure 5.31 PS21964 Total Power Loss vs I_C

Table 5.8 Effective Output Current at 5kHz and 15kHz Switching Frequencies

Sinusoidal RMS Current per Phase, V_{CC} = 300V, V_D = 15V, PF = 0.8, T_j = 125°C, T_f = 100°C

Part Number	Current (Amperes)	Voltage (Volts)	f_C = 5kHz	f_C = 15kHz
PS21962 (-A/S/T)	5	600	5.4	3.8
PS21963-E (-A/S/T)	8	600	6.6	4.5
PS21963 (-A/S/T)	10	600	7.2	4.7
PS21964 (-A/S/T)	15	600	8.9	5.7
PS21965 (-A/S/T)	20	600	10.3	6.5

5.7 Noise Withstand Capability

Large common mode dV/dt noise on the AC input line may cause the DIP-IPMs to malfunction. This section describes measurement techniques and countermeasures against this kind of failure.

5.7.1 Measurement Circuit

Figure 5.34 shows the measurement test circuit for input common mode noise. Using this circuit, ±2kV withstand capability has been confirmed for noise test of the DIP-IPMs. However, noise withstand capability heavily depends on the wiring patterns, parts layout and other factors. We therefore recommend that the noise test be performed on the actual finished system.

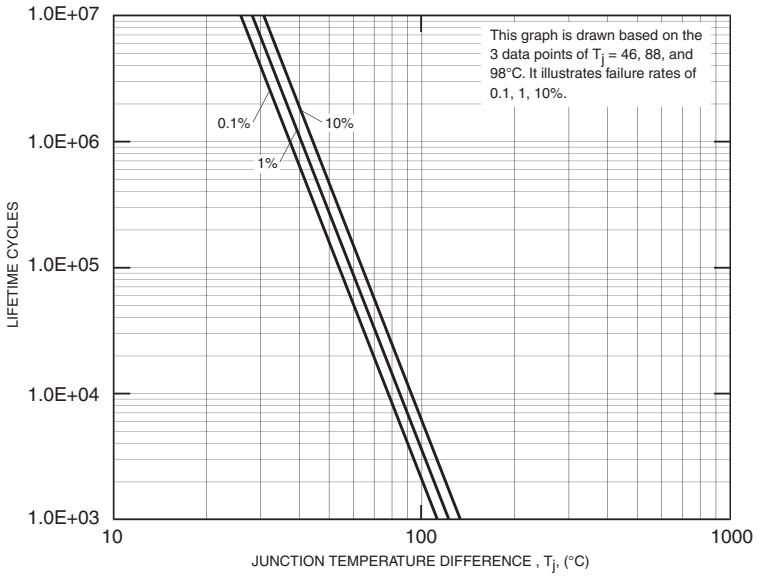


Figure 5.32 Power Cycling Curve

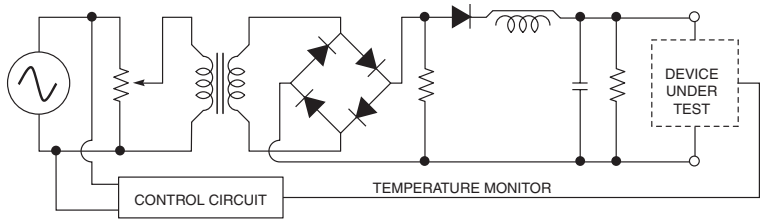
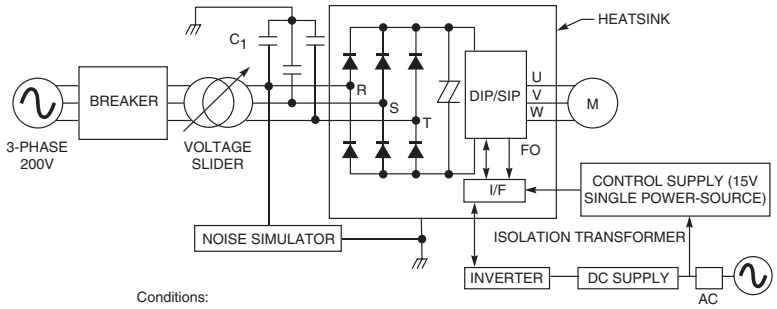


Figure 5.33 Power Cycle Test Circuit



Conditions:
V_{CC} = 300V, V_D = 15V, T_a = 25°C, no load
50nS-1μS wide pulses are applied at a random point in each 60Hz (16ms) cycle.

Notes:
1) C_1 is 4700pF AC line common-mode filter.
2) 15V single power source
3) PWM signals are supplied directly from the controller and through the optocoupler.
4) Test is performed for both induction and brushless DC motors.
(3 and 4 mean that there are a total of 4 different tests - 2 different motors each with 2 different signal interface circuits.)

Figure 5.34 Noise Test Measurement Circuit

5.7.2 Countermeasures

There were noise countermeasures implemented within the DIP-IPMs. They achieve improved noise withstand capability through optimized internal wiring to reduce inductance and optimized isolation to reduce leakage current to the heatsink.

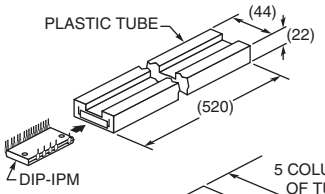
There are also noise countermeasures that can be executed outside of the DIP-IPMs. They are as follows:

- Improving power supply filtering (close to DIP-IPM terminals)
- Lowering impedance at fault line (reducing pull-up resistance)
- Adding RC filter on the control inputs
- Reduce length of wiring on control inputs

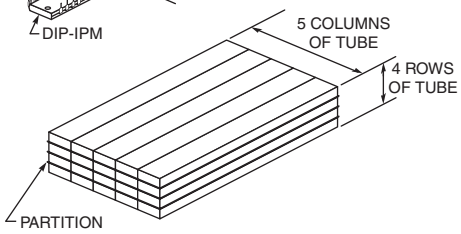
6.0 Packaging and Handling

DIP-IPM Packaging Specification

Per tube:
6 pieces of DIP-IPM per tube

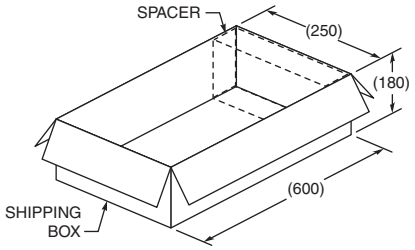


Per package (max):
Total number of tubes is 20.
(5 columns, 4 rows)
Total number of DIP-IPMs is 120.
(20 tubes, 6 pieces)



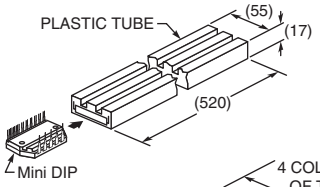
Weight:
Approximately 65g per DIP-IPM
Approximately 490g per tube
Approximately 11kg per package

(The above weights are ones when the maximum number of DIP-IPMs are packaged.)

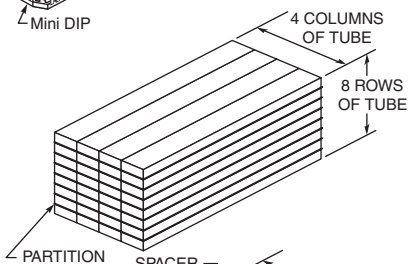


Mini DIP-IPM Packaging Specification

Per tube:
10 pieces of Mini DIP-IPM per tube

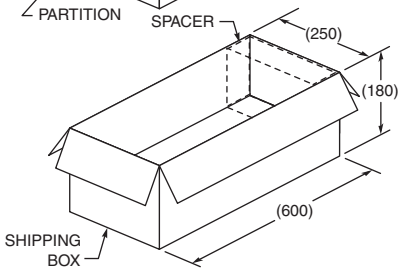


Per package (max):
Total number of tubes is 32.
(4 columns, 8 rows)
Total number of Mini DIP-IPMs is 320.
(32 tubes, 10 pieces)



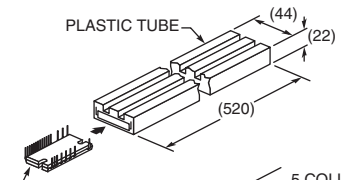
Weight:
Approximately 20g per Mini DIP-IPM
Approximately 310g per tube
Approximately 12kg per package

(The above weights are ones when the maximum number of Mini DIP-IPMs are packaged.)

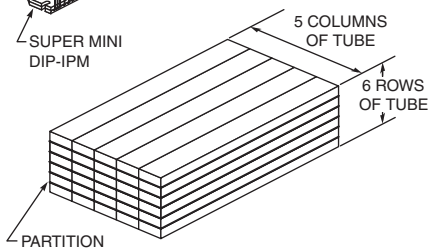


Super-Mini DIP-IPM Packaging Specification

Per tube:
12 pieces per 1 tube



Per package (max):
Total number of tubes is 30.
(5 columns, 6 rows)
Total number of DIP-IPMs is 360.
(30 tubes, 12 pieces)



Weight (max.)
Approximately 10g per 1pcs of DIP-IPM
Approximately 120g per 1 tube
Approximately 3.6kg per 1 box

(The above weights are ones when the maximum number of SIP-IPMs are packaged.)