A GaN HEMT Class F Amplifier at 2 GHz With $>80\%$ PAE

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***Abstract*—A Class F amplifier has been designed, fabricated, and tested using a GaN HEMT transistor and hybrid printed circuit board (PCB) packaging. The amplifier has a peak power-added efficiency (PAE) of 85% with an output power of 16.5 W. A gate-connected field-plated and a source-connected field-plated device of the same size and layout were measured in this topology. An output power and drain efficiency tradeoff, dependant on the drain impedance at the fundamental frequency due to the on-state resistance, is explored. A comparison between Class F and Inverse F, given particular operating conditions for this device, is made.**

***Index Terms*—Class F, field plate, GaN HEMT, inverse F.**

I. Introduction

A CLASS F amplifier can approach a theoretical 100% drain efficiency by wave shaping the intrinsic drain voltage and current waveforms [1]. When the amplifier is driven into saturation and the device is biased at cutoff, the voltage waveform is clipped and can be shaped like a square wave, and the current waveform can be shaped like a half sine wave with proper harmonic terminations. The voltage and the current waveforms do not overlap, eliminating the power dissipation in the switch. The squared voltage waveform contains only odd harmonic frequencies. Ideally, it must have all of the odd harmonics terminated with an open circuit at the intrinsic drain of the transistor. The half sine wave current waveform only contains even harmonics, and all the even harmonics need a short circuit termination for the harmonic current.

For an RF amplifier, it is not practical to terminate an infinite number of harmonics nor will they be present. Raab has shown that most of the gain in efficiency due to wave shaping can be had with just the first few harmonics present and correctly terminated [1]. For drain waveforms with up to and including the fourth harmonic present and terminated correctly, the efficiency of an ideal amplifier can be as high as 86%. In this Fourier analysis of the drain waveforms, no other harmonics beyond the fourth are present.

Realistically, the efficiency of the amplifier is limited by the transistor drain-source capacitance, $C_{\rm ds}$, its on-state resistance, $R_{\rm on}$, or knee voltage and power dissipation in the output and bias networks. $C_{\rm ds}$ is often difficult to absorb into a multiple harmonic matching network without compromising the ability to terminate higher harmonics. A device with a high $f_{\rm max}$ compared to the fundamental operating frequency is helpful to generate the higher order harmonics needed for waveshaping. In this respect, GaN HEMT transistors are good candidates for Class F amplifiers. GaN transistors have demonstrated a significantly higher power density ($>10\times$) than their GaAs and Si counterparts [2], resulting in lower input and output capacitances for the same power output. Like LDMOS, they have higher peak operating voltages and consequently higher drain impedances at the operating frequency, but the larger output capacitances of LDMOS reduce the maximum frequency that a switching amplifier can be designed for.

Several published reports have presented Class F amplifiers with power-added efficiencies (PAEs) up to 77% with GaAs transistors about the operating frequency of 2 GHz. To the authors' knowledge, there has not been a published report of a Class F with greater than 10 W of power and 80% PAE in this frequency range. A Class E amplifier with a similar GaN HEMT transistor from Cree has been demonstrated to have 85% PAE and 10 W output power in [3]. Implementing a Class F or Inverse F amplifier with a GaN transistor is very promising because of the greater power output capability compared to a Class E amplifier using the same transistor [4]. This paper demonstrates a successful Class F amplifier design using a GaN HEMT transistor.

II. Design

The GaN HEMT devices on a SiC substrate used in this amplifier were provided by Cree and have a 3.6 mm gate periphery and an estimated $f_{\rm max}$ of 40 GHz. The HEMT in the initial amplifier has a gate-connected field plate associated with the gate and the transistor has a breakdown voltage $V_{\rm br}$ greater than 90 V. An amplifier with an identically sized source-connected field-plated device was also fabricated and tested. The amplifier was designed to maximize PAE while maintaining a high output power for an operating frequency of 2 GHz.

A. Power and Efficiency

In [1], the calculations were based on an ideal amplifier with zero $R_{\rm on}$, where the voltage across the drain to the source is zero when the transistor is conducting. If the on-state resistance is added to the transistor model, there is a voltage drop $V_{\rm min}$ across the transistor when it is conducting. This causes power to be dissipated, equal to $R_{\rm on}\cdot I_{\rm rms}^2$, and the peak voltage swing is reduced, resulting in a drop of the expected efficiency. The waveform factors, (1) and (2), derived in [1] to relate fundamental amplitudes γ and peak waveform values δ to the DC

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values, can still be used but must include $V_{\min}$ to account for the effect $R_{\rm on}$ has on the drain efficiency and output power.

$$V_{\rm om} = \gamma_V (V_{\rm DD} - V_{\min}),\ V_{\max} = \delta_V (V_{\rm DD} - V_{\min}) + V_{\min} \quad \text{(1a-b)}$$

$$I_{\rm om} = \gamma_I I_{\rm DC},\ I_{\max} = \delta_I I_{\rm DC}. \quad \text{(2a-b)}$$

Continuing from (1) and (2), the output power, (3a), and drain efficiency, (4), are found with a dependency on $V_{\min}$. The intrinsic drain impedance R_L at the fundamental frequency is defined by (3b). This is defined at the intrinsic drain, such that $C_{\rm ds}$ and other transistor parasitic elements are absorbed into the output matching network. Equations (3) and (4) show that increasing $V_{\rm DD}$ and minimizing $V_{\min}$ will maximize drain efficiency and output power.

$$P_{\rm out} = \frac{V_{\rm om}^2}{2R_L} = \frac{\gamma_V^2 V_{\rm DD}^2}{2R_L}\left(1 - \frac{V_{\min}}{V_{\rm DD}}\right)^2,\ R_L = \frac{V_{\rm om}}{I_{\rm om}} \quad \text{(3a-b)}$$

$$\eta = \frac{P_{\rm out}}{P_{\rm dc}} = \frac{\gamma_V \gamma_I}{2}\left(1 - \frac{V_{\min}}{V_{\rm DD}}\right). \quad (4)$$

In order to make a first-order comparison of the effect of transistor parameters of different technologies, such as $R_{\rm on}$ and $V_{\rm br}$, a value for $V_{\min}$ must be estimated or calculated. The nonlinearities of driving the transistor into the linear or ohmic region make it hard to predict the actual $V_{\min}$ in simulation and in practice. Therefore, to make meaningful first-order comparisons, it is easier to assume an ideal transistor with a fixed $R_{\rm on}$ and ideal drain waveforms. In this case, the peak current $I_{\max}$ and $V_{\min}$ will coincide, and $V_{\min}$ is equal to the product of $R_{\rm on}$ and $I_{\max}$ shown in (5). $P_{\rm out}$ and drain efficiency are related to $R_{\rm on}$, $V_{\rm DD}$, R_L, and the ideal waveform factors in (6) and (7) using (3), (4), and (5).

Assuming that R_L is in an appropriate range such that the transistor is driven between the linear region and current cutoff, this simplified calculation will give drain efficiency trends for values of $P_{\rm out}$, $R_{\rm on}$, $V_{\rm DD}$, and R_L. Comparisons can be made between different technologies, operating conditions such as drain bias and load resistance, and between ideal Class F and Inverse F amplifiers.

$$V_{\min} = R_{\rm ON} I_{\max} = R_{\rm ON} \delta_I I_{\rm DC} \quad (5)$$

$$P_{\rm out} = \frac{\gamma_V^2 V_{\rm DD}^2}{2R_L}\left(\frac{1}{1 + \delta_I \frac{\gamma_V}{\gamma_I}\frac{R_{\rm ON}}{R_L}}\right)^2 \quad (6)$$

$$\eta = \frac{\gamma_V \gamma_I}{2}\left(\frac{1}{1 + \delta_I \frac{\gamma_V}{\gamma_I}\frac{R_{\rm ON}}{R_L}}\right). \quad (7)$$

The equations (6) and (7) do present the general trends for Class F and Inverse F amplifiers in their normal range of operation. Drain efficiency increases as R_L is increased but at the expense of output power. For demonstration purposes, $V_{\rm DD}$ can be set so that the peak voltage is approximately equal to the breakdown voltage of the device to achieve the highest output power for a given efficiency determined by R_L. For more reliable and stable operation, a $V_{\rm DD}$ should be set so that the peak drain voltage is 20% below $V_{\rm br}$.

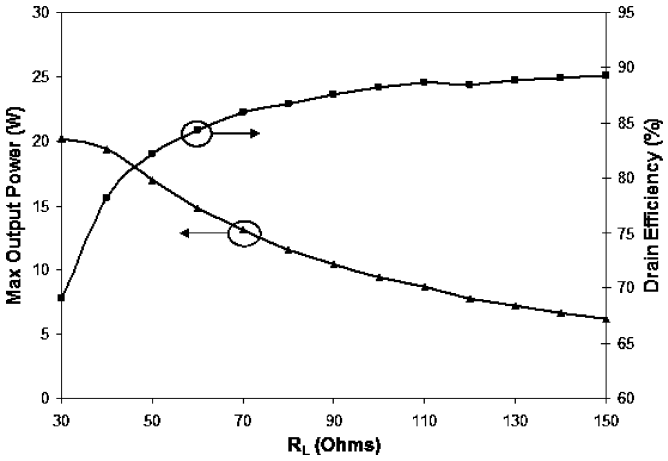

Fig. 1. Simulation results at 2 GHz: output power and drain efficiency at maximum PAE versus R_L.

B. Drain Impedance

Examining (7), it is evident that increasing R_L will increase efficiency at the expense of $P_{\rm out}$. This effect is much more pronounced for GaN transistors when compared to GaAs devices, which need much lower drain impedances to accommodate the lower operating voltages. For lower frequencies with the GaN devices, where a larger device's extra capacitance can be tolerated, a larger R_L can be used to mitigate the loss of efficiency due to $R_{\rm on}$.

Fig. 1 shows results of a harmonic balance simulation of the large signal GaN transistor model with the intrinsic drain ideally terminated with the second, third, and fourth harmonics. The transistor's input is optimally matched at the fundamental frequency, and the second harmonic impedance is short circuited. Since a large signal model is used, there are higher order harmonics beyond the fourth order present at the input and the output of transistor. All these higher order input and output harmonics in the simulation are terminated by 50 ohms. The transistor's gate is biased at cutoff and the drain bias voltage is set to 40 V. The high breakdown voltage of the transistor allows for a tradeoff of power for efficiency by the choice of R_L. The graph displays the drain efficiency and output power at maximum PAE versus R_L. This simulation predicts best case performance since there are no passive network losses and includes the condition that the higher order harmonics are terminated by 50 ohms. The maximum drain efficiency observed in this simulation is 89.3% at the highest value of R_L simulated. When the transistor is matched to a R_L larger than 150 ohms, there is an excessive loss in gain, and when matched to a R_L smaller than 40 ohms, the drain waveforms are distorted by driving the transistor excessively into the knee region. The efficiency is higher than the predictions based on waveform analysis in [1] because the transistor generates quite a bit more harmonic content beyond the fourth harmonic. Even though these harmonics are not terminated optimally, they contribute to a higher than expected efficiency.

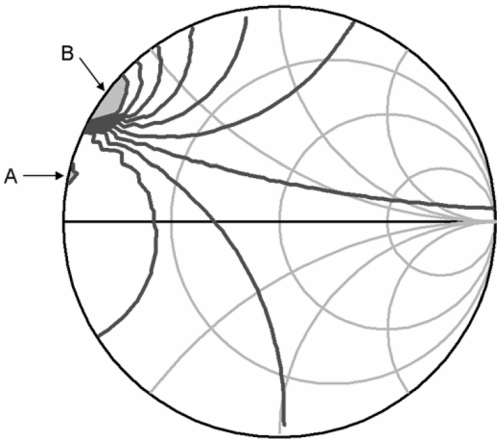

Fig. 2. Source pull simulation of PAE contours for the second harmonic input termination. PAE at region A equals 84%, PAE at region B equals 35%. PAE contours – 5% steps.

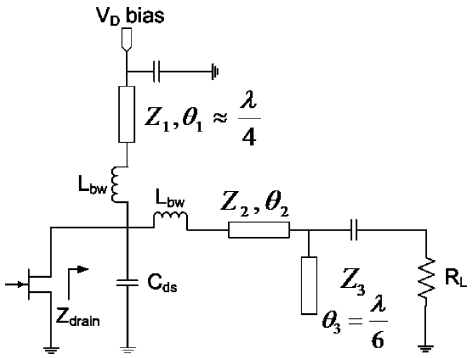

Fig. 3. The output matching network that presents approximately $Z_{\rm drain}$ to the intrinsic drain of the transistor.

C. Input Harmonic Matching

It has been observed in [5] and [6] that the input matching network must have proper harmonic terminations at the transistor's gate to preserve a sinusoid drive at the gate due to the nonlinear $C_{\rm gs}$. A simulation of a source pull for the second harmonic termination, Fig. 2, indicated that the Class F amplifier would have the highest PAE, 84%, at R_L of 70 ohms given a second harmonic termination near a short circuit at the region marked by A. Surprisingly, the impedance with the worst PAE of 35% has only 16 degrees of phase difference from the optimum point in the region marked by B. The proximity of the best and worst second harmonic terminations are much closer than observed by [6] using a GaAs pHEMT transistor.

Further simulation has shown that at 5% higher fundamental frequency, the extreme performance differences are still at the same input impedances. This could present a bandwidth limitation, as it would be natural for the phase of the impedance of an input network to increase in the direction of region B. Therefore, it is crucial to accurately model the second harmonic input termination presented to this transistor.

III. Implementation and Experimental Results

The output matching network must absorb $C_{\rm ds}$ and the interconnect inductance while providing the correct fundamental and harmonic resistances at the intrinsic drain of the transistor.

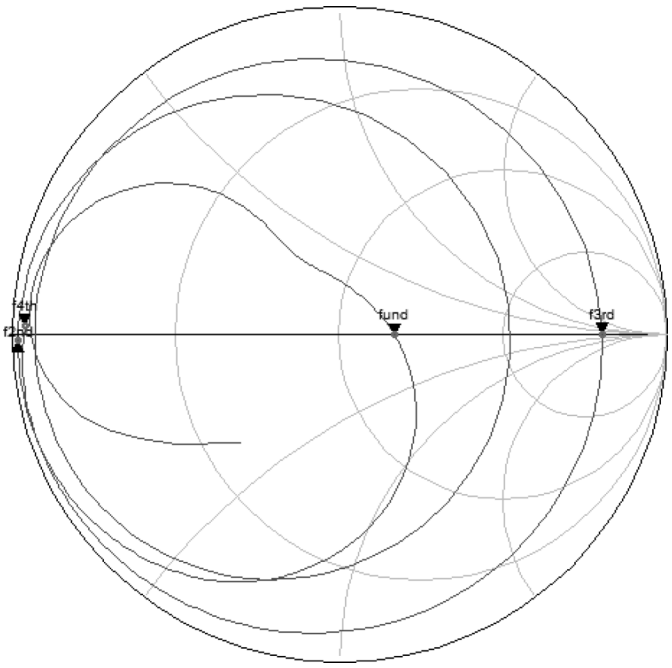

Fig. 4. Plot of the impedance presented to the intrinsic drain versus frequency. Markers indicated the impedances at the harmonic frequencies.

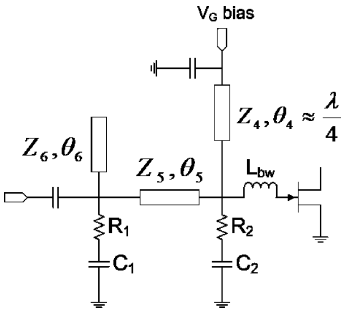

Fig. 5. The input matching network.

It is beneficial if the matching network can be tuned to different values of R_L so the amplifier can be designed for different supply voltages, especially for GaN transistors which can be matched to a range of impedances due to the high breakdown voltage capability.

Fig. 3 illustrates a matching network that can accomplish this. Two separate bondwires are used at the drain pad and approximated by $L_{\rm bw}$. This allows the bondwire inductance to be incorporated into the quarter-wave length drain bias transmission line giving the lowest even harmonic impedances at the drain. Z_2, θ_2, and Z_3 can be tuned to absorb $C_{\rm ds}$ and $L_{\rm bw}$ and simultaneously present a real impedance at the fundamental, R_L, and a very high real impedance at the third harmonic. Effectively, both matching networks terminate the second, third, and fourth harmonics and some of the higher order even harmonics as well.

An intrinsic drain impedance of 70 ohms was chosen for the design as it was a good tradeoff of efficiency and output power. Tuning the output matching network in Fig. 3 to a R_L equal to 70 ohms resulted in a third harmonic impedance of about 400 ohms. The second harmonic impedance was about 0.5 ohms and the fourth harmonic was about 0.7 ohms. Fig. 4 is a plot of

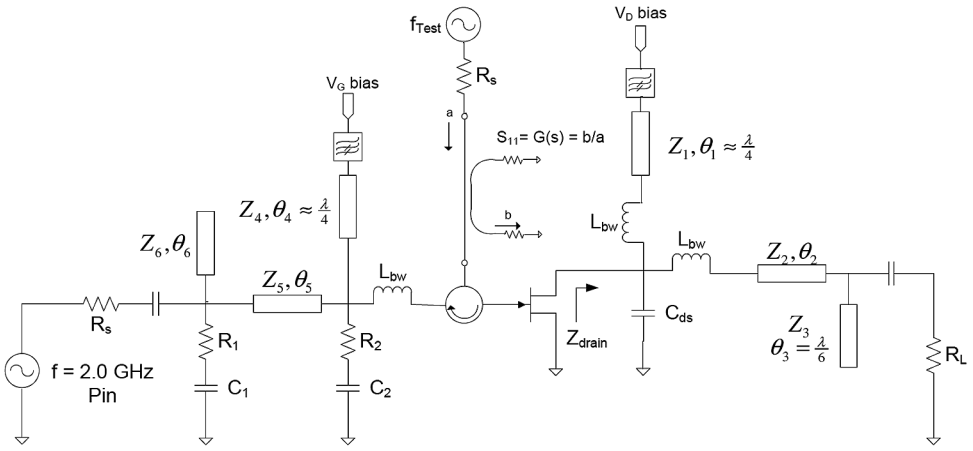

Fig. 6. Measuring the open-loop transfer function, $G(s)$.

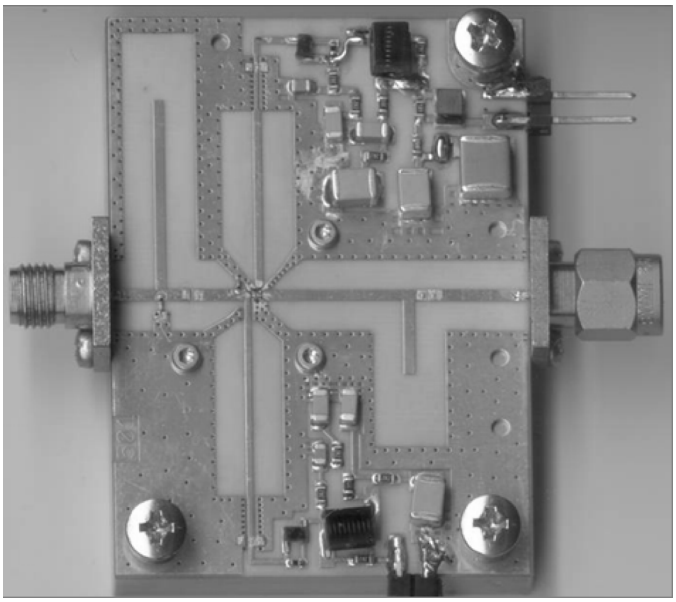

Fig. 7. Picture of amplifier.

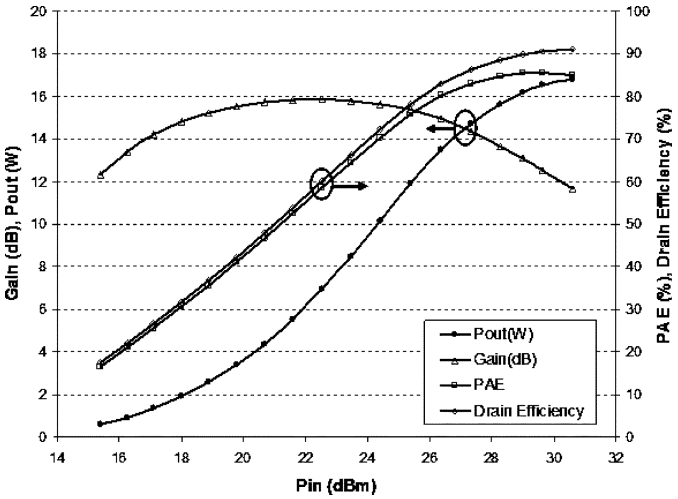

Fig. 8. Measured gain, PAE, and drain efficiency at 2 GHz with 42.5 V drain bias.

the impedance presented to the intrinsic drain versus frequency. Markers indicate the impedances at the harmonic frequencies.

The output matching network topology is a particularly good fit for this GaN transistor with a $C_{\rm ds}$ of about 0.9 pF. The output matching network was capable of tuning R_L from 25 to 120 ohms while maintaining a high third harmonic impedance and realizable transmission line impedance.

An input matching network was synthesized, Fig. 5, that provides a second harmonic short and fundamental match. A quarter-wave length transmission line, Z_4 and θ_4, located close to the gate provides the second harmonic input termination. The length of this line, θ_4, can be adjusted after fabrication to optimize the harmonic termination's phase. Two *RC* networks were added to provide stability. Stability was evaluated by a method similar to that used by [7]. A simulation with an ideal circulator was used to determine an open-loop transfer function of the amplifier, $G(s)$, as shown in Fig. 6. The Nyquist condition for stability is that the poles of the closed-loop transfer function have negative real parts. This condition is not true if the plot of $G(s)$ on the complex plane encloses the point $1+j\cdot 0$. This enabled stabilization by the *RC* networks without excessive loss in gain. Stability was tested over various input drive amplitudes and over a broad frequency range.

The amplifier was constructed on a low-loss printed circuit board (PCB) substrate with gold-plated traces mounted to a copper carrier. The GaN HEMT IC was directly mounted to the copper carrier and used wirebond interconnects. Fig. 7 shows a picture of the amplifier.

The amplifier was tested at 2 GHz and after some basic tuning to account for the differences between the transistor model and the actual device, the peak performance measured is in Fig. 8. Only the fundamental frequency component was measured for the results. The amplifier had a peak PAE of 85.5% with an output power of 16.5 W with a drain bias voltage of 42.5 V. The peak gain was 15.8 dB, and it had a compressed gain at peak PAE of 13.0 dB. The peak drain efficiency was 91%.

The measured performance of the amplifier at the peak PAE with respect to drain bias voltage is in Fig. 9. The peak PAE is above 80% for drain voltages greater than 27 V.

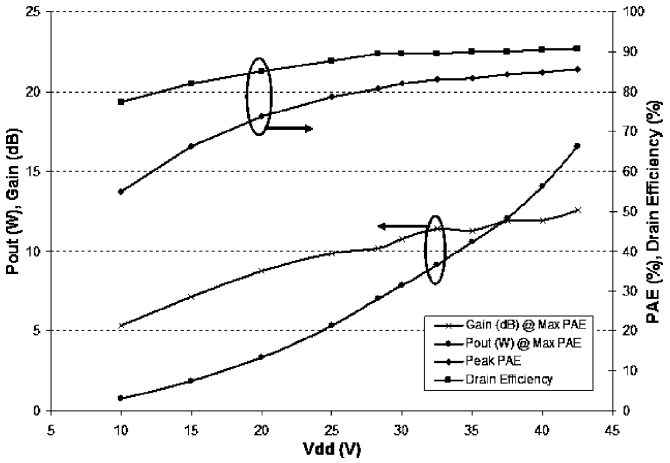

Fig. 9. Measured gain, output power, peak PAE, and drain efficiency at 2 GHz with respect to drain voltage bias.

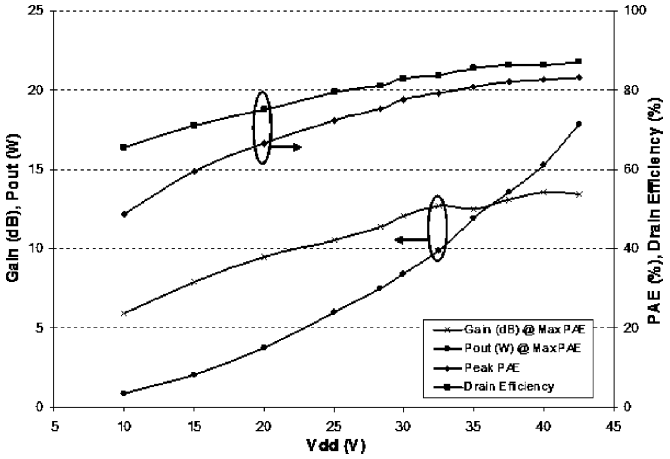

Fig. 10. Performance of amplifier with source-connected field-plated transistor. Measured gain, output power, peak PAE, and drain efficiency at 2 GHz with respect to drain voltage bias.

A similar amplifier was constructed with a source-connected field-plated GaN HEMT transistor of the same gate periphery and pad layout from Cree. No major modifications to the matching networks were made. The measured performance of the amplifier at the peak PAE with respect to drain bias voltage is in Fig. 10. The amplifier had a peak PAE of 83.0% with an output power of 17.8 W with a drain bias voltage of 42.5 V. The peak gain was 15.8 dB, and it had a compressed gain at peak PAE of 13.4 dB. The peak drain efficiency was 87%. The peak PAE is above 80% for drain voltages greater than 32.5 V. The performance was comparable to the gate-connected field-plated transistor for higher drain bias voltages and the gain very similar, but the performance drops faster with decreasing drain bias. According to the device designer, the $f_{\max}$ of the transistor with the source-connected field plate is about the same as the original device. The added field plate is said to improve the maximum stable gain. It also adds extrinsic gate-source and drain-source capacitance to the device. The peak performance of the two amplifiers was comparable, suggesting the circuit topology is somewhat insensitive to the device differences.

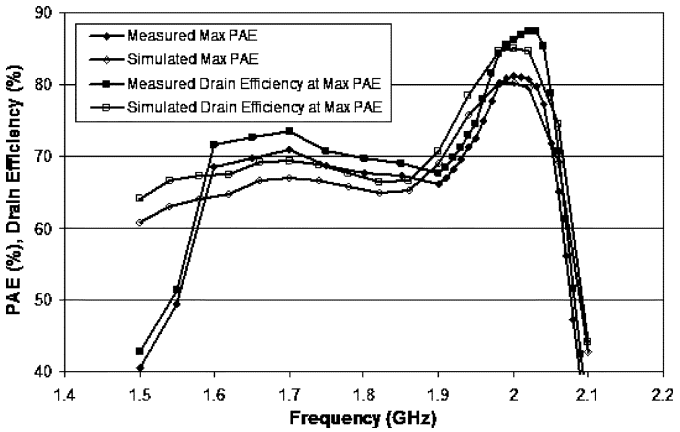

Fig. 11. Measured and simulated PAE and efficiency of amplifier with source-connected field-plated transistor.

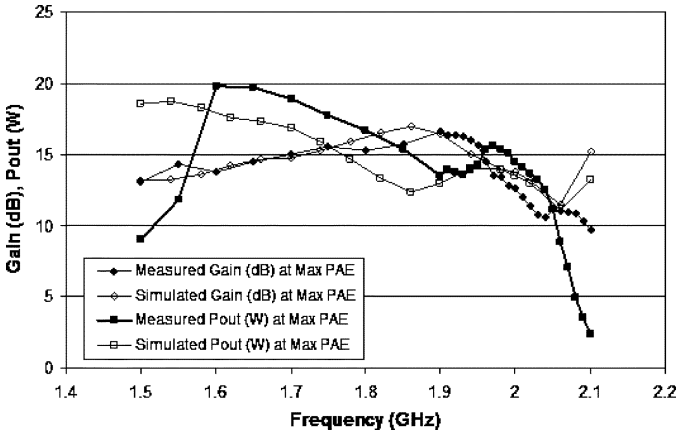

Fig. 12. Measured and simulated gain and output power of amplifier with source-connected field-plated transistor.

Figs. 11 and 12 show the comparison of the measured and simulated performance of the source-connected field-plated amplifier over frequency. There is good agreement between measured and simulation results. The performance rolls off at frequencies above 2.05 GHz primarily due the second harmonic input impedance of the matching network as discussed previously. The upper frequency limit can be extended at the expense of peak performance by shortening the quarter-wave line in the input network. The amplifier exhibits greater than 65% PAE and 12 W of output power between 1.6 GHz and 2.05 GHz, greater than a 20% bandwidth. For 75% PAE, the amplifier has a 4% bandwidth.

The measurements for both amplifiers exceed the simulation results for both efficiency and power. The simulation includes extensive 3-D modeling of all the packaging parasitics and predicts a peak PAE of 81%. The on-state resistance of the devices used in both amplifiers was measured by fully opening the transistor channel, applying a drain voltage close to the minimum voltage expected during full conduction and measuring the drain current. The gate-connected field-plated transistor had a measured $R_{\rm ON}$ of 0.96 ohms and the source-connected field-plated transistor had a $R_{\rm ON}$ of 1.45 ohms. From the simulated IV curves of the transistor model, the $R_{\rm ON}$ was found to be 2.35 ohms. Using (4) with ideal waveform factors, the effect of

the differences of the on-state resistances of the model and the measured device show a maximum expected 4.9% difference in drain efficiency. The model was conservative in its estimate of the performance, but overall it did predict the nonlinear behavior and bandwidth well.

The amplifiers were not evaluated for linearity. Since Class F operation requires significant gain compression to generate the higher harmonics, the carrier to intermodulation distortion ratio (C/IMD) will degrade rapidly. For example, [6] reports a two-tone measurement with a C/IMD of close to 20 dB for a GaAs Class F amplifier at peak efficiencies. Applications of Class F amplifiers that require high linearity would utilize EER or LINC style external linearization systems.

IV. Class F and Inverse F

Since the introduction of the inverse Class F amplifier [8], several papers have stated its superiority to the Class F amplifier for a given transistor. An ultimate comparison cannot be made, because one must consider the operating conditions and constraints. For instance, [9] demonstrated that an Inverse F amplifier has a higher efficiency than a Class F given that they are operating at the same drain bias and the peak voltage swings are less than the breakdown voltage.

If one would have to choose between the two amplifiers to maximize the PAE and output power using the same device, one would first need to consider the constraints the application presents. For instance, the drain bias may need to be fixed at a particular voltage because the amplifier will be used in a mobile application. Alternatively, if the amplifier would be used in a base station, the only constraint might be the device's own operating limits and the selection of the bias would be unconstrained.

Using (1), (2), and (5)–(7) and the waveform coefficients for a Class F and Class Inverse F found in [1], one can make an idealized comparison between the two. $P_{\rm out}$ and drain efficiency are found given $V_{\rm DD}$, R_L, and $R_{\rm on}$. The Class F and the Inverse F output power and efficiency are given in (8) and (9), respectively.

$$P_{\rm out} = \left(\frac{4}{\pi}\right)^2 \frac{V_{\rm DD}^2}{2R_L}\left(\frac{1}{1+\frac{8}{\pi}\frac{R_{\rm ON}}{R_L}}\right)^2, \quad \eta = \frac{1}{1+\frac{8}{\pi}\frac{R_{\rm ON}}{R_L}} \quad \text{(8a-b)}$$

$$P_{\rm out} = \left(\frac{\pi}{2}\right)^2 \frac{V_{\rm DD}^2}{2R_L^i}\left(\frac{1}{1+\frac{\pi^2}{4}\frac{R_{\rm ON}}{R_L^i}}\right)^2, \quad \eta = \frac{1}{1+\frac{\pi^2}{4}\frac{R_{\rm ON}}{R_L^i}}. \quad \text{(9a-b)}$$

In the first case of a fixed drain bias, to compare drain efficiency at equal output powers, one must solve for R_L for a given $P_{\rm out}$ and $R_{\rm on}$ for each amplifier, as they are not equal. In this case, the Inverse F has a larger R_L for the same output power. The Class F has a higher peak and rms current. Therefore, Inverse F has less power dissipated, $R_{\rm on} \cdot I_{\rm rms}^2$, in the transistor. As shown in [9], the drain efficiency is higher for the Inverse F for the same output power. Conversely, for the same drain efficiency, the Inverse F will have a higher output power.

To truly maximize the output power and drain efficiency of an amplifier, one must lift the constraint of fixing the drain bias so that it can be scaled such that the voltage swing across the device is as large as possible to diminish the effect of $R_{\rm on}$. $V_{\rm DD}$ and R_L for each amplifier can be solved for, given $P_{\rm out}$ and $R_{\rm on}$. Then drain efficiency can be calculated using (8) and (9). Fig. 13(a) and (b) illustrates the waveforms for both amplifiers given equal $V_{\max}$ and $P_{\rm out}$. The Class F amplifier has a higher $V_{\rm DD}$ and R_L, but a lower $I_{\rm rms}$. Therefore, the power dissipation, $R_{\rm on} \cdot I_{\rm rms}^2$, is lower than in the Inverse F and the Class F will have higher drain efficiency.

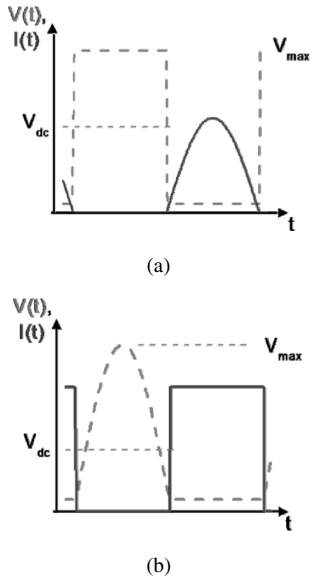

Fig. 13. (a) Ideal Class F drain waveforms with $R_{\rm on}$. Current is solid line and voltage is dashed line. (b) Ideal Inverse F drain waveforms with $R_{\rm on}$. Current is solid line and voltage is dashed line.

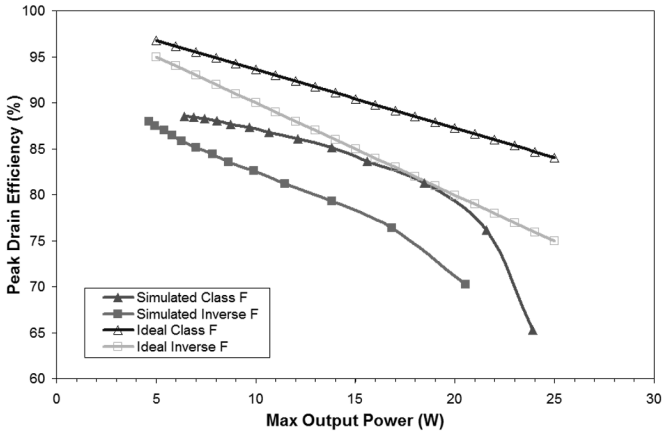

Fig. 14. Comparison of maximum drain efficiency versus peak output power of Class F and Inverse F amplifiers with a constant peak voltage of 80 V.

Using the large signal model of the GaN device, the calculated result was compared with simulations of both configurations of amplifiers. The simulations consisted of the amplifiers with the second and third output harmonics ideally terminated at the intrinsic drain. The second input harmonic was optimally terminated at the gate as well. The fundamental intrinsic drain impedance was swept and the peak drain efficiency and output power were measured. Comparing the simulations to the theoretical calculations in Fig. 14, good agreement in the slope and efficiency differences are observed. Therefore, when comparing amplifiers with the same device and equal peak voltages, the

Class F will have higher efficiency for the same output power or conversely higher $P_{\rm out}$ for the same efficiency.

V. Conclusion

GaN transistors offer the potential for significant improvement in the performance of Class F amplifiers over their GaAs counterparts. Implementing the amplifier in a hybrid PCB technology facilitates easy matching of higher order harmonics and results in high PAE. For a given technology, if the operational frequency considered is low, increasing the gate periphery to reduce $R_{\rm on}$ and increasing R_L will result in an efficiency improvement, perhaps at the expense of gain and bandwidth. For a given device, a Class F amplifier should ideally have higher drain efficiency than an Inverse F, when their peak voltages are equal.

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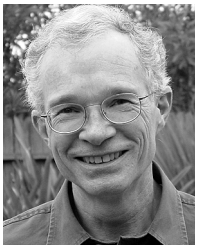

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