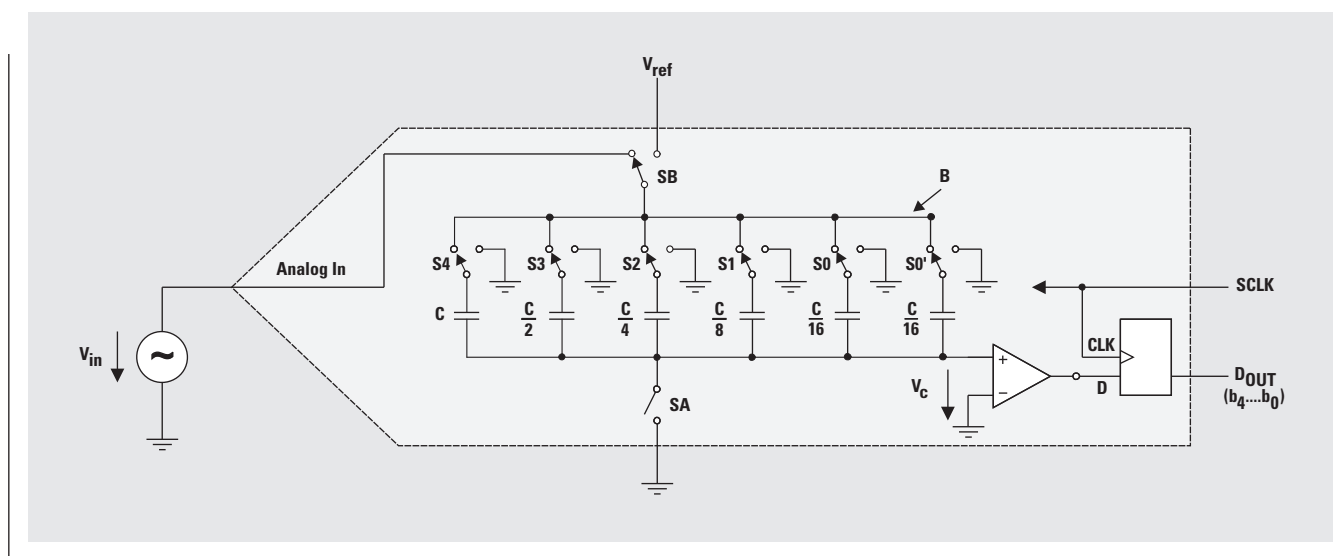


# The operation of the SAR-ADC based on charge redistribution

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**Figure 1. Five-bit SAR-ADC based on charge redistribution**



All Texas Instruments TLV- and TLC-series sequential serial analog-to-digital converters perform successive approximation based on charge redistribution. This article explains the operation of the SAR (successive approximation register)-ADC (analog-to-digital converter). It provides a concise description of a model SAR-ADC based on charge redistribution. Figure 1 shows the simplified circuit of a 5-bit charge redistribution converter using switched capacitor architecture.

All capacitors have binary weighted values, i.e.,  $C$ ,  $C/2$ ,  $C/4$ , ...,  $C/2^{n-1}$ . The last two capacitors having the value  $C/2^{n-1}$  are connected so that the total capacitance of the  $n+1$  capacitors is  $2C$ . MOS-transistors are used to implement the required  $n+3$  switches, and the voltage comparator provides the appropriate steering of the switches via auxiliary logic circuitry. The conversion process is performed in three steps: the sample mode, the hold mode, and the redistribution mode (in which the actual conversion is performed).

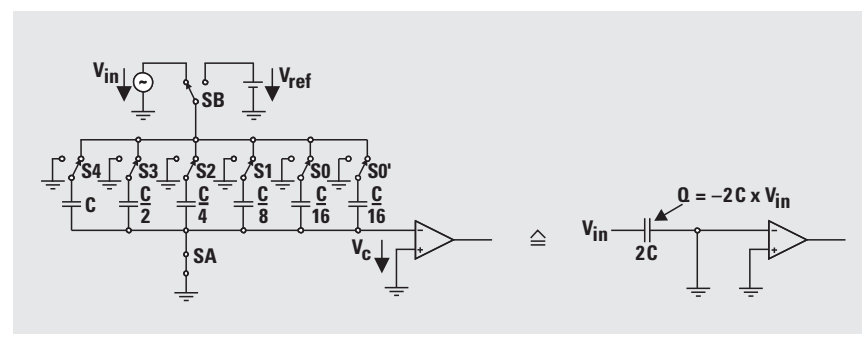
## Sample mode

In the sampling mode (Figure 2), switch SA is closed and SB is switched to the input voltage  $V_{in}$ . The remaining switches are turned to the common bus B. Due to charging, a total charge of  $Q_{in} = -2C \times V_{in}$  is stored on the lower plates of the capacitors.

## Hold mode

During the hold mode (Figure 3), switch SA is opened while the switches  $S4 \dots S0'$  are connected to ground,

**Figure 2. Sample mode**



thereby applying a voltage of  $V_C = -V_{in}$  to the comparator input. This means that the circuit already has a built-in sample-and-hold element.

### Redistribution mode

The actual conversion is performed by the redistribution mode. The first conversion step, shown in Figure 4, connects C (the largest capacitor) via switch S4 to the reference voltage  $V_{ref}$ , which corresponds to the full-scale range (FSR) of the ADC.

Capacitor C forms a 1:1 capacitance divider with the remaining capacitors connected to ground. The comparator input voltage becomes  $V_C = -V_{in} + V_{ref}/2$ . If  $V_{in} > V_{ref}/2$ , then  $V_C < 0$ , and the comparator output goes high, providing the most significant bit MSB (bit 4) = 1. On the other hand, if  $V_{in} < V_{ref}/2$ , then  $V_C > 0$ , and bit 4 = 0.

The second conversion step connects C/2 to  $V_{ref}$ . If the first conversion step resulted in bit 4 = 1, switch S4 is turned to ground again to discharge C as shown in Figure 5; otherwise it remains connected to  $V_{ref}$  if bit 4 = 0 (Figure 6), resulting in a comparator input voltage  $V_C = V_{in} + \text{bit 4} - V_{ref}/2 + V_{ref}/4$ .

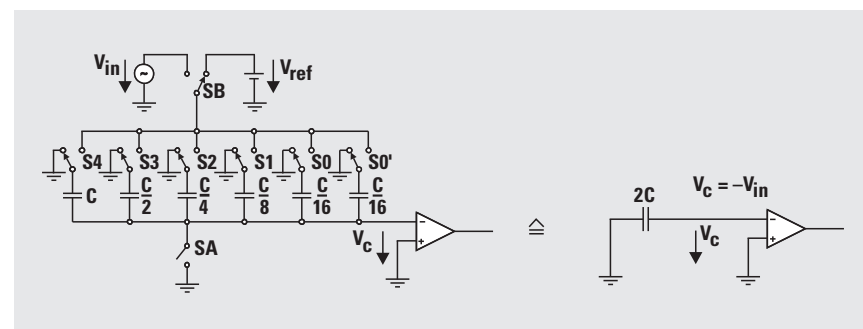
According to this voltage, the next most significant bit (bit 3) is obtained by comparing  $V_{in}$  to  $1/4 V_{ref}$  or  $3/4 V_{ref}$  through the different voltage dividers. Switch S3 is then either turned to ground if bit 3 = 1, thereby discharging C/2, or S3 remains connected to  $V_{ref}$  if bit 3 = 0.

This process continues until all bits are generated, with the final conversion step being performed at a comparator input voltage of  $V_C = -V_{in} + \text{bit 4} \times V_{ref}/2 + \text{bit 3} \times V_{ref}/4 + \text{bit 2} \times V_{ref}/8 + \text{bit 1} \times V_{ref}/16 + \text{bit 0} \times V_{ref}/32$ .

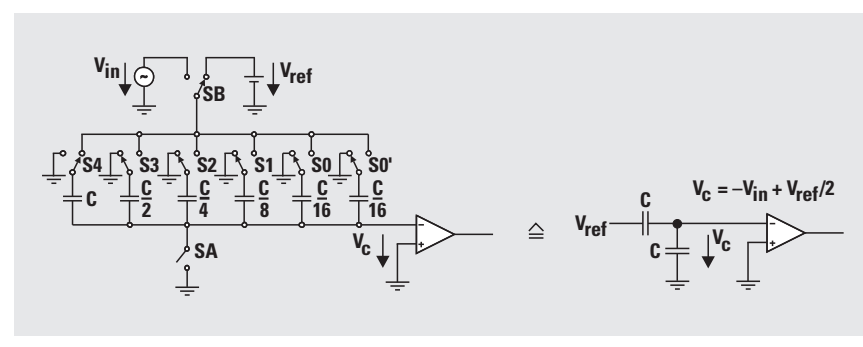
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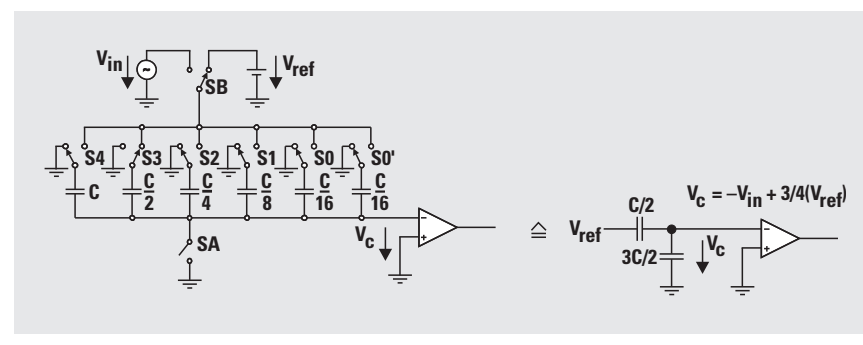
**Figure 3. Hold mode**



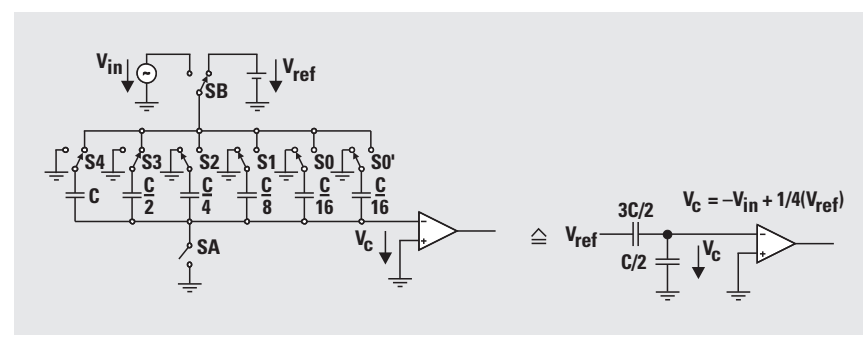
**Figure 4. Conversion Step 1 determines the MSB (bit 4)**



**Figure 5. If bit 4 = 1,  $V_{in}$  is compared with  $3/4 V_{ref}$**



**Figure 6. If bit 4 = 0,  $V_{in}$  is compared with  $1/4 V_{ref}$**



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