Designing Power Over Ethernet Using LM5070 and DP83865

National Semiconductor
Application Note 1408
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1.0 Introduction

Power over Ethernet (PoE) is widely used in the IP phone and the wireless access point applications. Using gigabit Ethernet instead of Fast Ethernet has the advantage of increasing the network bandwidth and reducing network traffic congestion. This application note provides a reference design for PoE on the Power Device (PD) side using National LM5070 and the physical layer device DP83865 Gig PHYTER® V.

For datasheet and additional information of DP83865 and LM5070, please refer to the National Semiconductor website:

http://ethernet.national.com

http://power.national.com

A basic block diagram of the PD is shown in *Figure 1*.

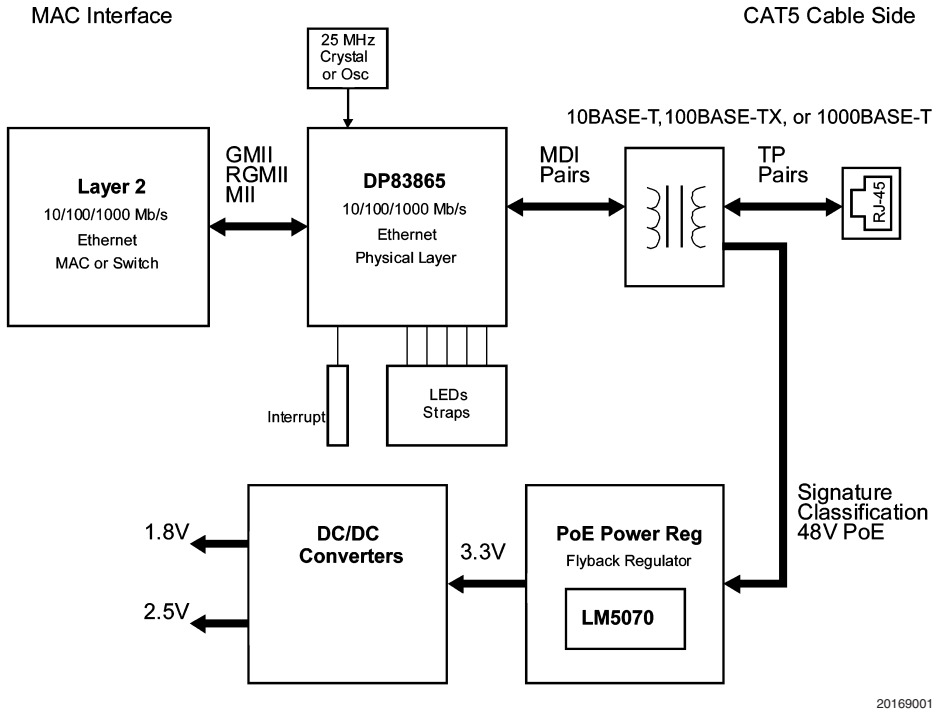

FIGURE 1. A Block Diagram of PD Using LM5070 and DP83865.

2.0 How Power Over Ethernet Works

2.1 A Brief History

The idea of PoE was introduced in the early 1990's while Ethernet was getting proliferated and becoming the standard communication interface of peripheral devices beyond networked computers. The Ethernet not only transports data between computers and devices, but in a PoE environment also provides power so that connected PoE capable devices do not need separate power supplies.

The Category 5 cable has become the industry standard for the Fast Ethernet (100BASE-TX). There are four twisted pairs in the cable and Fast Ethernet uses only two pairs for data transmission. Early adopters used the spare two pairs to deliver power to a destination device. However, most implementations used the two data transmission pairs to deliver power because in older Ethernet networks, potentially only two pairs were connected. In the late 1990s, Power over Ethernet gradually became an industry standard and is covered by IEEE 802.3af. The proposed standard can accommodate power over either the data transmission pairs or the spare pairs.

Around the same time, the Gigabit Ethernet (1000BASE-T) over copper was also adopted as an IEEE standard. Gigabit Ethernet uses all four pairs of the CAT5 cable for data transmission. (*Figure 2*.) The PoE power is carried on channel A and B pairs. Since all four pairs are present in the latest Ethernet installations, using all four pairs for transporting higher power is in the discussion to increase current carrying capability, i.e., the PoE Plus. Note that PoE Plus is outside the scope of this application note.

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2.0 How Power Over Ethernet Works (Continued)

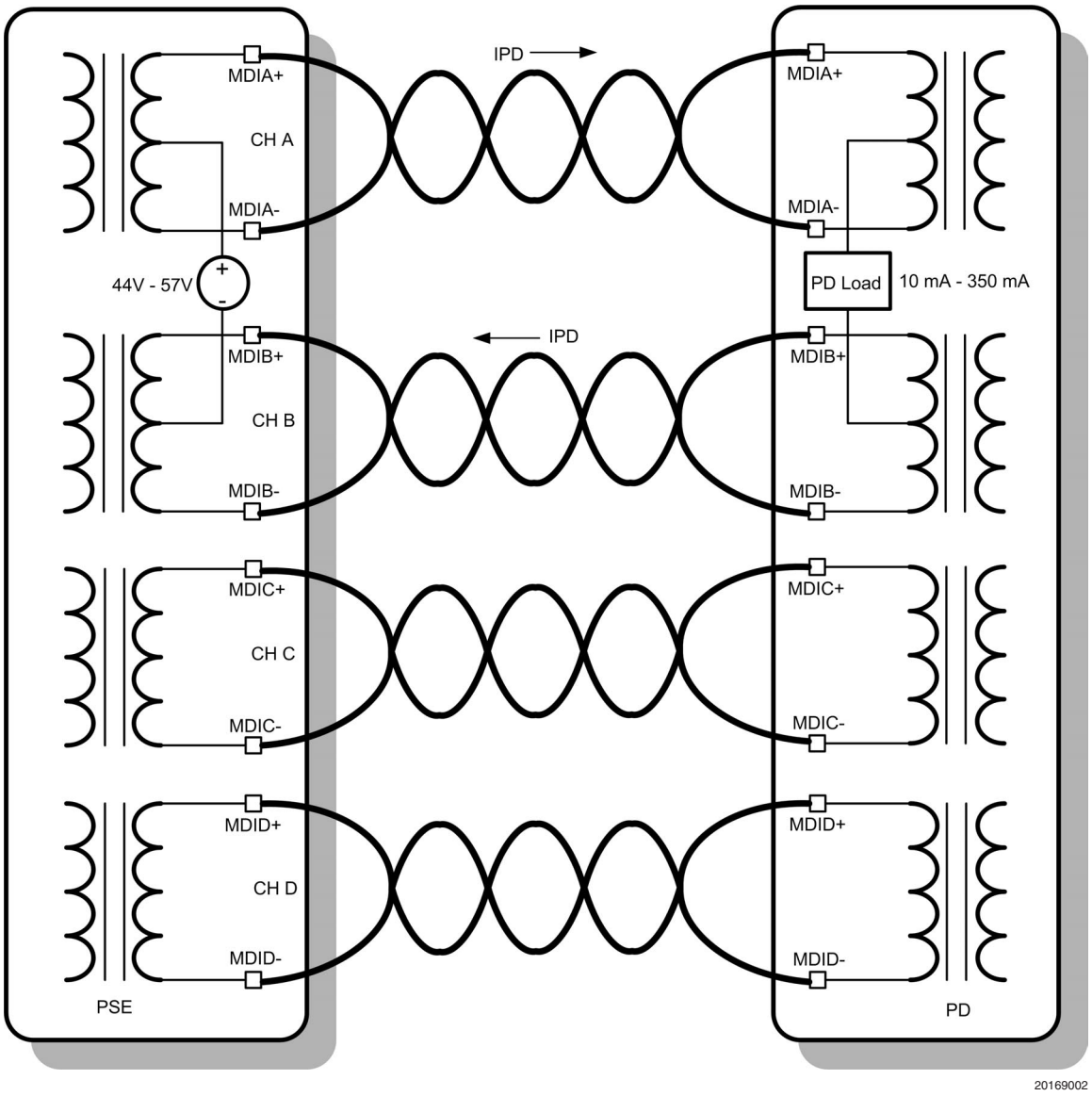


FIGURE 2. Simplified PoE on gigabit Ethernet.

2.2 How PoE Is Delivered

To deliver the power over Ethernet, the traditional isolation transformer needs to be modified. The power connection to the transformer is through cable side transformer center taps. The original transformer has all the center taps tied together through 75-Ohm resistors. That prevents positive and negative terminals from being isolated in the PoE application (*Figure 3*). To make the transformers PoE capable, AC couplings were added in the Bob Smith termination to DC isolate each separate winding (*Figure 4*).

2.0 How Power Over Ethernet Works (Continued)

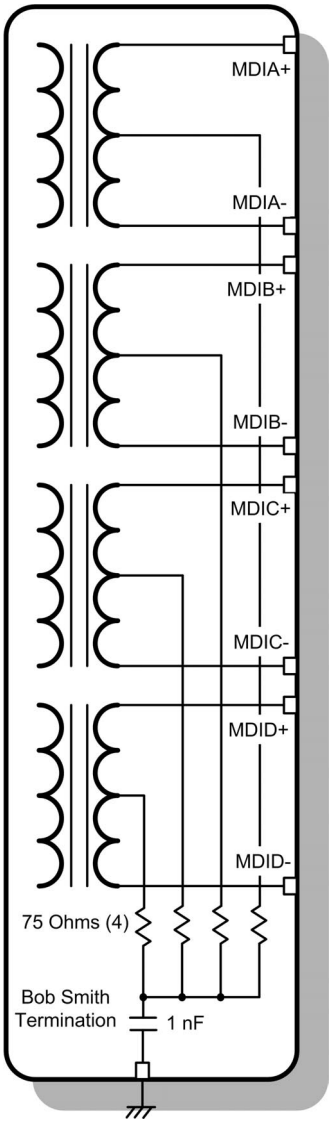


FIGURE 3. Legacy Ethernet Mag/Jack

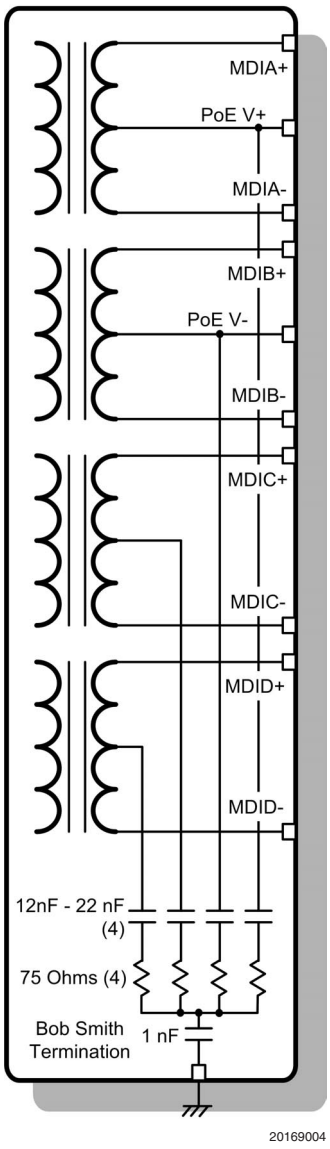


FIGURE 4. PoE Capable Mag/Jack

2.0 How Power Over Ethernet Works (Continued)

There are two sides to the Power over Ethernet system. The side that provides power is called Power Source Equipment (PSE) side, and the side that consumes power is called Power Device (PD) side. A detection scheme is designed to detect if there is PD connected at the destination. This prevents applying power to a legacy transformer shown in Figure 3. To detect PD device, the PSE applies a DC voltage between 2.8V to 10V across the power delivering lines. Based on the loop current, PSE determines if there is a PD connected. The PD should present a resistive load between 19 K to 27 K Ohms with a parallel capacitor 120 nF or less as a signature.

To match the power delivering capability of the PSE and the power consumption of the PD, the second stage is to determine the power classification. There are five classes that a PD may advertise. The PSE may opt to supply or not to supply the power based on the matching of supply capability and the consumption level. To determine classification, the PSE applies V_{class} between DC 15.5 V to 20.5 V across the delivering line with 100 mA current limit. The PD should behave as a constant current source to provide with discrete current levels (measured as I_{class}) to indicate the power classification. The details of the classification is beyond the scope of this documentation. For more information, refer to the IEEE 802.3af standard

TABLE 1. Power Classifications

Class	Usage	Min Power at PSE
0	Default	15.4 W
1	Optional	4.0 W
2	Optional	7.0 W
3	Optional	15.4 W
4	Future Use	Treat as Class 0

After a valid classification is determined and a match between PSE and PD is found, the PSE applies a nominal 48 V DC across the power delivering lines. The PD regulates the power down to its needs. The LM5070 complies to the power detection, level classification, and does the power regulation for the end system.

The PSE continues to monitor the current draw from the PD. A valid power-maintenance signature is a continuous DC current draw of greater than 10 mA and an AC impedance of 33 KOhms at frequency 500 Hz or lower. If this signature is invalid, the PSE waits 0.3 to 0.4 second before removing the power from the PD. This delay prevents accidental disconnect or PSE voltage sag. In addition, the PSE power disconnect prevents changing a PD device to a legacy Ethernet device that may short the PSE power supply.

Combining LM5070 with the DP83865, a Gigabit PD device can be implemented. This device could be a standalone storage device, a webcam, a wireless access point, etc. A reference schematic design is attached as an example. Design notes are summarized and can be used as a check list.

3.0 PD Reference Design

The LM5070 and DP83865 reference design is composed of three parts, PoE detection/regulation, Gigabit physical layer, and the MAC interface. For LM5070 and DP83865 part specific information and functional descriptions please refer to the respective datasheets.

The DP83865 requires 2 power supplies, 1.8V and 2.5V, and an optional I/O voltage 3.3V. The MAC and other digital peripheral devices typically requires 3.3V. The LM5070 provides the regulation down to 3.3V. The 1.8 and 2.5 are provided by an additional DC/DC converter. The schematic diagrams are at the end of this application note.

To reduce component selection time, a sample bill of materials is attached. To ease the PCB layout task, a sample layout guide line is attached.

4.0 PD Design Notes

To ensure the early success of the design, the layout notes should be closely followed to avoid performance degradation and delays in development.

4.1 General

Power supply decoupling (or bypass) capacitors should be placed as close to the IC device as possible. Place via close to the component pad and use one via for each capacitor connection to power and ground. (Do not share a via with multiple capacitors.)

4.2 GPHY

The gigabit PHY DP83865 layout guide lines are covered in application note AN1263. Please refer to the application notes for details. The following is a summary or a check list of the PHY design notes.

1. Reference clock input: When using clock oscillator, add series termination to reduce reflections. Use 0.1 uF multilayer cap to decouple the oscillator VDD. Minimize the clock trace length and place the oscillator toward the center of the PCB to minimize EMI. Provide a ground pad under the oscillator part and flush mount the device to the PCB surface.
2. If a clock crystal is used, place the crystal as close to the PHY device as possible. Follow the manufacturer's recommendations on load capacitance for the crystal.
3. It is strongly recommended to have a solid ground plane, a 1.8V plane and a 2.5V plane. Place the power and ground planes next to each other to create plane capacitance. The plane capacitance has low ESR and ESL, it is the best capacitor to decouple frequencies 100MHz and above. In addition, to maximize the plane capacitance, fill unused areas with copper and tie the copper to appropriate ground or power.
4. To decouple the power supply pins of the PHY, it is recommended to use one SMT capacitor to decouple every two supply pins. Alternate the capacitor values between 0.01 uF and 0.1 uF to disperse the resonant frequency. Place one 10 uF tantalum capacitor for each supply near each PHY device to decouple the lower frequency noise
5. The 1.8 V supply provides power to both the digital core and the sensitive analog receivers. The 1.8 V regulator should be placed as close to the MDI side of the PHY as possible to avoid noise from the digital core return (Figure 5)
6. PGM_AVDD requires an RC low pass filter, i.e., an 18-Ohm resistor, a 22 uF cap, and a 0.01 uF cap.

4.0 PD Design Notes (Continued)

7. A 1% 9.76 K resistor is needed for the BG_REF pin and the resistor should be placed as close to the BG_REF pin as possible.
8. On the MDI side, place a 49.9-Ohm resistor close to the MDI pin to 2.5 V power supply. Place a 0.01 uF decoupling cap between 2.5 V and ground near the 49.9-Ohm resistor. Place a 0.01 uF decoupling cap between the transformer center tap (2.5 V) and the ground.
9. Each of the MDI "+" and "-" traces should have 50-Ohm characteristic impedance control to ground or 100-Ohm between each other. Each of the MDI members within a pair should be trace length matched to 50 mils. Avoid placing vias on the MDI pairs and if a via is unavoidable, try to match the number of vias on each of member within a pair. To reduce the common mode trace coupling, the differential pairs should be placed close to each other. Members of adjacent channel pairs should be separated by at least ten times the distance of trace-to-ground spacing, or 0.25 inch, if possible.
10. On the MAC side, place a source series termination resistors to match the trace impedance if the trace length of the digital interface bus exceeds 1 inch.
11. As an application specific requirement for PoE, the Ethernet isolation transformer should be one recommended by the transformer vendors.

4.3 Flyback Regulator

The design guide lines for switching regulators are covered in the AN1149. The following list is a summary of LM5070 design notes and it can be used as a check list.

1. Inductor: Use low EMI emission toroid or encased E-core inductors.
2. Filter capacitors: 0.1 uF ceramic input filter capacitor should be placed as close to the IC Vin pin as possible. Use SMT type to reduce EMI coupling created by the capacitor lead.
3. Feedback: Pin 11 error amplifier feedback (FB) input is noise sensitive. The trace connecting FB pin should be as short and thick as possible. For isolated applications, such as in this application note, the FP pin is connected to ARTN (GND).
4. Pin 13 is the current sense (CS) feedback. A RC filter is provided at the CS to filter out noise. This filter capacitor should be placed between CS and ATRN pins. The inductors should be placed as far away from the CS input as possible. It is best to place the inductors and transformer opposite of where the feedback trace is. All the low power grounds should be connected together locally near the LM5070. A single connection should be made between the lower power grounds and the high power ground (i.e., the current sense resistor ground).
5. A current sense resistor (R57) connected at the source of the power MOSFET (Q1) should be low inductance SMT type.
6. External compensation: The optical coupler (U2) provides a regulation feedback. The optical coupler should be placed as close to LM5070 as possible and far away from inductors.
7. Flyback primary and secondary switching loops: The primary side of the flyback transformer (T2) is switched on and off by the power MOSFET (Q1) and the switching generates transient current. Decoupling caps (C27 - C29) should be placed as close to the transformer as possible. The decoupling caps, the transformer winding, the MOSFET, and the current sense resistor (R57) should be placed as close together to minimize current loop area. Flood copper under and around the components in the current loop. Tie the flooded copper to ground at one point near the farthest decoupling cap (C27).

   The secondary side of the flyback transformer (T2) switches on during the off time of the primary side. The current loop consists of the secondary side winding, rectifier diode (D8), and the filtering caps (C30 - C33). Place the components in the current loop as close as possible to reduce loop area. Flood copper around and under the components, and tie this copper to ground at one point near the farthest filtering cap (C35).

   The primary and the secondary loop components should be placed in a way that during the current conducting state, the direction of the current flow is consistent. This prevents magnetic field reversal caused by the traces between the two switching cycles and reduces radiated EMI.
8. PCB layout precaution: The traces connecting in high current loops should be as wide and thick as possible, and as short as possible. Make these traces with an absolute minimum of 15 mils per Ampere. It is also a good practice to use one via per 200 mA of current and use multiple vias when higher current carrying capability is expected.

4.4 Buck Regulator

The design guidelines for buck regulators are covered in the LM2734 datasheet Design Guide section, and in application notes AN1229. The design notes are summarized as follows.

1. Fast switching Schottky diode is recommended for catch diode (D13, D15). Place the catch diodes and input capacitors (C55 and C58) close together. A large isolated heatsink area may be required for catch diode.
2. Low ESL surface mount multilayer ceramic (X7R or X5R) or tantalum capacitors are recommended for input and output capacitors (C55, C57, C58, and C60). Place input decoupling capacitor close to VIN pin and avoid via on capacitor connections.
3. The FB pin is a high impedance input that is susceptible to noise pickup causing inaccurate regulation. Place feedback resistors (R60 and R63) close to FB pin. Route feedback trace correctly away from noise sources such as the inductor and the diode.
4. The GND connection of the output capacitors (C57 and C60) should be near the GND connections of input capacitors (C55 and C58) and the catch diodes (D13 and D15). Connect vias to a ground plane where available.
5. A continuous GND plane is recommended, except at the switching island.
6. High transient current flows through the VIN and SW traces so that they should be short and wide. However, widening the these traces could also increase the radiated EMI and the designer must aware of the trade-off. The radiated noise can be reduced by using a shielded inductor.
7. For higher power SMT applications, use 2 oz copper board for better thermal management with less copper area.

4.0 PD Design Notes (Continued)

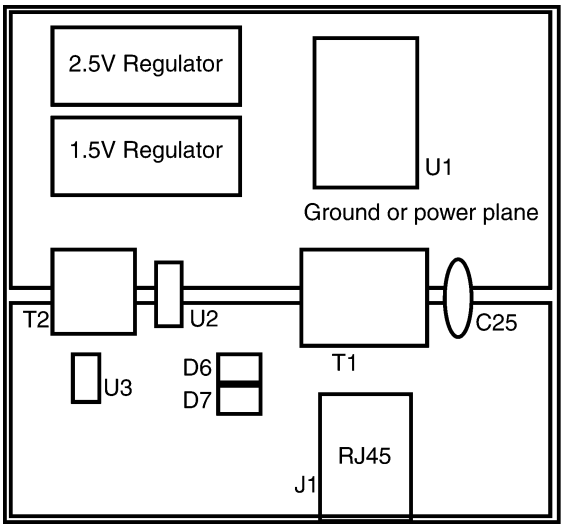


FIGURE 5. PoE Layout Planning

5.0 PoE Capable Magnetics

The following is a list of vendors and part numbers of magnetics that can be used with the National gigabit PHY. For the latest product information, please contact the vendors.

TABLE 2. PoE Capable Gigabit Ethernet Magnetics

Pulse Engineering, Inc. www.pulseeng.com	2x4 Integrated 10/100/1000 RJ45-magnetics	JOB-0045
	2x6 Integrated 10/100/1000 RJ45-magnetics	JOB-0263
	2x8 Integrated 10/100/1000 RJ45-magnetics	JOB-0029
	10/100/1000 magnetics, single port	H6062
	10/100/1000 magnetics, dual port	H6080
Bel Fuse, Inc. www.belfuse.com	1x8 Integrated 10/100/1000 RJ45-magnetics	0874-1X8T-66
	2x4 Integrated 10/100/1000 RJ45-magnetics	0854-2X4R-66
	2x6 Integrated 10/100/1000 RJ45-magnetics	0854-2X6R-66
	2x6 Integrated 10/100/1000 RJ45-magnetics with LED	0873-2X6R-66
	2x8 Integrated 10/100/1000 RJ45-magnetics	0854-2X8R-66
	2x8 Integrated 10/100/1000 RJ45-magnetics	0854-2X8R-69
	2x8 Integrated 10/100/1000 RJ45-magnetics with LED	0873-2X8R-66
Midcom www.midcom-inc.com	2x6 Integrated 10/100/1000 RJ45-magnetics	MIC68D10-5160W-LF3
	2x8 Integrated 10/100/1000 RJ45-magnetics	MIC61E10-5159W-LF3
Tyco, Inc. www.tycoelectronics.com	2x6 Integrated 10/100/1000 RJ45-magnetics with LED	1658821-1
	2x6 Integrated 10/100/1000 RJ45-magnetics	1658821-2
	2x6 Integrated 10/100/1000 RJ45-magnetics with LED	1658825-1
	2x6 Integrated 10/100/1000 RJ45-magnetics	1658825-2
	2x6 Integrated 10/100/1000 RJ45-magnetics with LED	1658827-1
	2x6 Integrated 10/100/1000 RJ45-magnetics	1658827-2
Note: Contact Magnetics manufactures for latest part numbers and product specifications. All Magnetics should be thoroughly tested and validated before using them in production.		

6.0 Reference Design Bill of Material

Item	Qty	Reference	Part Description	Foot Print	Manufacturer/Part
1	12	C1,C7,C9,C11,C14,C16,C18,	Cap, 0.01uF, Ceramic X7R	603	Kemet/C0603C103K5RACTU
		C19,C52,C54,C56,C59			
2	3	C2,C57,C60	Cap, 22uF, Electrolytic, Low ESR	4.3x4.6mm	Panasonic/EEV-FK1A220R
3	11	C3,C4,C8,C10,C13,C15,C17,	Cap, 0.1uF, Ceramic X7R	603	Kemet/C0603C104K5RACTU
		C20,C35,C51,C53			
4	2	C5,C6	Cap, 33pF, Ceramic X7R	603	Kemet/C0603C330J5GACTU
5	7	C12,C30,C31,C32,C33,C55,	Cap, 10uF 6.3V, Ceramic X7R	1206	TDK/C3216X5R0J106K
		C58			
6	5	C21,C22,C23,C24,C36	Cap, 0.22uF, Ceramic X7r	805	Vitramon/VJ0805
7	1	C25	Cap, 1nF 2000V	7.5mm	
8	1	C26	Cap, 470pF, Ceramic X7R	603	Kemet/C0603C471K5RACTU
9	3	C27,C28,C29	Cap, 2uF2 100V, Ceramic X7R	1812	TDK/C4532X7R2A225
10	1	C34	Cap, 330uF, Electrolytic, Low ESR	8.3x9.0mm	Panasonic/EEV-FK0J331P
11	4	C37,C38,C41,C42	Cap, 1nF 200V, Ceramic X7R	603	AVX/06032C102KAT2A
12	1	C39	Cap, 0.1uF 100V, Ceramic X7R	1206	Kemet/C1206C104K1RACTU
13	2	C40,C46	Cap, 1uF, Ceramic X5R	603	Kemet/C0603C105K8PACTU
14	1	C43	Cap, 4nF7, Ceramic X7R	603	Kemet/C0603C472K5RACTU
15	3	C44,R51,R53	NC (No component)		
16	3	C45,C48,C50	Cap, 1nF, Ceramic X7R	603	Kemet/C0603C102K5RACTU
17	1	C47	Cap, 47nF, Ceramic X7R	805	Kemet/C0805C473K5RACTU
18	1	C49	Cap, 27nF, Ceramic X7R	603	AVX/06035C273KAT2A

6.0 Reference Design Bill of Material (Continued)

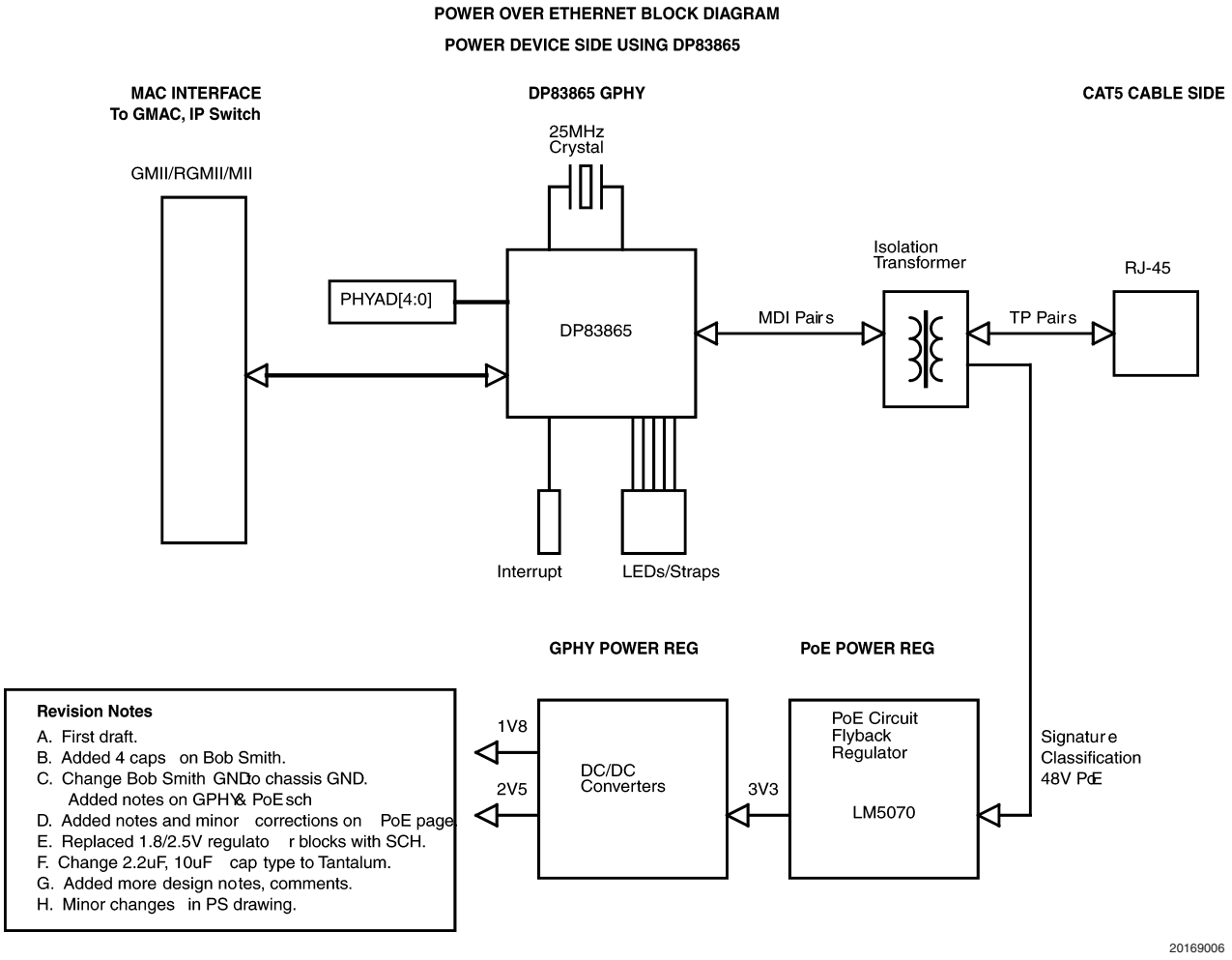
Item	Qty	Reference	Part Description	Foot Print	Manufacturer/Part
19	1	DZ1	SMAJ90A, Transient Suppressor Diode	SMA	Diodes Inc/SMAJ90A
20	1	DZ2	SMAJ60A, Transient Suppressor Diode	SMA	Diodes Inc/SMAJ60A
21	6	D1,D2,D3,D4,D5,D11	LED, Green, SMT. Vf=2.1	1206	LiteOn/LTST-C150GKT
22	2	D6,D7	Bridge Rectifier, HD01	MiniDip	Diodes Inc/HD01
23	1	D8	Diode, Shottky rectifier, 12CWQ03	DPAK	IR/12CWQ03
24	2	D9,D10	Diode, Small signal, MMSD4148	SOT-23	Vishay/MMSD4148
25	2	D12,D14	Diode, Fast switching, 1N4148W	SOD123	Vishay/1N4148W-V
26	2	D13,D15	Diode, Shottky, Power, MBRM110L	457-04	On Semi/MBRM110L
27	1	JP1	Header, 3-pin		
28	1	J1	Connector, Ethernet jack, RJ-45		Samtec/MODS-A-8P8C-X-C
29	2	J2,J4	Header, 2X8 pins		
30	1	J3	Header, 2X4 pins		
31	1	J5	Header, 2X6 pins		
32	1	L1	Inductor, 17uH. 1A	SMT	Pulse Eng/PE-53816S
33	1	L2	Inductor, 0.18uH, 5A		Coilcraft/DO1813P-181HC
34	1	L3	Common mode filter, 1A, PE-53913	SMT	Pulse Eng/PE-53913
35	1	L4	Inductor, 4.7uH, 0.75A	3.2x3mm	muRata/LQH43CN4R7M03L
36	1	L5	Inductor, 10uH, 0.65A	3.2x3mm	muRata/LQH43CN100K03L
37	1	Q1	MOS FET, N-Channel power, SI4848DY	SO-8	Vishay/SI4848DY
38	1	REF1	Regulator, Shunt, LMV431	SOT-23	National/LMV431
39	1	R1	Res, 18R2, Thick film, 1%	603	Panasonic/ERJ-3EKF
40	9	R2,R18,R24,R25,R27,R28,	Res, 2K0, Thick film, 1%	603	Panasonic/ERJ-3EKF
		R30,R32,R34			
41	8	R3,R4,R5,R6,R19,R20,R21,	Res, 49R9, Thick film, 1%	603	Panasonic/ERJ-3EKF
		R23			
42	11	R7,R8,R9,R10,R11,R12,R13,	Res, 33R, Thick film, 1%	603	Panasonic/ERJ-3EKF
		R14,R15,R16,R17			
43	1	R22	Res, 9K76, Thick film, 1%	603	Panasonic/ERJ-3EKF
44	6	R26,R29,R31,R33,R35,R42	Res, 200R, Thick film, 1%	603	Panasonic/ERJ-3EKF
45	4	R36,R37,R38,R39	Res, 75R, Thick film, 1%	603	Panasonic/ERJ-3EKF
46	1	R40	Res, 590K, Thick film, 1%	603	Panasonic/ERJ-3EKF
47	1	R41	Res, 10R, 1/4W, Thick film, 1%	1210	Panasonic/ERJ-14NF
48	1	R43	Res, 20R, Thick film, 1%	603	Panasonic/ERJ-3EKF
49	1	R44	Res, 33K2, Thick film, 1%	603	Panasonic/ERJ-3EKF
50	2	R45,R52	Res, 1K00, Thick film, 1%	603	Panasonic/ERJ-3EKF
51	1	R46	Res, 24K9, Thick film, 1%	603	Panasonic/ERJ-3EKF
52	1	R47	Res, 10R, Thick film, 1%	603	Panasonic/ERJ-3EKF
53	1	R48	Res, 590R, Thick film, 1%	603	Panasonic/ERJ-3EKF
54	1	R49	Res, 24K3, Thick film, 1%	603	Panasonic/ERJ-3EKF
55	3	R50,R60,R63	Res, 10K0, Thick film, 1%	603	Panasonic/ERJ-3EKF
56	1	R54	Res, 100R, Thick film, 1%	603	Panasonic/ERJ-3EKF
57	1	R55	Res, 12K1, Thick film, 1%	603	Panasonic/ERJ-3EKF
58	1	R56	Res, 107K, Thick film, 1%	603	Panasonic/ERJ-3EKF
59	1	R57	Res, 0.33-Ohm, Thick film, 1%	1210	Panasonic/ERJ-14RQJ

6.0 Reference Design Bill of Material (Continued)

Item	Qty	Reference	Part Description	Foot Print	Manufacturer/Part
60	1	R58	Res, 14K7, Thick film, 1%	603	Panasonic/ERJ-3EKF
61	2	R59,R62	Res, 100K, Thick film, 1%	603	Panasonic/ERJ-3EKF
62	1	R61	Res, 12K4, Thick film, 1%	603	Panasonic/ERJ-3EKF
63	1	R64	Res, 21K5, Thick film, 1%	603	Panasonic/ERJ-3EKF
64	1	T1	Transformer, Isolation, H6062	SOIC24	Pulse Eng/H6062
65	1	T2	Transformer, PoE, PA1269	EP13	Pulse Eng/PA1269
66	1	U1	IC, GPHY, DP83865	PQFP128	National/DP83865DVH
67	1	U2	IC, Opto-coupler, PS2501-1-H	DIP4-SMT	NEC/PS2501L-1-H
68	1	U3	IC, PWM controller, LM5070	TSSOP16	National/LM5070-50
69	2	U4,U5	IC, Voltage regulator, LM2734X	TSOT6	National/2734X
70	1	Y1	Crystal, 25MHz 50PPM	HC49/U	CTS/MP250

7.0 Reference Power Over Ethernet Schematic

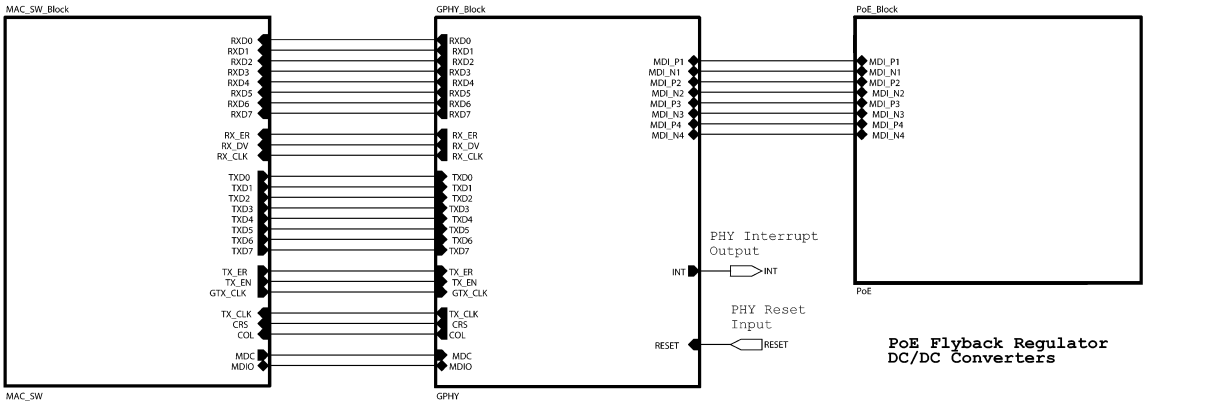
7.1 Block Diagram



7.0 Reference Power Over Ethernet Schematic (Continued)

7.2 Top Hierarchy

PoE PD REFERENCE DESIGN WITH DP83865 TOP HIERARCHY



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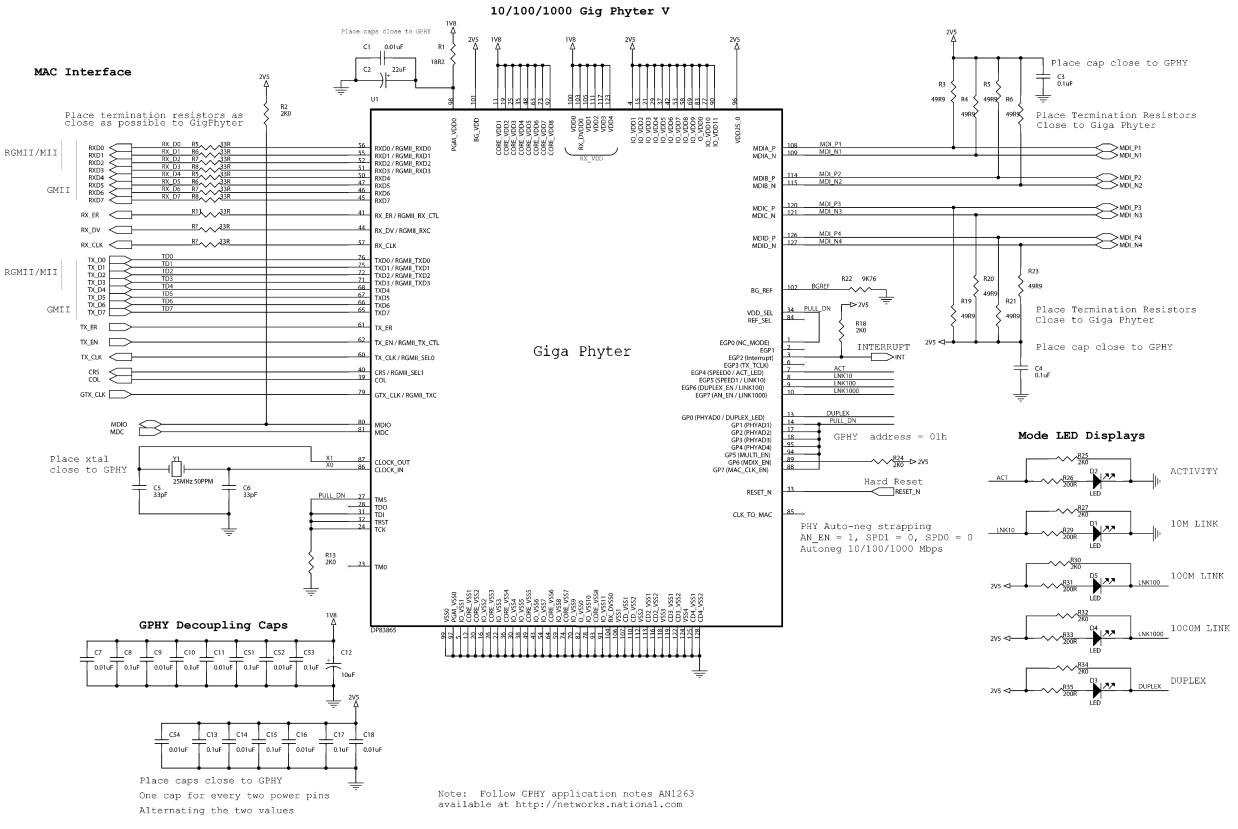
7.3 Physical Layer



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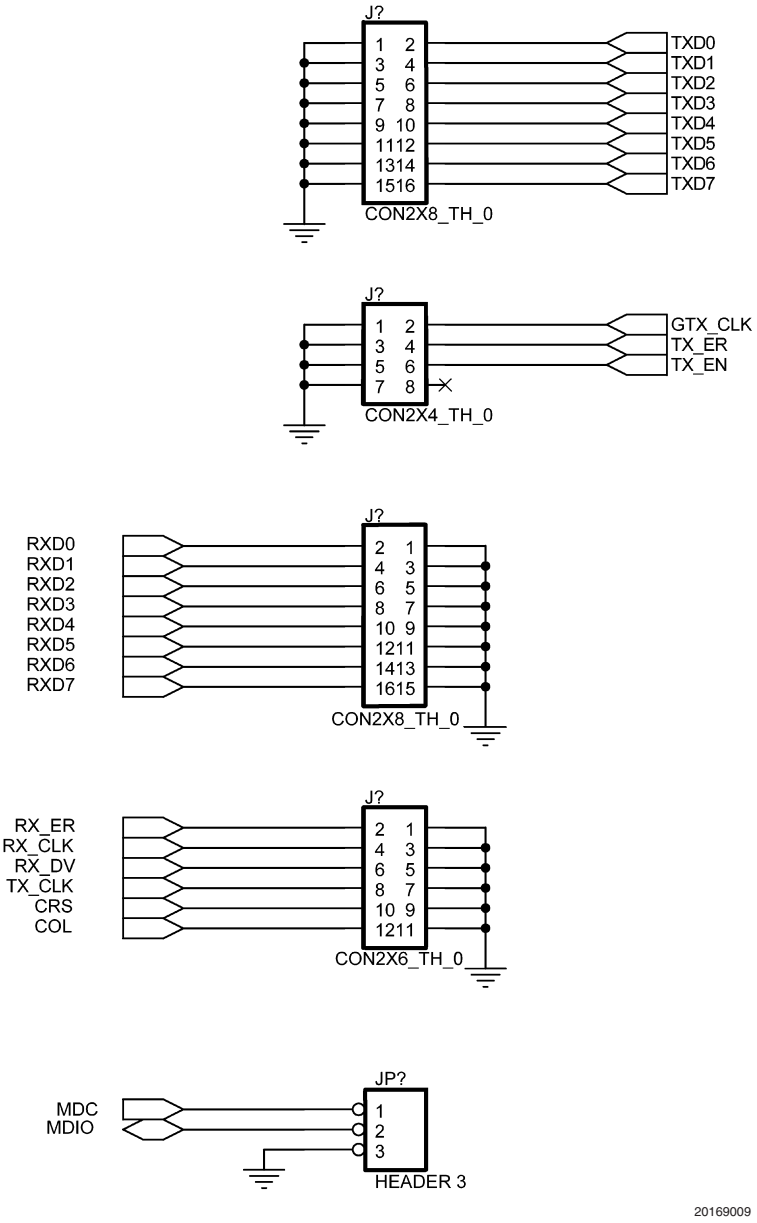
7.0 Reference Power Over Ethernet Schematic (Continued)

7.4 Mac or Switch Interface

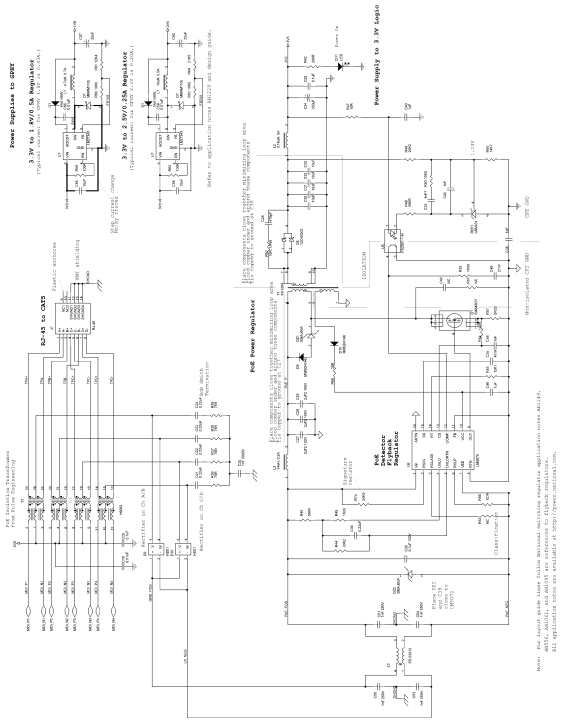


7.0 Reference Power Over Ethernet Schematic (Continued)

7.5 PoE Power Supply

For a larger size schematic, please go to the following:

http://www.national.com/appinfo/networks/files/an1408_schmatic.pdf



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