

# DP83848 and DP83849 100Mb Data Latency

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Application Note 1507  
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August 2006



## 1.0 Introduction

In many real-time system implementations, the Ethernet packet data transfer latencies are important parameters for proper system operation. The fixed and variable components of the transmit and receive latencies within the Ethernet Physical Layer can be critical components of the system latency calculations. The purpose of this document is to define the 100Mb Transmit and Receive latencies of the National Semiconductor DP83848 and DP83849 Ethernet Transceiver family, and to document their contributions for end-to-end packet transfer in both MII and RMII modes of operation.

The architecture of the DP83848 Ethernet Transceiver and the DP83849 Dual Ethernet Transceiver is designed to limit the variability of the receive data latencies and therefore provides for very deterministic system delay. In particular, the DP83848 and DP83849 do not suffer from a common non-determinism due to aligning receive data to the receive clock, thus providing significantly more deterministic receive data latency in both MII and RMII modes. In addition, the DP83849 reduces a common non-determinism in the Transmit RMII latency.

### Product Applicability:

DP83848C  
DP83848I  
DP83848YB  
DP83848M  
DP83848T  
DP83848H  
DP83848J  
DP83848K  
DP83849C

DP83849I  
DP83849ID  
DP83849IF

### 1.1 NON-DEPENDENCIES

The DP83848 and DP83849 do not suffer from dependencies on certain modes of operation. These include the following functions or modes of operation:

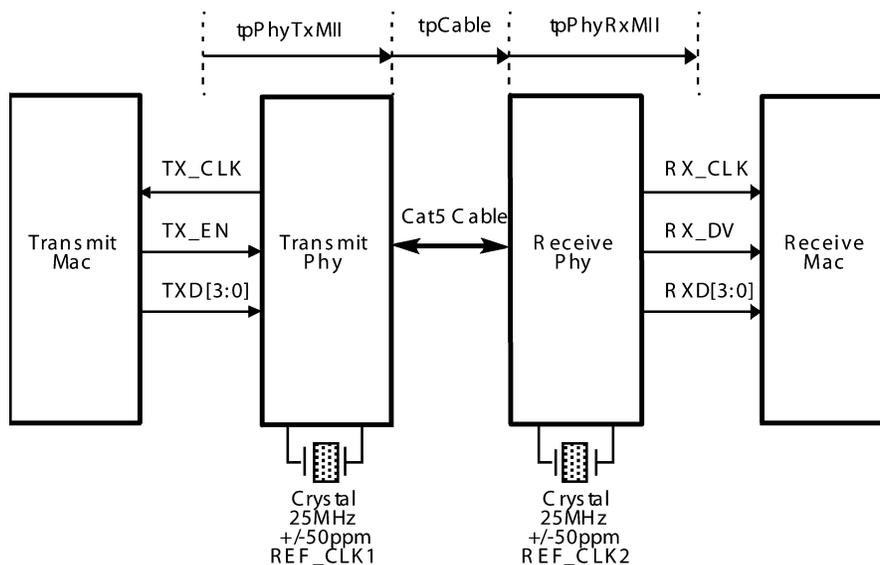
- MDI vs. MDIX
- Auto vs. Manual MDI/MDIX configuration
- Auto-negotiation vs. Forced modes of operation
- Half- vs. Full-Duplex operation

## 2.0 MII System Latency

MIl system latency is the delay from the transmitting Mac to the receiving Mac as measured at the MII interface. Transmit MII data is generated synchronous to the Transmit MII clock generated by the Transmit Phy. Receive MII data is generated synchronous to the Receive MII clock. The Receive MII clock is recovered from the data by the Receive Phy. Because the Receive MII clock is recovered from the Receive data, the skew between the Transmit and Receive MII clocks is more a function of the data delay and does not have a relationship to the Receive Phy's reference clock, REF\_CLK2.

The following diagram shows the basic components of a single transmit to receive Ethernet path from the Transmit Mac to the Receive Mac over twisted pair cable (100BASE-TX). The total transmit time of the link, from measurement at the Transmit MII to the Receive MII is:

$$tp_{TotalPhyMII} = tp_{PhyTxMII} + tp_{Cable} + tp_{PhyRxMII}$$



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FIGURE 1. MII System Timing Diagram for Twisted Pair

## 2.0 MII System Latency (Continued)

In addition to twisted pair mode, the DP83849 also supports fiber mode (100BASE-FX). The system is similar to the above diagram with the addition of fiber transceivers between the Phy and the fiber medium. In this case,  $tpCable$  could be replaced with:

$$tpCable = tpXcvrTX + tpFxCable + tpXcvrRX$$

where  $tpXcvrTX$  and  $tpXcvrRX$  are the transmit and receive latencies for the fiber transceivers.  $tpFxCable$  is the propagation delay for the signal on the fiber medium.

### 2.1 MII TRANSMIT LATENCY

MII Transmit latency is measured from transmit data at the MII interface to the first bit transmitted on the wire (usually Cat5 cable). To eliminate system dependencies (i.e. transmit

data setup to TX\_CLK), measurement is made from the rising edge of TX\_CLK that samples the transmit data. The latency measurement is made from TX\_EN assertion to first bit of JK symbol on the wire. As the latency is consistent for all transmit data nibbles, measurements could be made from the Start of Frame Delimiter (SFD) or any other data in the packet. While the measurements are not made relative to the reference clock, REF\_CLK1, it is worth noting that TX\_CLK is phase aligned to REF\_CLK1.

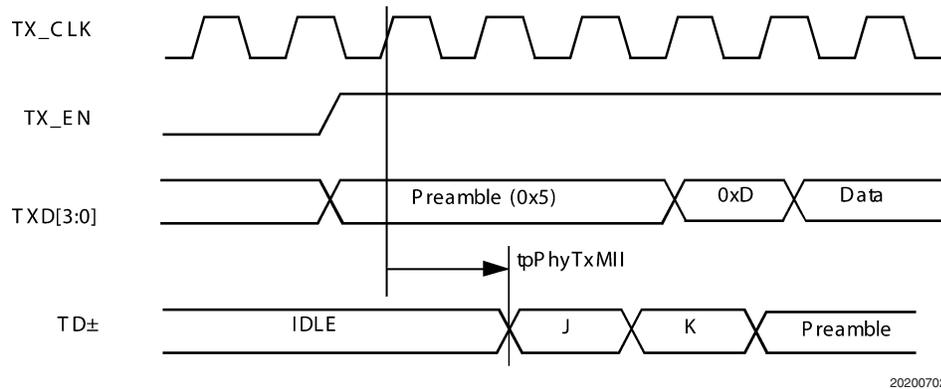


FIGURE 2. Phy Transmit Delay Diagram

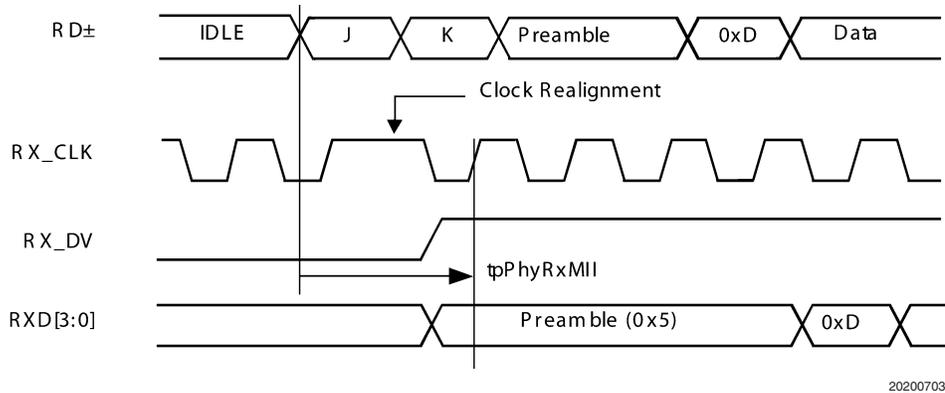
Transmit Delay time,  $tpPhyTxMII$ , is comprised of a fixed delay and an uncertainty in propagation delay due to Process, Voltage, and Temperature (PVT) variations. The fixed delay is nominally 5 bit times (bit time = 10ns) and the uncertainty is significantly less than 1 bit time. Transmit Delay time is the same for both twisted pair and fiber modes of operation.

### 2.2 MII RECEIVE LATENCY

MII Receive latency is measured from the first symbol bit received on the wire (usually Cat5 cable) to the data symbol on the Receive MII data bus. The measurement is made

from the first bit of JK to the wire to the first bit of preamble (which replaces JK) on the MII interface. As with the transmit side, the measurements are made to the RX\_CLK rising edge which samples the receive data. The measurement may also be made from the first bit of SFD on the wire to the SFD (0xD) on the RX MII.

## 2.0 MII System Latency (Continued)



**FIGURE 3. Phy Receive Delay Diagram**

Many 100Mb Ethernet Phy devices will have delay uncertainty of 1 to 5 bit times (in 8ns bit time increments). This is the result of aligning the incoming receive data to an arbitrary phase of the 125MHz recovered clock. The DP83848 and DP83849 eliminate this uncertainty in the receive latency by deriving the receive clock (RX\_CLK) from the data alignment. This process can in theory occur at the beginning of each packet (following assertion of CRS), but in practice will only occur for the first packet. Since IDLE data is sent as data symbols, subsequent packets will all arrive with the same alignment as the initial received packet. By eliminating this variability, the DP83848 and DP83849 provide significantly more deterministic receive latency.

Receive Delay time,  $t_{pPhyRxMII}$ , is comprised of a fixed delay and an uncertainty in propagation delay due to Process, Voltage, and Temperature (PVT) variations. The fixed delay, as measured to the rising RX\_CLK edge, is nominally 25.5 bit times (bit time = 10ns) for twisted pair mode and 16 bit times for fiber mode. The PVT uncertainty is less than 1 bit time.

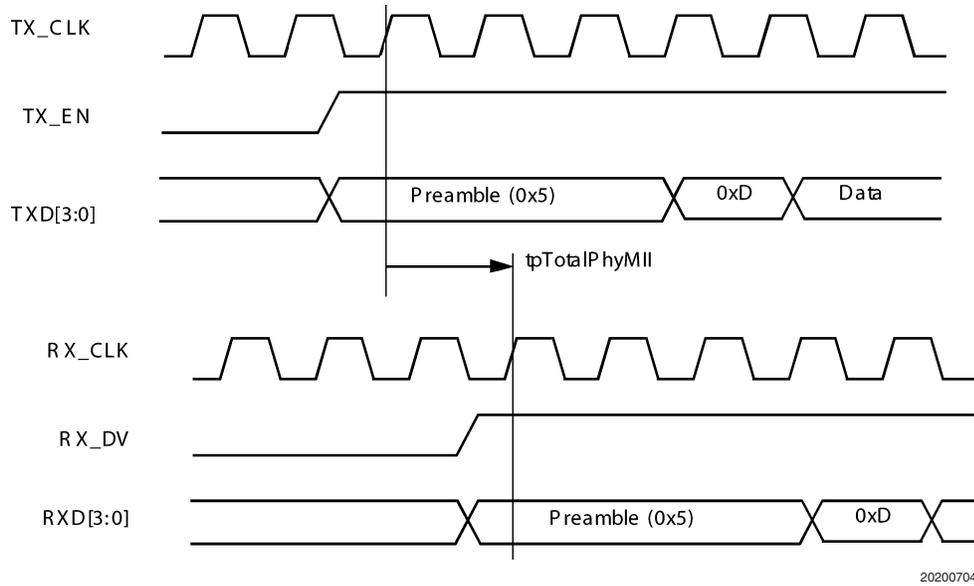
If a realignment of the RX\_CLK is required at the start of a packet (again, this should only occur for the first packet), the realignment is accomplished by holding the RX\_CLK high for an extra 8ns to 32ns prior to the assertion of RX\_DV. This

mechanism guarantees that RX\_DV and RXD transition coincident with the falling edge of RX\_CLK, thus guaranteeing setup and hold times are consistent. In addition, the mechanism guarantees that the minimum clock high and low times will not be violated. The result is that the RX\_CLK high time may be between 20ns and 52ns prior to RX\_DV assertion for the first packet.

### 2.3 MII SYSTEM LATENCY MEASUREMENTS IN TWISTED PAIR MODE

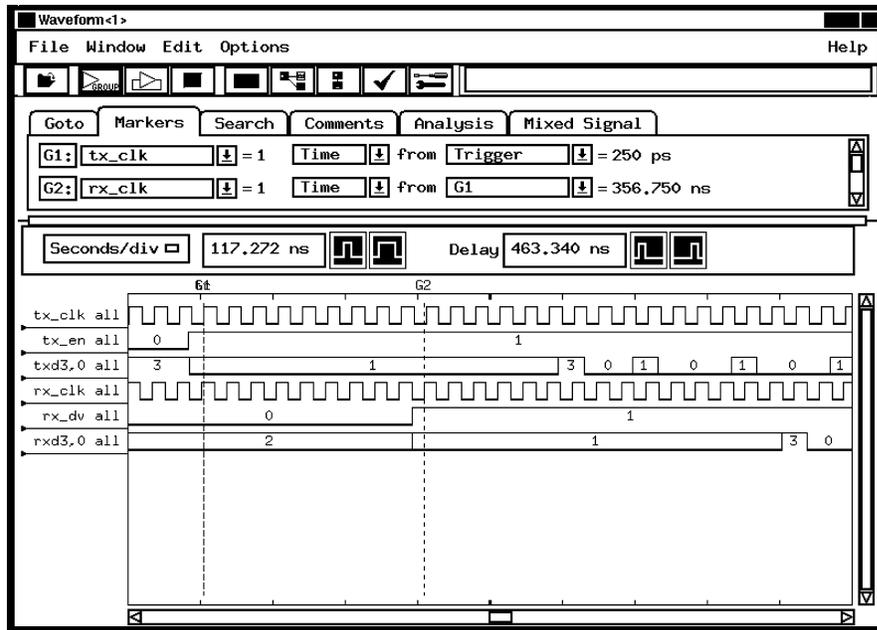
The following End-to-End measurements were made for the total propagation delay between two DP83848 devices operating in 100Mb full-duplex and MII mode and connected through a Cat5 twisted pair cable. Measurements were made from the TX\_CLK which samples TX\_EN at the Transmit MII, to RX\_CLK which samples first preamble data on the Receive MII. The measurements were repeated 10 times with a power cycle between each measurement. A power cycle is more likely to reveal any phase alignment issues than just dropping link. Measurements were made using a logic analyzer with 250ps resolution. Note that measurements were made on a single device at nominal voltage and room temperature. Results will vary slightly across Process/Voltage/Temperature.

## 2.0 MII System Latency (Continued)



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FIGURE 4. MII System Delay Measurement



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FIGURE 5. Example Trace for MII Latency Measurement

## 2.0 MII System Latency (Continued)

The first set of measurements was made using a straight 10m cable.

**TABLE 1. Measurements of tpTotalPhyMII with 10m Cable**

	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10
Delay (ns)	356.75	357.5	356.5	358	356.5	357.25	356.5	358	357.25	358

- Min: 356.50ns
- Max: 358.00ns
- Range: 1.5ns

A second set of measurements was made in loopback using a loopback plug (0m cable).

**TABLE 2. Measurements of tpTotalPhyMII with 0m loopback Cable**

	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10
Delay (ns)	310.5	310.5	310.5	310.5	310.5	311.25	310.5	310.5	310.5	310.5

- Min: 310.50ns
- Max: 311.25ns
- Range: 0.75ns

were connected through Agilent HFBR5803 fiber transceivers and 10ft of fiber cable. The test procedure was otherwise identical to the procedure in Section 2.3 *MII SYSTEM LATENCY MEASUREMENTS IN TWISTED PAIR MODE*.

Based on these results, the 10m Cat5 cable delay (tpCable) is approximately 46ns greater than the delay for the loopback plug. Measurements of the 10m cable showed a delay of approximately 49ns as measured at the pins of the RJ45 connectors. In both cases the variability in the system tests is significantly less than 1 bit time.

The following measurements were made for delay through the system:

### 2.4 MII SYSTEM LATENCY MEASUREMENTS IN FIBER MODE

The following End-to-End measurements were made for the total propagation delay between two DP83849 devices operating in 100Mb full-duplex and MII mode. The devices

**TABLE 3. Measurements of tpTotalPhyMII with FX transceivers and 10ft fiber cable**

	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10
Delay (ns)	233.5	233.25	233.25	233	233	233.5	233.25	233.25	233.75	233.5

- Min: 233.00ns
- Max: 233.75ns
- Range: 0.75ns

mit RMII data is generated based on the Transmitting Station's 50MHz reference clock, REF\_CLK1. Receive RMII data is generated based on the Receiving Station's 50MHz reference clock, REF\_CLK2. The two reference clocks are independent.

The nominal Phy transmit and receive delays add to 21 bit times (or 210ns). This leaves an approximate tpCable of 23ns for delay through the fiber transceivers and the fiber cable. As expected, the variability in the system tests is significantly less than 1 bit time.

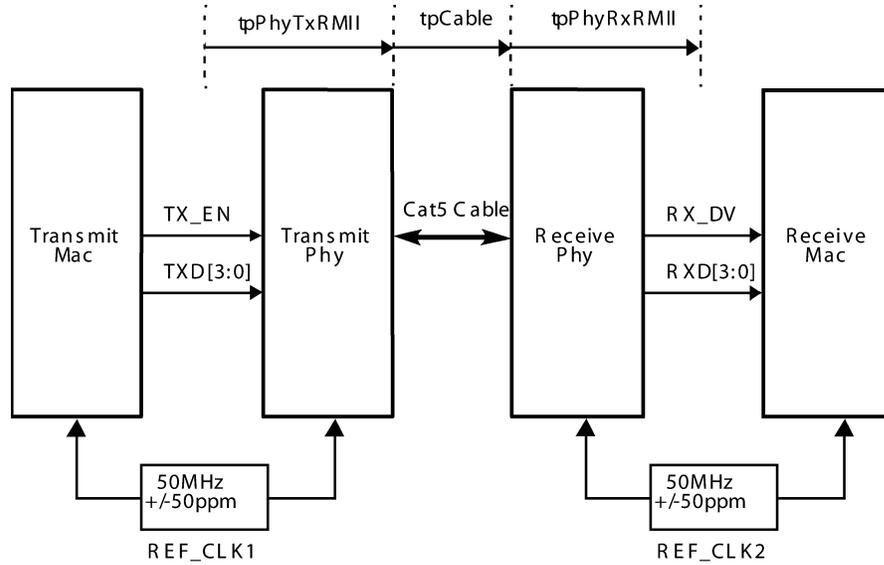
The following diagram shows the basic components of a single transmit to receive Ethernet path from the Transmit Mac to the Receive Mac over twisted pair cable (100BASE-TX). The total transmit time of the link, from measurement at the Transmit RMII to the Receive RMII is:

## 3.0 RMII System Latency

RMII system latency is the delay from the transmitting Mac to the receiving Mac as measured at the RMII interface. Trans-

$$\text{tpTotalPhyRMII} = \text{tpPhyTxRMII} + \text{tpCable} + \text{tpPhyRxRMII}$$

### 3.0 RMII System Latency (Continued)



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FIGURE 6. MII System Timing Diagram

In addition to twisted pair mode, the DP83849 also supports fiber mode (100BASE-FX). The system is similar to the above diagram with the addition of fiber transceivers between the Phy and the fiber medium. In this case, tpCable could be replaced with:

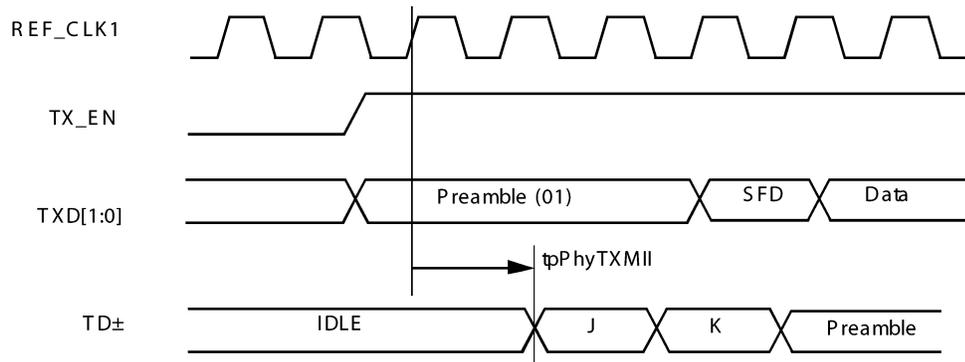
$$tpCable = tpXcvtX + tpFxCable + tpXcvtRX$$

where txXcvtX and tpXcvtRX are the transmit and receive latencies for the fiber transceivers. tpFxCable is the propagation delay for the signal on the fiber medium.

data setup to REF\_CLK1), measurement is made from the rising edge of REF\_CLK1 that samples the transmit data. The measurement is made from TX\_EN assertion to first bit of JK on the wire. As the latency is consistent for all transmit data nibbles, measurements could be made from the Start of Frame Delimiter (SFD) or any other data in the packet.

#### 3.1 RMII TRANSMIT LATENCY

RMII Transmit latency is measured from transmit data at the RMII interface to the first bit transmitted on the wire (usually Cat5 cable). To eliminate system dependencies (i.e. transmit



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FIGURE 7. Phy RMII Transmit Delay Diagram

## 3.0 RMI System Latency (Continued)

### 3.1.1 DP83848 RMI Transmit Latency

In RMI mode, the DP83848 derive a 25MHz clock from the 50MHz Reference clock, REF\_CLK1. The DP83848 then generates an internal 125MHz transmit clock from this 25MHz clock. The 25MHz clock is also used to generate the alignment of symbol data for serialization, including the transmission of IDLE symbols. The symbol clock may not be aligned with the first two bits (or di-bit) of data on the RMI interface. When the device switches from sending IDLEs to sending packet data, it must keep the same symbol alignment. Thus if the RMI data is not aligned to the symbol clock, the data must be delayed by 20ns to match the symbol alignment. Because of this, there is a 20ns variability in the Transmit Delay time (note that the delay is either 0 or 20ns, not any intermediate value). This variability will be selected at initialization time (reset) and will not change once the device is operational. This variability will be referred to as the RMI Transmit variability in subsequent paragraphs.

Transmit Delay time,  $tpPhyTxRMII$ , includes an uncertainty in propagation delay due to Process, Voltage, and Temperature (PVT) variations. Due to the 20ns (2 bit times) RMI Transmit variability, the delay is nominally 17 or 19 bits times. The PVT uncertainty is significantly less than 1 bit time.

### 3.1.2 DP83849 RMI Transmit Latency

In RMI mode, the DP83849 reduces the Transmit Latency variability in RMI mode. An IEEE 802.3 receiver must be able to detect the Start of Stream Delimiter at any alignment and does not require that IDLE bits arrive in an integer number of symbols. The receiver must operate on a stream of single bits as recovered from the physical medium. If the RMI data is not aligned to the symbol clock, the DP83849

will realign the symbol clock with the closest 125MHz Transmit clock. In this case, the DP83849 will send a series of IDLE symbols plus 1 to 4 additional IDLE bits before sending the Start of Stream Delimiter. Since the 125MHz Transmit clock is not an integer multiple of the frequency of the reference clock, one phase of the reference clock is aligned with the negative edge of the 125MHz Transmit clock. In this case there is an additional 4ns latency to sample data to the positive edge of the Transmit clock. The result is a 4ns variability in RMI Transmit latency, which will be selected at initialization time (reset) and should not change once the device is operational.

Transmit Delay time,  $tpPhyTxRMII$ , includes an uncertainty in propagation delay due to Process, Voltage, and Temperature (PVT) variations. In addition to minimizing the RMI Transmit variability, the DP83849 also reduced the nominal delay. Due to the 4ns (0.4 bit times) RMI Transmit variability, the delay is nominally 10.8 or 11.2 bits times. The PVT uncertainty is significantly less than 1 bit time. Transmit Delay time is the same for both Twisted Pair and Fiber modes of operation.

### 3.2 RMI RECEIVE LATENCY

RMI Receive latency is measured from the first symbol bit received on the wire (usually Cat5 cable) to the data symbol on the Receive RMI data bus. The measurement is made from the first bit of JK on the wire to the first bit of preamble (which replaces JK) on the RMI interface. As with the transmit side, the measurements are made to the REF\_CLK2 rising edge which samples the receive data. The measurement may also be made from the first bit of SFD on the wire to the SFD on the RX MII. Although not an official part of the RMI specification, RX\_DV is shown in the diagram rather than the combined CRS\_DV signal.

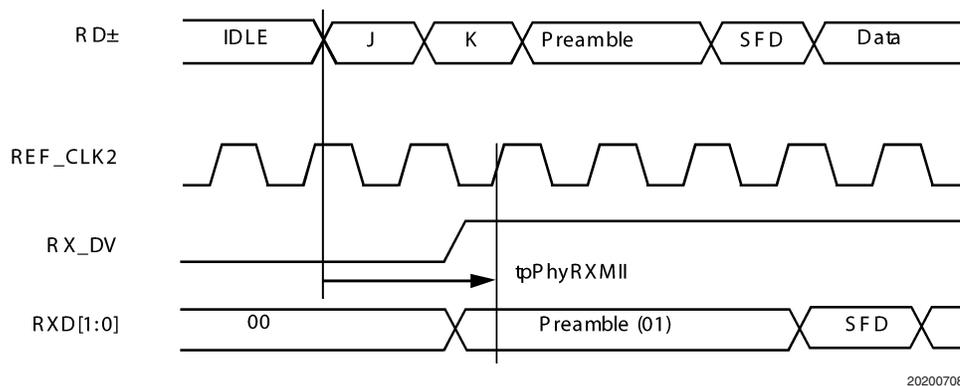


FIGURE 8. Phy Receive Delay Diagram

Many 100Mb Ethernet Phy devices will have delay uncertainty of 1 to 5 bit times (in 8ns bit time increments). This is the result of aligning the incoming receive data to an arbitrary phase of the 125MHz recovered clock. The DP83848 eliminates this uncertainty in the receive latency by deriving the receive clock from the data alignment. This process can in theory occur at the beginning of each packet (following assertion of CRS), but in practice will only occur for the first packet. Since IDLE data is sent as data symbols, subsequent packets will all arrive with the same alignment as the

initial received packet. By eliminating this variability, the DP83848 provides significantly more deterministic receive latency.

RMI latency includes additional delays to transfer data from the recovered Receive clock domain to the reference clock domain (REF\_CLK2). The result is an uncertainty of up to 20ns due to the potential skew between the reference clocks. This 20ns variation will be referred to as the RMI Receive variability in subsequent paragraphs. In addition the

### 3.0 RMII System Latency (Continued)

RMII interface must include an elasticity buffer to tolerate frequency differences between the transmitting and receiving stations. Due to the clock domain boundary and the elasticity buffer, the overall magnitude of the delay is greater than in MII mode.

Receive Delay time,  $tpPhyRxRMII$ , includes an uncertainty in propagation delay due to Process, Voltage, and Temperature (PVT) variations. The receive delay, as measured to the rising REF\_CLK2 edge, is nominally 40 to 42 bit times (bit time = 10ns) for Twisted Pair mode and 29 to 31 bit times for Fiber mode. The PVT uncertainty is less than 1 bit time.

#### 3.2.1 Effects of RMII Frequency Offset on Latency

Because RMII data is transferred between two clock domains with a frequency offset, data latency can vary across a single packet. The initial latency (for preamble/SFD) is essentially fixed, but the latency for subsequent data in a packet could have an increasing or decreasing latency dependent on the difference in the clock frequency. Assuming each reference clock is +/-50ppm, then the worst case frequency difference is a total of +/-100ppm.

For example, assume the transmitting clock is at 0ppm, but the destination clock is running at -50ppm. This means the destination clock is running slower (49.9975 MHz) than the

source clock (50.0000 MHz). This corresponds to a REF\_CLK2 clock period of 20.001ns. For each di-bit transferred on the RMII, the subsequent data will have an increased latency of 1ps.

For a 64-byte packet, data transferred is 8 preamble + 64 data bytes = 72 bytes = 288 di-bits. Thus the final nibble of data will have a latency approximately 288ps longer than for the first nibble of preamble. For a 1514 byte packet, data transferred is 8 preamble + 1514 data bytes = 1522 bytes = 6088 di-bits. Thus the final nibble of data will have a latency approximately 6.088ns greater than for the first nibble of preamble.

For the worst case where source and destination are +50ppm and -50ppm, the initial/final latency difference will be as large as 1.2 bit times for a full-size Ethernet frame. On the other hand, the total packet transfer time is dependent on the destination reference clock frequency. This is because the total packet latency is the initial latency plus the packet transfer time across the destination RMII

Total packet transfer time can be determined as:

$$tpPacketTotal = tpTotalPhyRMII + ((PktLength + 8) * 4 / Clk2Freq)$$

Clock2Freq is the frequency of the destination RMII clock, REF\_CLK2.

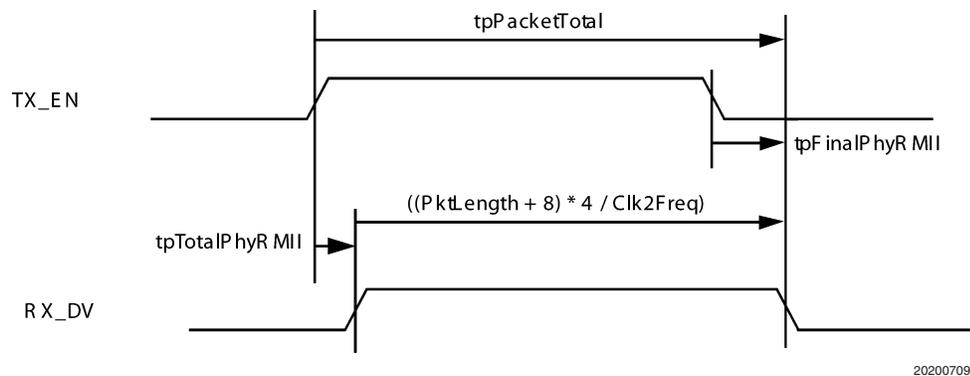


FIGURE 9. RMII Total Packet Transfer time

The final data latency,  $tpFinalPhyRMII$  can be determined based on the difference between the clock periods and the packet length:

$$tpFinalPhyRMII = tpTotalPhyRMII + (PktLength + 8) * 4 * (1/Clk2Freq - 1/Clk1Freq)$$

The system designer needs to be aware of which latency times are important: initial data latency, final data latency, or the total packet transfer time.

#### 3.2.2 RMII Programmable Elasticity Buffer

The DP83848 has a programmable Elasticity Buffer to provide tolerance for frequency offset between the transmitting and receiving devices. The typical latency numbers assume the minimum FIFO setting for the elasticity buffer, which is appropriate for standard Ethernet Frames at frequency tolerance of +/-50ppm. For larger frame sizes or to tolerate larger frequency offsets, the Elasticity Buffer can be programmed to handle the larger amount of data variation by changing the FIFO threshold. The first stage (default setting)

provides 2 bits of tolerance, which is plenty to handle the 1.2bit variance for standard Ethernet frames at +/-50ppm. Each of the 3 additional FIFO stages adds 4-bits to the total tolerance, but in doing so, also adds 4 bits to the receive latency. Thus if a system changes the Elasticity Buffer setting, the designer should expect an equal change in initial data latency.

### 3.3 RMII SYSTEM LATENCY MEASUREMENTS

The following End-to-End measurements were made for the total propagation delay between two DP83848 devices operating in 100Mb full-duplex and RMII mode. Measurements were made from the REF\_CLK1 which samples TX\_EN at the Transmit RMII, to REF\_CLK2 which samples first preamble data on the Receive RMII. The measurements were repeated 20 times with a power cycle between each measurement. Doing a full power cycle on both transmit and receive Phy devices is necessary to show the variability due to the transmitter alignment. Just dropping the link could

### 3.0 RMI System Latency (Continued)

show any receive effects but, in some cases, will not show the RMI Transmit variability described in Section 3.0 RMI System Latency.

In addition to the delay number, a measurement was made of the reference clock skew between the transmitting and

receiving Phy devices (REF\_CLK1 to REF\_CLK2). Measurements were made using a logic analyzer with 250ps resolution. Note that measurements were made on a single device at nominal voltage and room temperature. Results will vary slightly across Process/Voltage/Temperature.

Measurements were repeated for the DP83849 using the same method.

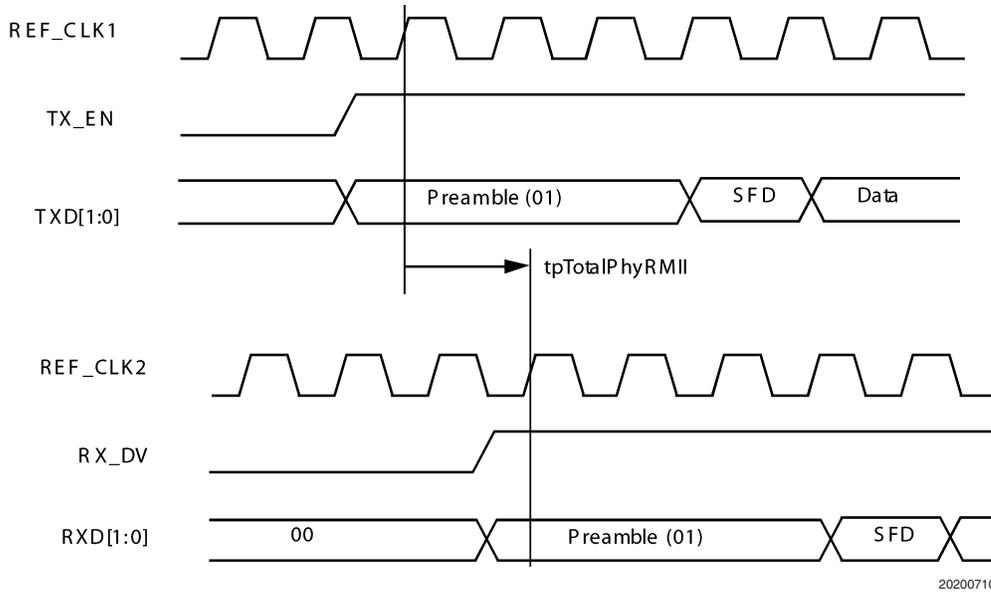


FIGURE 10. RMI System Delay Measurement

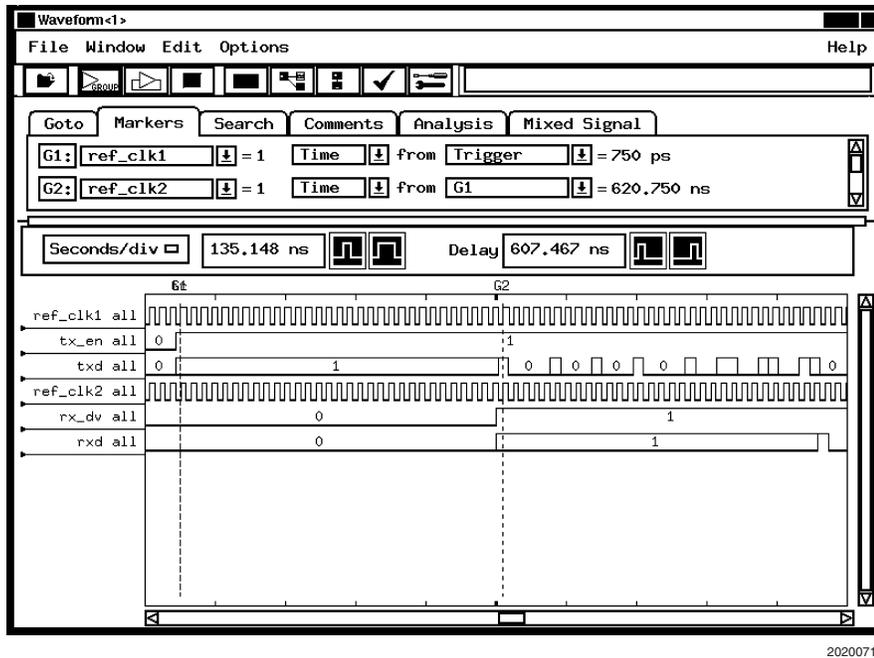


FIGURE 11. Example Trace for RMI Latency Measurement

## 3.0 RMI System Latency (Continued)

### 3.3.1 DP83848 RMI System Latency Measurements

The first set of measurements was made using a straight 10m cable.

**TABLE 4. Measurements of tpTotalPhyRMII with 10m Cable**

	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10
Delay (ns)	638.5	645.5	629.5	637	644.25	633.5	646	619.25	619	650
Clock Skew (ns)	17.75	5	9.5	17	3.75	13.75	6	19.5	19.25	10.25
	#11	#12	#13	#14	#15	#16	#17	#18	#19	#20
Delay (ns)	620.25	650.75	618.5	647	620.5	634.5	654	621.5	627	651.75
Clock Skew (ns)	0.25	10.75	18.5	6.75	0.5	14.5	13.75	1.5	7	11.25

- Min: 618.50ns
- Max: 654.00ns
- Range: 35.50ns

The limited number of data points and the range of reference clock skews does not quite show the possible range of values. As described in Section 3.0 RMI System Latency and Section 3.0 RMI System Latency, the total range of variability for the DP83848 is 40ns. The contributors are the 0ns/20ns step RMI Transmit variability (Section 3.1.1 DP83848 RMI Transmit Latency) and the 0ns-20ns range for RMI Receive variability (Section 3.2 RMI RECEIVE LATENCY).

**TABLE 5. Measurements of tpTotalPhyRMII with 0m Loopback Cable**

	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10
Delay (ns)	580.25	580.25	580.25	580.25	580.25	580.25	600	600	597.75	600.25
Clock Skew (ns)	0	0	0	0	0	0	0	0	0	0

- Min: 580.25ns
- Max: 600.25ns
- Range: 20ns

Note that a 46ns approximate cable delay, as determined from MII measurements, places these data within the range of values for the 10m cable. Also, note that this is not necessarily the minimum delay since the minimum delay is likely to be at a clock skew value that is non-zero.

**TABLE 6. Measurements of tpTotalPhyRMII Dropping Link (10m Cable)**

	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10
Delay (ns)	644.75	646.75	637.5	649.25	651.5	645.75	650.25	645.5	647.5	640.75
Clock Skew (ns)	4.25	6.25	17	8.75	10.75	5.25	9.75	5	7	0.25
	#11	#12	#13	#14	#15	#16	#17	#18	#19	#20
Delay (ns)	640.25	638.75	652.5	652.75	638.25	645.25	649	651.75	638	646
Clock Skew (ns)	19.5	18.25	12	12.25	17.75	4.75	8.5	11.25	17.5	5.5

- Min: 638.00ns
- Max: 652.75ns
- Range: 14.75ns

The limited number of data points and the range of reference clock skews does not show the possible range of values.

### 3.3.2 DP83848 RMI Transmit Variability

A second set of measurements was made with a loopback plug (0m cable). In loopback, the reference clock is the same for transmit and receive (0ns skew), eliminating that source of variability. Since the variability is limited, only 10 sets of measurements were made. This test shows just the 0ns/20ns step variability due to the phase of the Transmit Reference clock.

### 3.3.3 DP83848 RMI Receive Variability

A third set of measurements was made using just a re-link (by unplug/plug the cable). This mechanism shows the limitations in this test as it eliminates any variation on the transmit RMI. The uncertainty that remains is just the Receive variability. For this test, 20 measurements were made with a 10m straight cable.

Since only receive variability applies, the total range of variability is 20ns.

### 3.0 RMI System Latency (Continued)

#### 3.3.4 DP83849 RMI System Latency Measurements in Twisted Pair Mode

The first set of measurements was made using a straight 10m cable.

**TABLE 7. Measurements of tpTotalPhyRMII with 10ft Cable**

	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10
Delay (ns)	562.75	569.5	557.25	557.25	556.75	562.5	567	561.5	559.25	555.25
Clock Skew (ns)	2.75	9.5	17.25	17.25	16.75	2.5	7	1.5	19.25	15.25
	#11	#12	#13	#14	#15	#16	#17	#18	#19	#20
Delay (ns)	560.75	555.75	570	560.5	566.75	571.25	550.75	555.5	560.5	572.75
Clock Skew (ns)	0.75	15.75	10	0.5	6.75	11.25	10.75	15.5	0.5	12.75

- Min: 550.75ns
- Max: 572.75ns
- Range: 22.0ns

The limited number of data points and the range of reference clock skews does not quite show the possible range of values. As described in Section 3.0 RMI System Latency and Section 3.2 RMI RECEIVE LATENCY, the total range of variability for the DP83849 is 24ns. The contributors are the 0ns/4ns step RMI Transmit variability (Section 3.1.2 DP83849 RMI Transmit Latency) and the 0ns-20ns range for RMI Receive variability (Section 3.2 RMI RECEIVE LATENCY).

**TABLE 8. Measurements of tpTotalPhyRMII with 0m Loopback Cable**

	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10
Delay (ns)	520	520	520	520	520	520	520	520	520	520
Clock Skew (ns)	0	0	0	0	0	0	0	0	0	0

- Min: 520.00ns
- Max: 520.00ns
- Range: 0ns

Note that a 46ns approximate cable delay, as determined from MII measurements, places these data within the range of values for the 10m cable. Also, note that this is not necessarily the minimum delay since the minimum delay is likely to be at a clock skew value that is non-zero.

**TABLE 9. Measurements of tpTotalPhyRMII dropping link (10m cable)**

	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10
Delay (ns)	556.5	563.75	575.25	564	568	565.5	567.25	562	559	572.75
Clock Skew (ns)	16.5	3.75	15.25	4	8	5.5	7.25	2	19	12.75
	#11	#12	#13	#14	#15	#16	#17	#18	#19	#20
Delay (ns)	573.75	557.25	561.25	567	560.5	555.75	558	567.5	562.75	575.75
Clock Skew (ns)	1375	17.25	1.25	7	0.5	15.75	18	7.5	2.75	15.75

- Min: 555.75ns
- Max: 575.75ns
- Range: 20.00ns

Although the test involved a limited number of datapoints, it does appear to show the full possible range of values. Since

#### 3.3.5 DP83849 RMI Transmit Variability

A second set of measurements was made with a loopback plug (0m cable). In loopback, the reference clock is the same for transmit and receive (0ns skew), eliminating that source of variability. Since the variability is limited, only 10 sets of measurements were made. Since the step variability is only 4ns for the DP83849, the test is unable to show this variability. Since the reference clocks are identical, only variations in multiples of reference clocks will be detected. The results showed a consistent value of 520ns. This test shows just the Transmit Variability is less than 1 reference clock period.

#### 3.3.6 DP83849 RMI Receive Variability

A third set of measurements was made using just a re-link (by unplug/plug the cable). This mechanism shows the limitations in this test as it eliminates any variation on the transmit RMI. The uncertainty that remains is just the Receive variability. For this test, 20 measurements were made with a 10m straight cable.

only receive variability applies, the total range of variability is 20ns.

### 3.0 RMI System Latency (Continued)

#### 3.3.7 DP83849 RMI System Latency Measurements in Fiber Mode

The RMI system latency measurements were also made between two DP83849 devices operating in 100Mb full-

duplex Fiber mode. The devices were connected through Agilent HFBR5803 fiber transceivers and 10ft of fiber cable. The test procedure was otherwise identical to the procedure described in Section 3.3.1 *DP83848 RMI System Latency Measurements*.

**TABLE 10. Measurements of tpTotalPhyRMI with 10ft of Fiber Cable**

	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10
Delay (ns)	430.25	425.25	430.75	443.75	440.25	433.75	446.75	440.5	435.75	433.5
Clock Skew (ns)	10.25	5.25	11	3.75	0.25	13.75	6.75	0.5	15.75	13.5
	#11	#12	#13	#14	#15	#16	#17	#18	#19	#20
Delay (ns)	430.75	430.75	437	429.25	434.25	434.75	440.5	430.25	438	430
Clock Skew (ns)	10.75	10.75	17	9.25	14.25	14.75	0.5	10.25	18	10

- Min: 426.25ns
- Max: 446.75ns
- Range: 21.50ns

The limited number of data points and the range of reference clock skews does not quite show the possible range of values. As described in Section 3.0 *RMI System Latency* and Section 3.2 *RMI RECEIVE LATENCY*, the total range of variability for the DP83849 is 24ns. The contributors are the 0ns/4ns step RMI Transmit variability (Section 3.1.2 *DP83849 RMI Transmit Latency*) and the 0ns-20ns range for RMI Receive variability (Section 3.2 *RMI RECEIVE LATENCY*).

### 4.0 Conclusions

This document provides detailed information on the transmit and receive latencies of the National Semiconductor DP83848 and DP83849 Ethernet Transceiver family. The information should be used as a guide for system designers who are concerned with the overall system latencies for data transfer. The following table summarizes the transmit and receive latencies for various modes of operation (1 bit time = 10ns). The table also includes the uncertainty due to clock alignment for each mode of operation. The uncertainty does not include the small amount of variability due to variations in Process, Voltage, or Temperature.

**TABLE 11. Summary of Transmit and Receive Latencies**

MII	Transmit Latency (bit times)	Uncertainty (ns)	Receive Latency (bit times)	Uncertainty t(ns)	Total TX+RX Uncertainty (ns)
DP83848 100BASE-TX	5	0	25.5	0	0
DP83849 100BASE-TX	5	0	25.5	0	0
DP83849 100BASE-FX	5	0	16	0	0
RMI					
DP83848 100BASE-TX	17 or 19	20	40 or 42	20	40
DP83849 100BASE-TX	10.8 or 11.2	4	40 or 42	20	24
DP83849 100BASE-FX	10.8 or 11.2	4	29 or 31	20	24

The results show that in MII mode, the device has minimal uncertainty in latency, even in the receive direction. **The DP83848 and DP83849 do not suffer from a common 1 to 5 bit variability due to aligning receive data to the receive clock.**

In RMI mode, the main sources of non-determinism are due to uncertainty in data alignment relative to the 50MHz reference clock. Some variability is due to the nature of the RMI interface and will exist with any RMI Ethernet device. **The DP83849 reduces the RMI Transmit variability from 20ns to 4ns.** The DP83849 produces the minimum RMI Receive variability of 20ns. Again, RMI receive latency does not include the 1 to 5 bit time variability due to receive data alignment.

In addition, it is important to note that system latencies are very much dependent on the cable connecting the two devices. This document has not attempted to quantify variations due to cable length or cable type, other than to show that the variation does exist and can be significant.

Opportunities exist to further reduce fixed components and variances in end-end system latency. By better understanding customer needs and system requirements, National Semiconductor will continue to offer devices delivering industry leading performance for Industrial and Real-time Ethernet applications.

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