

TOSHIBA

2004-1

PRODUCT GUIDE

CMOS ASICs

2004 semiconductor
<http://www.semicon.toshiba.co.jp/eng>

To ensure competitiveness in the marketplace, you will need to produce more sophisticated, more technology-intensive and higher value-added products, using a process of technological innovation and systematic marketing. Toshiba's application-specific integrated circuits (ASICs) will give you an edge beyond your expectations. You can select from gate arrays, cell-based ICs and embedded arrays, depending on your performance and time-to-market objectives. For the latest updates on our ASICs, please visit the ASIC section on our website.

GATE ARRAY CELL-BASED IC EMBEDDED ARRAY

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System ASICs

In keeping with our overriding commitment to meeting customers' present and future needs, Toshiba continuously pursues new goals in the exploration of both silicon technologies and design techniques.

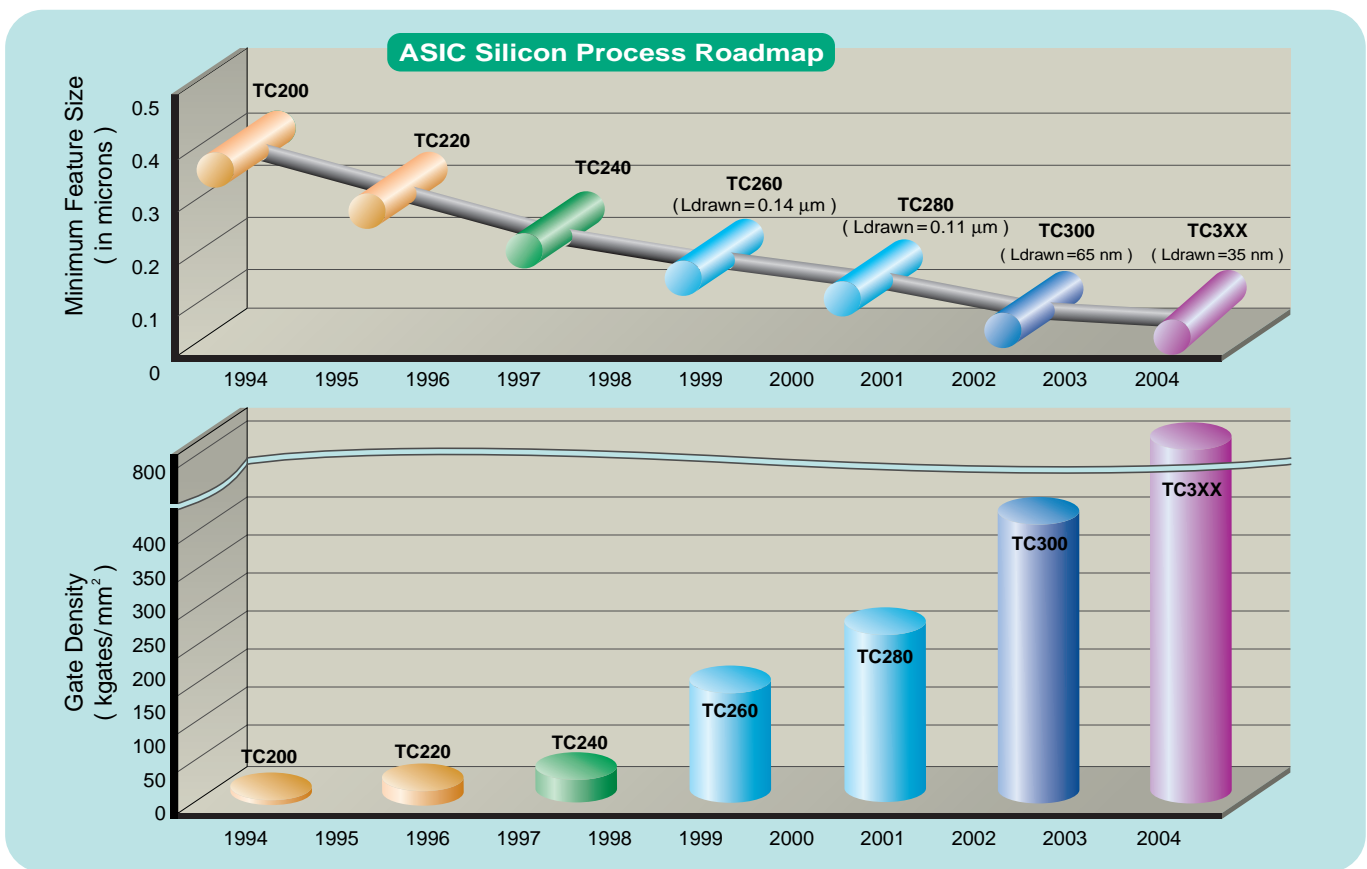
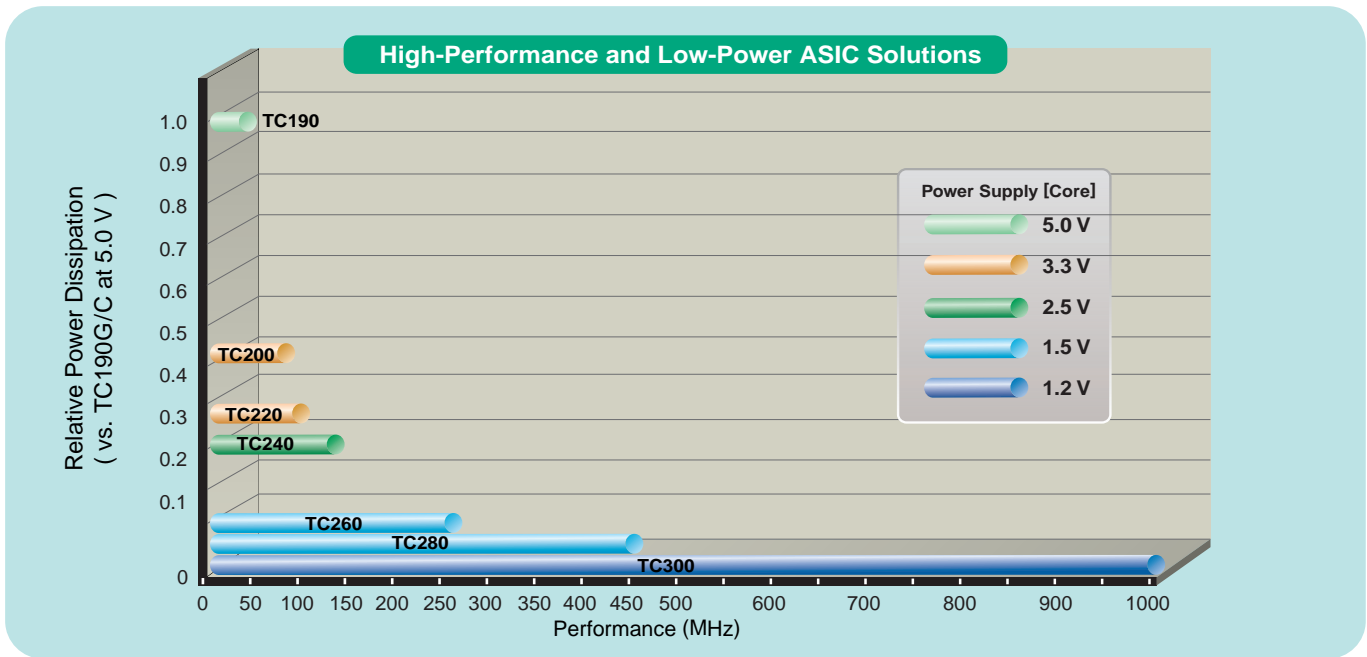
With its endeavors to stay at the leading edge of technology has come yet another paradigm shift—a transformation from an integrated circuit to an integrated system-on-a-chip. That trend is already well under way.

For true system-scale integrations, ASIC silicon technologies must cover a full spectrum of application requirements with a broad range of power, density and speed solutions, complete with support of core functions and high-performance I/Os.

The high-density and low-power features of Toshiba ASICs are essential elements for the success of advanced ASIC designs for consumer, communications, and data processing applications.

In addition, Toshiba offers the right combinations of innovative design capabilities to meet your performance requirements.

With Toshiba's pre-defined cells and design techniques, you can maximize design productivity while minimizing costs.



Applications

AV Systems

Communications Equipment

Office / Business Equipment

Mass Storage Devices

Entertainment

Technology Enablers

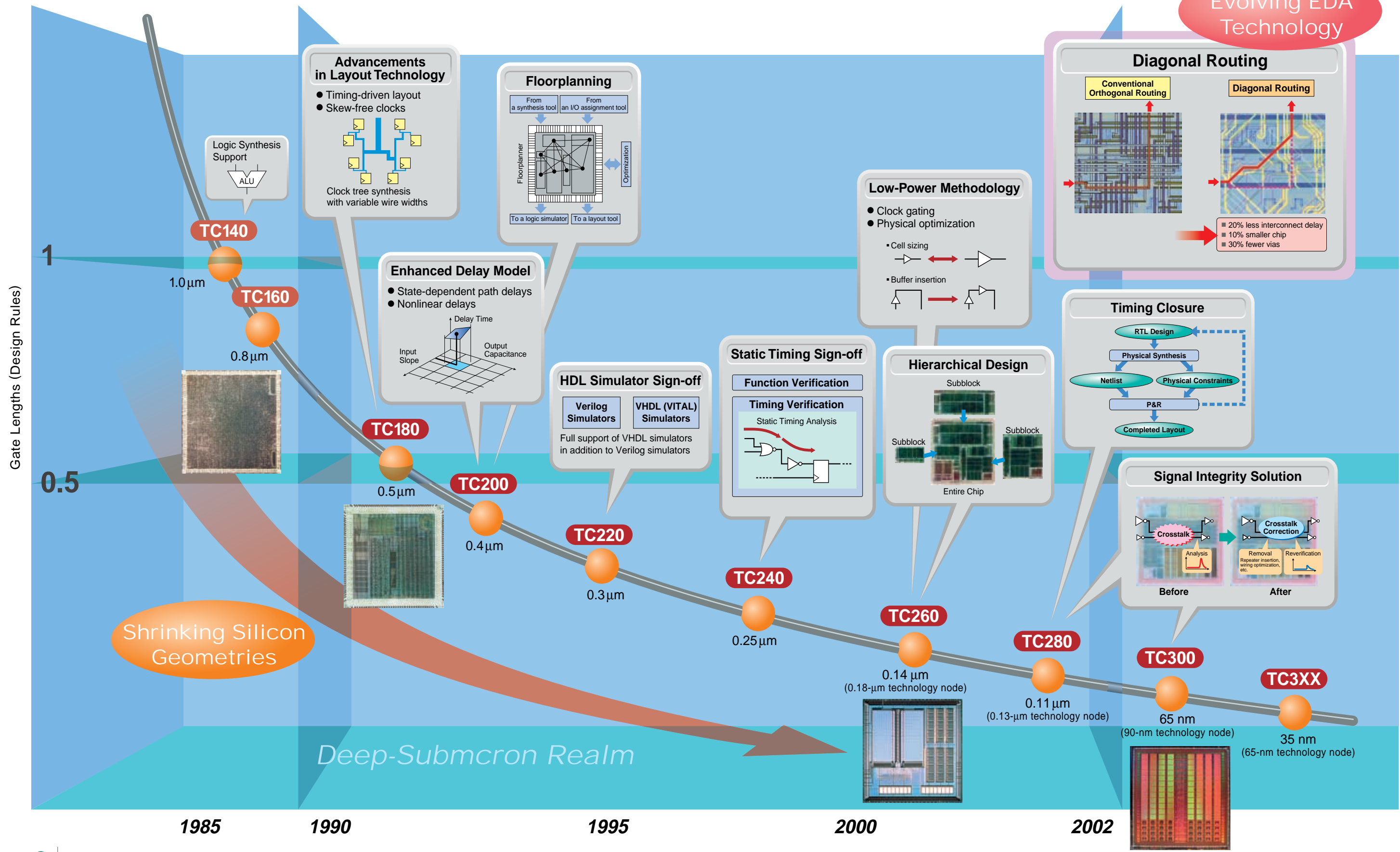
- **High density**
TC300 family
TC280 family
- **Low power**
1.5-V, 2.0-V, 2.5-V, 3.3-V, or mixed I/O voltage levels, aggressive cell architecture, power-driven layout
- **Advanced packaging**
(Reduced footprint size, low profile and high pin count)
Stacked PFBGA (SiP), PFBGA, PBGA, etc.

- **System interconnect I/Os**
LVDS, GTL, PCI, USB, etc.
- **Precision analog cells**
A/D and D/A converters, analog PLL, etc.
- **Large-capacity & high-speed on-chip memory**
DRAM, SRAM, FIFO
- **Embedded CPU cores**
RISC cores, CISC cores

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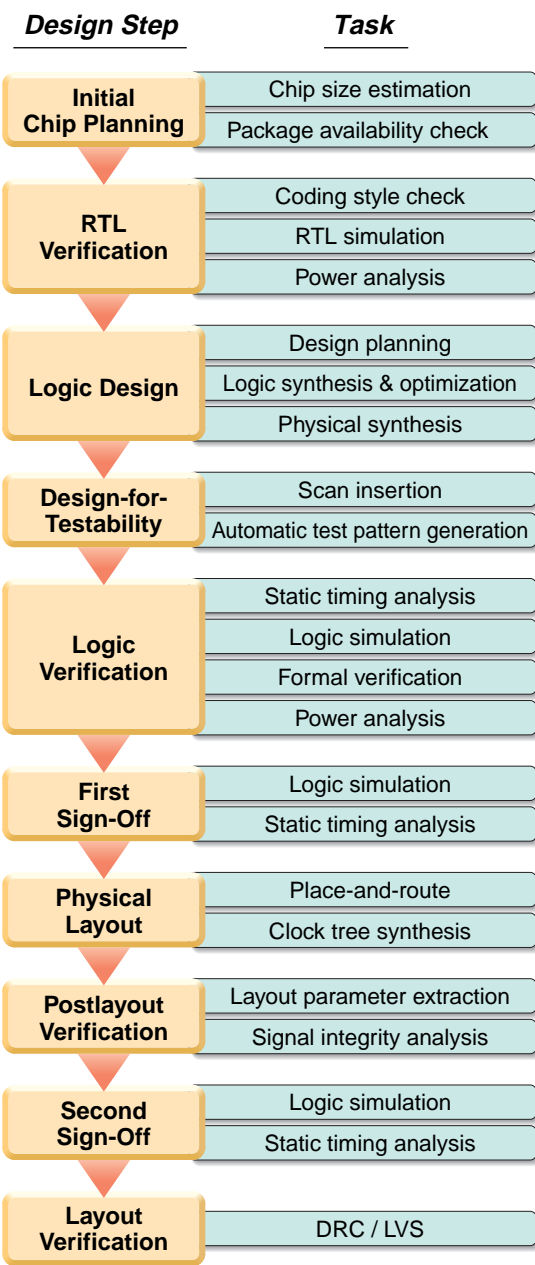
Toshiba's ASIC EDA Solutions

Toshiba's Evolving SoC EDA Solutions



Design Kit Support

Typical Design Flow



Supported EDA Tools and Design Kit Availability

ASIC Product Family EDA Tool		Cell-Based ICs										Gate Arrays					Embedded Arrays						
		TC 300C	TC 280C	TC 260C	TC 240C		TC 223C	TC 222C	TC 220C	TC 203C	TC 200C	TC 190C	TC 223G	TC 220G	TC 203G	TC 200G	TC 190G	TC 260E	TC 240E	TC 223E	TC 220E	TC 203E	TC 200E
Logic Synthesis Tools	Design Compiler																						
	BuildGates																						
Simulators	Verilog-XL																						
	VCS																						
	NC-Verilog																						
	ModelSim																						
	NC-VHDL																						
Static Timing Analysis Tools	PrimeTime																						
Formal Verification Tools	Design VERIFYer																						
	Formality																						
	Conformal LEC																						
DFT Tools	DFT Compiler / BSD Compiler																						
	DFTAdvisor / FastScan																						
	TetraMAX																						
Power Analysis and Optimization	Power Theater																						
	Power Compiler																						

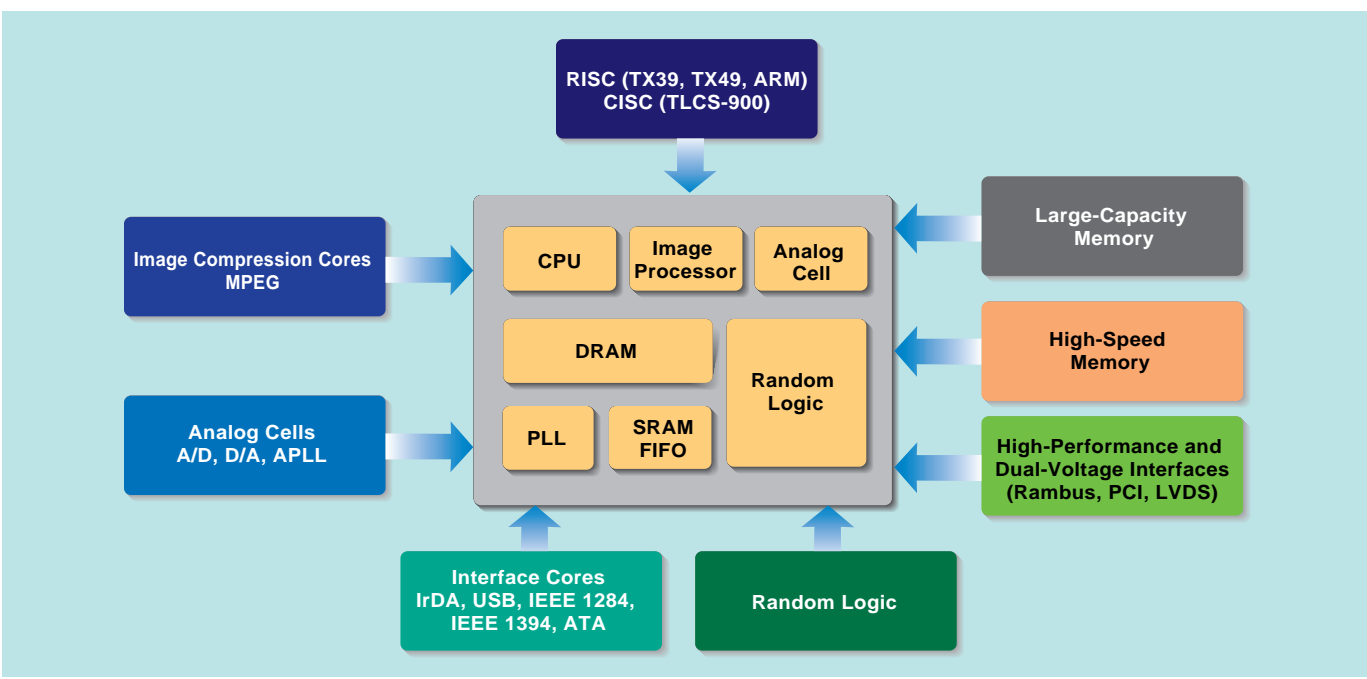
The above table shows the basic cell availability status. For availability of megacells such as RAMs and ROMs, ask the nearest Toshiba ASIC design center. Please obtain the latest technical material before you begin creating a design.

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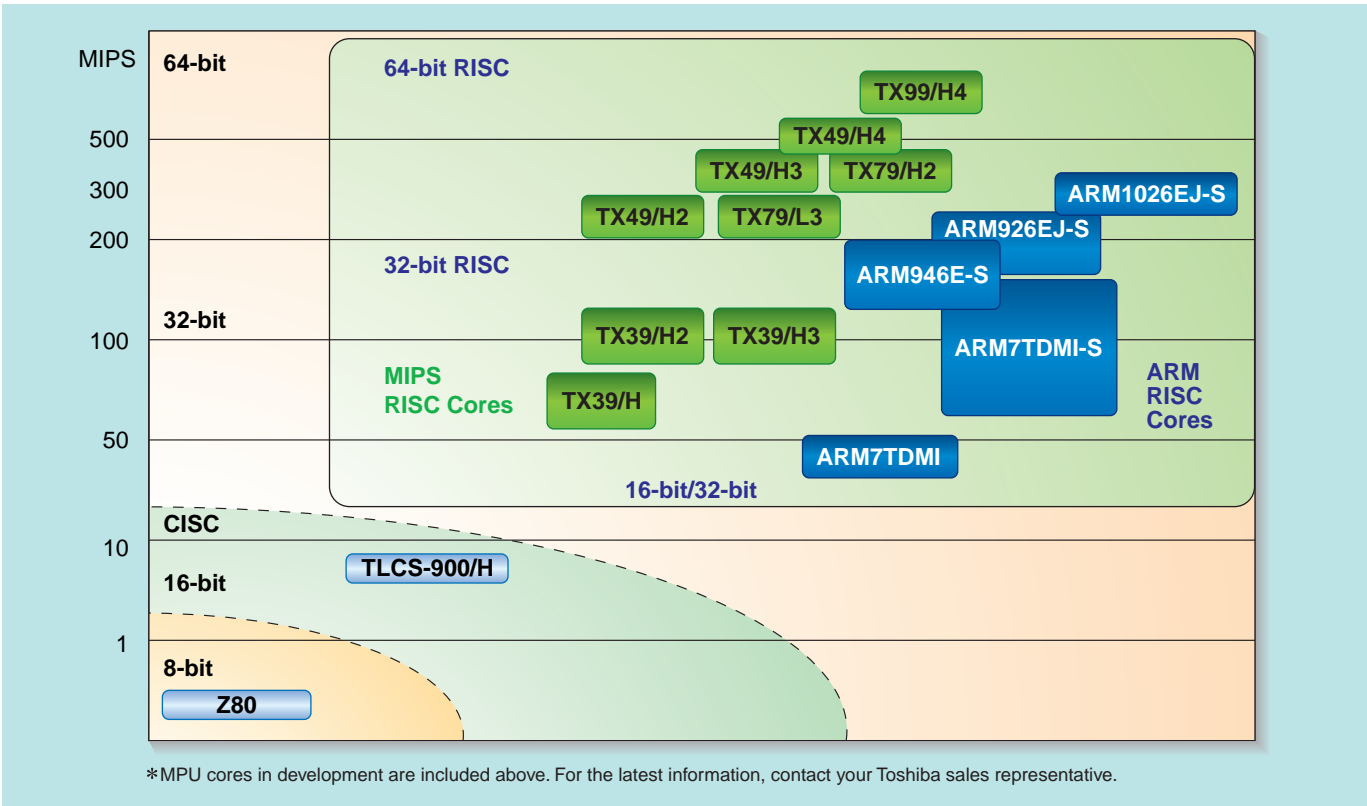
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System ASIC Implementation

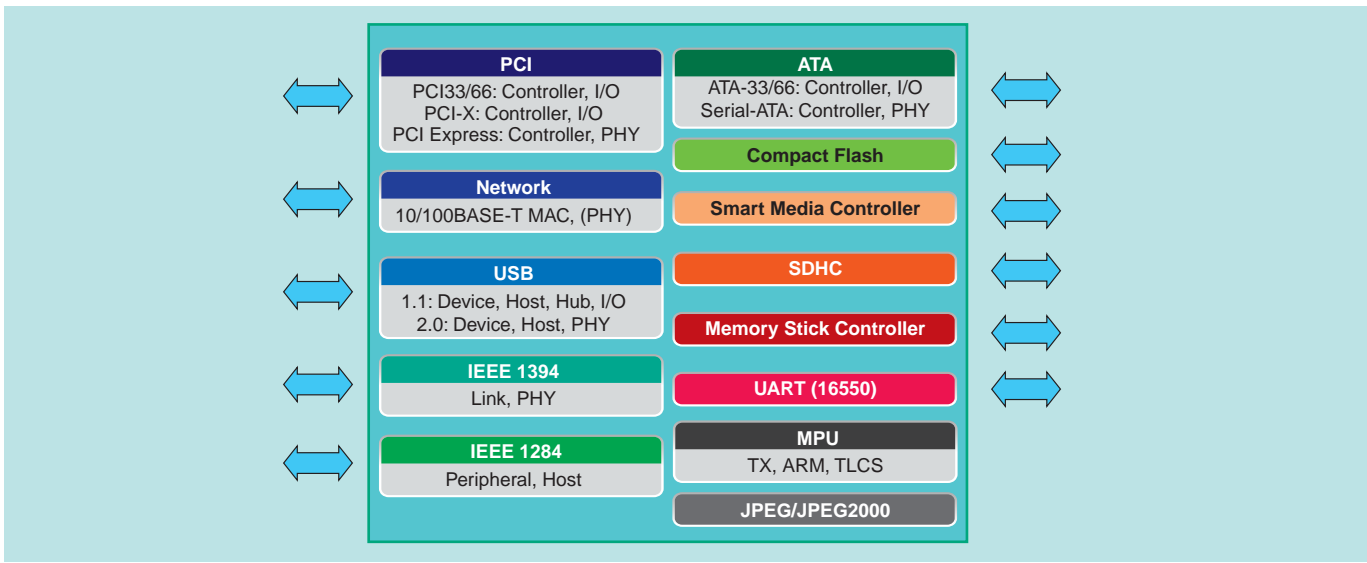
Toshiba offers a gallery of IP cores for system ASICs, including TX39 RISC cores, TLCS-900 CISC cores, DRAM cores and interface cores. Toshiba is also designing discrete components in such a manner as to make it easy to implement them as ASIC-ready IP cores.



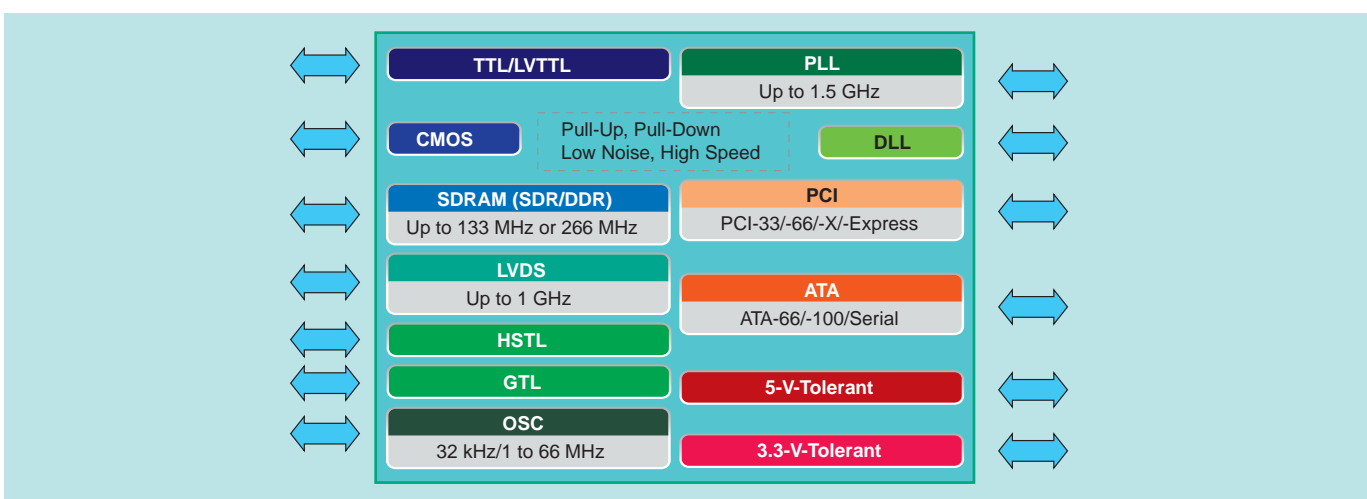
MPU Cores



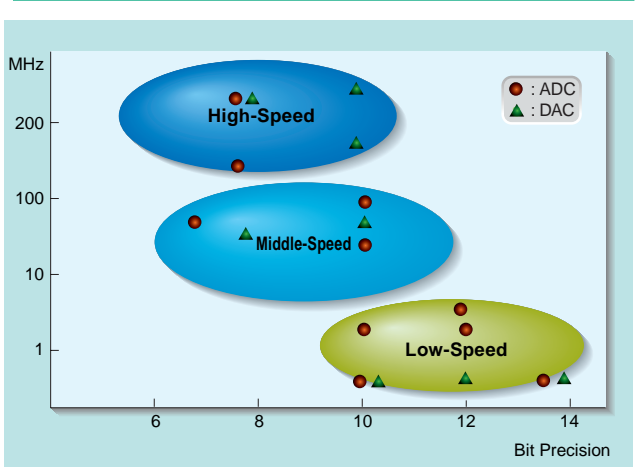
IP Cores



I/O Cells



A/D and D/A Converters



Memory (SRAM/ROM)

	Async.	RAM		Register File	ROM
		1- Port, Sync.	2- Port, Sync.		
TC190 (0.6 μm)	RAMA RAMC (~4 Kbits)	RAMB RAMC (~16 Kbits)	RAMC RAMC (~16 Kbits)	FV (1R/1W) FW (2R/1W) FX (2R/2W) FY (3R/1R)	ROMA ROMC ROMD
TC200 TC203 (0.4 μm)	RAMC (~4 Kbits)	RAML (~16 Kbits) RAMM (~128 Kbits)	RAMP (~64 Kbits)		ROMC ROMD
TC220 TC223 (0.3 μm)		High-Density, 1-Port	High-Density, 2-Port	High-Speed, 1-Port	High-Speed, 2-Port
TC240 (0.25 μm)	RAMS1A (~512 Kbits)	RAMS2A (~72 Kbits)	RAMS1B	RAMS2B	RFS11A (1W/1R) RFS12A (1W/2R) RFS13A (1W/3R) RFS14A (1W/4R) RFS22A (2W/2R)
TC260 (0.14 μm)	RAMS1D (~512 Kbits) RAMS1F	RAMS2D (~256 Kbits) RAMS2F	RAMS1E (~512 Kbits)	RAMS2E (~256 Kbits)	RFS11D (1W/1R) RFS12D (1W/2R) RFS14D (1W/4R) RFS22D (2W/2R)
TC280 (0.11 μm)	RAMS1G (~512 Kbits) RAMS1J	RAMS2G (~256 Kbits) RAMS2J	RAMS1H (~512 Kbits)	RAMS2H (~256 Kbits)	RFS11G (1W/1R) RFS12G (1W/2R) RFS14G (1W/4R) RFS22G (2W/2R)
TC300 (65 nm)	RAMS1L (~512 Kbits) RAMS1M	RAMS2M (~72 Kbits) RFS11M	RAMSxx		RFS11L (1W/1R) RFS12L (1W/2R)

Embedded DRAM Cores

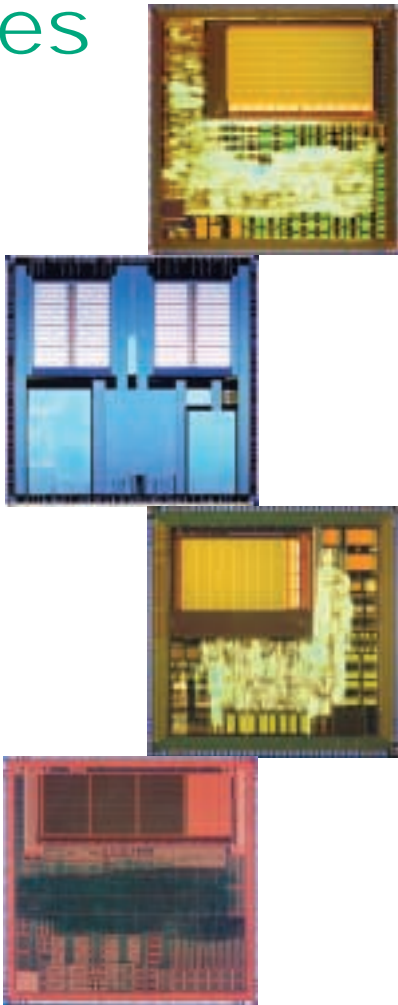
With high memory data transfer rates and low power consumption, EDRAM SoCs enable high-performance and high-value-added systems. EDRAM SoCs also reduce system board area. —SoCs with synchronous DRAMs and fast-access DRAMs

The ever-increasing design complexity and the drive for system-on-chips (SoCs) are driving demand for a greater capability to take advantage of pre-designed, re-usable building blocks. Many analysts see the embedded DRAMs (EDRAMs) as the last piece of the architectural puzzle necessary for SoCs for the next-generation products. Through six generations of experience in EDRAMs, Toshiba has developed EDRAMs with differentiating data transfer rates and low power consumption.

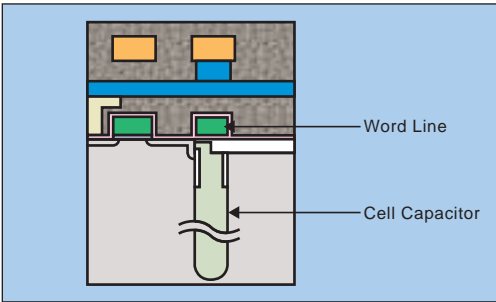
Toshiba's EDRAMs offer the following features and benefits:

- High performance with fast data transfer rates due to wide on-chip memory buses
- Much denser than SRAM
- Low power
- Soft error prevention
- System architecture optimization and reduction of discrete components
- Easy and effective testing with a direct-access test and DRAM BIST
- High yield through redundancy in DRAM macros
- Various types of DRAM macros with configurable depth and width

The low-power and high-bandwidth characteristics of Toshiba's embedded DRAM make it ideal for a wide range of applications, including video/image processing devices such as graphics and display controllers; storage devices such as HDD controllers; and digital communication and networking devices.



DRAM Core Features



Trench Process

The one-transistor (1T) DRAM cell structure utilizes the trench process. The trench capacitor allows for a planar surface topology that enhances reliability without compromising logic performance.

High Bandwidth

Freed from I/O restrictions, embedded DRAM cores provide high memory bandwidth with a synchronous interface and a bus width selectable from 64, 128 and 256 bits.

Configurable Macros

DRAM macros are configurable in depth and width to suit particular application requirements, allowing great system flexibility.

Low Power Consumption

DRAM macros consume less than 5% of power, compared to commodity DRAMs.

DRAM Cores for the TC300 Family

90 nm

The TC300C cell-based ASIC family, fabricated with drawn gate lengths of 65 nano meter offers a variety of embedded DRAM cores. Designers can use the same primitive and I/O cells as well as any IP cores available for the TC300C pure logic process without compromising logic performance. The power-saving mode reduces the standby power of the DRAM cores, broadening the range of their applications in mobile equipment. The TC300C offers two types of DRAM cores.

Standard Synchronous DRAM (SD) macros

The standard SD macros are available in capacities from 2 Mb to 32 Mb and can operate over a wide range of clock frequencies. The SD macros are suitable for applications requiring fast page-mode accesses.

The Fast-Access (FA) DRAM macros offer significant advantages over the SD macros in random-access cycle times or data output times.

1. FA-RC macros have fast random-access cycle times

With random-access cycle times of 8 ns, the FA-RC macros are efficient for applications dominated by small random accesses.

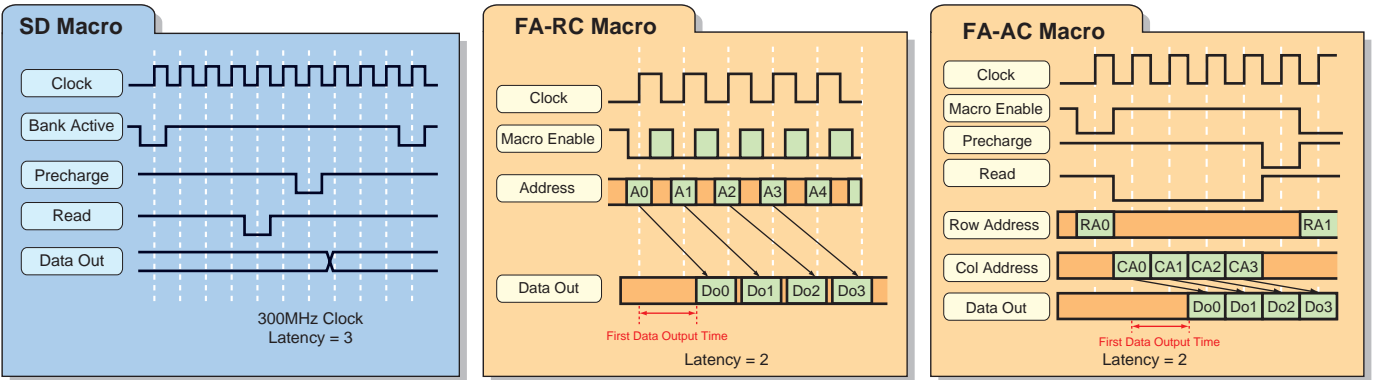
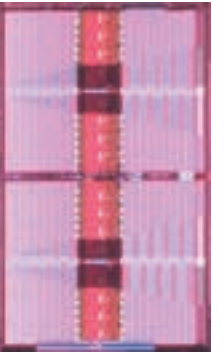
2. FA-AC macros have fast 1st data output times

The FA-AC macros achieve an address-to-data-out delay as low as 6 ns for the first access. These cores are ideal for applications requiring extremely fast page-mode accesses.

SD Macro



FA-Macro



Characteristic	SD	FA-RC	FA-AC
Random Access Cycle Time	33.3 ns	8 ns	9.99 ns
Latency	1, 2, 3	1, 2, 3	1, 2, 3
First Data Output Time		12 ns	6 ns
Max Clock Frequency (Page Mode)	300 MHz		300 MHz
Memory Capacity	2 to 32 Mbit	2, 4, 8, 16 Mbit	2, 4, 8, 16 Mbit
Bit Width	64/128/256	32/64/128	32/64/128

DRAM Cores for the TC280 Family

0.13μm

DRAM cores are also offered for use in ASICs based on the 0.11-micron drawn-gate-length TC280 family. SD and FA cores are available.

Characteristic	SD	FA-RC	FA-AC
Random Access Cycle Time	40 ns	10 ns	12 ns
Latency	1, 2, 3	1, 2	2, 3
First Data Output Time		14 ns	10 ns
Max Clock Frequency (Page Mode)	250 MHz		250 MHz
Memory Capacity	2 to 32 Mbit	2, 4, 8 Mbit	2, 4, 8 Mbit
Bit Width	64/128/256	128/256 144/288	128/256 144/288

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ASIC Packaging

There are a number of factors to consider when selecting an optimal package configuration: I/O requirement, package footprint/form factor, thermal dissipation, electrical performance, and cost-to name a few. With ASICs now being introduced exceeding 16-million gate and operating at clock frequencies of 250 MHz and beyond, accurate package data and selection is critical. To meet system-level performance and density requirements, packages with better thermal and electrical characteristics that do not impact the performance of the die are needed. New advanced packaging technologies, such as Chip Scale Package(CSP) are currently available to meet the ever increasing market demand for smaller size, more I/Os, and lower cost.

Toshiba offers a broad and varied range of package options for all ASIC families to suit all applications. Whether your design requires a 16-lead DIP or 2304-PBGA[FC], Toshiba offers expert guidance and innovative solutions to help you achieve Your design goals.

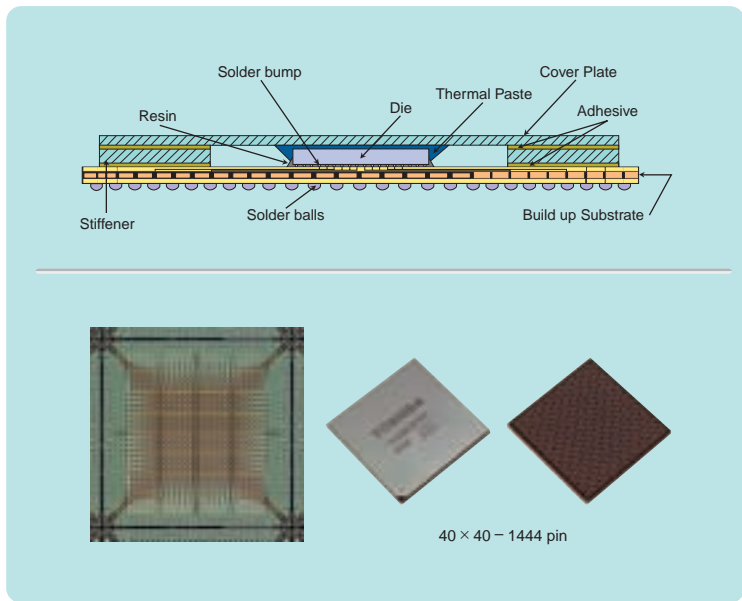
PBGA [FC]

PBGA[FC] stands for “plastic ball grid array with flip-chip bonded die”.

Characterized by its ability to support more than 1000 pins, the PBGA[FC] is mainly used in network and communications applications.

Externally the package can have as many as 2304 pins and can support a complete ball matrix with a pitch of 1.0 mm.

The die, which has lattice-pattern solder balls, is mounted face down on a built-up substrate and reflow-soldered.



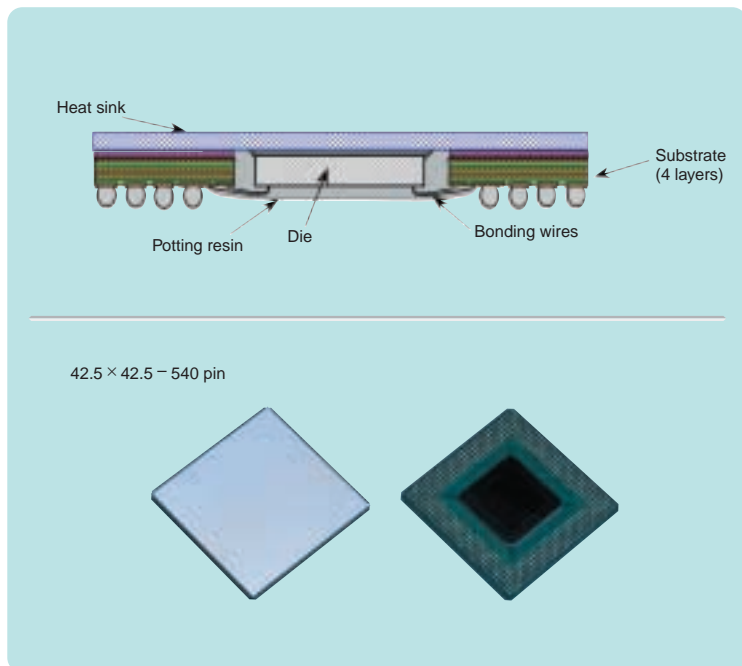
EBGA [4L]

EBGA[4L] stands for “enhanced ball grid array with four layers”.

Characterized by its excellent electrical characteristics and low thermal resistance despite its slim profile, the EBGA[4L] is mainly used in network and communications applications.

Externally the package has between 352 and 540 pins, a ball pitch of 1.27 mm and a four-layer plastic substrate.

The die is directly connected to a heat slag for low thermal resistance and achieves high-speed operation and noise suppression by virtue of its multiple layers. This package has an advanced-function structure capable of supporting high-end products.



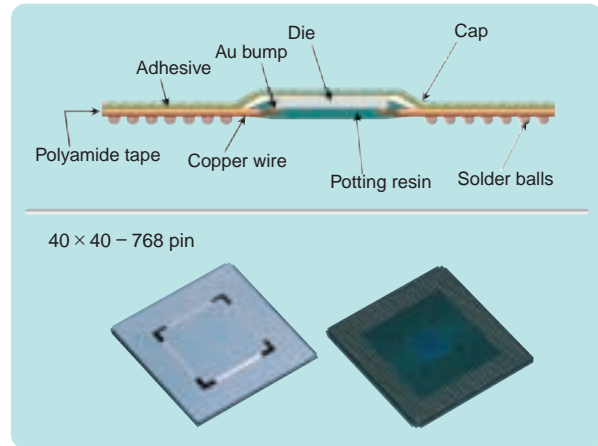
TBGA

TBGA stands for “tape ball grid array”.

Characterized by its low cost and excellent heat dissipation despite its high pin count, the TBGA is mainly used in PC and network applications.

Externally the package has between 256 and 868 pins, and has a ball pitch of 1.00 mm to 1.27 mm.

The die is bonded using TAB (tape-automated bonding) technology and a cover plate is attached after sealing.



PFBGA

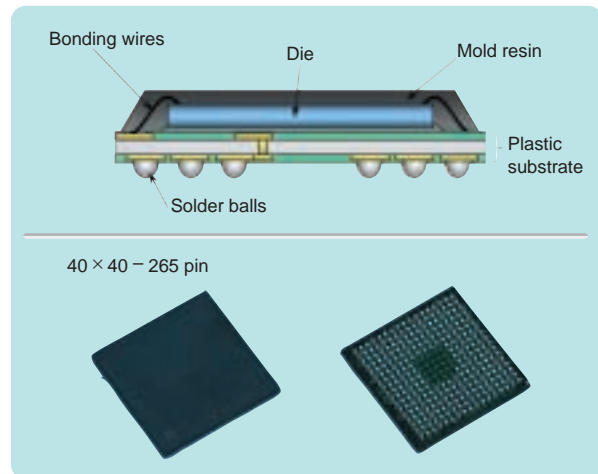
PFBGA stands for “plastic fine-pitch ball grid array”.

Characterized by its small size, slim profile and low cost, the PFBGA is mainly used in PCs, DVC (desktop video conferencing) applications and cell phones.

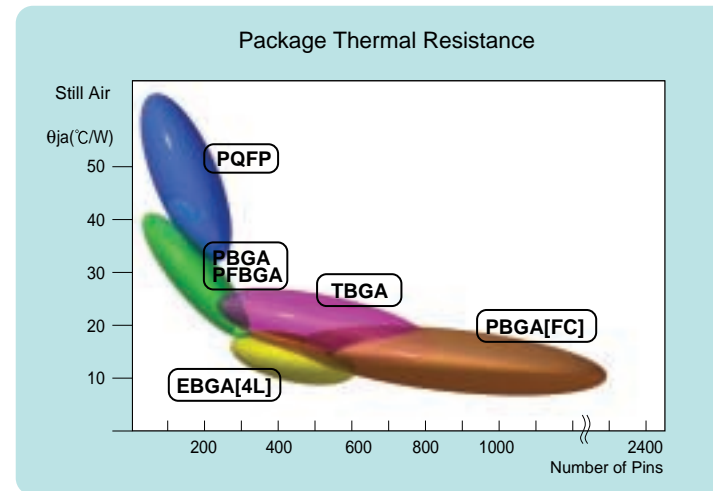
Externally the package has between pitch 97 and 361 pins, and has a ball pitch of 0.8 mm and 0.65 mm.

0.5-mm packages are also scheduled for development.

The die is mounted on a plastic substrate, bonded with wire and molded.

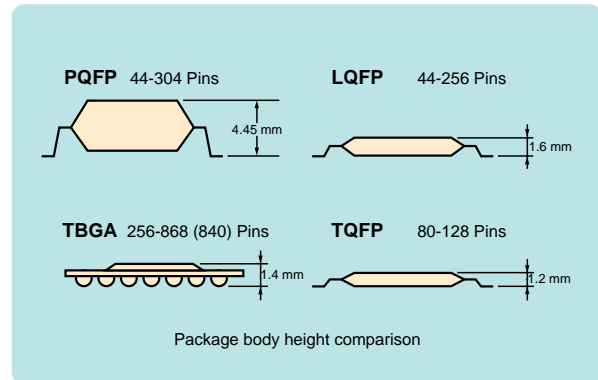


Package Thermal Resistance Comparison



To enable new electronic products, the heat removal capability is an important aspect of packages. Thermal resistance varies with the style and pin density of the package.

Thin-Profile Packages



A need to constantly reduce the size of products is driving the demand for small, thin packages. For applications where overall package height is a concern, Toshiba offers packages with a body thickness of 1.6 mm or less. TBGA packages support pin counts higher than achievable with PQFP packages.

Package Electrical and Thermal Characteristics

The following table shows the electrical and thermal characteristics of the packages available from Toshiba. Upon request, Toshiba provides support for electrical and thermal analysis of the packages. For details, contact your nearest Toshiba ASIC Design Center.

Electrical Specification						Thermal Resistance		
Package Type	Body Size	Pin Count	L (nH)@100Mz	C (pF)@100Hz	R (Ω)@100Hz	θjc (°C/W)	θja (°C/W)	
							0 (m/s)	
PBGA[FC]	27x27	625	0.4 to 7.7	0.1 to 1.4	0.03 to 0.72	Typ. 0.2	Typ. 5 to 10	
	31x31	841	0.4 to 9.9	0.1 to 1.7	0.03 to 0.93			
	35x35	1089	0.2 to 11.5	0.03 to 2.0	0.02 to 1.08			
	40x40	1444	0.2 to 13.7	0.03 to 2.4	0.02 to 1.3			
	45x45	1849	0.4 to 16.5	0.1 to 2.9	0.03 to 1.5			
EBGA[4L]	50x50	2304	0.2 to 19.2	0.03 to 3.4	0.02 to 1.8	Typ. 0.3	Typ. 10	
	35x35	352	4.1 to 9.5	0.2 to 1.4	0.3 to 0.6			
TBGA[1B]	42.5x42.5	540	3.8 to 11.1	0.2 to 1.7	0.3 to 0.7	Typ. 1 to 3	Typ. 10	
	27x27	256	2.5 to 10.6	0.4 to 1.9	0.2 to 0.5			20 to 29
		336						
		304						
	31x31	400	2.6 to 10.6	0.5 to 1.9	0.2 to 0.5			17 to 29
		480						
		352						
	35x35	420	1.7 to 11.8	0.3 to 2.3	0.1 to 0.7			16 to 24
		480						
		648						
	40x40	576	3.7 to 13.7	0.7 to 2.6	0.2 to 0.8			15 to 18
644								
768								
868								

θjc: Junction to case thermal resistance θja: Junction to local ambient thermal resistance
1. These values were calculated using simulation models.
2. These values are typical values and vary with die sizes, etc.
3. For information about packages not listed in the above table, contact your nearest Toshiba ASIC Design Center.

Lead Count Chart / ASIC Package Lines

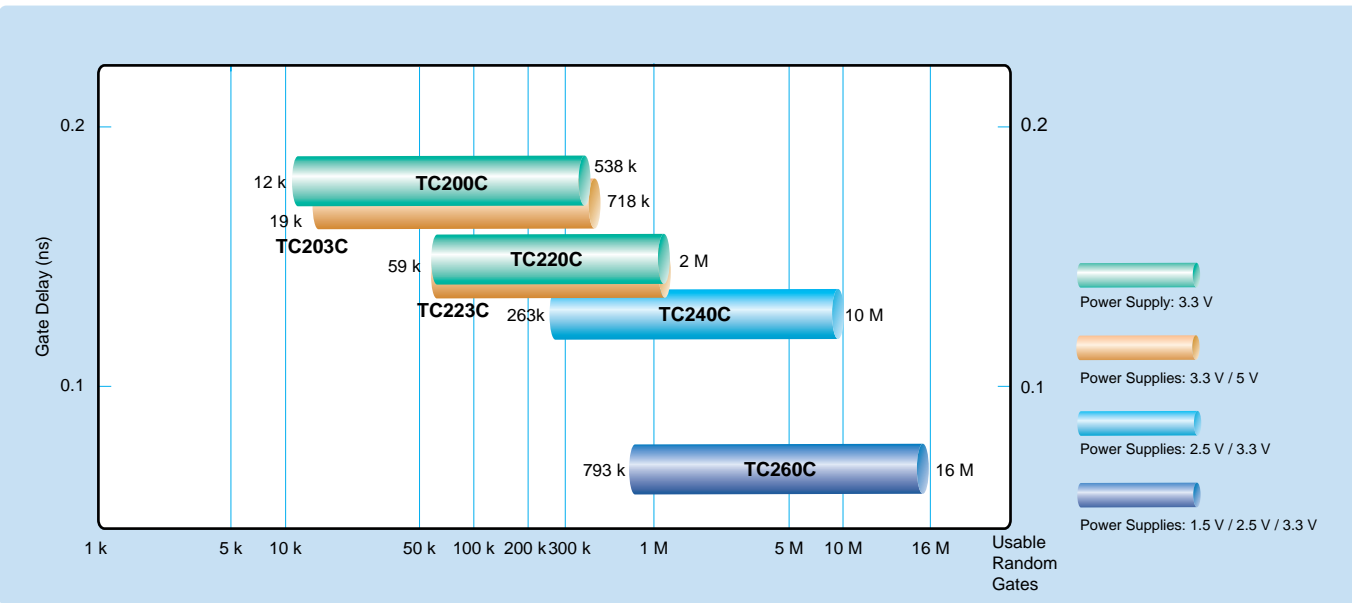
Package Type	Pin-Pitch	Number of Pins	100	200	300	400	500	600	700	800	900	1000	1500	2000		
TBGA	1.27 mm				256	304	352	420	480	576						
	1.0 mm					336		480	560	648	768	868				
PBGA	1.27/1.0mm			256	272	304	329	352	388	420	484	500	564	648(1.0)		
EBGA[4L]	1.27 mm					352				540						
PBGA[FC]	1.27 – 1.0 mm								625		841		1089	1444	1849	2304
PFBGA	0.8(0.65) mm		97	121	141	177	201	217	241(0.65)	265	337(0.65)	361				
PQFP	1.0mm	R64/RP64														
	0.8mm	44 60 R80/RP80 120/Pd120														
	0.65mm	R100/RP100 160/Cu160/Pd160 184														
	0.5mm	100 144 176 208/Cu208/Pd208 240 304														
HQFP	0.65 – 0.4 mm				160	184	208	240	296							
LQFP [Cu]	0.5 mm	48 64 80 100 144 176 208														
	0.4 mm			128	176	216	256									
	0.8 mm	44														
TQFP[Cu]	0.5 – 0.4 mm	80 100 120 128														

For further information, please contact your nearest Toshiba ASIC design center.

The cell-based technique assembles pre-designed and pre-optimized cells that users select, place, and interconnect on-chip to produce the required circuit functions with optimum chip size. These cells include basic gates, as well as various memory blocks, core functions, and analog cells. Because all of the mask set needs defining, the initial engineering charge is slightly higher than for a gate array for a given gate complexity. Also, the lead times to prototypes and production is longer than for a gate array. However, sized to fit individual design specifications, cell-based ICs leave little unused silicon area, thus giving generally lower chip cost. This makes cell-based ICs suitable for high-volume products.

Toshiba's cell-based IC libraries include many specialized functions such as RAMs, ROMs, FIFOs, multipliers, adders, subtractors, barrel shifters and CPU peripherals. In addition, a wide selection of system cores such as RISC processor cores and DRAM cores are available. Cell-based ICs also provide broad mixed signal support. Among analog cells available are A/D converters, D/A converters, analog PLLs (APLLs), etc.

Cell-Based IC Product Chart



Product		I/O: Mixed 2.5/3.3 V			I/O: Mixed 2.5/3.3 V	I/O: 3.3 V	I/O: 5 V	I/O: Mixed 3.3/5 V	I/O: 5 V	I/O: Mixed 3.3/5 V
		Core: 1.2 V / 1.0 V			Core: 2.5 V	Core: 3.3 V	Core: 5 V	Core: 3.3 V	Core: 5 V	Core: 3.3 V
		TC300C	TC280C	TC260C	TC240C	TC220C	TC200C	TC190C	TC223C	TC203C
Process		90 nm (Ldrawn = 65 nm)	0.13 μm (Ldrawn = 0.11 μm)	0.18 μm (Ldrawn = 0.14 μm)	0.25 μm	0.3 μm	0.4 μm	0.6 μm	0.3 μm	0.4 μm
Gate* Delay	Fanout = 1	12 ps @ High Speed lib	17ps@ High Speed Lib	35~43 ps	0.05 ns	0.06 ns	0.10 ns	0.10 ns	0.06 ns	0.10 ns
	Fanout = 2 + wiring	—	—	46~56 ps	0.07 ns	0.14 ns	0.17 ns	0.22 ns	0.14 ns	0.17 ns
Gates (Usable)		—	—	16 M	10 M	2.1 M	538 k	538 k	2.1 M	718 k
Gate Density		403 kG/mm ²	206 kG/mm ²	125 kG/mm ²	36 kG/mm ²	—	—	—	—	—
Pads	Wirebond	—	—	652	644	512	432	432	504	504
	TAB	—	—	1028	1568	1028	868	868	1028	1028
Power**	ND2 (fanout =1)	(CND2X1)0.007 μW	(CND2X1)0.014 μW	0.026 μW	0.17 μW	0.41 μW	0.91μW	1.74 μW	0.41 μW	0.91 μW
	ND2R (fanout =1)	—	(CND2XL) 0.010 μW	0.019 μW	0.11 μW	0.24 μW	0.48 μW	0.94 μW	0.24 μW	0.48 μW
Masterslice		Fabricated for each design	Fabricated for each design	120	40	40	39	39	40	38

* High-drive 2-input NAND gate, **μW/gate/MHz; ND2: 2-input NAND; ND2R: 2-input NAND, low-power type

Extended Temperature Range

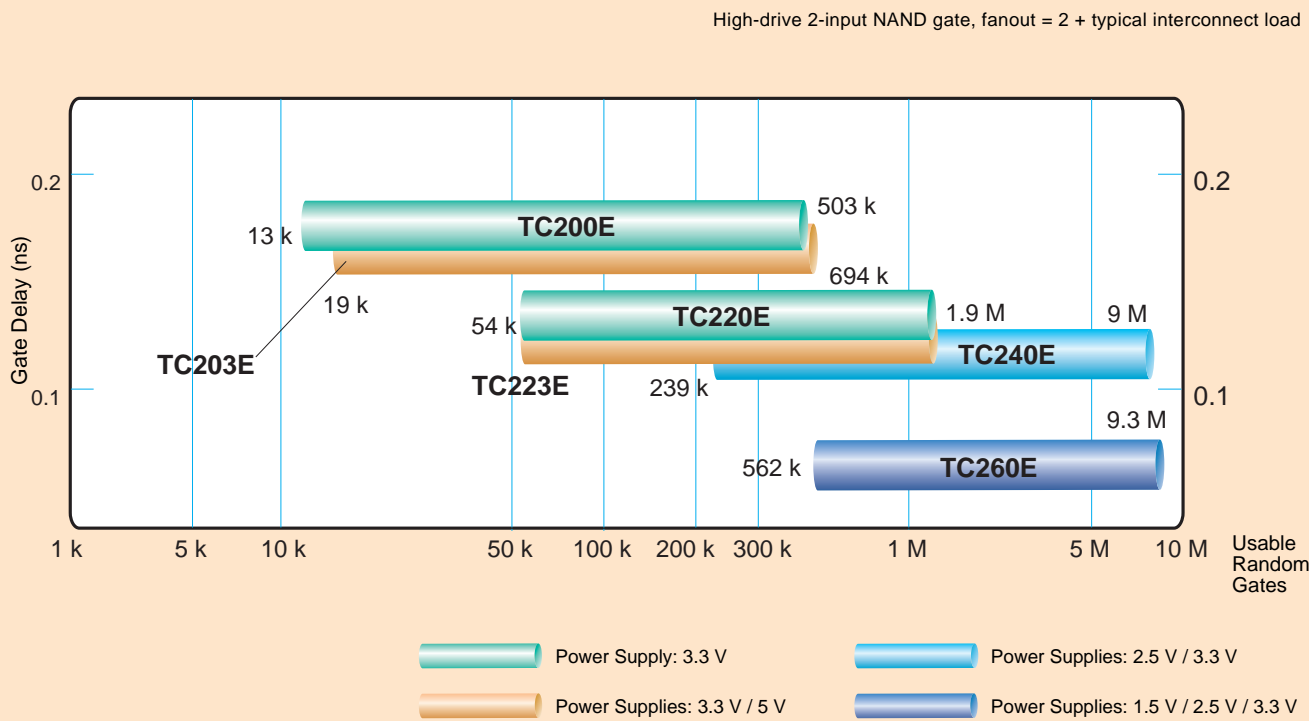
For support of an extended circuit's operating temperature range, contact your nearest Toshiba ASIC design center.

Toshiba ASIC Product Lines: Embedded Arrays

Embedded arrays combine high-performance functions of cell-based ICs with the gate array advantage of quick turnaround. They span the gap between gate arrays and cell-based ICs in terms of costs, performance, and prototype and production turnaround.

Embedded arrays use the same sea-of-gates technology as gate arrays, but allow designers to "embed" dense memory blocks and specialized functions in a gate array base by replacing part of its sea-of-gates core area with cell-based versions of the blocks.

Embedded Array Product Chart



Product	I/O: Mixed 2.5/3.3 V Core: 1.5 V		I/O: Mixed 2.5/3.3 V Core: 2.5 V		I/O: 3.3 V Core: 3.3 V		I/O: Mixed 3.3/5 V Core: 3.3 V	
	TC260E	TC240E	TC220E	TC200E	TC223E	TC203E		
Process	0.18 μm (Ldrawn=0.14 μm)		0.25 μm		0.3 μm		0.4 μm	
Delay*	Fanout = 1	0.05 ns	0.06 ns	0.07 ns	0.11 ns	0.07 ns	0.11 ns	
	Fanout = 2 + wiring	0.06 ns	0.08 ns	0.15 ns	0.19 ns	0.15 ns	0.19 ns	
Gates (Usable)	9.3 M		9 M		1.9 M		503 k	
Gates Density	65 kG/mm ²		32 kG/mm ²		—		—	
Pads	Wide Pitch	652	644	512	432	504	504	
	Narrow Pitch	1028	1568	1028	876	1028	1028	
Power**	0.036 μW		0.156 μW		0.65 μW		1.14 μW	
Masterslice	120		40		38		39	

* High-drive 2-input NAND gate, ** μW / gate / MHz, 2-input NAND, fanout = 1

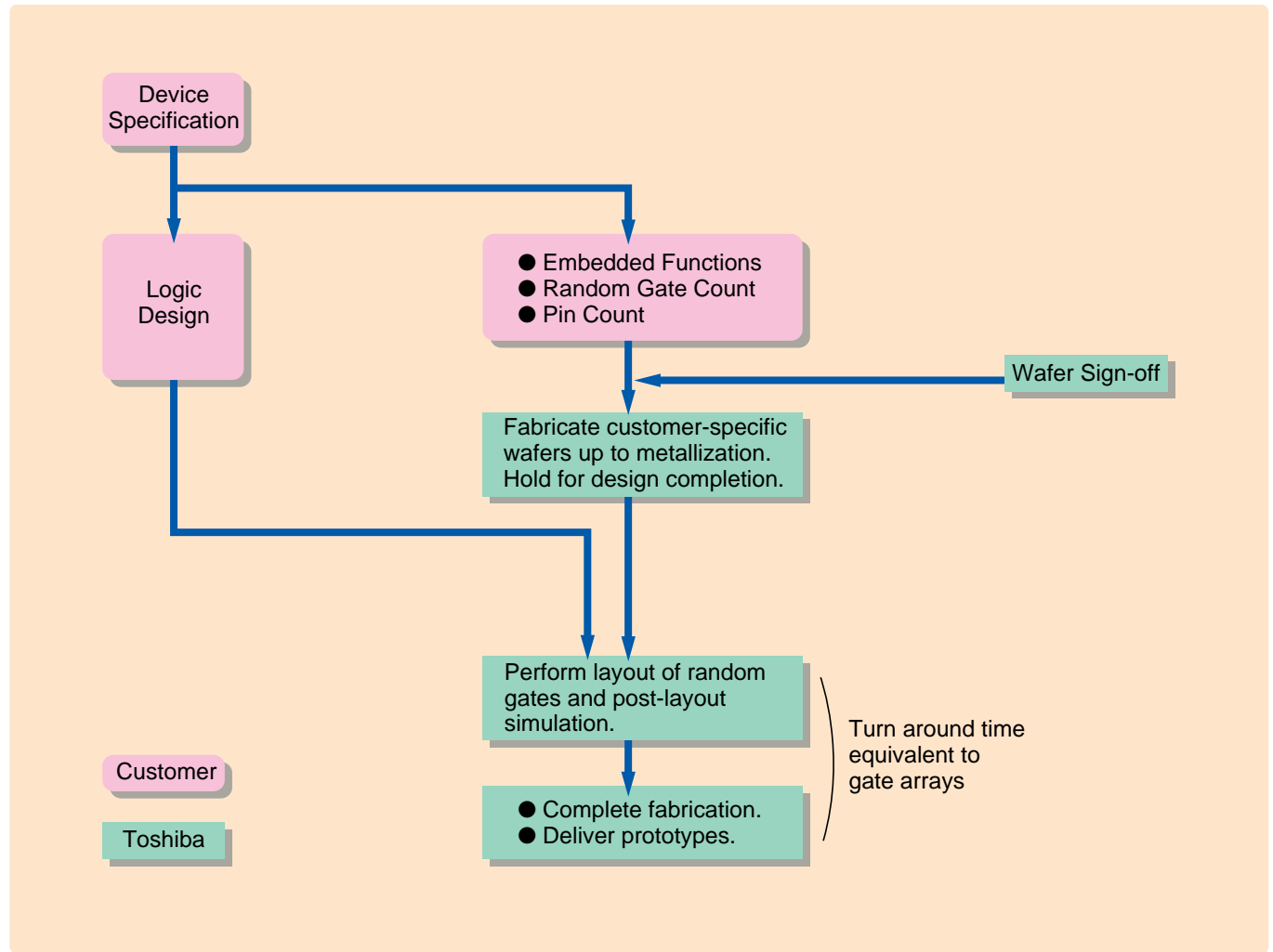
Extended Temperature Range

For support of an extended circuit's operating temperature range, contact your nearest Toshiba ASIC design center.

Embedded Array Design Flow

The figure below illustrates the embedded array design flow.

Early in the design cycle, the customer determines the appropriate area of logic gates, functions to be embedded, and the number of I/Os required. The customer then continues development work while Toshiba fabricates customer-specific base arrays (or master wafers). Once the customer completes the design, the layout of the gate array portion of the design is performed on the inventoried customer-specific master wafers. Post-layout simulation is then performed to verify that the design works to specifications. On customer approval of the design, prototype production can begin with the pre-defined master wafers already waiting at the metal mask step. Toshiba personalizes the master wafers by the use of up to six layers of metallization in much the same way as—and as quickly as—a gate array. As such, if any design re-spins are necessary, they can be produced with the gate array lead times.



Toshiba ASIC Product Lines: Gate Arrays

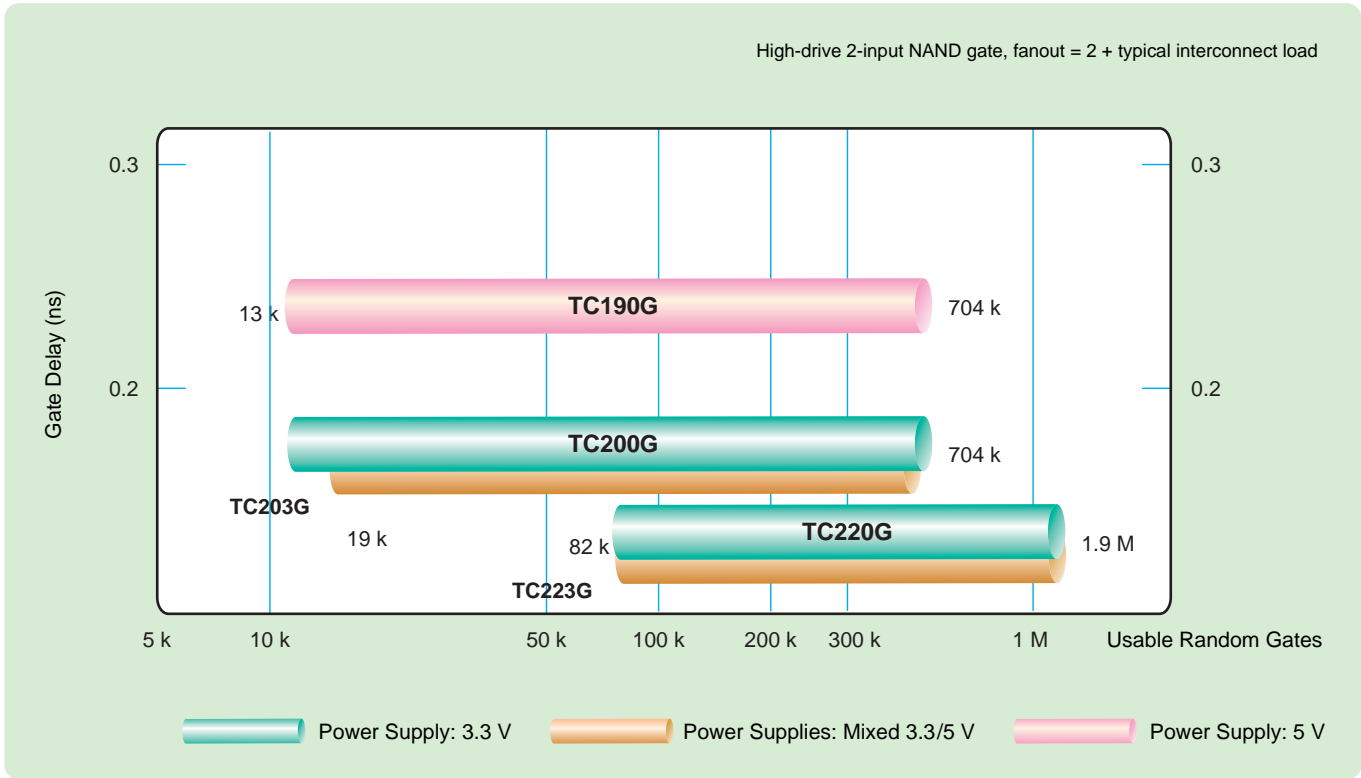
A gate array is a matrix of uncommitted, potentially active transistors whose interconnection is "programmed" at the metal wiring level.

Gate array wafers may be pre-fabricated in volume up to the final processing steps, thus achieving manufacturing economies of scale. These wafers are personalized at the metal wiring stage by applying a unique interconnection pattern that implements the customer's logic design.

Therefore, development cost is low and development time is short.

All of Toshiba's gate array products employ the sea-of-gates architecture. Computer software determines which transistors should be utilized for the circuit design and which transistors should be left unused so the area above can be used for signal routing. This placement and routing flexibility of sea-of-gates makes it possible to integrate large cells such as RAMs, ROMs, and multipliers on the same chip. Toshiba's gate arrays offer single gate array solutions for a wide variety of digital logic applications ranging in size from 300 to 1.9-M gates.

Gate Array Product Chart



Product		I/O: 3.3 V Core: 3.3 V		I/O: 5 V Core: 5 V	I/O: Mixed 3.3/5 V Core: 3.3 V	
		TC220G	TC200G	TC190G	TC223G	TC203G
Process		0.3 μm	0.4 μm	0.6 μm	0.3 μm	0.4 μm
Delay*	Fanout = 1	0.07 ns	0.11 ns	0.15 ns	0.07 ns	0.11 ns
	Fanout = 2 + wiring	0.15 ns	0.19 ns	0.24 ns	0.15 ns	0.19 ns
Gates (Usable)		1.9 M	704 k	704 k	1.9 M	694 k
Pads	Wirebond	512	512	512	504	504
	TAB	1028	1036	1036	1028	1028
Power**		0.65 μW	1.14 μW	2.46 μW	0.65 μW	1.14 μW
Masterslice		24	28	28	24	26

* High-drive 2-input NAND gate, **μW/gate/MHz, 2-input NAND, fanout=1

Extended Temperature Range

For support of an extended circuit's operating temperature range, contact your nearest Toshiba ASIC design center.

Toshiba ASIC Design Flow

Development Flow and Customer Interfacing

The Toshiba adaptable EDA design environment lets you work the way you like, using the EDA tools with which you are most comfortable. We do not believe you should have to change your design approach to take advantage of our silicon technology.

That is why we put the most powerful EDA tools in the industry at your command and support the third-party design tools you like best. Toshiba's "plug and design" concept balances a wide level of support for EDA tools and a broad ASIC product line to afford maximum flexibility in accommodating the designer's individual need.

When you "plug into" the Toshiba ASIC design environment, you immediately have access to multiple EDA tools, sign-off simulators, and design methodologies, as well as our advanced tools for compiling megacells, clock tree synthesis, power and simulation analysis, design-for-testability, and many other functions.

Our long-standing commitment to flexibility is also reflected in our approach to working with you. You can work with us as early or as late in the design process as you choose, at a wide variety of levels from schematics through physical design database.

The degree of customer involvement in the sequence of ASIC development is called customer interface.

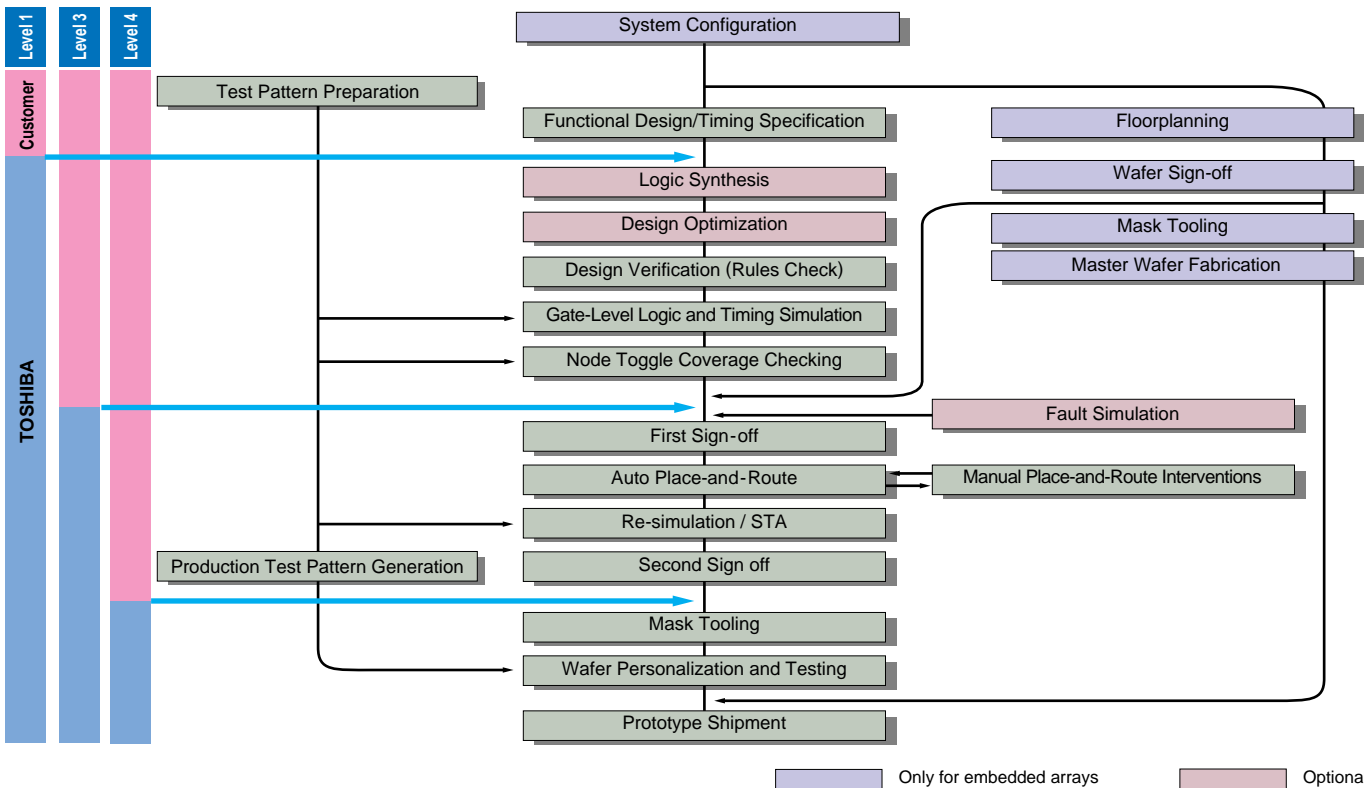
Toshiba offers three levels of customer interfacing in the design of ASICs, providing a flexible ratio of cost to customer involvement. While our interface levels are well defined, our interaction with you can be tailored to fit your unique needs. Thus, you can select your level of design participation to make best use of your in-house capabilities.

Level 1: You submit the verified RTL code to Toshiba for logic synthesis and gate-level simulation. Alternatively, you can provide Toshiba with gate-level netlists and test patterns.

Level 3: You perform pre-layout simulation using your own EDA tools.

Level 4: You perform all development work up to and including mask data generation. Toshiba only manufactures actual devices.

Toshiba's design kits support a whole host of EDA environments on multiple platforms. Tool support is tailored to fit the specific local needs. Please ask your nearest Toshiba ASIC Design Center for detailed information.



Toshiba ASIC Design Centers

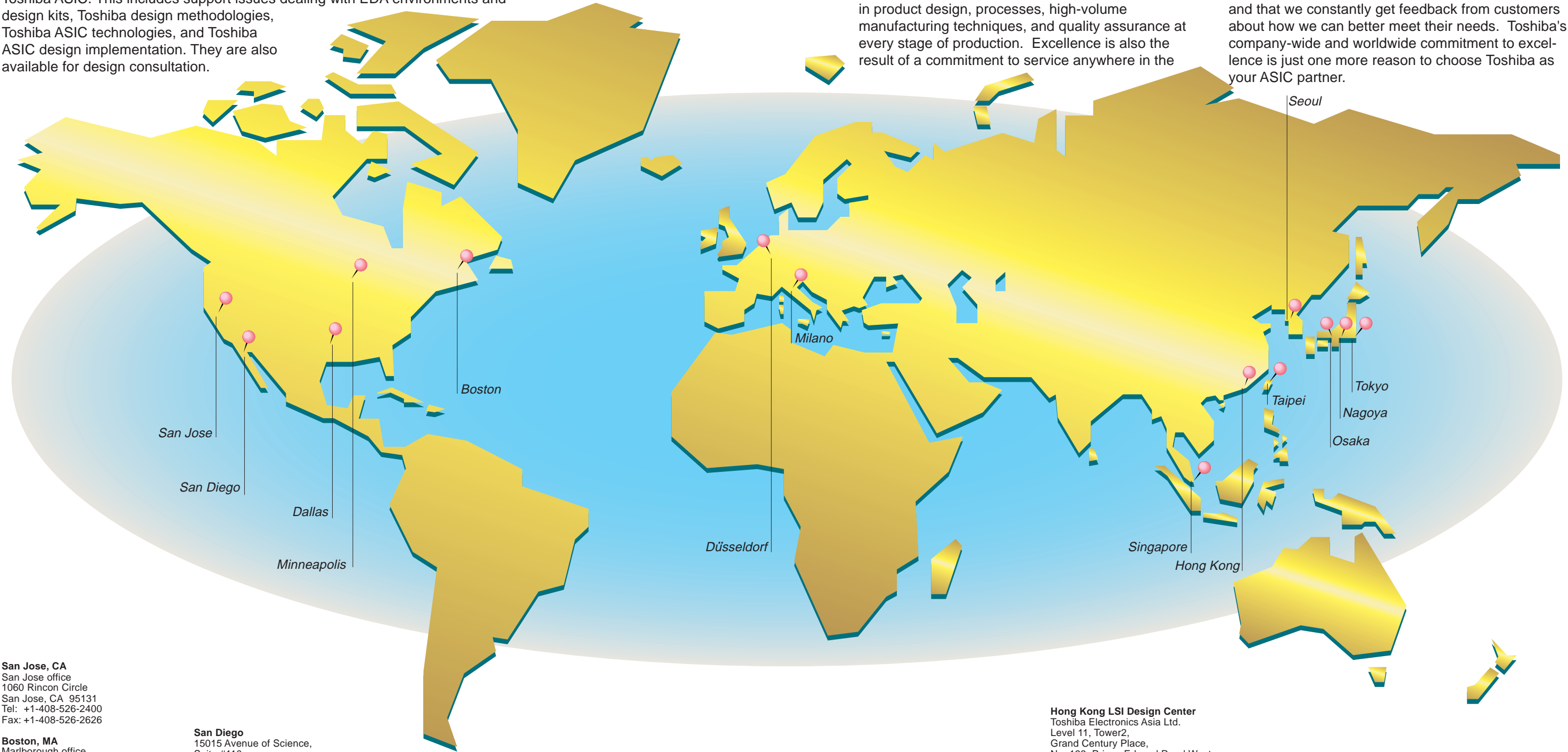
Design centers provide technical support and design expertise

Support and technical excellence are the areas that are given the highest priority at Toshiba. Toshiba ASIC Design Centers are located around the globe and provide a high level of technical expertise for support before, during, and after the design of a Toshiba ASIC. This includes support issues dealing with EDA environments and design kits, Toshiba design methodologies, Toshiba ASIC technologies, and Toshiba ASIC design implementation. They are also available for design consultation.

A worldwide commitment to excellence

Toshiba has built a reputation around the world for delivering high-performance, trouble-free products at competitive prices. This reputation is no accident. It stems from a corporate culture dedicated to excellence in product design, processes, high-volume manufacturing techniques, and quality assurance at every stage of production. Excellence is also the result of a commitment to service anywhere in the

world, before, during, and after the design. This not only means that Toshiba application engineers work with customers to develop the best and most cost-effective product for each individual application. It also means that products are delivered as specified and that we constantly get feedback from customers about how we can better meet their needs. Toshiba's company-wide and worldwide commitment to excellence is just one more reason to choose Toshiba as your ASIC partner.



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