International
IOR Rectifier

Application Note AN-990

Application Characterization of IGBTs

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This application note covers some of the major issues normally encountered in the design of an IGBT power conditioning circuit. It is the companion to INT-983, "IGBT Characteristics."

Application Characterization of IGBTs

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Topics Covered:

Gate drive for IGBTs
Safe Operating Area
Conduction losses
Statistical models
Switching losses
Device selection and optimization
Spreadsheets to calculate power losses and junction temperature
Thermal design
How to replace a power MOSFET
Paralleling
How to select devices for paralleling
Curve fitting methods to derive model parameters

SCOPE:

This application note covers some of the major issues normally encountered in the design of an IGBT power conditioning circuit. It is the companion to INT-983, "IGBT Characteristics," which covers the details of the device, rather than its application.

I. GATE DRIVE REQUIREMENTS

A . Impact of the impedance of the gate drive circuit on switching losses

The gate drive circuit controls directly the MOSFET channel of the IGBT and, through the drain current of the MOSFET, the base current of its bipolar portion. Since the turn-on characteristics of an IGBT are determined, to a large extent, by its MOSFET portion, the turn-on losses will be significantly affected by the gate drive impedance. Turn-off characteristics, on the other hand, are chiefly determined by the minority carrier recombination mechanism, which is only indirectly affected by the MOSFET turn-off. An increase in gate drive impedance prolongs the Miller effect and causes a delay in the current fall time that is similar to a storage time. This delay is emphasized in Figure 1 with the addition of a 47W gate resistor. The impact of the gate drive impedance on total switching losses depends on the basic design of the IGBT and its speed. The impact on *turn-on losses* is appreciable for all IGBTs from International Rectifier, regardless of speed. The impact on *turn-off* losses depends on the speed of the device: the faster the IGBT the greater its sensitivity to the gate drive impedance. In any event, *additional* gate drive impedance has a *marginal* impact, i.e. the same amount of additional drive impedance will have a lower effect if the gate drive impedance is already high.

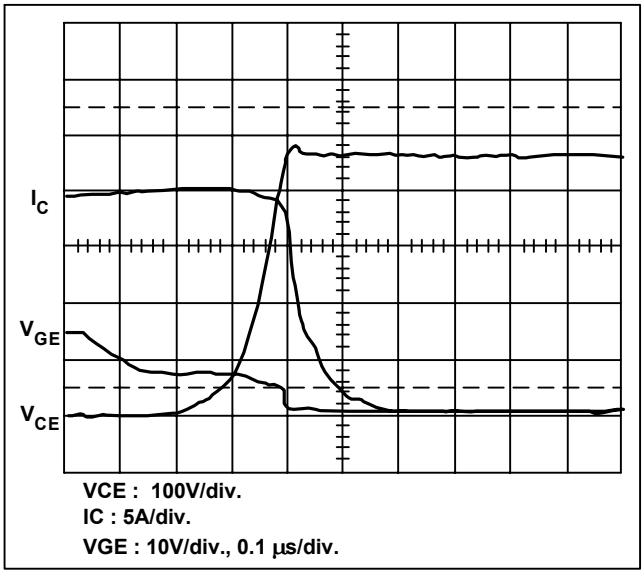


Figure 1. Turn-off waveform of an IRGBC40F with a 47W gate resistor. Notice the turn-off delay of the current waveform during the Miller effect.

It follows that the *total switching losses* of Fast IGBT will be less affected by the characteristics of the gate drive circuit than the Ultrafast IGBTs. These last ones are more sensitive to it and stand to benefit the most from a low impedance gate drive. The specific dependence of the switching energy on gate drive resistance is shown in the data sheet.

B. Impact of the gate drive impedance on noise sensitivity

As explained in INT-936, in a MOS Gated transistor, any dv/dt that appears on the collector/drain is coupled to the gate through a capacitive divider consisting of the Miller capacitance and the gate-to-source/emitter capacitance. If the gate is not solidly clamped to the source/emitter, a large enough dv/dt will take the gate voltage beyond its threshold and the transistor will conduct. As it goes into conduction it clamps the dv/dt that is causing it to conduct so that the gate voltage never goes much beyond its threshold. The end result is a limited amount of "shoot-through" current, with an increase in power dissipation. To reduce noise sensitivity and the risk of this dv/dt-induced turn-on, the gate must be shorted to the emitter through a very low impedance. Frequently a negative gate bias is used to improve noise immunity. An effective alternative is to design a layout that minimizes the inductance of the gate charge/discharge loops with parallel tracks or twisted wires for the gate drive.

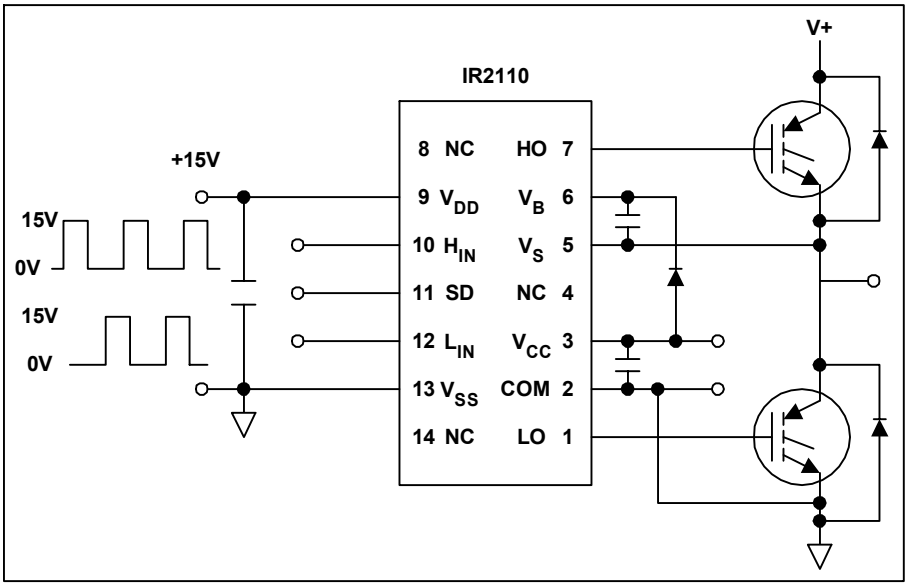


Figure 2. The IR2110 provides a simple, high performance, low cost solution to the problem of driving a Half-Bridge.

This can be as effective in taking care of this problem as the negative bias, eliminating the need for isolated negative supplies. In many cases the effects of a contained amount of dv/dt induced turn-on, i.e. a small increase in power dissipation, can be an appealing alternative to the added complexity of the negative gate bias.

C. Impact of gate drive impedance on "dynamic latching"

Some manufacturers suggest the use of significant amounts of gate resistance to reduce the possibility of "dynamic latch-up" (see INT-983, Section I.d), particularly when short circuit currents have to be switched off. This increases the switching energy and the sensitivity to dv/dt induced turn-on. Under these conditions a negative gate bias may be required.

Although IGBTs from International Rectifier will not latch even with no gate resistance, there may be practical reasons to add them, mainly to reduce the current spike at turn-on due to reverse recovery of the diode and reduce ringing.

This resistance can be safely bypassed with an anti-parallel diode to reduce the turn-off losses and the amount of dv/dt induced turn-on, as explained in INT-978, Section 3.b. For most applications, the circuit shown in Figure 2 provides a simple, low cost, high performance solution to the gate drive requirements of most applications.

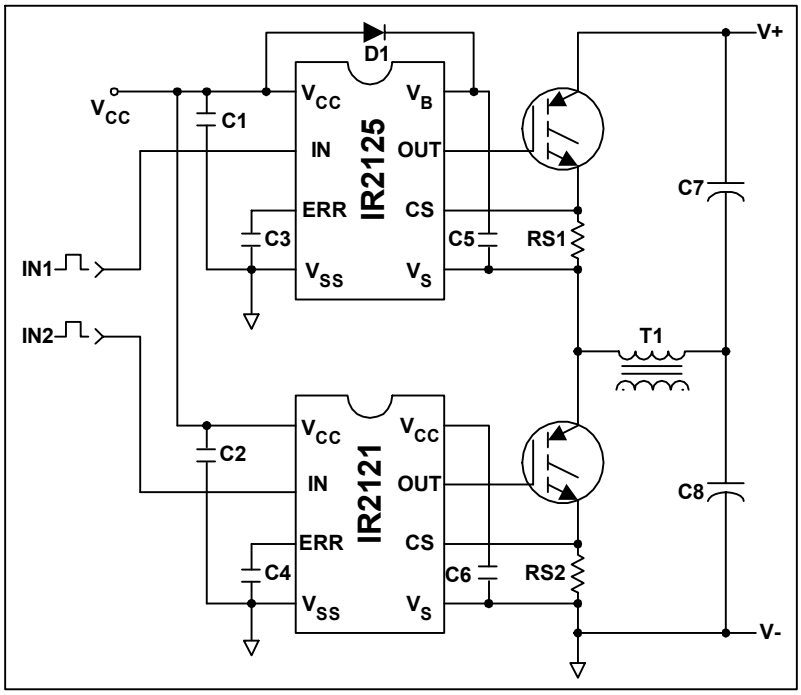


Figure 3. Short circuit protection performed with MOS gate driver ICs

D. Using gate voltage to improve short circuit capability

The gate terminal can be advantageously used to control the short-circuit withstand capability of the IGBT. A lower gate drive voltage reduces the collector current and the power dissipation during short circuit, at the expenses of a higher conduction drop. As an alternative, simple circuits can be implemented to reduce the gate voltage within 1-3 ms from the inception of the short circuit. INT-984 provides an example of how this function can be performed.

MOS-Gate Driver integrated circuits are available to perform the current limiting and short circuit protection function by means of the gate voltage. One such example is shown in Figure 3.

E. Contribution of "common emitter inductance" to the impedance of the gate drive circuit

The "common emitter inductance" is the inductance that is common to the collector circuit and the gate circuit (Figure 4a). This inductance establishes a feedback from the collector circuit to the gate circuit that is proportional to $L di_C/dt$. The voltage developed across this inductance subtracts from the applied gate voltage during the turn-on transient and adds to it during turn-off. In so doing, it slows down the switching.

This phenomenon is similar to the Miller effect, except that it is proportional to the di/dt of the collector current rather than the dv/dt of its voltage. In both cases the feedback is proportional to the transconductance of the IGBT, which is much larger than that of a MOSFET of the same die size. A di_C/dt of 0.5A/ns is quite common in IGBT circuits and voltages in the order of 10V could be expected in 20 nH of common emitter inductance, except that the feedback mechanism slows down the turn-on process and limits the dic/dt.

No additional common emitter inductance should be added to what is already in the package. Separate wires to the emitter pin should be provided for the emitter and the gate return, as shown in Figure 4b. The gate lead and the gate return lead should be twisted or run on parallel tracks to minimize inductance in the gate drive path. This improves immunity to dv/dt induced turn-on and reduces ringing in the gate.

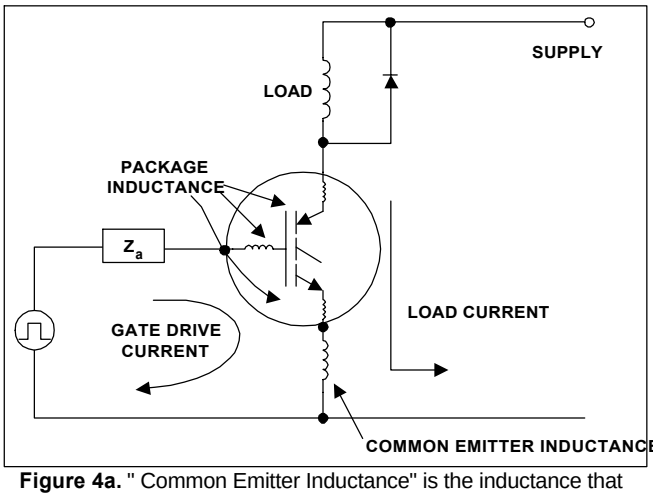


Figure 4a. " Common Emitter Inductance" is the inductance that is common to the collector current and the gate drive current

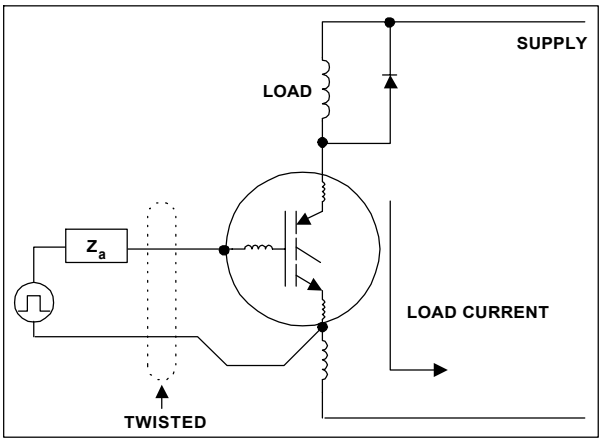


Figure 4b. " Common Emitter Inductance" can be eliminated by running separate wires to the emitter pin, one for the emitter, the other for the gate drive return.

F. Gate charge vs. input capacitance

The difference between gate capacitance and gate charge is covered in INT-944. Designers that are familiar with the limited usefulness of the input capacitance concept can safely skip this section.

Input capacitance is frequently used for two purposes:

- as a figure of merit of switching performance;
- as a reference point to design a gate drive circuit.

On both counts, the use of data sheet capacitance values gives results that are wrong or misleading.

As shown in Figure 5, IGBT capacitances change significantly with collector voltage to the point that no capacitance number is, in itself, meaningful unless a voltage is associated with it.

Even disregarding the voltage dependence, input capacitance is not a good figure of merit of switching performance, neither for MOSFETs, nor for IGBTs. As far as MOSFETs go, a device with lower input capacitance can be slower than one with higher input capacitance, depending on threshold, transconductance and total gate charge (see Figure 6 of INT-944). A conspicuous example of this is the fact that logic level devices are faster than their standard gate counterparts, in spite of a larger input capacitance [1].

In the specific case of IGBTs, which are minority carrier devices, the switching behavior is dominated by injection and recombination phenomena and only the turn-on behavior is affected by gate drive conditions in a significant way.

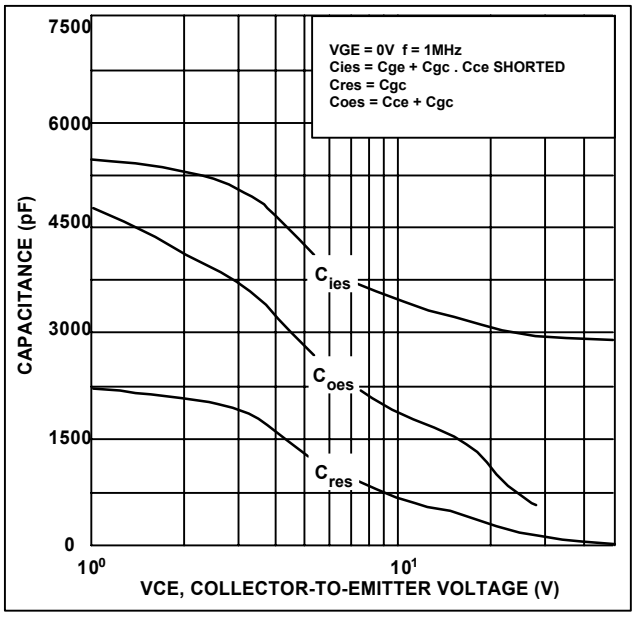


Figure 5. Typical capacitance vs VCE, IRGPC50U. The variation of Cres and Cies with collector voltage makes the concept of capacitance virtually useless.

As a guideline to design the gate drive circuit, the input capacitance underestimates the gate drive requirements. Normally, the charge required by the gate for one switching operation corresponds to an input capacitance that is two to three times larger than the data sheet value. As explained in INT-944, this is due to the Miller component of the input capacitance.

Thus, gate drive circuits designed on the basis of input capacitance are generally inadequate and result in poor switching operation and noise susceptibility. The sizing of the gate drive circuit is more appropriately done using the gate charge specified in the data sheet.

II. SWITCHING TRAJECTORIES AND SAFE OPERATING AREA CONSIDERATIONS

Minority carrier devices, when subjected to high levels of voltage and current, can experience uneven current distributions within the die that, taken beyond safe limits, can cause device failure. The current distribution takes different forms, depending on the sign of the di/dt associated with it. Hence, the Safe Operating Area curve, which was devised as a convenient representation of this limitation, is frequently differentiated into "Forward Biased SOA" and "Reverse-Biased SOA".

The Forward Biased SOA curve applies to linear operation in Class A or Class B or during short circuit, which can be considered an extreme case of Class B operation. Thermal limitations for pulsed operation are frequently included in this curve, even though the Transient Thermal Response curve provides this same information in a more comprehensive and accurate way. Due to the limited use of these devices in linear operation, the FBSOA curve has been omitted from the data sheet. The Reverse Biased SOA applies when switching off a clamped inductive load, including the turn-off from a short circuit condition.

Figure 6 shows the importance of the Reverse Biased SOA. During the turn off of a clamped inductive load, the voltage across the transistor goes from the low value of $V_{CE(sat)}$ to the full supply voltage while the collector current stays constant. After the collector voltage exceeds the supply voltage by a diode drop, the diode starts to conduct, thereby taking over the inductor current from the transistor. Thus the trajectory of the operating point moves along a constant current line until it intercepts the supply voltage, at which point a voltage overshoot normally occurs, whose magnitude depends on the amount of stray inductance L_S and the turn-off speed. A more detailed explanation of the switching trajectories can be found in Ref. [2].

It will be appreciated that, for a safe commutation of the load current, the entire trajectory must lay within the turn-off SOA and that any limitation to the SOA will translate into a limitation of turn-off capability of inductive loads. Load-shaping snubbers have been used in conjunction with bipolar transistors to lower the trajectory below the second breakdown limit.

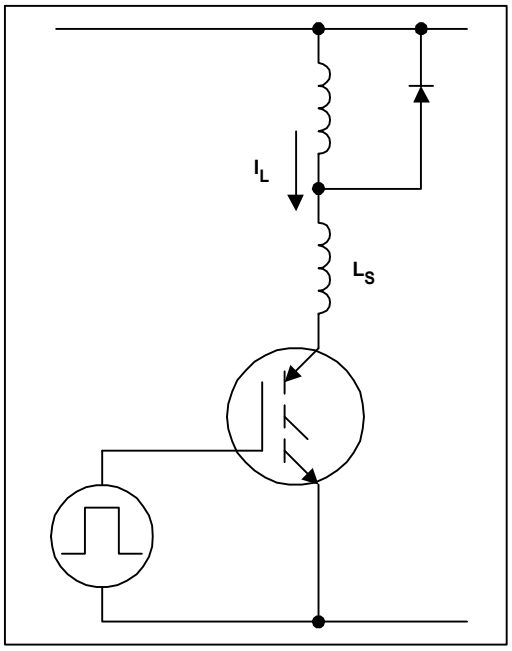


Figure 6a. Typical clamped inductive load

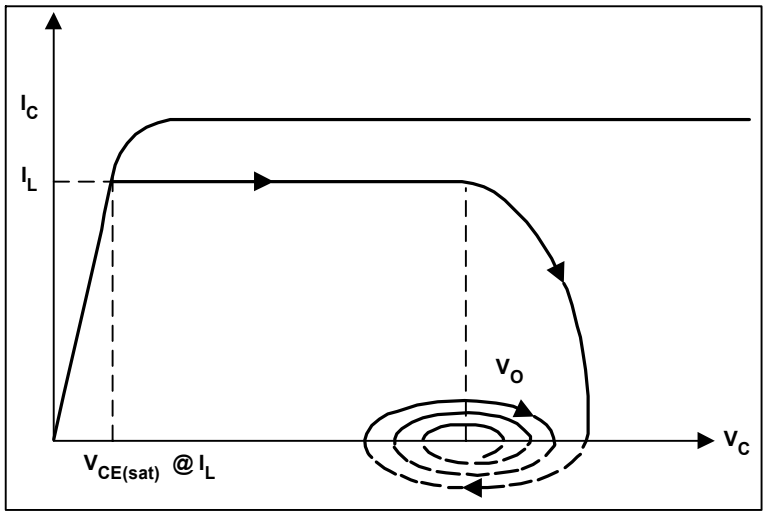


Figure 6b. During a turn-off transient, the trajectory of the operating point traverses the SOA curve. Second breakdown would place limits to the free evolution of the trajectory.

Due to the wide base and, hence, low gain of its bipolar portion, the second breakdown of International Rectifier's IGBTs occur at current and voltage levels that are significantly higher than what is normally encountered in a practical application, as shown in the data sheets. Notice that the values therein contained apply at 125°C and that load-shaping snubbers are not necessary, as long as the switching trajectory is confined within the turn-off SOA. During an inductive turn-off, a bipolar-mode device can undergo a partial loss of blocking capability, similar in many respects to second breakdown. This phenomenon is generally explained as being due to excessive concentration of minority carriers in the base region [3], rather than lateral thermal instability. For the IGBTs available from International Rectifier at the time of writing, this phenomenon occurs well beyond the SOA limits published in the data sheet. In addition to load shaping, snubbers can be used to limit overshoots and/or reduce EMI. This function is not related to SOA and is covered in more detail in INT-936.

III. CONDUCTION LOSSES

At any given time, the energy dissipated in the IGBT can be obtained with the following expression:

$$E = \int_0^t V_{CE}(i)i(t)\,dt$$

where t is the length of the pulse. Power is obtained by multiplying energy by frequency, if applicable. When the transistor is off i(t) » 0 and losses are negligible. Unfortunately, no simple expression can be found for the voltage and current functions during a switching transient. Hence, for analytical expediency, we resort to a somewhat artificial distinction between conduction and switching losses.

We define conduction losses the losses that occur between the end of the turn-on interval and the beginning of the turn-off interval, as defined for the switching losses characterization. Since the turn-on energy is measured from 5% of the test current to 5% of the test voltage and the turn-off energy is measured starting from 5% of the test voltage, conduction losses occur when the voltage across the IGBT is less than 5% of the test, or supply, voltage (see INT-983, Section 8.5). The function $V_{CE}(i)$ in the formula above expresses the conduction behavior of the IGBT. International Rectifier characterizes the conduction losses in the following ways:

- with tabular information in the data sheet;
- with graphs in the data sheet;
- with the model Parameters of INT-MODEL.

A. Calculating the voltage drop from data sheet parameters

The tabular information in the data sheet provides a few limit points that, with the help of the graphs, can be used to generate the information necessary to calculate the conduction losses. To obtain the max voltage drop at any current and temperature, from the data sheet supplied values, a two step procedure can be followed. First a typical value is obtained by interpolating a curve in Figure 5 of the data sheet at the desired current level. Then, to obtain a maximum value, the voltage drop read from this curve at the appropriate junction temperature is multiplied by the ratio between maximum and typical from the Table of Electrical Characteristics. If the current waveform is not constant during the conduction interval, it should be broken up into smaller intervals, calculating the losses for each sub-interval and summing the results, rather than averaging or taking its RMS value. An appealing alternative, for those cases where the current waveform has a simple mathematical expression, e.g. sinusoidal or triangular or trapezoidal, is to calculate the conduction losses with the integral above, with the help of the conduction model.

B. Conduction model

The solution of the integral requires a mathematical expression for the current waveform and one for the voltage drop. The expression shown below for the voltage drop as a function of current was found to be more than satisfactory for the general accuracy that is expected from these calculations.

$$V_{CB} = V_t + a\, I^b$$

Information on the accuracy of the model and how it was derived is contained in Appendix 1.
The specific parameters for the families of IGBTs from International Rectifier can be found in INT-MODEL. The purpose of this model, as well as the one presented in Section IV.B is to accurately predict the junction temperature of the IGBT in order to get the most out of the device. They differ from the common SPICE model in significant ways:

- they are representative of a population of devices, characterized by averages and sigmas, rather than an *undefined* "typical" device;
- they model electrical magnitudes that are time-independent, hence increments, and convergence are not an issue;
- temperature is an integral part of the model, not an after thought;
- the models are integrateable to calculate averages or losses in complex modulation schemes;
- the model is suited to provide aggregate values, like average power, average temperature, average peak reverse recovery.

These models do not provide information on the details of collector or gate waveforms. It should be kept in mind, however, that these waveforms are determined by circuit parasitics that cannot be modeled without breadboard characterization.

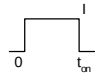
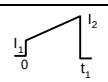
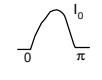
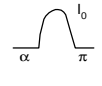
CURRENT WAVEFORM	MATHEMATICAL EXPRESSION	$E = \int V_{CE}(i)\, i(t)\, dt,\ V_{CE}(i) = V_t + a i^b \quad E = \int \left[V_t i(t) + a i(t)^{(b+1)} \right] dt$
	$i(t) = I$	$E = \int_0^{t_{on}} \left(IV_t + aI^{(b+1)} \right) dt = \left(IV_t + aI^{(b+1)} \right) t_{on}$
	$i(t) = I_1 + (I_2 - I_1)\frac{t}{t_1}$	$E = \int_0^{t_1} \left[V_T \left(I_1 + \frac{(I_2 - I_1)}{t_1} \right) + a \left(I_1 + \frac{(I_2 - I_1)}{t_1} t \right)^{(b+1)} \right] dt = V_t \frac{(I_2 + I_1)}{2} t_1 + \frac{I_2^{(b+2)} - I_1^{(b+2)}}{(I_2 - I_1)} \frac{at_1}{b+2}$
	$i(t) = I \frac{t}{t_1}$	$E = \int_0^{t_1} \left(V_t I_0 \sin \omega t + a I_0^{(b+1)} \sin^{(b+1)} \omega t \right) dt = \frac{2I_0}{\omega} \left[V_t + \frac{\sqrt{\pi}}{2} a I_0^b \frac{\Gamma\left(\frac{b+2}{2}\right)}{\Gamma\left(\frac{b+3}{2}\right)} \right]$
	$i(t) = I_0 \sin \omega t$	$E = \int_0^{t_1} \left(V_t I_0 \sin \omega t + a I_0^{(b+1)} \sin^{(b+1)} \omega t \right) dt = \frac{2I_0}{\omega} \left[V_t + \frac{\sqrt{\pi}}{2} a I_0^b \frac{\Gamma\left(\frac{b+2}{2}\right)}{\Gamma\left(\frac{b+3}{2}\right)} \right]$
	$i(t) = I_0 \sin \omega t$	for $\alpha \frac{\pi}{2}$ $E = \frac{I_0}{\omega} \left[V_t + \frac{\sqrt{\pi}}{2} a I_0^b \frac{\Gamma\left(\frac{b+2}{2}\right)}{\Gamma\left(\frac{b+3}{2}\right)} \right]$ otherwise $E = \frac{I_0}{\omega} \left[V_t (1 + \cos \alpha) + a I_0^b \int_\alpha^\pi \sin^{(b+1)} \alpha\, d\alpha \right]$

Table I. Conduction Energy for Simple Waveforms

Table I shows the expressions to calculate conduction energy for five simple current waveforms, assuming that the conduction behavior is accurately expressed by the model presented.

As shown in Sections V and VI, this model, as well as the companion switching model that will be described in the next Section, is extremely useful in performing comparative evaluations for device optimization. Section VI shows how it can be used to simplify and automate the calculation of junction temperature for any operating condition.

IV. LOSSES IN HARD SWITCHING

Like conduction losses, "hard switching" operation is characterized in the following ways:

- with tabular information in the data sheet;
- with graphs in the data sheet;
- with the model parameters of Table INT-MODEL.

As explained in INT-983, Section 8.5, the Switching Energy reported in the data sheet makes specific reference to a test circuit that simulates a clamped inductive load operated with an ideal diode. Hence, it does not include the losses in the IGBT when, in turning on, it carries the full load current, plus the reverse recovery current of the freewheeling diode.

It follows that, to obtain the total turn-on losses or the total switching losses, two components have to be calculated:

- turn-on or total losses with an ideal diode
- the additional turn-on losses in the IGBT due to the reverse recovery of the freewheeling diode.

The following sections show how to calculate these two components. It should be kept in mind that active devices in flyback converters do not normally have turn-on losses, nor are they subject to recovery transients. The same is true for those bridge circuits where the output voltage and duty cycle is controlled by phase shifting the output of one leg with respect to the other, both being 50% duty cycle.

A. Calculation of switching losses with an ideal diode from data sheet information

Total switching losses with an ideal diode for any given current and temperature can be obtained from data sheet information following a three step procedure, similar to the one for obtaining the on-state voltage drop.

First a typical value is obtained, by interpolating a curve in Figure 10 of the data sheet for the desired current. From this typical value a maximum value can be obtained by multiplying the typical by the ratio between maximum and typical that is in the Table of Switching Characteristics.

Finally, since the switching energy is proportional to voltage, the result is scaled by the ratio of the actual circuit voltage to the test voltage (normally 80% of device rated voltage).

An additional correction may be necessary to account for the gate resistor. This can be done with the help of Figure 9 of the data sheet.

B. Calculation of switching losses with an ideal diode from switching model

A simpler alternative to the method outlined below is to make use of the simple model shown in Table III, together with the specific parameters for the three families of IGBTs from International Rectifier. Losses calculated with these parameters assume the following:

- supply voltages equal to 80% of rated $V_{(BR)CES}$.
- a gate drive circuit similar to the one in the data sheet.
- ideal diode.

The results should be scaled linearly for the appropriate supply voltage and should be scaled according to Figure 9 of the data sheet to take into account a different gate drive impedance.

C. Contribution of the diode reverse recovery

In a typical clamped inductive load in continuous current mode, the turn-on of a switch causes a reverse recovery in the freewheeling diode and a large current spike in the device that is being turned on (Figure 7). This increases the turn-on losses in the IGBT with respect to the calculations of the previous sections and data sheet characterization. The *forward recovery* of the diode, on the other hand, has a secondary impact on the turn-off losses and will not be analyzed here.

No simple expression can be provided for these additional losses, as they depend on a number of factors: turn-on speed di/dt, stray inductance and diode characteristics. Several have been proposed, based on simplifying assumptions. The following assumes that the voltage across the diode stays close to 0V during the length of t_a, rising to the supply voltage during t_b.

$$E = VI_L[(1+\frac{1}{2}\frac{I_{rr}}{I_L})t_a + \frac{1}{4}\frac{I_{rr}}{I_L}t_b]$$

$$= V(I_L t_a + Q_a + \frac{1}{2}Q_b)$$

where V and I_L are supply voltage and load current, I_{rr} is the peak reverse recovery current, t_a and t_b are the two components of t_{rr} and Q_a and Q_b the charges associated with them. The first two terms represent the losses during t_a, one due to the load current, the other due to the reverse recovery current. The third term represents the losses during t_b, which are partly in the IGBT, partly in the diode.

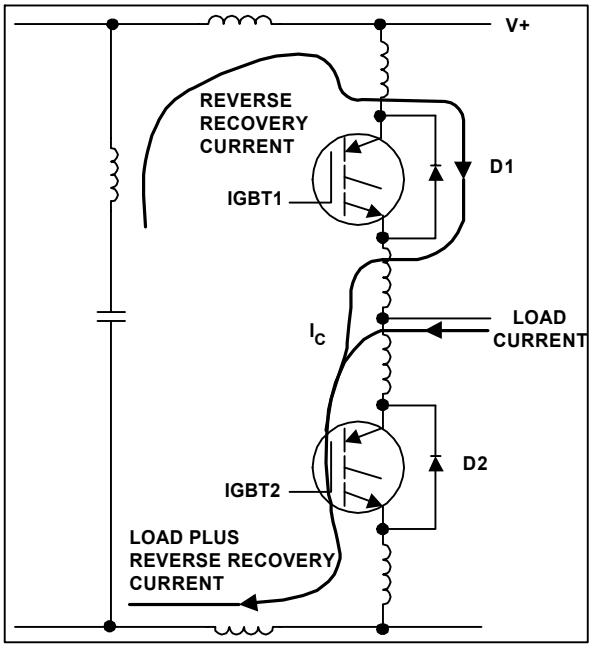


Figure 7a. Typical clamped inductive load showing stray circuit inductances. Load current was flowing in D1 previous to IGBT2 turning on. At turn-on IGBT2 takes over load current and reverse recovery current of D1

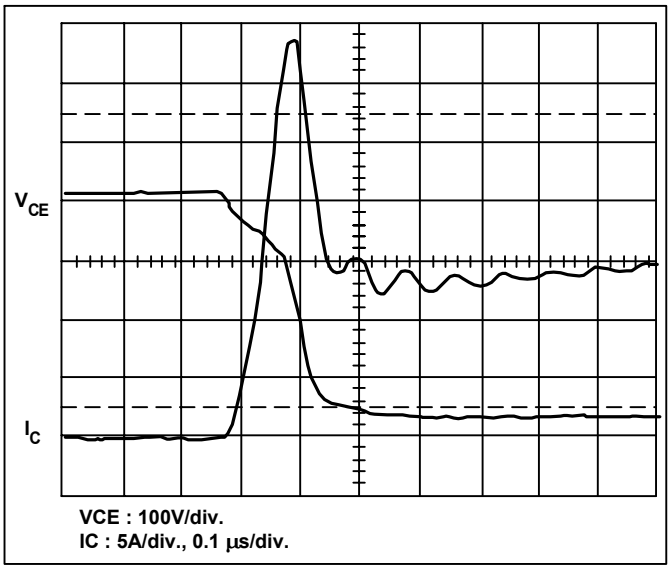


Figure 7b. Turn-on current in IGBT2.

V. TRADE-OFF BETWEEN CONDUCTION AND SWITCHING LOSSES: DEVICE OPTIMIZATION

To compare different devices or technologies, silicon designers often resort to curves of voltage drop vs. current density like those shown in Figure 8. These curves ignore the dynamic behavior of the device and, since in a typical Switchmode application a significant portion of the temperature rise is due to the switching losses, they are not useful in the device selection.

Furthermore, it is frequently inferred, from those curves, that a technology is superior if it is capable of operating at higher current densities. In a specific application, operation at higher current densities means smaller die sizes and, consequently, higher thermal resistances. If total losses stay the same, this implies higher operating junction temperature, with all its negative connotations.

It follows that, for a given thermal design, operation at higher current densities will be advantageous only if the higher thermal resistance is compensated by lower total losses.

To quantify these considerations a simple method has been developed comparing different power devices in a typical Switchmode environment. This method takes all critical aspects into account: thermal constraints, conduction and switching losses.

The popular half-bridge operated with a clamped inductive load was chosen as the benchmark circuit to compare the Performance of different IGBTs. Operating conditions are listed in Figure 9. None of the operating conditions are critical and they can all be changed as necessary. Flyback or resonant circuits could be used in place of the half-bridge to obtain results that are specifically tailored to a given application.

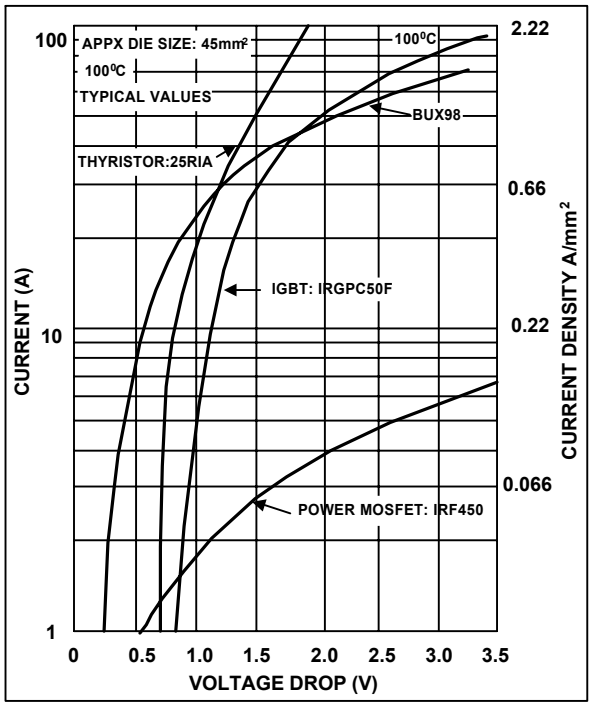


Figure 8. Conduction characteristics for devices of similar die size implemented in different technologies.

This figure shows in a clear and concise way to what extent higher switching frequencies impact the current output of the pair.

It also provides a simple way of selecting the optimum device for the application, which is the one that gives the highest output current at the frequency of Operation.

Once the thermal constraints are properly factored into the operating conditions, the graph carries important application information. In a motor control, the RMS component of the fundamental is directly related to torque.

In a power supply, on the other hand, the total RMS content of the square wave contributes to power. The ratio between the two is 1.11. Although the graph shown in Figure 9 can be generated with a relatively simple test circuit, we have made use of the model presented in the previous sections and of a spreadsheet like the one shown in Figure 10. Starting from the top, the IGBT model parameters are entered first, as appropriate for the junction temperature at which the performance is being evaluated.

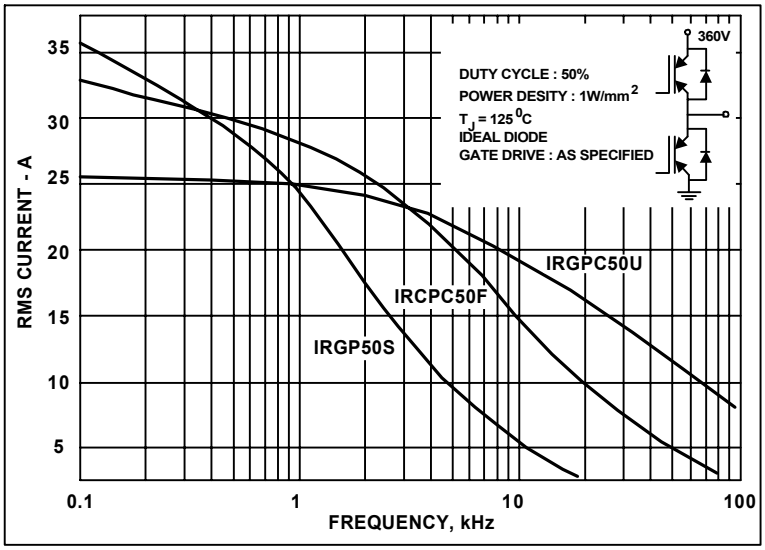


Figure 9. RMS current vs. frequency for a Half Bridge with two IGBTs of same die size, same package, different speed, operated in the conditions indicated in the inset.

Next the diode model is entered, which will be used to calculate the component of turn-on losses in the IGBT due to the reverse recovery of the diode. The conduction model for the diode can also be entered for completeness and to calculate its conduction losses. This will not affect the losses in the IGBT but could provide useful information related to the total losses, efficiency, etc.

The reference voltage for the switching loss model (normally 80% of device rated voltage) is entered next, followed by the actual operating voltage that, for a rectified 220V line, would be approximately 360V. Finally the thermal information is entered in the form of thermal resistance and ambient temperature, from which the allowable Power dissipation is calculated.

The value "Current for balanced losses" is the current at which the conduction losses equal the switching losses for the specific thermal operating conditions. The corresponding frequency is shown at the bottom of the first column under "frequency, ideal diode". These values are calculated by means of a "solve for" function in the spreadsheet and are accurate to the number indicated on the right of the current value. The rest of the spreadsheet performs the calculations of losses for different levels of current. Losses are broken down into two classes: conduction and switching. The formulas in the spreadsheet are described in the next Section. All the losses are summarized at the bottom.

These values are used to generate the Current vs Frequency graph that is reported in each data sheet as Figure 1. If the diode is co-packaged with the IGBT its losses cannot be dissociated from the losses in the main switching device. In this case the thermal information and allowable power dissipation should be for the combination of both devices. Losses should include conduction and switching losses of both devices and the formulas should be modified accordingly.

Part Number:

IGBT MODEL Tj = 125

Conduction model:	Vt = 0.86	a = 0.1834	b = 0.6999
Turn-on model, ideal diode		h = 0.0028	k = 1.6741
Turn-off model:		m = 0.018	n = 1.2486

DIODE MODEL Tj = 125

Conduction model:	Vt = 1.00	a = 0.040	b = 1.000
Switching model:	Peak Irr/If = 1.00	ta = 0.035	tb = 0.030µs

Switching parameters at	480 V
Operating voltage:	360 V
Thermal resistance j-c	0.77 K/W
Thermal resistance c-s	0.24 K/W
Thermal resistance s-a	1.5 K/W
Allowable power dissipation	27.89 ^Ta = 55
Current for balanced losses	13.85 1E-05

Peak Current	**A**	**13.85**	**8**	**10**	**15**	**17.5**	**19.5**
CONDUCTION							
Voltage drop	V	2.01	1.65	1.78	2.08	2.22	2.33
Losses (50% duty cycle)	W	13.94	6.58	8.89	15.6	19.42	22.68
SWITCHING LOSSES							
Turn-on, ideal diode	mJ	0.1685	0.0673	0.0977	0.1927	0.2494	0.299
IGBT losses due to diode	mJ	0.2991	0.1728	0.216	0.324	0.378	0.4212
Turn-off losses	mJ	0.3595	0.1812	0.2394	0.3972	0.4815	0.5512
Diode, switching losses	mJ	0.0374	0.0216	0.027	0.405	0.0473	0.0527
SUMMARY:							
Conduction losses	W	13.94	6.58	8.89	15.6	19.42	22.68
Sw. losses, ideal diode	mJ	0.53	0.25	0.34	0.59	0.73	0.85
Pole RMS Current (fund.)	A	12.46	7.200	9.000	13.5	15.75	17.55
Frequency, ideal diode	kHz	26.41	85.74	56.33	20.82	11.58	6.12
Sw. losses, real diode	mJ	0.83	0.42	0.55	0.91	1.11	1.27
Frequency, real diode	kHz	16.86	50.57	34.34	13.44	7.64	4.09

Figure 10. Spreadsheet to calculate Output current vs. Frequency

Part Number: IRGPC50U

THERMAL OPERATING CONDITIONS

Ambient temperature	°C	60.0
Thermal resistance j-to-c	°C/W	0.640
Thermal resistance c-to-s	°C/W	0.240
Thermal resistance s-to-a	°C/W	1.400

		Allowable current at stated Tj		Junction Temperature for state current	
Power dissipation	W	28.5		29.16	
Junction temperature	°C	125	*	126.50	

IGBT MODEL

Vt, Vt1, Vt2	V	0.8000		0.7958	1.0994	-2.40E-03
a, a1, a2	Ohm	0.1120		0.1136	0.2021	-7.00E-04
b, b1, b2		0.7117		0.7085	0.4656	1.92E-03
h, h1, h2	mJ/A	0.0038		0.0037	0.0045	-6.10E-06
k, k1, k2		1.6376		1.6399	1.6162	1.87E-04
m, m1, m2	mJ/A	0.0128		0.0155	-0.0114	2.13E-04
n, n1, n2		1.3382		1.336	1.9457	-4.82E-03
Reference Voltage	V	480		480		

DIODE MODEL

Vt		0.8		0.8	
a, b		0.04	1	0.04	1
Ratio Irr/If		1		1	
ta, tb	µS	0.04	0.03	0.04	

ELECTRICAL OPERATING CONDITIONS **RECT. WAVEFRM, CLAMPED IND. LOAD**

Switching voltage	V	360	360
Operating frequency	kHz	40	40
Duty cycle		0.45	0.45
Peak current	A	9.82	9.82
Voltage drop at peak current	V	1.37	1.37
Conduction losses	W	6.05	6.05
Turn-on losses	W	4.76	4.76
Correction factor for gate resistance		1.00	1.00
Corrected turn-on losses	W	4.76	4.76
Turn-off losses	W	8.14	9.87
Correction factor for gate resistance	W	1.00	1.00
Corrected turn-off losses		8.14	9.87
Turn-on losses due to diode recovery	W	9.55	8.48
Total losses	W	28.50	29.16
Junction temperature	°C		126.49

RMS current, fundamental	A	8.84	15.6
RMS current, total	A	9.82	9.82
Output voltage, RMS funda mental	V	162.000	162.00
Output power, fundamental	kVA	1.59	1.59
Output power, total	kVA	1.77	1.77

* Data entered

Figure 11. Analysis of the operating conditions of an IGBT in a clamped inductive load.

VI. THE ANALYSIS: METHODS TO CALCULATE JUNCTION TEMPERATURE AND POWER DISSIPATION FOR A GIVEN OPERATING CONDITION.

In the previous section we have developed an application related tool to compare the performance of different devices over temperature and frequency. In this section we present a different tool, aimed at analyzing the operating conditions of the power devices, particularly its junction temperature, *in a specific application environment.*

Since temperature affects conduction and switching losses which, in turn, affect temperature, a direct mathematical solution is not possible. However, the models introduced in Sections III and IV, applied iteratively, permit the characterization of a given operating condition with relative ease.

Figure 11 shows an example of such a spreadsheet. It provides junction temperature for a given a value of load current and a given operating environment. It also provides a comprehensive analysis of the losses and temperatures in the thermal system.

This spreadsheet is quite general and applicable to any Switchmode conditioner. It is customized to our application, by entering in the appropriate cells the expressions for power losses that characterize its operation.

In this example they represent a clamped inductive load, typically a Buck converter of Dual Forward. Equivalent spreadsheets for motor drives and UPS would look similar, while containing different formulas to reflect a different relationship between voltage, current, modulation and output power.

A spreadsheet has several advantages over other circuit analysis software:

- can be easily customized for specific applications without special programming expertise;
- all the operating conditions that are important to the designer are summarized in less than half a page;
- energy, power, peak and average currents and voltages are calculated and displayed, as opposed to waveforms on nanosecond scales;
- it is guaranteed to converge and provides a result in a fraction of a second
- it allows true real-time interactive design: the impact of a change in voltage or current or frequency or heatsink is assessed in a fraction of a second without printing stacks of waveforms.

The spreadsheet is divided in the three sections described below.

Input, output and gate drive conditions

All the parameters marked with an "X", like supply voltage, frequency, duty cycle, line current and turn-on gate resistor, should be entered, the others are calculated from the data supplied. Within reasonable limits, the gate resistor at turn-off is not as important, as the turn-off mechanism of an IGBT is mostly dictated by minority carrier recombination

Thermal operating conditions

Ambient temperature and thermal resistances must be entered. Junction temperature is calculated from the losses listed in the last box of the spreadsheet. Junction temperature is used to calculate the device parameters which, in turn, are used to calculate the losses.

This is the fundamental iteration process that yields the operating junction temperature.
The thermal calculations would be somewhat different, depending on whether the inverter is implemented with discrete devices, co-packaged IGBT-diodes or modules.

Fig. 11 applies to discrete devices sharing the same heatsink with additional heat sources. The junction temperature is calculated for IGBTs and diodes.

For power modules this box would be modified to take into consideration the fact that the IGBTs and diodes contribute both to raise the base temperature of the module. Except for the modules which are already isolated, discrete and co-packaged devices are assumed to be isolated from the heatsink. The thermal resistance of the insulating interface is entered in this box.

IGBT and diode model parameters

The third box contains the IGBT model parameters for the specific device, as explained in Section III.B, IV.B and XI. These parameters are used to calculate the voltage drop and switching energy as a function of current *at the specific temperature* indicated in the previous box. They are automatically fetched from a table that is part of the spreadsheet but not shown in Fig. 11.

The diode conduction model is shown in the right-hand side of this box. Recovery parameters are calculated here from the turn-on di/dt of the IGBT which is, in turn, a function of the turn-on gate resistor entered in the first box. The recovery parameters are important to calculate the turn-on losses of the IGBT and the switching losses of the diode.

Power losses

The fourth box lists the components of power losses and junction temperature for one IGBT and the freewheeling diode.

Although the most important information provided by the spreadsheet is the operating junction temperature of the IGBT and of the diode, the additional information provided in the last box is also very useful in optimizing the choice of the power devices. The following observations can be used as examples:

♦ If the switching losses are much larger than the conduction losses, a faster IGBT is desirable. If none is available, it may be advisable to lower the junction temperature to avoid the risk of thermal run-away due to the fact that turn-off losses increase significantly with temperature. This can be done by improving the thermal system, e.g. by increasing the size of the heatsink or isolating the heatsink rather than the IGBT.

The risk of thermal runaway can be easily checked with the help of the spreadsheets by increasing ambient temperature by a few degrees. If junction temperature increases by more than the increase in ambient temperature, there is cause for concern.

♦ If, on the other hand, conduction losses are the dominant component, a slower device may reduce the overall losses and operate at a lower junction temperature.

♦ If a large share of the IGBT losses are due to the diode recovery, a faster diode should be used or faster turn-on of the IGBT. This increases the turn-on spike, but reduces the turn-on losses.

♦ In a well balanced thermal design the case temperature of the active devices is between one-half and three-fourths the temperature rise between ambient and junction. If it lower than that, the heatsink could be reduced. If it is higher, it may be too small.

♦ When a suitable device cannot be found, designers frequently turn to paralleling, a method that has proven quite successful with power MOSFETs. It is somewhat less successful with IGBTs because their dominant losses are switching and switching losses do not decrease with paralleling. They may, in fact, increase, if the gate drive is not adequate. The generally negative temperature coefficient of the conduction drop complicates the task of paralleling, as indicated in Section IX and X. The main advantage in paralleling IGBTs is in the reduction of the thermal resistance between junction and sink, hence junction temperature and turn-off losses.

This spreadsheet allows convenient analysis of the same circuit in different operating points, e.g. under stresses of transitory nature, like shorts in the output, where the junction temperature could be allowed to go to, say, 150°C. In this case the duty cycle would probably be lower and peak current higher.

The spreadsheet contains several formulas, most of them requiring no explanation. From the top:

- ☞ Power dissipation: the ratio between temperature rise and thermal resistance between junction and ambient.
- ☞ The voltage drop is calculated from the model (Section III.B).
- ☞ Conduction losses depend on the specific application. Table I provides some common expressions.
- ☞ Turn-on and turn-off losses are calculated as explained in Sections III and IV
- ☞ The turn-on losses due to diode recovery can be calculated as explained in Section IV.C.
- ☞ The total losses are the sum of conduction and switching losses, including losses due to diode recovery.

VII. BRIEF NOTES ON THERMAL DESIGN

Quite unlike bipolar transistors, whose fundamental limitation in a practical circuit is its limited gain, IGBTs, power MOSFETs and thyristors are thermally limited. Hence, a good thermal design is the key to its cost effective utilization.

When the objective of the thermal design is just the selection of the heatsink that keeps the junction at, or below, a given temperature, the following expression provides the answer.

$$R_{\theta S-A} = \frac{\Delta T}{P_D} - R_{\theta J-C} - R_{\theta C-S}$$

The power dissipation can be calculated with the help of the spreadsheet of Figure 11.

In general, the objective of the thermal design is the selection of the best device-heatsink combination and may require an iterative use of the spreadsheet of Figure 11.

In order to obtain a thermal resistance case-to-sink that is close to the data sheet value, the mounting torque should be close to the maximum specified in the data sheet. An excessive mounting torque causes the package to bow and may crack the die. An inadequate mounting torque, on the other hand, gives poor thermal performance.

The temperature rise due to pulses of short duration can be calculated with the transient thermal response curves (Data sheet Figure 6). The section "Peak Current Rating" in INT-949, describes the procedure in detail.

For short pulses (50ms or less) the temperature rise calculated with the transient thermal response curve tends to be too conservative. A more accurate method to calculate temperature rise can be found in Ref. [4].

VIII. REPLACING MOSFETS WITH IGBTS:

International Rectifier' s 500V IGBTs have switching characteristics that are very close to those of power MOSFETs, without sacrificing the superior conduction characteristics of IGBTs. They offer advantages over MOSFETs in high voltage, hard-switching applications. These advantages include lower conduction losses and smaller die area for the same output power. The smaller die area results in lower input capacitance and lower cost.

Because the package style and the pinout of MOSFETs and IGBTs are identical, no mechanical or layout changes are required.

The gate drive requirement for IGBTs is similar to MOSFETs. A gate voltage between 12V and 15V is sufficient for turn-on, and no negative voltage required at turn-off. The value of the series gate resistor may have to be increased to avoid ringing at the gate of IGBT due to smaller die size.

VIII.A. Power Dissipation

In high voltage MOSFETs, the power dissipation is mostly due to conduction losses; the switching losses being negligible up to 50kHz. On the other hand, the conduction losses in the IGBT are less than in the MOSFET, but the switching losses become significant above 10kHz. The following design example illustrates the point.

Switched DC Current	=	7.5A
Duty cycle	=	0.5
Bus voltage	=	310V
Junction temperature	=	125°C
MOSFET used	=	IRFP450
$R_{DS(on)}$ (25 °C)	=	0.4Ω
Operating frequency	=	50kHz
Current waveform	=	square wave

The on-resistance of the IRFP450 MOSFET at 125°C is (from the data sheet):

$R_{DS(on)}$ (125°C) = 0.816Ω.

The conduction loss in the MOSFET at 125°C:

$P_D = R_{DS(On)}$ (125°C) * I^2 * D = 23W

Assuming 75ns switching times and 50kHz switching frequency, the switching losses in the MOSFET at 7.5A are approximately:

P_{SW}= 6.5 W

The total power loss in the MOSFET is:

P_{tot} = 29.5W

Replacing the MOSFET with a IRGP430U IGBT, the conduction loss in the IGBT is:

$P_c = V_{CE}$ (125°C) * I_c * D

The on-state collector-emitter voltage at 125°C and 7.5 A is from Figure 5 on the data sheet:

$V_{CE\ @\ 125°C}$ = 2.03V.

The conduction loss in the IGBT is:

P_c = 2.03V * 7.5A * 0.5 = 7.62W

Due to the IGBT's higher usable current density, the same power dissipation in the IGBT and MOSFET results higher junction temperature for the IGBT because of higher junction to case thermal resistance.

To maintain the junction temperature parity, the power dissipation in the IGBT needs to be reduced to:

$P_{DIGBT} = P_D * (R_{\theta SA} + R_{\theta CSM} + R_{\theta JCM}) / (R_{\theta SA} + R_{\theta SI} + R_{\theta JCI})$

Where:

$R_{\theta SA}$ Heatsink to ambient thermal resistance.
$R_{\theta CSM}$ MOSFET case to sink thermal resistance.
$R_{\theta JCM}$ MOSFET junction to case thermal resistance.
$R_{\theta SI}$ IGBT case to sink thermal resistance.
$R_{\theta JCI}$ IGBT, junction to case thermal resistance.

The total power dissipation is composed of both conduction and switching losses. Conduction losses were calculated above. Using the formula above yields P_{DIGBT} = 23.2W.

The maximum allowable power loss due to switching losses:

$P_{SW} = P_{TOT} - P_{COND}$
P_{SW} = 23.2W - 7.6W = 15.6W

The maximum switching frequency for same junction temperature in same thermal environment:

f_{max} = 10.3W/0.226mJ = 56.4kHz

The switching energy number comes from data sheet information. It will be appreciated that, being operated with lower losses, the IGBT design is more efficient.

The sources of power dissipation in the IRFP450 MOSFET and IRGP430U IGBT are shown in Figure 12.

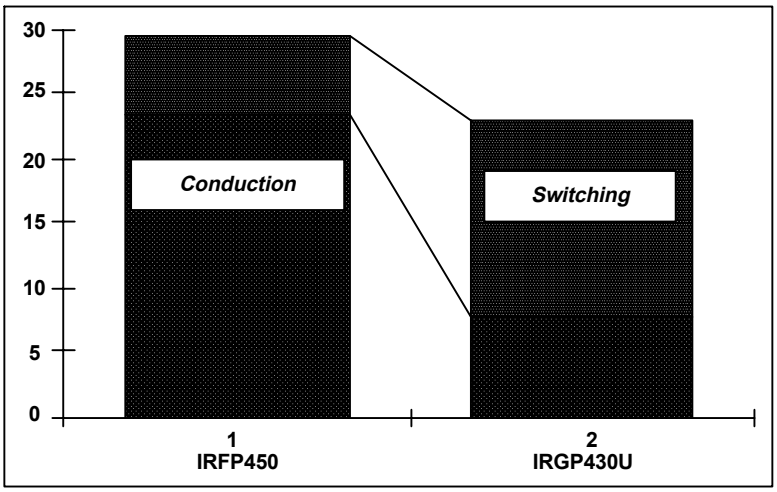


Figure 12. Power losses in an IRGPC450 MOSFET and a IRGP430U IGBT at 7.5A current both switching at 50kHz.

VIII.B Selecting IGBT:

Figure 13 provides an easy method to select an IGBT which can replace IRFP460, IRFP450 or IRFP440 MOSFET in hard-switching applications. The first step is to find the proper curve in the chart, based on the MOSFET's part number.

The part number of the recommended replacement IGBT is shown next to the curve. In general, a given MOSFET can be replaced with a two die size smaller 500V IGBT (e.g. IRFP450 → IRGP430U). The IGBT's die size is typically approximately 40% of the MOSFET's die size.

Next step is to find the maximum operating frequency for the IGBT. By definition, at the maximum operating frequency the IGBT operates at the same junction temperature as the replaced MOSFET.

To find the maximum operating frequency, select the operating current on the horizontal axis and read the maximum operating frequency on the vertical axis.

Using the power dissipation values for the IGBT in Figure 13, the heatsink can be sized for a given ambient temperature.

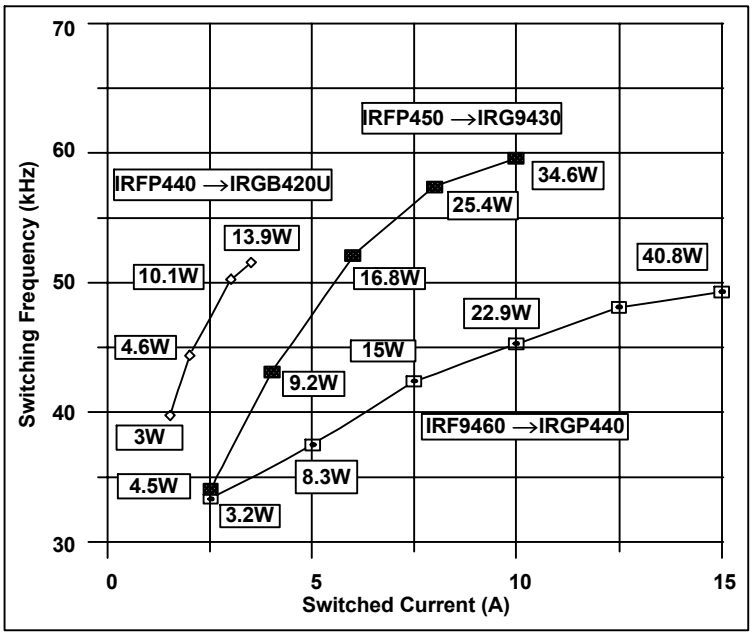


Figure 13. Maximum operating frequency of the IGBT vs. switched current. The IGBT replaces a two size bigger MOSFET in hard-switching application. Operating the IGBT at the frequency indicated by the graph, the junction temperature of the IGBT will be the same to the junction temperature of the MOSFET it replaces.
($T_{ambient}$ = 65^{0}C, T_j = 125^{0}C, Duty cycle = 0.5)

VIII.C. Gate Resistor and Snubber:

The smaller die size and input capacitance of the IGBT may result in faster switching speed than the MOSFET replaced. A larger value gate resistor slows down the turn-on speed, but has little effect on turn-off. Unlike the MOSFET, the turn-off speed of the IGBT cannot be controlled with the series gate resistor.

The high turn-off speed can generate excessive ringing and voltage spikes in the circuit. If a snubber is used, resizing the components helps reducing the noise. Minimizing the stray inductances in the wiring and in the transformer is the most effective way of reducing noise in new designs.

VIII.D. Emitter-Collector Diode:

In applications where the body diode of the MOSFET is used, IGBT-HEXFRED® diode co-packs improve performance and efficiency, while reducing current spikes. This is due to better diode performance.

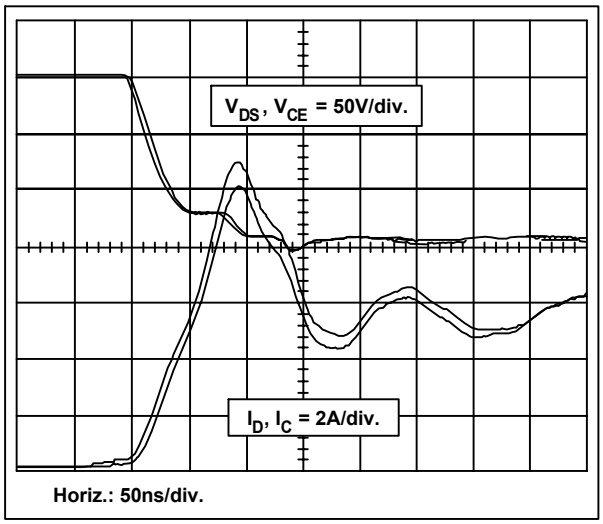


Figure 14. Turn-on waveforms. The IRFP450 and IRGP430 are switching 5.5A at 160V

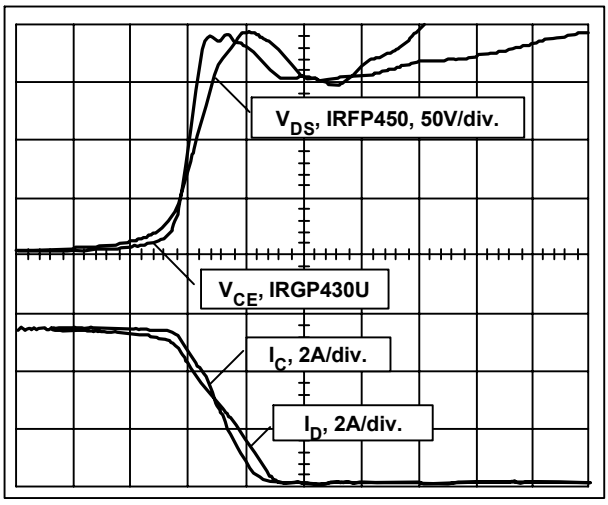


Figure 15. Turn-Off Waveforms, 5.5A at 160V.

VIII.E. Test Results

Figure 14 and Figure 15 show the turn-on and turn-off waveforms for a IRFP450 MOSFET and an IRGP430U IGBT, both switching 5.5A at 160V. The switching waveforms were taken in a 400W, single ended forward converter. Because of different die sizes, a 10 Ohm gate resistor was used for the MOSFET and 33 Ohm for the IGBT. The waveforms show same turn-on speed and faster turn-off for the IGBT.

IX. GUIDELINES ON PARALLELING

Whenever devices are operated in parallel, due consideration should be given to the sharing between devices to ensure that the individual units are operated within their limits. Items that must be considered to successfully parallel IGBTs are: gate circuitry, layout considerations, current unbalance, and temperature unbalance between devices. Paralleling helps to reduce conduction losses and junction to case thermal resistance.

However, switching losses remain the same, or may even increase. If they are the dominant losses, only a thermal resistance improvement will be achieved by paralleling. Paralleling to take advantage of lower price of smaller devices should not be attempted without due consideration of the technical risks. Experimental results should be obtained at the extremes of the manufacturing tolerances.

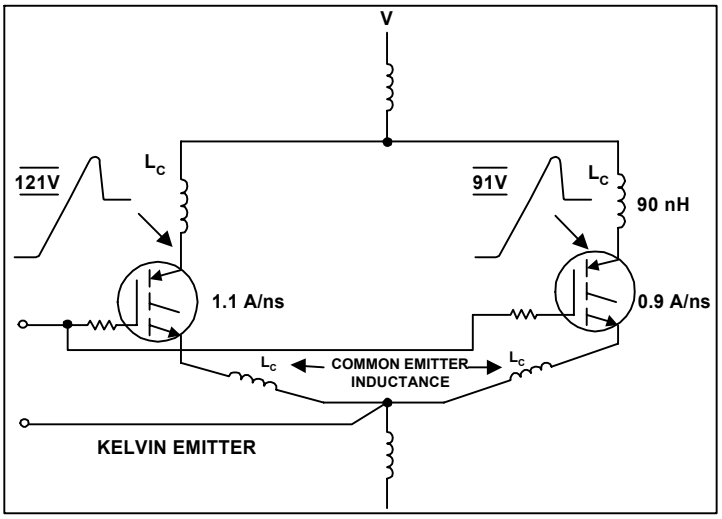


Figure 16. The effect of different di/dt and stray inductances on collector voltages.

Power MOSFETs parallel relatively well due to their positive temperature coefficient. The IGBT, being a combination of a power MOSFET and BJT, cannot be simply described as having either a negative or positive temperature coefficient. The temperature coefficient is dependent on the technology used in the IGBT's design; even within the same technology, it changes depending on the current density.

The three most important parameters from this point of view are: voltage, current and junction temperature. Voltage unbalances will be briefly examined in a qualitative way in the next section with other general considerations. The effects of current and temperature unbalances will be analyzed in detail in the following sections.

A. General paralleling guidelines

Generally speaking, voltage equality is ensured by the fact that the devices are in parallel. However, under transient conditions, voltage differentials can appear across devices, due to di/dt effects in unequalized stray inductances.

The stray inductances of a typical power circuit, like the one shown in Figure 16, have different effects, depending on where they are situated. The effects of the emitter and collector inductances that are common to the paralleled pair have been analyzed in INT-936 and will be ignored here.

An unbalance of 10% in the stray inductances that are in series with each collector, combined with a di/dt unbalance of 10% translates in an unbalance of 20% in the overshoot seen at turn-off (81 vs. 121V). To minimize these differentials both di/dt's and stray inductances have to be matched. However, if the overshoot does not violate the ratings of the IGBT, the differential in the turn-off losses is negligible.

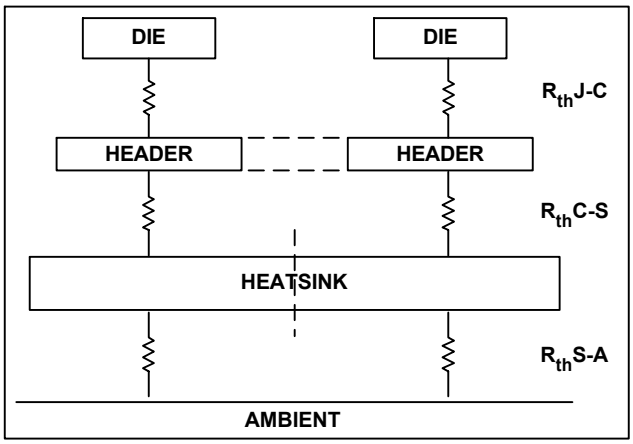


Figure 17. The characteristics of the thermal system of the paralled IGBTs.

The impact of the common emitter inductance on switching energy, on the other hand, is far from negligible, as explained in Section I.E. Furthermore, the IGBT with lower common source inductance turns off before the other, which is left to shoulder the entire load current during the turn-off transient [5]. It follows that Switchmode operation of paralleled IGBTs should not be undertaken unless the common emitter inductances are matched in value.

Finally, like power MOSFETs, parasitic oscillation have been observed on paralleled IGBTs without individual gate resistors. It is assumed that the cause for this oscillation is the same as that reported in Ref. [5], Figure 17.

In summary, the following general guidelines should be followed when paralleling IGBTs:

- Use individual gate resistors to eliminate the risk of parasitic oscillation;
- Equalize common emitter inductance and reduce it to a value that does not greatly impact the total switching losses at the frequency of operation;
- Reduce stray inductance to values that give acceptable overshoots at the maximum operating current.
- Ensure the gate of the IGBT is looking into a stiff (voltage) source with as little impedance as practical. This advice applies equally well to both paralleled and single device designs.
- Zener diodes in gate drive circuits may cause oscillations. Do not place them directly gate to emitter/source to control gate overvoltage, instead place them on the driver side of the gate isolation resistor(s), if required.
- Capacitors in gate drive circuits may also cause oscillations. Do not place them directly gate to emitter/source to control switching times, instead increase the gate isolation resistor. Capacitors slow down switching, thereby increasing the switching unbalance between devices.

Stray components are minimized by a tight layout and equalized by symmetrical position of components and routing of connections.

These guidelines ensure that the voltage and switching unbalances due to the layout are negligible with respect to those due to the IGBTs themselves, analyzed in the next section.

B. Current and temperature unbalance

In this section we will examine the steady state conduction and temperature unbalance due to the IGBTs themselves and the effects of frequency and duty cycle. When paralleling power semiconductors, the first issue that comes to mind is how well they share the total current. But, semiconductors are more sensitive to temperature than to current, so the real issue is how closely they are matched in junction temperature and whether or not one of the devices approaches the rated junction temperature. As junction temperature directly correlates to reliability, it should be of primary concern to the designer

Given two different IGBTs, each $V_{CE(on)}$ for any given current level will be slightly different. When these two IGBTs are operated in parallel, the $V_{CE(on)}$ across both devices is forced to be the same.

Thus, for a given load current, one IGBT will carry more current than the other, resulting in a current unbalance. *As long as the current remains below the maximum specified on the data sheet, current unbalance is not critically important.* At lower currents, it can be 75-100%.

Since the voltage drop is the same for both IGBTs, the device that carries more current has a higher junction temperature that may exceed the maximum rated junction temperature of 150°C. Combined with reliability issues, this factor should focus the designer's primary concern on temperature unbalance.

Current unbalance may not be affected significantly by thermal coupling. This is shown in the figures in the following section depicting current unbalance for IGBTs mounted on both separate and common heat sinks. However, the more important criteria, temperature unbalance, is affected significantly. In fact, the figures in the following section show that the maximum current is limited by the hotter device exceeding the 150°C maximum junction temperature rating. See Reference [1] Section VIII.B.3 for more information.

The complexity of the algebraic equations does not allow a direct, closed form solution of general applicability. However, with the help of the models presented in Sections III and IV and a spreadsheet, we can establish the operating conditions of two paralleled IGBTs in a given application environment. The results, although specific to the application, provide a useful insight into the factors that come into play and their respective effects.

1. Selection Criteria For The IGBTs

As far as this analysis goes, two IGBTs (IRGPC50U) have been selected from a population of 15 devices from three different lots. The two IGBTs were at the two extremes of the distribution of voltage drop, one being the highest (IGBT 1), the other being the lowest (IGBT 2). Temperature and current were not a factor since both IGBTs remained, respectively, the highest and the lowest throughout the temperature and current range.

The conduction and switching parameters were generated for both IGBTs and are listed in the spreadsheets we will use to calculate the operating conditions, together with the average parameters for the entire population.

Notice that the analysis carried out in the following sections is based on two extreme but real IGBTs, chosen from a given population. As it should be expected, the IGBT with better conduction characteristics has worse switching characteristics.

From that same population we could have constructed the model for *two fictitious* IGBTs with extreme conduction *and* switching behavior. This, however, would have been at odds with the fundamental trade-off between conduction and switching characteristics, typical of the device itself.

2. The Thermal System

The heat generated by the two IGBTs is transmitted to a sink and, ultimately, to a common ambient. Two cases will be examined: common and separate heatsinks (Figure 17).

A common heatsink establishes a thermal coupling between the two dice that limits their temperature differential. As it will be seen later, if the thermal coupling is tight, as with dice mounted on the same spreader, the temperature differential is in the order of few degrees.

3. Steady State Operating Conditions

Being in parallel, the voltage drop across the IGBTs is the same. Hence, the IGBT with better conduction characteristics carries a larger share of the load current to make its voltage drop the same as the other. Its power dissipation and junction temperature are higher by an amount that depends on the thermal design, as we will now see.

IGBT MODEL PARAMETERS

	IGBT 1 high drop		IGBT 1 high drop	nominal
Vt1	1.1784		1.0128	1.0994
Vt2	-0.0024		-0.0023	-0.0024
a1	0.3804		0.106	0.2021
a2	-0.0019		-7.00E-05	-0.0007
b1	0.3111		0.6148	0.4656
b2	0.0029		0.00	0.00

APPLICATION ENVIRONMENT

Current	25	
Ta	45	
Rth s-a	1.20	
Rth subs-sink	0.35	
Rth j-subs	0.30	(single die)

OPERATING CONDITIONS

Tj	107.79		112.38	109.9
Vt	0.9197		0.7543	0.8356
a	0.1756		0.0984	0.1252
b	0.6194		0.7222	0.6766
Delta I	39.98%	5.00	-39.98%	
I	7.50		17.50	12.50
Voltage drop	1.53		1.53	1.53
Cond. losses W	11.49		26.80	19.09
Delta T j-subs	3.45		8.04	5.73
Delta T subs-a		59.35		59.17
Tj	107.79		112.38	109.90
%	-1.91%		2.26%	0%

Alt-S	{for b35, 1, 6, 1, b37} 7
Iterate	{/ Math; Solve Go} {/Block; Values} b29..d29~ b17~

Figure 18. Spreadsheet used to establish the operating conditions of two specific IGBTs in parallel. Model parameters are shown at the top. The parameters for the entire population are also listed for reference.

For a given set of thermal conditions and a given common current, the individual currents and junction temperature can be calculated with a spreadsheet like the one shown in Figure 18. The spreadsheet is laid out to establish the operating point in the following way:

* Reasonable junction temperatures appear at the top of the Operating Conditions.
* The model parameters for that temperature are calculated.
* The current unbalance is calculated by means of the "solve" function. The equations that govern this relationship can be found in Appendix 2.
* Calculate conduction losses and temperature rise between junction and common sink for both IGBTs.
* Calculate temperature rise between common sink and ambient.
* Calculate both junction temperatures.
* Enter the junction temperatures thus calculated to the top of the box and repeat the process until the two temperatures become the same.

The results of this analysis are shown in Figure 19. For low currents the conduction unbalance can be as high as 100%, i.e. one IGBT takes the entire current, operating, however, well within its limits.

As the load current increases the current unbalance decreases and, long as the IGBTs are mounted on a common heatsink, the two temperatures stay within ±10°C.

The use of separate heatsinks causes large current unbalances and very significant temperature differentials..

The first factor that keeps the unbalance in check is the thermal feedback between the two junctions. The one with higher power dissipation increases the sink temperature and, consequently, the junction temperature of the other, by an amount that is inversely proportional to the thermal resistance between the junctions.

If the thermal coupling between dice is tight, the temperature differential cannot be significant. The other factor that reduces the current unbalance is the temperature coefficient of the voltage drop.

Although they are both negative, the IGBT with lower voltage drop has a lower temperature coefficient.

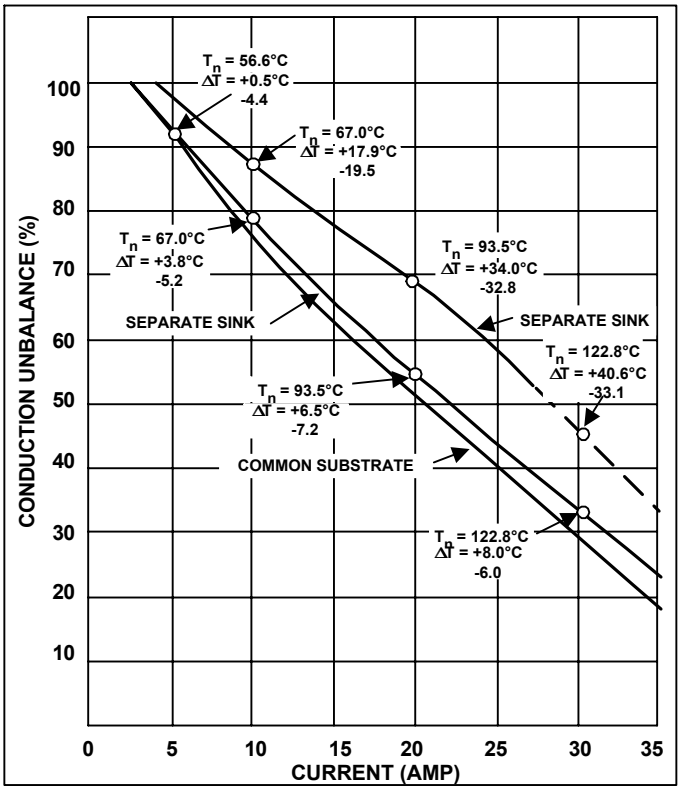


Figure 19. Conduction unbalance for two paralleled IGBTs as a function of current for three different thermal designs.

As current and temperature increase, its voltage drop changes little, while the voltage drop of the IGBT that was carrying little current comes down significantly, thereby closing the gap in current, as well as temperature.

There is a third balancing mechanism: as collector current increases, the voltage drop of the two IGBTs converge toward the average of the distribution. This intrinsically reduces the unbalance at higher currents.

4. The Effect of Frequency and Duty Cycle

In a practical applications the two IGBTs would be operated at some frequency and the losses in both devices would have a switching component.

The IGBT that carries more current will also be switching a higher current. Hence, it has higher conduction, as well as higher switching losses. The unbalance in losses is further compounded by the fact that, as we have mentioned previously, this same IGBT exhibits a worse switching behavior, which further increases its switching losses.

Thus, it would appear that a regenerative process is in place that will quickly take the junction temperature of the IGBT with lower conduction losses beyond its rated limits and that this regenerative process is accelerated by the operating frequency. In practice this does not happen and frequency helps bring about balanced operation, as we are about to see.

One additional unbalancing element, disregarded in the following calculations, is due the fact that, with a clamped inductive load, the IGBT that goes off last, ends up carrying the entire load current. This turn-off unbalance can be disregarded only to the extent that the turn-off times of the devices is short compared to the individual stray inductances, which tends to reduce this source of unbalance.

The operating conditions can be calculated with a spreadsheet similar to that shown in Figure 18, except that additional entries are required for the switching losses (Figure 20).

IGBT MODEL PARAMETERS

	IGBT 1 high drop		IGBT 1 high drop	nominal
Vt1	1.1784		1.0128	1.0994
Vt2	-0.0024		-0.0023	-0.0024
a1	0.3804		0.106	0.2021
a2	-0.0019		-7.00E-05	-0.0007
B1	0.3111		0.6148	0.4656
b2	0.0029		0.00	0.00
p1	-0.0033		-0.01	0.00
p2	0.0001		0.00	0.00
q1	1.8428		1.7941	1.7994
q2	-0.0027		-0.0029	-0.0026

APPLICATION ENVIRONMENT

Duty cycle	0.5		
Operating voltage	360		
Ipeak	44.43	Irms, pole, fund.	40
Ta	45		
Rth s-a	1.20		
Rth c-s	0.24		
Rth j-c	0.64		
Frequency (kHz)	0.4		

OPERATING CONDITIONS

Tj	115.64		123.13	118.43
Vt	0.9009		0.7296	0.8152
a	0.1607		0.0976	0.1192
b	0.6418		0.7325	0.693
p	0.0127		0.0186	0.0148
q	1.5306		1.4407	1.4915
I	16.15	-27.31%	28.28	22.21
Voltage drop	1.86		1.86	
Cond. losses W	15.01		26.29	20.41
Sw losses W	0.27		0.69	0.45
Delta T j-subs	9.78		17.26	13.35
Delta T subs-a		60.85		60.07
Tj	115.62		123.11	118.42
%	-2.37%		3.96%	0%
Delta T	-2.8°C		4.7°C	0.0

Figure 20. Spreadsheet to calculate the operating conditions of two paralleled IGBTs operated in switchmode.

Curves of current and temperature unbalance have been generated for the popular "half-bridge" circuit, as shown in Figure 21a. From these curves we observe the following:

1. As the frequency increases the current unbalance decreases. The rate of decrease increases with frequency.

2. As the current increases the amount of unbalance decreases. This result is consistent with the observations made in the Previous section.

3 . As the frequency increases the temperature differential increases. then decreases rapidly.

The key balancing mechanism in this, as in the steady state mode of operation, is the different temperature coefficients of the voltage drop.

As we have seen in the previous section, an increase in current causes an increase in temperature which, in turn, causes a reduction in voltage drop that is larger for the IGBT with a higher voltage drop. Hence, an increase in temperature results in a reduction in current unbalance.

Switching losses increase junction temperature of both IGBTs and contribute to reduce the current unbalance.

However, the increase in temperature is higher for the IGBT which carries the higher current, on account of its higher conduction and switching losses.

This delays the balancing mechanism and causes the increase in temperature differential noticeable in Figure 21 between 10 and 30 kHz ($I = 20A_{RMS}$). The thermal coupling and the difference in temperature coefficients gradually cause a reduction in the current unbalance.

This, in turn, reduces conduction and switching losses in the IGBT that was carrying more current, thereby bringing about a more balanced operating condition at an exponential rate. For the specific IGBTs we have modeled the point of current balance occurs at a temperature that is somewhat higher than 150°C.

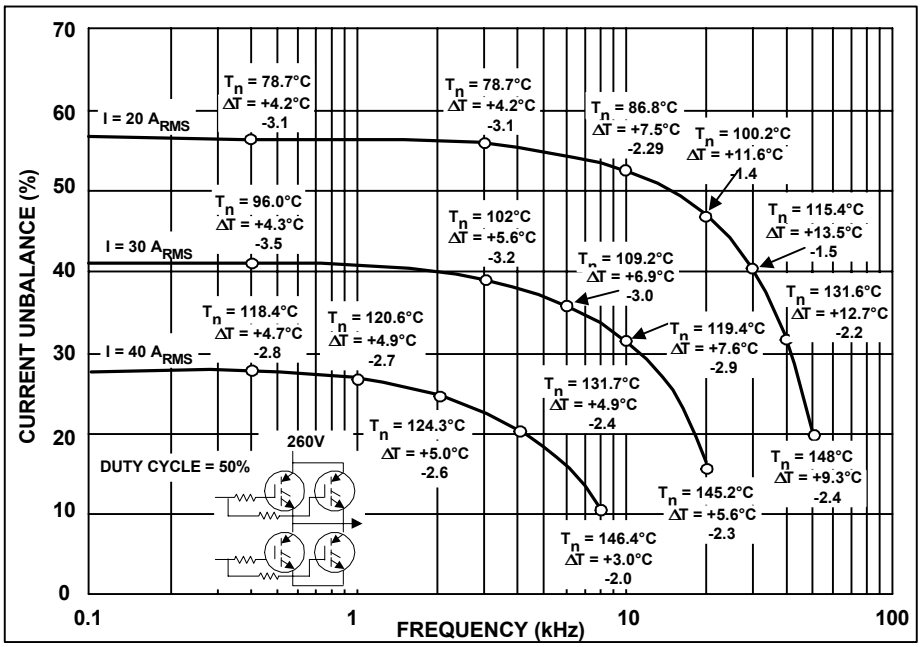


Figure 21a. Duty cycle at 50%

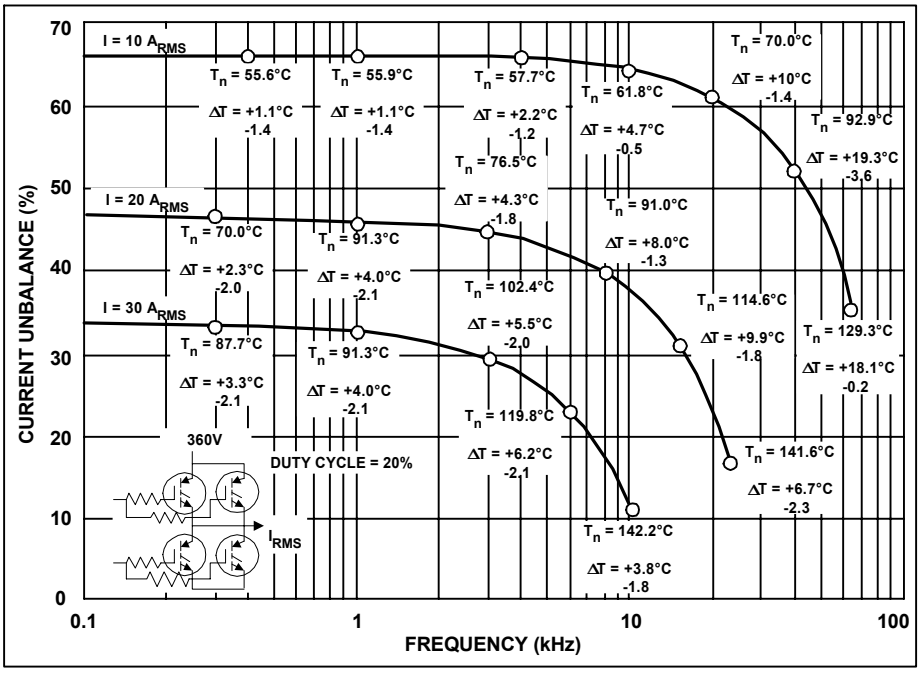


Figure 21b. Current and temperature unbalance as a function of frequency of two IGBTs operated in parallel.

At this point there will still be a temperature differential, on account of different switching losses. It is entirely possible that IGBTs with different characteristics may reach current balance at a lower temperature, beyond which the unbalance would reverse.

Operation at lower duty cycles is not significantly different from what we have just described (Figure 21b), except that the current unbalance for a given output current is lower.

This is due to the third balancing mechanism, whereby the voltage drops converge at higher currents. To generate the same output current with a lower duty cycle a higher peak current is necessary, with intrinsically better current sharing.

C. Conclusions

Although the analysis presented in the previous sections is limited to one specific type of IGBTs in a specific operating mode, the results have been found to be equally applicable to the other families of IGBTs available from International Rectifier at the time of writing. They can he summarized as follows:

1. Paralleled IGBTs will operate with a current unbalance that, in a practical application, can be as high as 50 to 70% at low currents. Temperature unbalance, on the other hand, is generally less than 10°C, provided they are on the same heatsink.

2. Three balancing mechanisms tend to reduce the current unbalance:

    * thermal feedback;
    * different temperature coefficients of the voltage drop;
    * converging voltage drop characteristics at higher currents.

3. The tighter the thermal coupling, the lower the unbalance. Operation of paralleled IGBTs on separate heatsinks should be avoided.

4. An increase in junction temperature reduces the unbalance, on account of the different temperature coefficients of the voltage drop. An increase in frequency has the same effect, for the same reason.

5. An increase in current reduces the unbalance, due to converging dynamic resistances. It would also cause an increase in temperature and, consequently, a further reduction in unbalance.

6. For a given output current, a decrease in duty cycle causes an increase in peak current, hence a reduction in unbalance.

X. SCREENING OF IGBTS FOR PARALLELING

In this section we will cover the following:

* Discuss one method of device selection to achieve better sharing, and compare performance achieved for IR's 600V Fast IGBTs.
* Compare performance achieved for IR's 600V UltraFast™ IGBTs.
* Discuss multiple (> 2) parallel IGBT designs.

X.A. Screening method for IR' 600V Fast IGBT

Device selection is an effective method to reduce derating that is intrinsically associated with paralleling and ensure that IGBTs are operated within data sheet limits. As a selection criteria, the voltage across each IGBT was measured at a certain current level. The configuration of this measurement is what we call "diode mode" (Figure 22) which means the gate is tied to the collector, and voltage is applied across that combined terminal and the emitter.

The voltage is increased until the desired current is conducted through the IGBT. This measurement must be done in pulse mode to avoid device self-heating. The voltage required for this amount of current is recorded. This measurement not only takes into account variations in $V_{CE(on)}$, but also threshold, as well as g_{fs}. This "diode mode" voltage results in a convenient way to select IGBTs that will be paralleled.

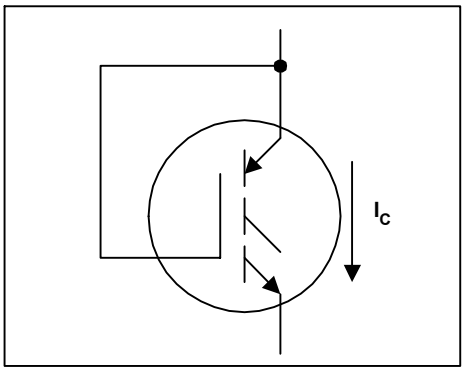


Figure 22. Connection for Measuring "Diode Mode" Voltage, V diode

Matching only $V_{CE(on)}$ would be more appropriate for IGBTs not operated in Switchmode. In the following two sections, simulations have been run on different pairs of IGBTs to compare temperature unbalance and current unbalance versus device variation measured using the "diode mode" voltage of the IGBT.

Using this device selection strategy, we set out to devise a method of determining how well various pairs of IGBTs parallel in a typical half-bridge configuration. To this end, an empirical model was used for our IGBTs that models conduction and switching loss described in Sections III.B and IV.B.

Five devices from each lot, using three lots, were examined and ranked in order of conduction voltage. Using this information, it is possible to obtain the operating point of IGBTs in parallel operation.

To compare performance of various sets of IGBTs, graphs of percent current unbalance versus total current were developed. These graphs depict how much D.C. current unbalance can be expected for a given total current, for a particular pair of IGBTs.

Two cases are plotted - devices mounted on separate heat sinks and devices mounted on a common heat sink. Also generated were graphs of junction temperature of the higher of the two junctions versus total current. In these graphs, three curves are plotted: 1) perfectly matched devices with no unbalance, 2) devices unmatched by a value of ΔV_{diode}, mounted on the same heat sink, and 3) devices unmatched by a value of ΔV_{diode}, mounted on separate heat sinks.

Figure 23 depicts the percent current unbalance at different current levels for the two IRGPC50Fs at both ends of the spectrum: one has the lowest $V_{CE(on)}$, while the other has the highest $V_{CE(on)}$ of all the devices tested. The ΔV_{diode} for this pair of IGBTs was 0.69V. The operating conditions were: two devices mounted on either a common heat sink with an $R_{\theta SA}$ of 2°C/W, or separate heat sinks with $R_{\theta SA}$s of 4°C/W, with an ambient temperature of 45°C.

As Figure 23 shows, at low currents, one IGBT carries all the current. As the current increases, the unbalance improves due to the three balancing mechanisms we mentioned above for the lower curve (same heat sink, therefore tight thermal coupling) and just the two related to current for the upper curve (separate heat sink).

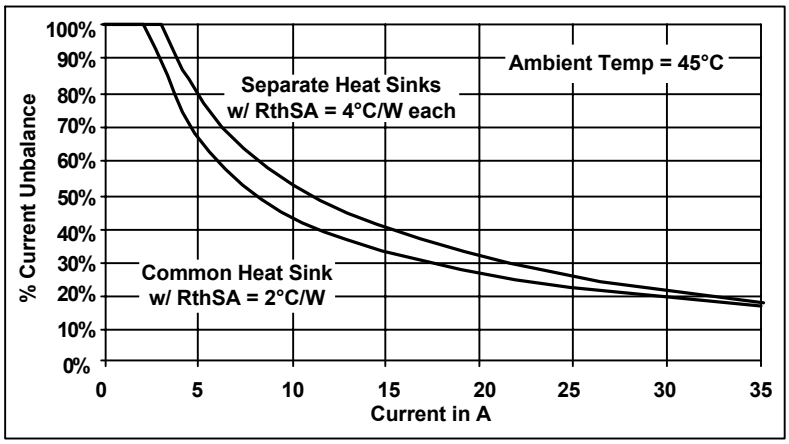


Figure 23. Percent Current Unbalance versus Total Current, IRGPC50F with ΔVdiode = 0.69V

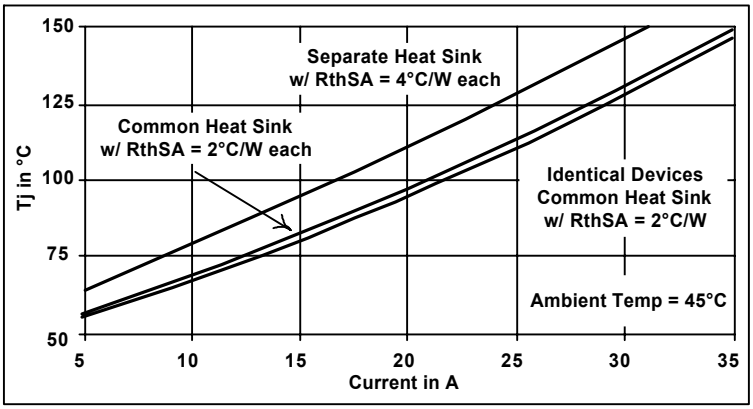


Figure 24. Junction Temperature versus Total Current, IRGPC50F with DVdiode = 0.69V

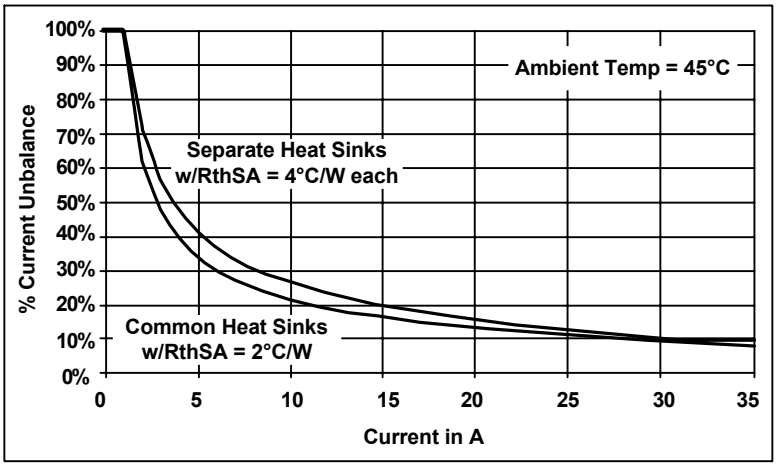


Figure 25. Percent Current Unbalance versus Total Current, IRGPC50F with ΔVdiode = 0.33V

Figure 24 depicts the higher junction temperature of the two IGBTs in parallel for three different cases: perfectly matched devices, the above two devices mounted on the same heat sink and the above two devices mounted on different heat sinks. This figure provides the strongest argument for placing separate devices on the same heat sink: while conducting 20 A, the two worst case IGBTs' junction temperatures are within 2.5°C of the ideal case of perfectly matched IGBTs. However, the junction temperature of one of these same two devices mounted on separate heat sinks operates at an increased junction temperature of 16°C. Also note that the maximum allowable current is reduced from 35 A to 31 A. All solely due to the devices' being mounted on separate heat sinks.

The two devices in Figures 23 and 24 exhibited the largest range in V_{diode} of all 15 devices tested. The difference in "V_{diode}" voltages was 0.69 V measured at 20 A.

For two devices that had a difference of 0.33 V at 20A, the graphs are shown in Figures 25 and 26. These devices, mounted on separate heat sinks, are limited to a maximum current of 33 A, while devices on a common heat sink can operate to 35 A.

While conducting 20 A, the two IGBTs' junction temperatures are within 1.5°C of the ideal case of perfectly matched IGBTs when mounted on a common heat sink. The same two devices mounted on separate heat sinks operate at an increased junction temperature of 8.3°C.

Figures 27 and 28 depict the correlation of current unbalance and junction temperature to the "Vdiode" screening parameter.

From these two figures, it is possible to predict the operation of a parallel pair of IGBTs given the difference in their "diode mode" voltages.

Figure 29 depicts the reduction in output current in a half-bridge circuit due to junction temperature limitations between unmatched IGBTs.

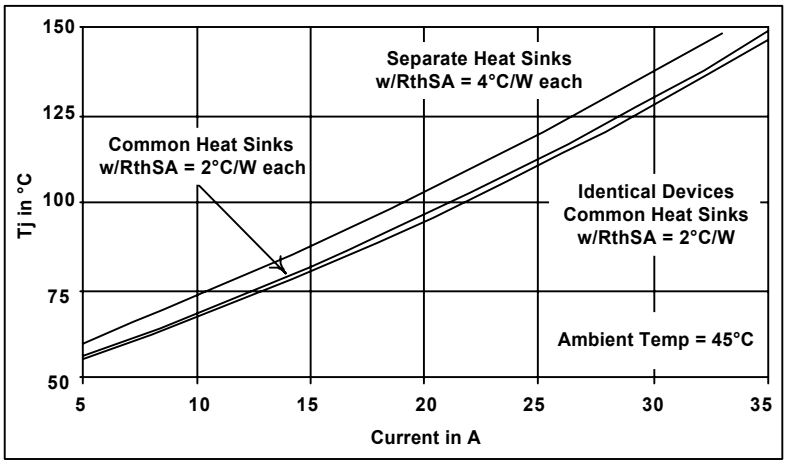


Figure 26. Junction Temperature versus Total Current, IRGPC50F with ΔVdiode = 0.33V

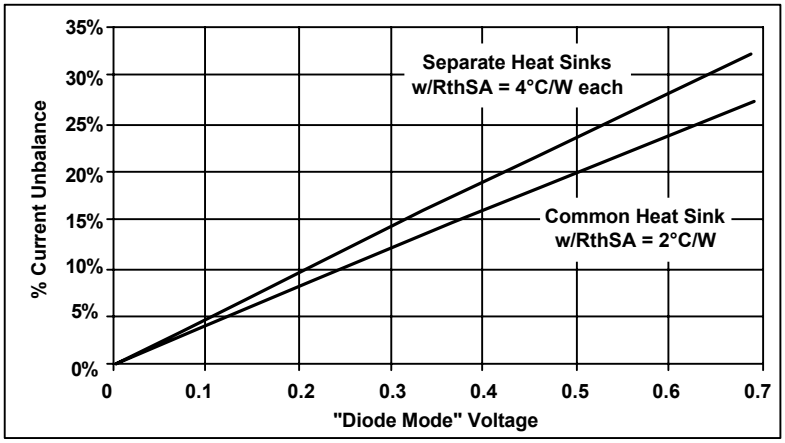


Figure 27. Percent Current Unbalance versus ΔVdiode, IRGPC50F

The circuit is operated under the same conditions as the previous ones, but instead of the current being fixed, the junction temperature is fixed at 125°C. Neither IGBT is allowed to exceed 125°C. The graph plots the maximum output current versus switching frequency. Notice that little or no derating is necessary under common applications or conditions.

The curves in Figure 29 were calculated assuming the two devices were mounted on a common heat sink. The case of separate heat sinks was not addressed due to concerns previously mentioned.
The output current would be significantly reduced if the devices were on different heat sinks.

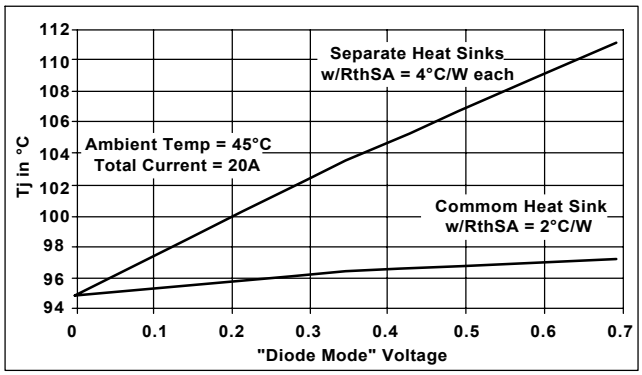


Figure 28. Junction Temperature versus ΔVdiode, IRGPC50F

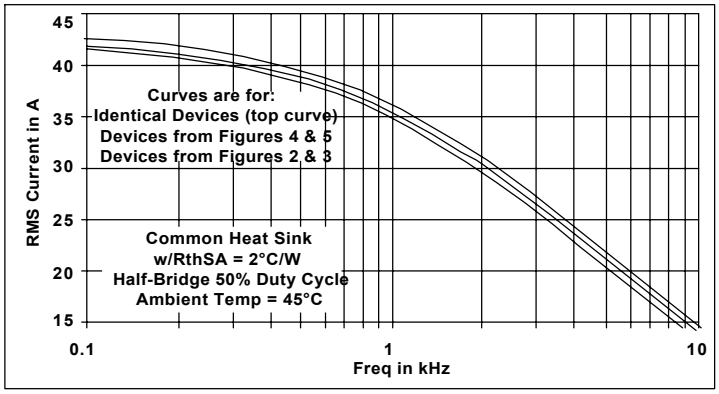


Figure 29. Current versus Frequency Graph for Three Pairs of IRGPC50Fs with ΔVdiode = 0.00, 0.33, & 0.69V

X.B. Device Selection for IR's 600V Ultra Fast IGBT

The method presented in the previous section was found to be inappropriate when the amount of lifetime killing has a significant impact on the behavior of the device. For these devices, a simple $V_{CE(on)}$ matching scheme has been implemented. The following figures describe the performance achieved using various pairs of paralleled UltraFast IGBTs.

Figure 30 depicts the percent current unbalance at different current levels for the two IRGPC50Us at both ends of the spectrum: lowest and highest $V_{CE(on)}$s of the entire population of 15 devices from three lots. The $\Delta V_{CE(on)}$ for these was 0.55 volts measured at 30 amps. The operating conditions were: two devices mounted on a common heat sink with an $R_{\theta SA}$ of 2°C/W with an ambient temperature of 45°C.

While the current sharing displayed in Figure 30 may appear to be unacceptable, as discussed in the previous section, the more important factor is the junction temperature, which is shown in Figure 31. The upper curve in Figure 10 is for the devices in Figure 30, while the lower curve is for two identical (i.e., $\Delta V_{CE(on)}$ is zero). For any current the penalty resulting from mismatched devices is only a few degrees Celsius.

To compare closer matched devices, the above two figures were repeated using two devices with a $\Delta V_{CE(on)}$ = 0.36V measured at 30 amps. Figure 32 depicts the percent current unbalance at different current levels for two mismatched IRGPC50Us. The operating conditions are the same as the previous two figures.

Figure 33 depicts the junction temperature versus current. The upper curve in Figure 33 is for the devices in Figure 32, while the lower curve is for two identical (i.e., $\Delta V_{CE(on)}$ is zero).

Figure 34 depicts the higher of the two junction temperatures for the parallel combination of several different pairs of IRGPC50Us with increasing $\Delta V_{CE(on)}$s. This graph shows that screening is not very effective and that it is critically important that paralleled devices be mounted on a common heat sink.

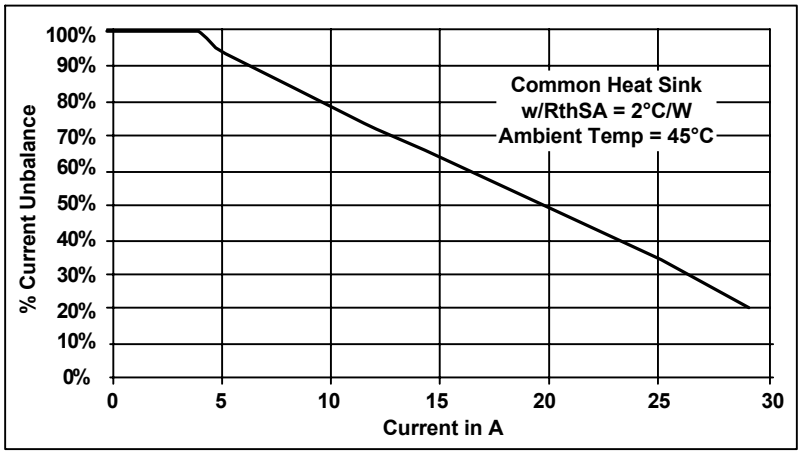


Figure 30. Percent Current Unbalance versus Total Current, IRGPC50U with $\Delta V_{CE(on)}$ = 0.55V

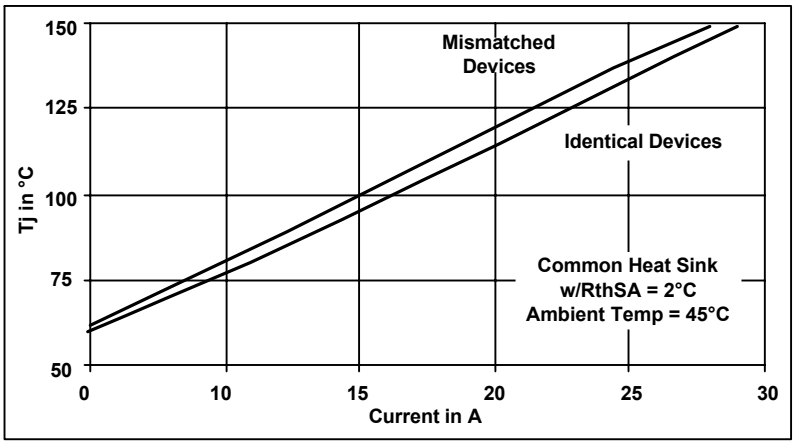


Figure 31. Junction Temperature versus Total Current, IRGPC50U with ΔVCE(on) = 0.55V

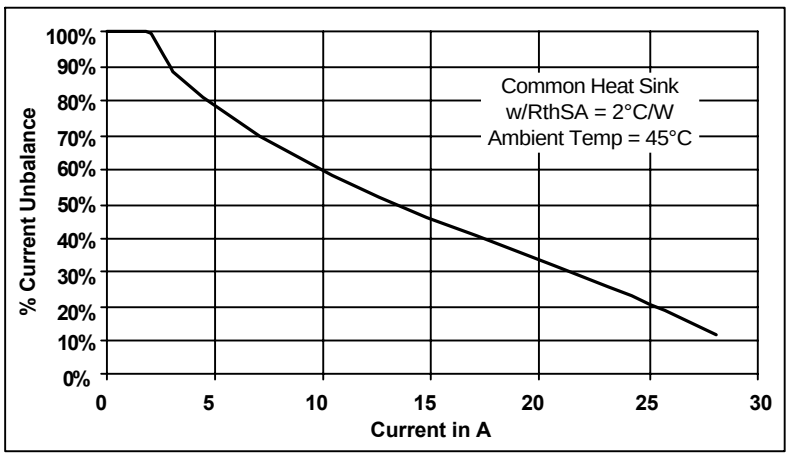


Figure 32. Percent Current Unbalance versus Total Current, IRGPC50U with $\Delta V_{CE(on)}$ = 0.36V

The final graph, Figure 14, depicts the RMS current versus switching frequency for a parallel pair of IRGPC50Us operated in a typical half-bridge configuration with 50% fixed duty cycle. The devices are mounted on a common heat sink with a thermal resistance of 2°C/W with an ambient temperature of 45°C. Neither IGBT is allowed to exceed a junction temperature of 125°C.

The upper curve is for identical devices, the next curve is for the devices described in Figures 11 and 12, while the lower curve is for the devices described in Figures 9 and 10.

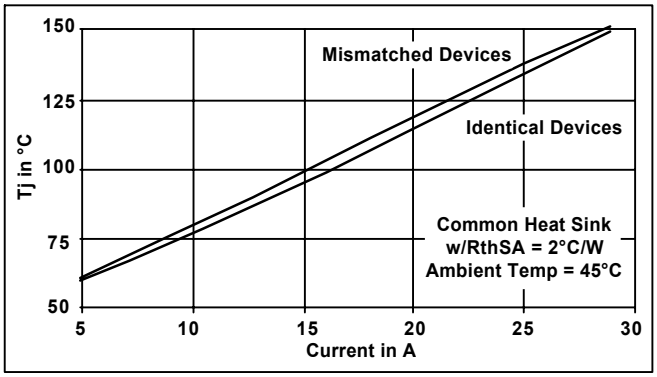


Figure 33. Junction Temperate versus Total Current, IRGPC50U with $\Delta V_{CE(on)}$ = 0.36V

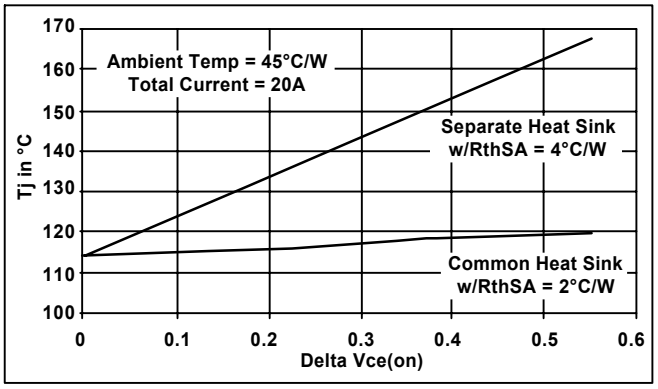


Figure 34. Junction Temperature versus ΔVCE(on), for IRGPC50Us

Comparing the output current vs frequency of the IRGPC50U (Figure 35) with that of the IRGPC50F (Figure 29) we notice that:
- Current output of Ultrafast devices operated in parallel degrades more that that of Fast IGBTs
- $\Delta V_{CE(on)}$ screening is more effective on the Fast IGBTs than on the Ultrafast

X.C. Multiple Paralleled Devices

The previous discussions have been limited to two paralleled devices, the only case that can be treated with simple analytical tools.

This does not limit the generality of the conclusions, however, as in any group of paralleled devices, there will be two with extreme voltage drops.

As explained in Section IX.B.1., these two are also likely to have extreme switching characteristics. The selection criteria, would apply to these two extreme devices, with all others falling in between.

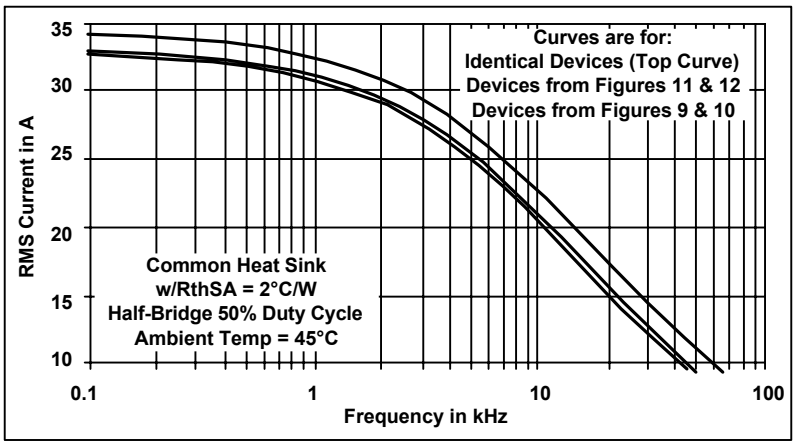


Figure 35. Current versus Frequency Graph for Three Pairs of IRGPC50Us with ΔVdiode = 0.00, 0.36, & 0.55V

References:

[1] Switching Waveforms of the L^2FET, by C.F. Wheatley and H.R. Ronan IEEE Transactions on Power Electronics. April 1987 p. 81

[2] Analysis and characterization of power MOSFET switching performance, by S.M. Clemente, A. Isidori, B.R. Pelly. Proceedings of Powercon 8, 1981, H2.

[3] Nondestructive RBSOA characterization of IGBTs and MCTs by Dan Y. Chen, VPI Current, Fall 91

[4] Transient Thermal Response of Power Semiconductors to Short Power pulses, by S. Clemente, Proceedings of the European Power Conference, Florence 1991.

[5] AN-941: A Chopper for Motor Speed Control

APPENDIX 1: DESCRIPTION OF THE CURVE FITTING METHODS USED TO DERIVE THE MODEL PARAMETERS.

The conduction model presented in Section III fulfills the basic requirements of accuracy and simplicity. As it shown in Table II, it lends itself to easy integration, thus providing a closed form expression for the conduction losses of common waveforms.

The parameters of the model are extracted from the averages and standard deviations taken at a given temperature on a population of IGBTs from three different lots, as shown in Table A.1.

VCE(ON)
DEVICE BC40F
LOT #'S: FS4
FQ8
FB3

TEMP 100°C

IC (A) >	0.6	8	16	32	50
1	0.694	1.127	1.418	1.925	2.46
2	0.678	1.114	1.413	1.94	2.5
3	0.677	1.097	1.382	1.885	2.4
4	0.685	1.112	1.399	1.899	2.42
5	0.711	1.178	1.485	2.01	2.57
6	0.743	1.263	1.604	2.19	2.83
7	0.732	1.223	1.541	2.09	2.67
8	0.723	1.206	1.524	2.08	2.66
9	0.746	1.264	1.602	2.19	2.81
10	0.731	1.223	1.543	2.09	2.67
11	0.694	1.157	1.47	2.01	2.6
12	0.714	1.193	1.513	2.06	2.65
13	0.714	1.189	1.506	2.05	2.65
14	0.7	1.147	1.512	1.98	2.55
1 5	0.706	1.1 51	1.47	1.99	2.56
MINIMUM	0.677	1.097	1.382	1.885	2.400
MAXIMUM	0.746	1.264	1.604	2.190	2.830
AVERAGE	0.71	1.176	1.492	2.026	2.600
STD	0.021	0.051	0.066	0.091	0.122
AVG + 6STD	0.838	1.484	1.888	2.572	3.331
AVG-6STD	0.581	0.868	1.097	1.480	1.869

Table A.1. Conduction Characteristics of a Population of IGBTs from three different slots

To calculate a and b the model is manipulated as follows:

$V_{ce} = V_t + a\, I^b$
$V_{ce} - V_t = a\, I^b$
$\ln (V_{ce} - V_t) = \ln a + b \ln I$

This last expression is a straight line fit to the natural logarithms of I and $V_{ce} - V_t$.

Using the least square method, the values of ln a and b can be obtained by the following formulas:

$$b = \frac{n\sum\left\{(\ln)_i \, x\left[\ln\left(V_{CE} - V_t\right)\right]_i\right\} - \left[\sum(\ln I)_i\right] x \sum\left[\ln\left(V_{CE} - V_t\right)_i\right]}{n\sum(\ln I)_i^2 - \left[\sum(\ln I)_i\right]^2}$$

$$\ln = \frac{\sum \ln\left(V_{CE} - V_t\right)_i}{n} - b\frac{\sum(\ln I)_i}{n}$$

$$a = {}_e\ln_a$$

The value of V_t has been defined as the voltage drop at a current density of approximately 0.035 a/mm2, which, for the IGBT of Table A.1, corresponds to 0.6A. With this in mind, Table A.2 shows the calculations and the error.

A	V	V cal	V-Vcal	Error	V-vt	ln(V-Vt)	ln(I)	(XiYi)
0.60	0.71	0.77	-0.0645	-9.08%				
8.00	1.18	1.17	0.0026	0.22%	0.4660	-0.7636	2.0794	-1.5878
16.00	1.49	1.50	-0.0035	-0.23%	0.7820	-0.2459	2.7726	-0.6818
32.00	2.03	2.04	0.0155	-0.76%	1.3160	0.2746	3.4657	0.9517
50.00	2.60	2.58	0.0198	0.76%	1.8900	0.6366	3.9120	2.4903
				n =	4	-0.0983	12.2298	1.1724
						Sum Yi	Sum Xi	Sum XiYi
						Varian	0.4837	

b = 0.7614 ln a = -2.3524

a = 0.0951

Table A.2. Calculation of the Voltage Drop Parameters

The values entered in Table A.2 correspond to the averages of Table A.1. If the average-plus-three-sigma values had been entered, the model parameters would correspond to the data entered.

This process can be repeated for different temperatures and a set of model parameters would be obtained. Each element of the set provides an accurate model of the specific IGBT at a specific temperature.

Temp	a	a (calc)	Error	b	b (calc)	Error	Vt	Vt Calc	Error
25		0.0778			0.7391			0.85	
50	0.0814	0.0832	-2.23%	0.7523	0.7469	0.72%	0.80	0.80	-0.40%
75	0.0899	0.0886	1.27%	0.7496	0.754-	-0.69%	0.76	0.76	0.28%
100	0.0951	0.0941	1.13%	0.7614	0.7626	-0.16%	0.71	0.71	0.34%
125	0.1009	0.0995	1.40%	0.7668	0.7704	-0.48%	0.66	0.66	0.26%
150	0.103	0.1049	-1.86%	0.7829	0.7733	0.59%	0.61	0.61	-0.49%
500	0.4703			3.8129			3.5380	6.83E-02	
(XiYi) =	48.3873		(XiYi) =	383.2507			(XiYi) = 341.7250		
Sxi^2 =	56250								

a = a1 + a2*T a1 = 0.0724 a2 = 2.17E-04
b = b1 + B2*T b1 = 0.7313 b2 = 3.13E-04
Vt = Vt1 + Vt2*T Vt1 = 0.9008 Vt2 = -1.9E-03

Table A.3. Linear Regression for Temperature Coefficient of Voltage Drop Parameters

Unfortunately, in most design problems the junction temperature is the unknown (see Figure 11, 18 and 20) and fixed temperature parameters, like those shown in Table A.2 are not useful.

Assuming that these parameters have a simple temperature dependence, a linear regression has been done, as shown in Table A.3.

This provides the expression of the voltage drop as a function of current and temperature with which we have analyzed the operating conditions of Figure 11, 18 and 20. As shown in Table A.3 the accuracy of the parameter obtained with the linear regression is within few Percent.

The switching model parameters are obtained in a very similar way, using the same type of expression, except for the threshold. The accuracy of the linear regression to calculate the temperature coefficients is acceptable for some IGBTs, particularly the Standard and the Fast, while an exponential regression is more accurate for the Ultrafast. For the sake of simplicity, only the linear regression is listed in Tables I and III.

APPENDIX 2: Equations to identify the operating point of paralleled IGBTs.

In the system described in sections IX.B.1 and B.2 the parameters listed in the two top boxes of Figure 20 are known, while those listed in the third box have to be calculated. The two fundamental constraints that determine the current distribution between the IGBTs are the following:

* voltage drop across the two IGBTs is the same;
* the sum of the currents is the same and equal to the load current.

Imposing these two constraints to the voltage drop model we obtain the following:

$$V_{CE-1} = V_{CE-2}$$

$$V_{T-1} + a_{-1} I_{-1}^{(b_{-2}1)} = V_{T-2} + a_{-2} I_{-2}^{(b_{-2})}$$

$$\left(\frac{I_L}{2} + \Delta I\right) = \exp\left\{\frac{1}{b_{-2}} \ln\left[\frac{V_{T-1} - V_{T-2}}{a_{-2}} + \frac{a_{-1}}{q_{-2}}\left(\frac{I_L}{2}\right)^{(b-1)}\right]\right\}$$

where the index after the dash identifies the IGBT, while the index before the dash identifies the model parameter, e.g. VTI 2 identifies the first threshold parameter (see Figure 18) of the second IGBT.

Since the key unknowns are ΔI, T l and T 2, we need two additional expressions, which can be obtained from the thermal equations:

$$T_{-2} = T_A + I_L\left(V_{T-2} - a_{-2} I_{-2}^{(b-2)}\right)\theta_{SA} + \left(I_{-2} V_{T-2} + a_{-2} I_{-2}^{b-2+1}\right)\theta_{JS}$$

$$T_{-1} = T_A + I_L\left(V_{T-2} + a_{-2} I_{-2}^{b-2}\right)\theta_{SA} + \left[I\left(V_{T-2} + a_{-2} I^{(b-2)}\right) - \left(I_{-2} V_{T-2} + a_{-2} I_{-2}^{b+1}\right)\right]\theta_{JS}$$

The first of these expression is calculated in the cell shown on the right of the Operating Conditions box with the "solve for" function, with the parameters shown in the box. Successive calculations of current and temperature yield the final result. For these calculations the following simplification was made in the first expression:

$$V_{T-1} - V_{T-2} \cong (V_{T2-1} - V_{T2-2})(T_1 - T_2)$$

of minimal impact on overall accuracy.