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Modeling FPGA Current Waveform and Spectrum and PDN Noise Estimation

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Abstract

Dynamic current variations in FPGA or microprocessors are major characteristics for analyzing noise in a power delivery network (PDN). Direct measurement of FPGA dynamic current variation is a very difficult problem, and is less studied than other PDN design questions. In this paper, a methodology to model the FPGA dynamic current waveform and its spectrum is developed and presented. Implementation of an impedance transfer function allows predicting noise at a remote point on the PCB. Using modeling results, the noise waveform and spectrum in the PDN on the PCB is estimated. Measurements at the remote point on the PCB help evaluate the proposed methodology and show a good correlation between theory and experiments. This research demonstrates also the implementation of a dynamic current modeling methodology for PDN analysis and PCB decoupling design.

Author Biographies

Iliya Zamek, a member of technical staff at Altera Corporation, has over twenty years of experience with high-speed analog and digital circuits, memory, system design, project management, and products development. Besides developing testers and measurement methodology for FPGA characterization, he leads R&D projects on modeling jitter and dynamic current in FPGA and prediction noise in power distribution networks. Prior to Altera, he worked for U.S. crystal oscillator manufacturers Q-Tech and Statek Corp., and, earlier, the leading Russian instrumentation corporation, "Quartz." He has BS and MS degrees in physics and electronics from Gorky University, and a PhD in measurement techniques. He has published more than 50 papers, including 12 patents, with six more pending.

Peter Boyle received his BCE from the Georgia Institute of Technology in 1999. He currently works for Altera Corporation as a manager in the product engineering characterization group, where his group is responsible for measurement of I/Os, PLLs, external memory interface, and SSN. His interests include system-level measurement techniques and modeling. He has several inventions pending.

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1. Introduction

Modern FPGAs, ASICs, and microprocessors are complex devices, which draw significant static and dynamic current during switching of internal components. The increased switching current of nm-sized devices is a new problem for system designers. The switching core logic and I/O currents inside the IC constitute sources of disturbance for the power supply voltages associated with the power delivery network (PDN). Voltage variations are consequences of such switching current that may affect all the ICs connected to the common PDN. Dynamic currents inside modern nm-sized IC represent numerous very short pulses, occurring at different times. That is why the IC's total dynamic current has very wide spectrum $I(f)$ in a frequency domain, and causes wide spectrum $V_{PDN}(f)$ of PDN voltage variations (or PDN noise):

$$V_{PDN}(f) = Z_{PDN}(f) \cdot I(f)$$

where $Z_{PDN}(f)$ is a PDN impedance.

Power supply voltage variations (or PDN noise) cause increasing logic-level variations [1-5] and jitter [6-9]. Increased noise and jitter decrease the voltage and timing margins, and limit the achievable device speed. Therefore, the increase in speed and power consumption of modern FPGAs requires more work on noise analysis and design simulation. In recent years, there has been an increased amount of literature on PDNs and related issues. These studies include three main fields of research associated with the three members in the above equation: PDN impedance and PCB transfer impedance, device current variations due to toggling of internal chip components, and study of the effects (logic variations and jitter) and developing decoupling methodology.

Voltage and current variations are major features of interest when analyzing the noise characteristics observed within a PDN [10-12]. The dynamic current is less studied as compared to others, due to the difficulties of dynamic current measurement over a wide frequency range. These measurements require the placement of probes inside the chip, or as close as possible to it, to avoid the effects of FPGA package parasitics. Measurement devices inside the chip have even been inserted [5, 6]. While these solutions are desirable for research purposes, they are impractical for a standard IC. A methodology is presented herein for modeling the voltage and current variations for FPGAs, and can be extended for microprocessors and ASICs, as well. The proposed methodology determines the current variations by processing data from FPGA software pattern analysis with Altera® Quartus® II development software, which implements the FPGA programming and pattern design [13].

Two methods for dynamic current modeling are introduced in Section 2. One method is based on knowledge of device internal node signal timing diagrams. These diagrams are available with implementation of the standard FPGA tools Timing Analyzer, or TimeQuest, both of which are part of the Quartus II software. This method may be useful for a relatively simple pattern where one primary clock signal dominates. The second method is based on the implementation PowerPlay Power Analyzer [14], also part of the Quartus II software. This method can be implemented for any complex pattern.

The dynamic current methodology test vehicle is described in Section 3. The methodology evaluation requires developing the impedance calculation of a system of die-package-PCB-decoupling. Section 4 is devoted to the system impedance calculation with respect to the die, and transfer impedance on the PCB. In Section 5, the data of dynamic current, system impedance with respect to the die, and transfer impedance on PCB are used for the prediction of voltage noise at any point on the PCB. Predicted noise is compared with the direct noise measurements for the evaluation of the proposed dynamic current modeling methodology. This evaluation is performed

in Section 5 for both noise waveform and spectrum in remote points on the PCB. The experiments show a good agreement between theory predictions and measurement results, which proves the dynamic current waveform and spectrum modeling.

Section 6 demonstrates the implementation of the developed methodology of the system impedance calculation (with respect to the die) and transfer impedance on PCB to the design of the decoupling and PDN. The results show a strong correlation between the calculated total impedance transfer function and the measured PDN noise spectrum on PCB. The results of Sections 5 and 6 have their own importance at system-level design for impedances simulations, developing the decoupling, and PDN design.

2. Current Source Modeling

Two methods for dynamic current modeling are developed. One is based on a device's internal signal timing diagrams, and other is based on implementating the PowerPlay Power Analyzer. Both the timing diagrams and power analysis simulation tool are part of Quartus II software [13].

2.1. Routing Pattern

For the methodology evaluation, a simple FPGA logic (pattern) was created (Figure 1) with a single frequency, a simultaneously toggling flip-flop (TFF) pattern with one clock input, and one testing output pin terminated using the LVTTL standard. This type of a pattern simplifies the methodology evaluation.

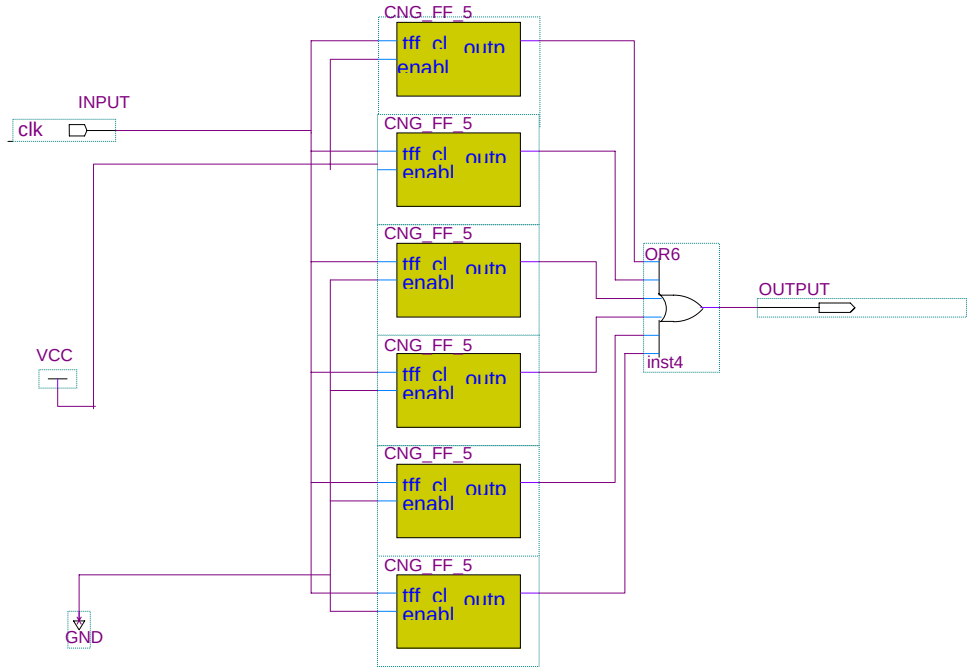


Figure 1. TFF pattern to implement noise current on PDN study

The clock input pin directly drives six parallel TFF modules, each module including approximately 2.7K TFFs, or 5% of the total FPGA logic utilization. A total of 30% of the FPGA utilization can be implemented using this pattern. The advantage of using all six blocks for a percentage between 0% and 30% utilization is to maintain a certain degree of routing and clock tree structure so that it is easy to quantize the core noise from the routing and clock tree noise.

The top two blocks are connected to the VCC to implement a 10% parallel TFF pattern, and the rest are connected to the ground or VCC in order to change the number of toggling TFFs. All the TFFs are then connected with an OR gate to the output pin in order to check if the signals are correctly passed through the FPGA. The output pin creates a certain amount of I/O noise despite the core noise created by the parallel toggling logic inside the chip. The noise of one I/O is relatively small, and also is a constant as compared against the core noise.

2.2. Modeling Dynamic Current Using TCO Distribution

Semiconductors contain complex circuits, which draw significant dynamic current. All complex circuits consist of a numerous logic elements (LEs). The dynamic current of a chip is the sum of the dynamic currents of all LEs included in the design. To model the chip dynamic current, assume a triangular shape of an elementary LE current pulse $I(t - t_{tco})$, as shown on Figure 2.

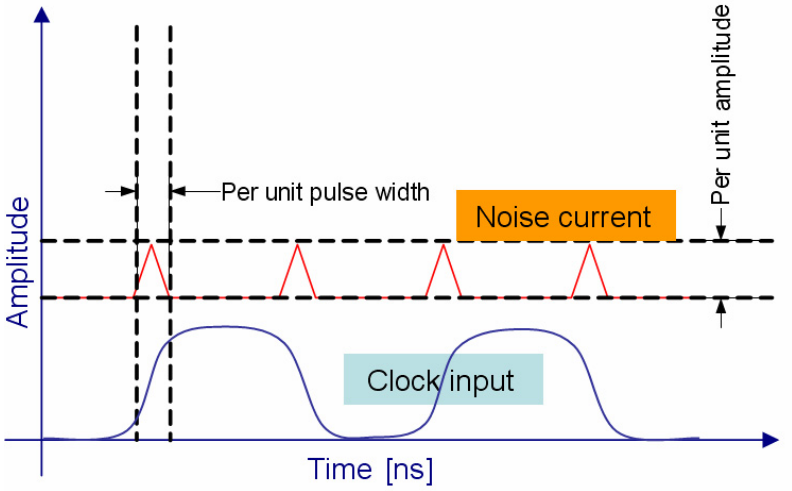
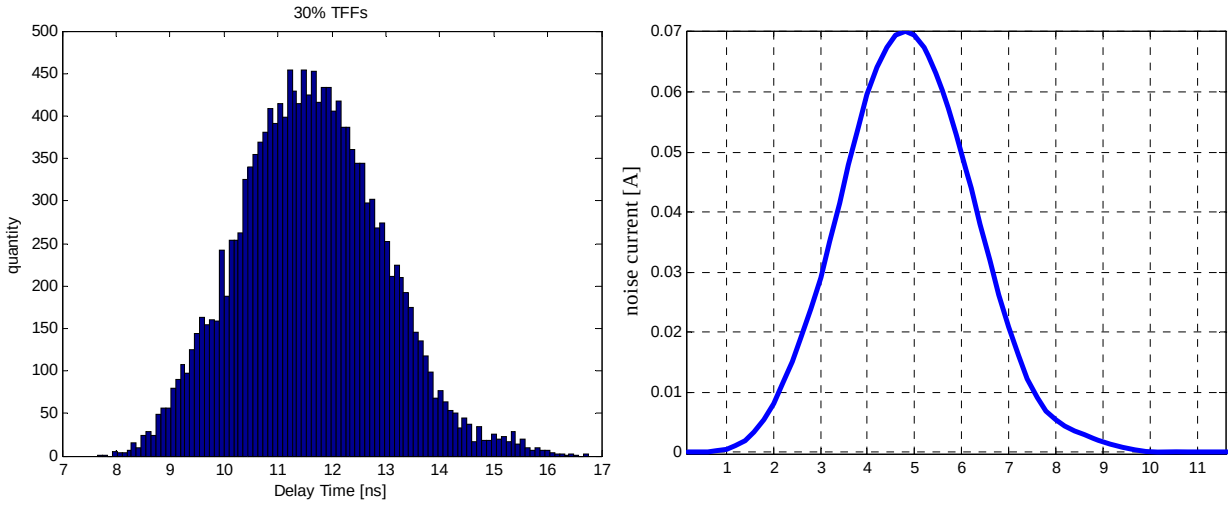


Figure 2. Current source model of elementary LE

The speed of the transistors (or how fast the flip-flops toggle) determines the pulse width of the triangular current waveform, while the propagation time t_{tco} (time from TFF to output) defines the current pulse time position. The pulse amplitude may be derived from the LE simulation or experimentally. There are numerous LEs included in each particular design due to the FPGA reconfiguration, and each of these is switching at a different moment of time.

The primary problem in the dynamic current calculation is the accurate prediction of the switching moments of each LE in a design. However, the FPGA tool has already collected this information and stored it in a software file. During the Quartus II software design process, the Timing Analyzer (part of the software itself) has already collected these data. The Timing Analyzer predicts signal transition timing positions at each node of the design. The methodology proposed in this article determines the variation of the FPGA currents by processing data from the pattern analysis recorded with the Quartus II Timing Analyzer.

The TFF pattern above was simulated with Quartus II software, and the information from the Timing Analyzer was extracted and processed with The MathWorks' MATLAB. The propagation time t_{tco} distribution of the signal edges through different paths inside the FPGA was obtained. Figure 3(a) shows an example of the path delay distribution $W_{TFF}(t_{tco})$ extracted from the Timing Analyzer. The TFF pattern uses 30% of all LEs of the FPGA, or 16,300 TFFs, with a path electrical length of 10 ns, and a standard deviation distribution of 1.32 ns (Figure 3(a)).



(a) **(b)**

Figure 3. Illustration of the equivalent current pulse calculation: a) distribution $W_{TFF}(t_{tco})$ of the TFF switching pulse, b) Equivalent total current pulse estimated

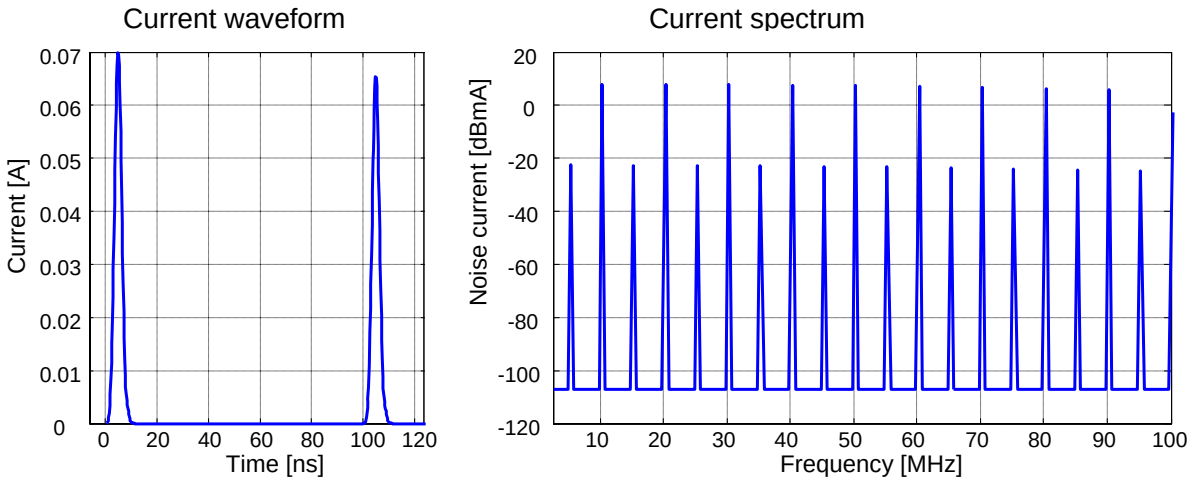
Using the distribution $W_{TFF}(t_{tco})$, the equivalent total dynamic current pulse waveform can be calculated,

$$I_{total}(t) = \int_{-\infty}^{\infty} I_{TFF}(t - tco) \cdot W(t_{tco}) dt_{tco}$$

The equivalent current pulse $I_{total}(t)$ is presented in Figure 3 (b).

Both current waveforms correspond to the rising and falling edges of the switching signals were calculated, and results are presented in Figure 4(a). The current pulse amplitudes for the rising and falling edges are different due to the flip-flop specific design and because the logic paths delays are different for the rising and falling edges. By using a Fourier transform of the waveform in Figure 4(a), and knowing the pulse repetition rate, the spectrum of the dynamic current can be obtained, shown in Figure 4(b). The pulse amplitudes can be found through simulation or by curve fitting, as will be explained later in Section 5.1.

This method [15] may be implemented for modeling the dynamic current waveforms and spectra of the relatively simple patterns when we approximately know the waveform shape (for example, for the patterns where one switching clock dominates).



(a) **(b)**

Figure 4. Dynamic current waveform and spectrum for a TFF pattern with 10-MHz clock; (a) dynamic current waveform and (b) dynamic current spectrum

2.3. Modeling Dynamic Current Using PowerPlay Power Analyzer

Another way of predicting the current consumption in the core is to use the PowerPlay Power Analyzer tool in the Quartus II software [14]. This tool estimates the power consumed by an FPGA for a pattern at a particular clock frequency and time interval.

The PowerPlay power analyzer has several features that are useful for dynamic current calculations, including:

- Device resource usage and place-and-route results
- Functional and timing simulation I/O stimuli
- Statistical analysis of expected design-node activity rates when the simulation vector inputs are not available
- Detailed reports that pinpoint which device structures and design hierarchy blocks are dissipating the most thermal power

In order to use the PowerPlay tool as a current prediction tool, the pattern is first simulated with Quartus II software. Once a successful simulation is produced, a value change dump (VCD) file is obtained. A VCD file is an ASCII file that contains header information, variable definitions, and the value changes for specific or all variables of a given design. The value changes for a variable are given in scalar or vector format, based on the nature of the variable. The PowerPlay tool then can be used to import and analyze this VCD file. The analysis uses all the signal activities information from the generated VCD file to estimate the dynamic current drawn by any given pattern.

One way to predict the switching current is by doing restricted time analysis of the VCD file. The PowerPlay tool has an option to analyze the current or power estimation for a limited period. This option gives an opportunity to obtain the current value within a small interval. By changing the position of the time interval, it is possible to obtain a current waveform. Figure 5 shows the current waveform along with the timing diagrams. Comparing the timing diagrams with the current waveform shows that current pulses happen two times more often than the trigger output pulses (TFF).

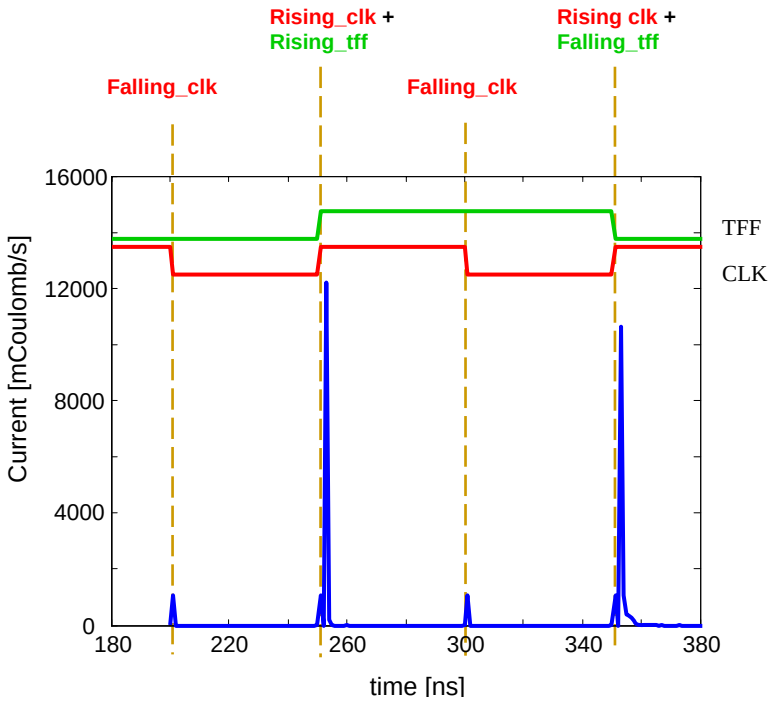


Figure 5. Blue: Current waveform of a TFF pattern estimated using the PowerPlay power analyzer; Red: Timing diagram of a clock signals; Green: Timing diagram of switching core flip-flops

Figure 6 shows the current spectrum calculated with using Fourier transform for the current waveform in Figure 5.

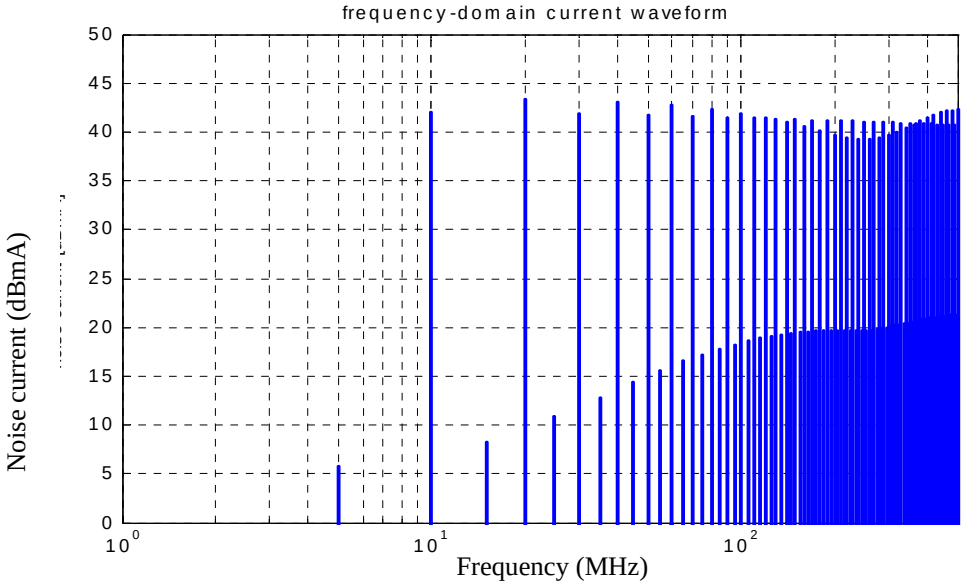


Figure 6. Dynamic current spectrum of FPGA estimated using the Fourier transform of current waveform from the Quartus II PowerPlay Power Analyzer

The amplitudes of the current pulses, which correspond to the rising and falling edges, are similar for both methods (Figures 4(a) and 5). The first pulse, the rising edge, has a higher amplitude

compared to the second current pulse, the falling edge. Both methods provide correct calculations (the current pulse differences are attributed to specific flip-flop switching performance and propagation time through routing components). However, the first method misses the numerous pulses caused by the clock signal transitions, while the second method can register these current pulses. This explains why the waveform spectrum calculated of the data in Figure 5 and presented in Figure 6 is more complex than the spectrum in Figure 4(b).
Since a unique current signature is obtained for any given pattern simulated, the method [16] can be generalized to any complex pattern.

3. Test Vehicle for Dynamic Current Modeling Methodology Evaluation

A 90-nm Altera Stratix® II GX FPGA was tested using the standard Quartus II software with the Timing Analyzer and the PowerPlay Power Analyzer. A special PCB was designed and manufactured for the proposed methodology evaluation. The board was designed to isolate a core power plane from rest of the power planes, avoid any symmetries associated with FPGA placement, provide measurements points to measure noise directly on the core power plane, provide an adequate number of decoupling capacitor pads, and provide enough signal measurement pins from all banks of the FPGA.

Figure 7 illustrates the PCB and SMA connectors' layout, with SMAs attached to the power layer to measure noise directly on the power plane. One of the SMAs is located far from the FPGA (Port 1), while the other is located close to the FPGA (Port 3) in order to observe the noise at two different locations. Port 2 is a "virtual" port at the FPGA die that is used for the impedance calculations later in Section 4.

As can be seen from Figure 7, SMAs connecting with the power plane through vias. These via inductances and spreading inductances on the PCB power and ground planes must be taken into account in the impedance calculations.

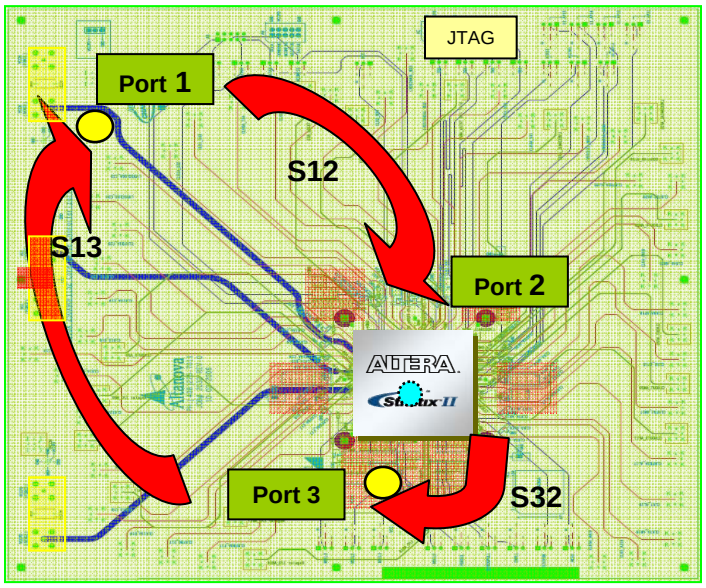


Figure 7. Test PCB and port placement

The Stratix II GX FPGA required three power levels: VCC, VCC-I/O, and VDD-predriver (PD) for I/O. The VCC layer was placed at the top of the stack in order to achieve the highest degree of isolation from the other planes, Figure 8. Backdrilling was performed, in order to avoid coupling

between the power planes due to the vias, including all the SMA connectors and capacitors' pads. The FPGA pins were not backdrilled for signal probing underneath the FPGA. All the ground vias were stitched together across the PCB.

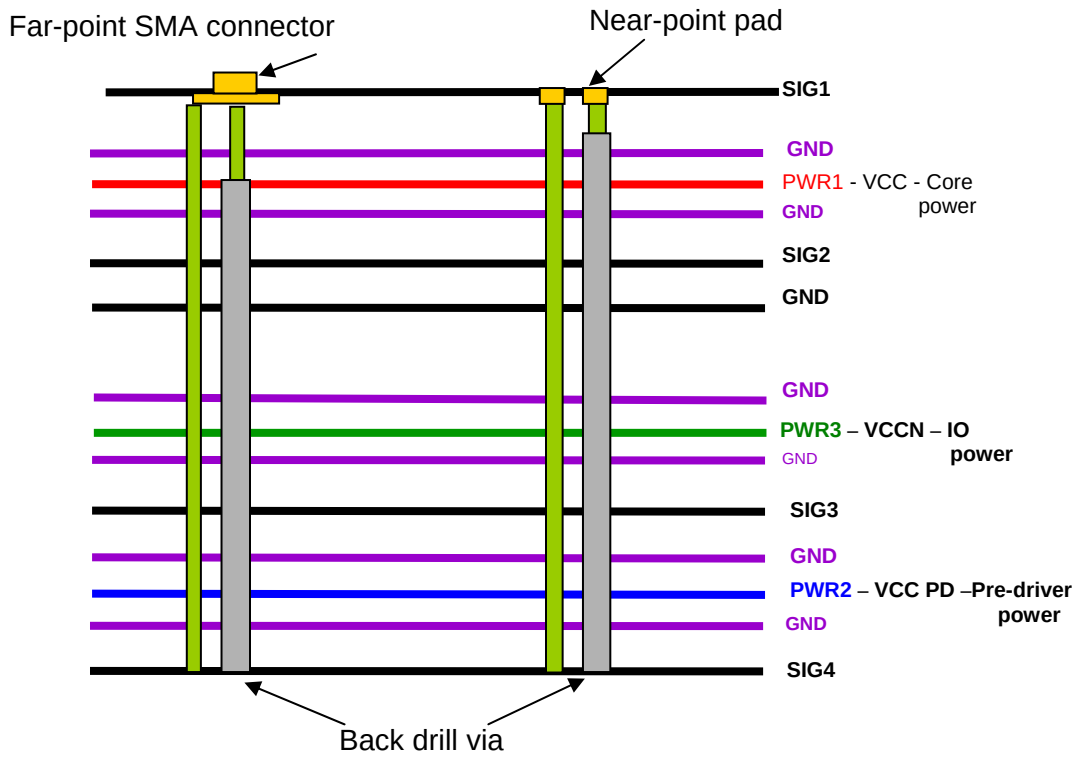


Figure 8. PCB stack up and connector placement for power planes

All the capacitors for the VCC power plane were placed on the top of the board and all the capacitors for VCCN and VCC-PD were placed on the bottom of the board. This minimized the inductance associated with the capacitor interconnects, as well as eliminated the possibility of coupling between capacitors' vias connected to different power planes.

4. Impedance Modeling

Evaluation of the proposed dynamic current modeling methodology is a separate problem, which present significant difficulties. The switching current in modern nm-size devices is made up of short current pulses occurring inside the chip. Hence, dynamic current has a very wide frequency bandwidth. The exiting die current pulses are distorted first inside the package due to package parasitics and then distorted further by coming to the PCB planes through the package balls, PCB pads, and vias. This is why direct measurements of dynamic current on the die with wide frequency bandwidth and resolution are practically impossible.

While power supply voltage variations on PCB may be easily measured, these voltage variations differ significantly from the voltage variations that the die "sees." Hence, for the methodology evaluation, the voltage variations or their spectrum at the remote point on the PCB should be able to be calculated and the results compared with direct voltage measurements. The comparison of the calculated voltage with the measured voltage will reflect the merit of the proposed methodology.

To calculate the voltage spectrum of the noise excited from the die, the modeled die's current spectrum must be multiplied by the impedance of the measured point that the die sees. This approach therefore requires knowledge of the impedance of the whole system (die-package-PCB-remote port) with respect to the FPGA die. This impedance includes three main parts:

- From FPGA die to PCB
- Transfer impedance from one port to other on the PCB with decoupling capacitors
- Transfer impedance from remote point on PCB plane to the measurement instrument, which includes vias, a SMA connector, and the input impedance of the measurement device

The transfer impedance can be measured directly. These impedance simulation results were then compared with the measured data to verify the accuracy of modeling. In contrast, the first part of the total impedance, from FPGA die to PCB, could only be simulated. The evaluation of the total impedance, including the impedance from die to PCB, was performed together with the evaluation of the noise in the system. If the calculated and measured system noises have a strong correlation, it can be concluded that impedance with respect to the die was also modeled correctly. In the methodology evaluation, dynamic current, impedance respect to the die, and transfer impedance are modeled, and the voltage characteristics are calculated.

4.1. Modeling Transfer Impedance From Core to Measurement Points

Figure 9 illustrates different parasitics of a system FPGA-PCB for FPGA with a flip-chip package.

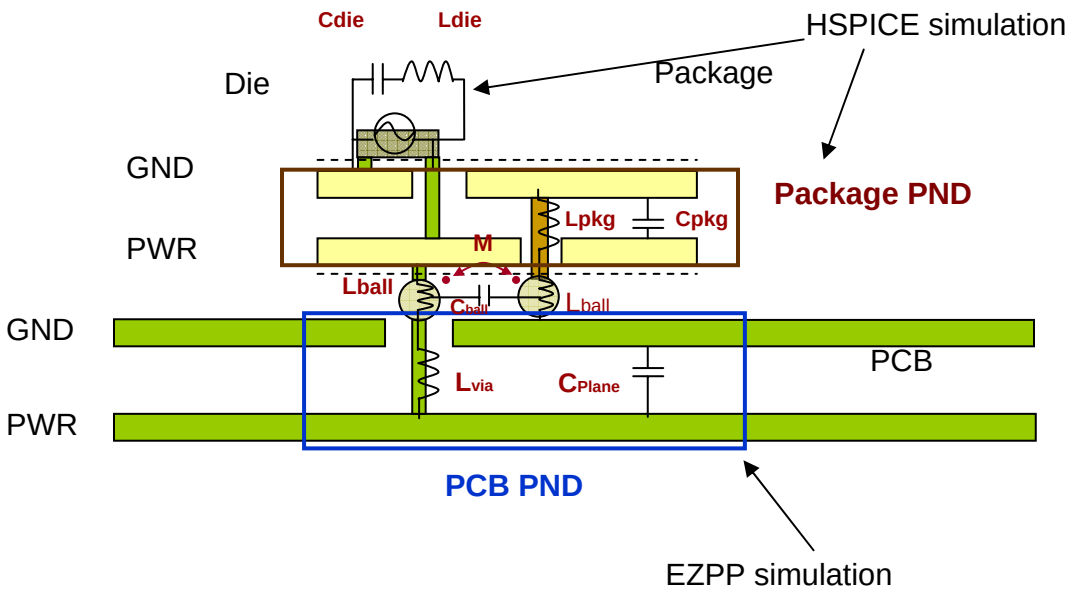


Figure 9. Illustration of a parasitics in a system FPGA die, package, and PCB

The main components of the system include FPGA die capacitance C_{Die}, die inductance, package inductance L_{pkg} and capacitance C_{pkg} (which might include the on-package capacitance), balls inductances and capacitances between them, PCB vias inductances, inductances distributed on PCB power planes, and PCB distributed plane capacitance C_{Plane}. Part of this system with bare PCB (without decoupling capacitors), vias inductances L_{via}, and plane inductances L_{Plane} is

presented in Figure 10. In this figure, the FPGA L_{FPGA} inductance is an equivalent inductance that represents a sum of the inductances of FPGA package and package balls. There are many power and ground pairs for the core power supply of the device. This causes a small value of the FPGA equivalent inductance L_{FPGA}, in a range of some Pico Henry, typically. For other power supplies, with small number of the power and ground pairs, the value of this inductance may be significantly higher.

The FPGA pairs of the package and balls inductances then are connected serially with PCB inductances, which include inductances of power and ground pads for the balls, PCB power and ground vias L_{via} inductances, spreading inductances L_{Plane} on the PCB planes, and inductances of the decoupling capacitors (not shown on the figure). All serially connected inductances in each path from power ball to ground ball are then connected in parallel for different power and ground pairs. All these components define the impedance Z_{PP} of the cavity part of a system, Figure 10. The cavity model method [12, 17] for modeling the distributed plane impedance Z_{PP}, which includes the inductance of the via portion between the planes, was utilized for impedance simulations, and HSPICE was used to include the effects of package, PCB, and port inductances and capacitances. Then the complete HSPICE model was simulated to get the S-parameter data between all three ports, as shown in Figure 7. Finally, the S-parameters were converted into Z-parameters to get the transfer and self impedances (as seen in Figures 11, 12, and 13).

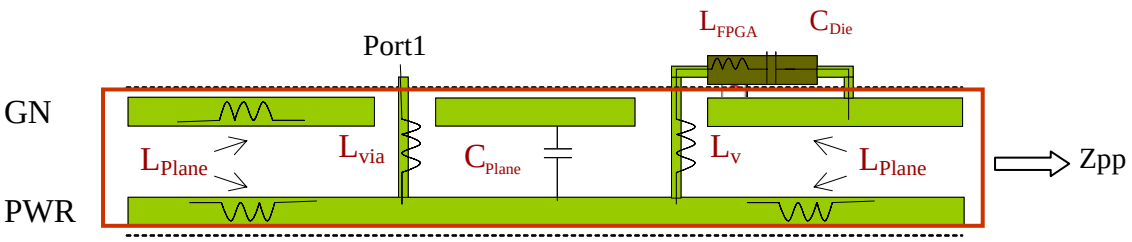


Figure 10. Lamped FPGA and bare PCB model

Figure 11 presents the measured and calculated transfer impedance from Port 3, near the FPGA package, to Port 1, a remote Port on PCB (see Figure 7 for the port locations), for a bare PCB without capacitors. HSPICE is used to include additional ports inductances associated with the connector's vias. A strong agreement between the calculated and the measured transfer impedance says that both were made correctly. As we see from Figure 11, the PCB transfer impedance has two main maximums of approximately 90 MHz and 300 MHz with numerous smaller peaks at frequencies above 550 MHz.

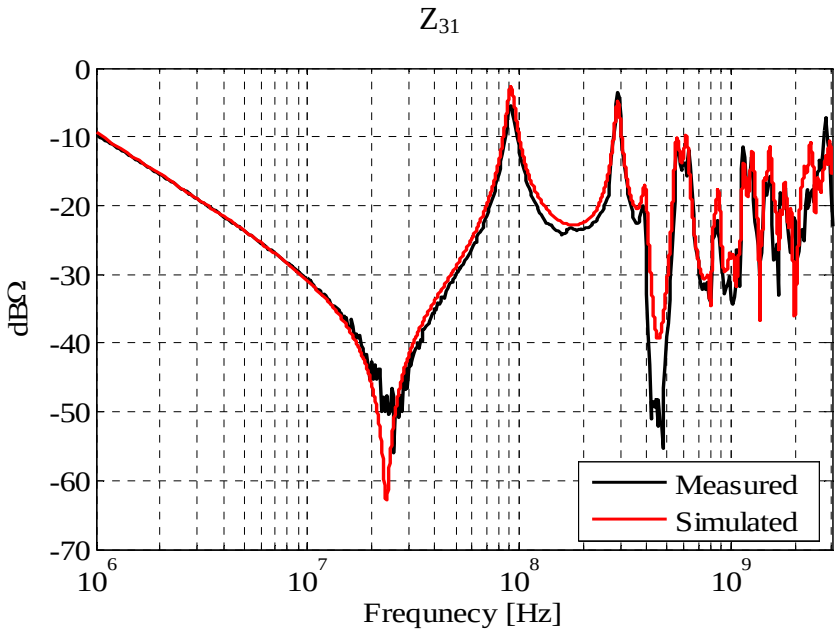


Figure 11. Simulated vs. measured transfer impedance from Port 3 to Port 1 with bare board and FPGA powered on

Figure 12 shows the measured and calculated impedance Z_{11} in Port 1. HSPICE is used to include additional port inductance associated with the connector via. From Figure 12, we also see pretty good agreement between the measurements and simulations. A small difference between the curves in Figure 12 can be explained by a possible difference of the actual connector inductance value used in the measurements and the nominal value used in the simulations. While this difference might affect the accuracy of methodology evaluation, connectors were added just for the evaluation purposes and are not present in a real system. Therefore, the connectors' inductances will not affect the noise inside the PDN during real device implementation.

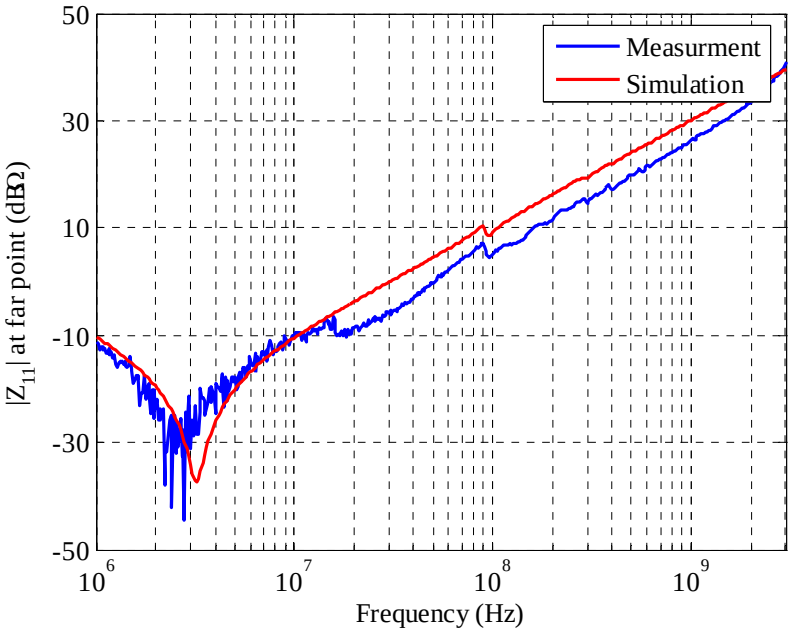


Figure 12. Simulated vs. measured input impedance at remote Port 1

Total system impedance in the remote Port 1 with respect to the die is shown in Figure 13 (red line). For the dynamic current methodology evaluation, the self impedance and transfer impedances between any ports on the PCB were simulated both with and without decoupling capacitances.

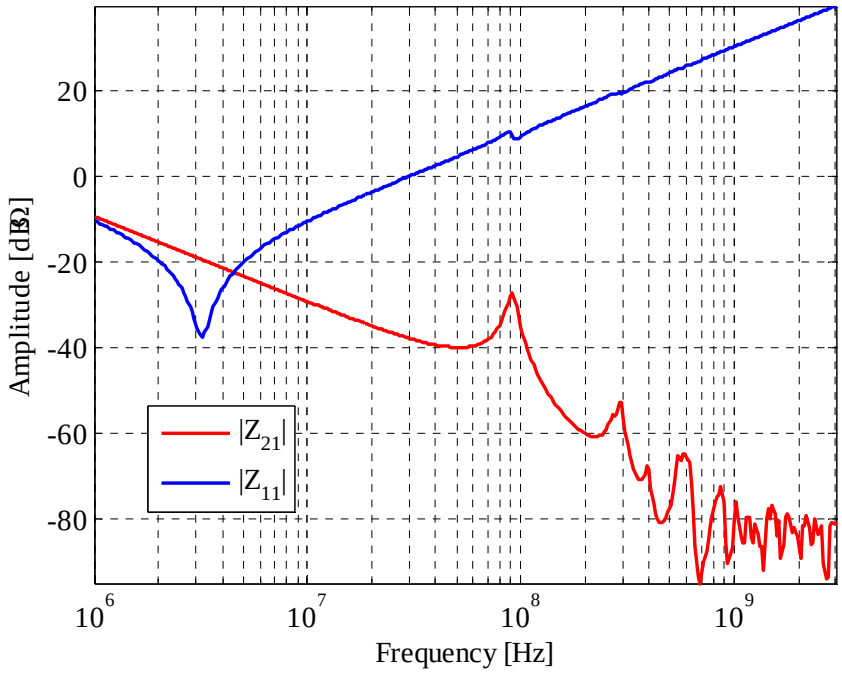


Figure 13. Simulated total transfer impedance from die to the far point - Port 1 (red) and the self impedance looking into Port 1 (blue) for PCB without decoupling capacitors

We see that the impedance transfer function has two main peaks at 90 and around 300 MHz, which correspond to the peaks of the PCB impedance transfer function in Figure 11.

5. Methodology Evaluation by Modeling and Measuring Noise Waveform and Spectrum

Spectrum analyzer and oscilloscope measurements were conducted to obtain the frequency-domain noise spectrum and time-domain waveform of a noise voltage. The measurement setup with required components is shown in Figure 14. The FPGA is programmed using Quartus II software and configured to realize the TFF pattern described in Section 2.1. Once the pattern was loaded and running, the spectrum analyzer was connected to the Port 3 or Port 1 to take measurements. The oscilloscope measurements were collected using the same setup.

The measurements are made at either the near point or the far point with different clock frequencies, different percentages of TFFs, and with and without decoupling capacitors. The spectrum analyzer measurements were made in a closed, shielded chamber.

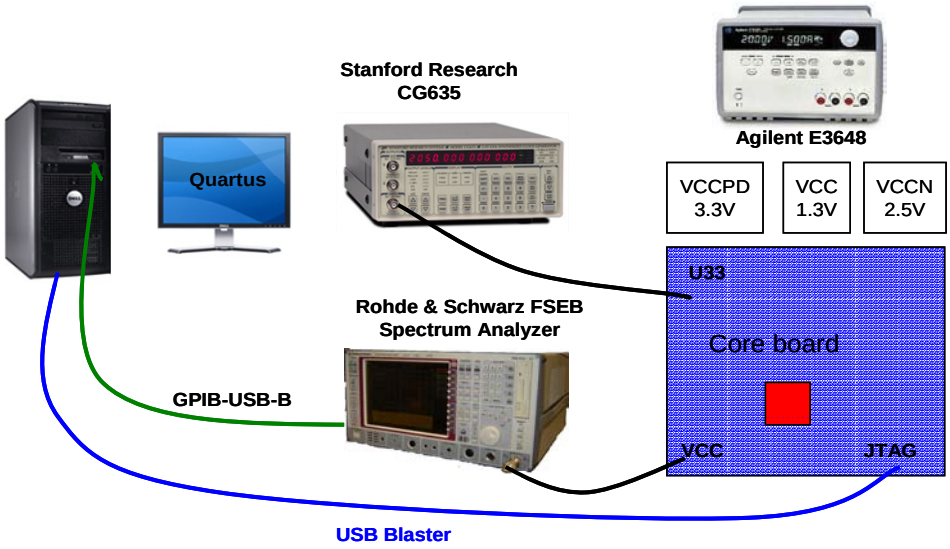


Figure 14. Measurement setup

As noted above, there were two observation points used, one close to the FPGA and another far from it. The far point had an SMA, while the near port was constructed by a SMA with a coax-cable probe mounted on the pads of a decoupling capacitor (as shown in Figure 15). S-parameter measurements were made between these two points with the board turned on, with and without decoupling capacitors.

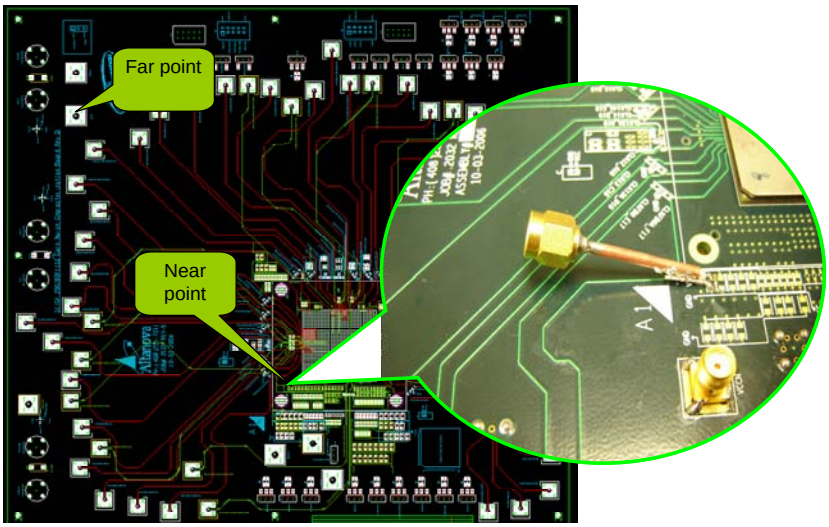


Figure 15. Near point SMA connection

Equivalent schematic of the voltage spectrum measurements is shown in Figure 16. The measurement instrument was connected to Port 1, and Port 2 is the port associated with the noise current on the die, as shown in Figure 9.

For the voltage modeling, dynamic current I_2 was estimated either by using a TCO distribution or by using the PowerPlay Analyzer. The noise V_1 spectrum was at a measurement point calculated by using transfer and self impedances with the following formulas, where the impedance matrix is a total system impedance with respect to the die, as described in Section 4. The transfer impedance Z_{21} includes the package parasitics, the on-die capacitance, and the SMA connectors' via inductance for the measurement instrument with 50Ω input impedance.

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \times \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

$$V_1 = -I_1 \times 50\Omega$$

$$V_1 = Z_{11} \times I_1 + Z_{12} \times I_2 = Z_{11} \times (-\frac{V_1}{50}) + Z_{12} \times I_2$$

$$V_1 = Z_{21} I_2 \Big/ (1 + Z_{11}/50)$$

$$\left| P_{spec} \right| = \left| \left| V_1 \right|^2 \Big/ Z_0 \right| = \left| Z_{21} I_2 \Big/ (1 + Z_{11}/50) \right|^2 / 50$$

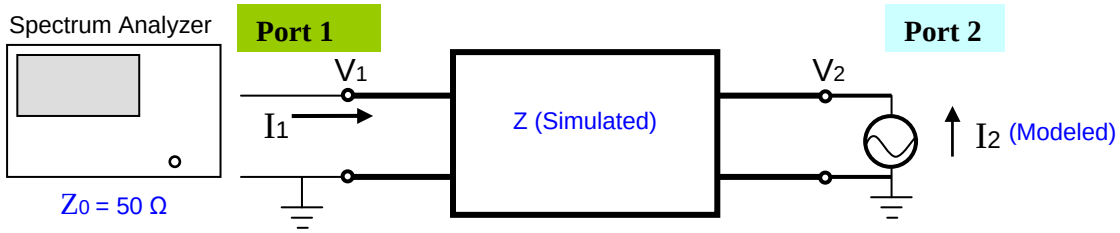


Figure 16. Noise power estimation circuit

Results of the calculations were then compared with the direct measurements as shown in Figure 16. The voltage waveform was calculated by using the inverse Fourier transform of the current spectrum and system transfer impedance.

5.1. Evaluation of Methodology Using TCO Distribution

While estimating noise power spectrum using a TCO distribution [15], the value of current pulse width was determined. The current pulse amplitude was founded by curve fitting to the measured spectrum. The pulse width and amplitude were determined using the measured result of a pattern with 25-MHz clock and 10% of TFF implementation in the FPGA. The measurements were made on the bare board. The current waveform parameters are single TFF current pulse amplitude 5.5e-6 A; single TFF current pulse width = 1e-9 s; clock pulse amplitude = 45e-6 A; and clock pulse width = 1e-9 s.

Then the estimated power spectrum is calculated using the above equations. Once these parameters are determined, the same parameters are used to calculate for other frequencies and other percentages of logic used, as shown in Figures 17, 18, and 19. The discrepancies between the modeling and the measurements are mainly due to the missing of some current pulses, the origin of the clock signals, in this methodology.

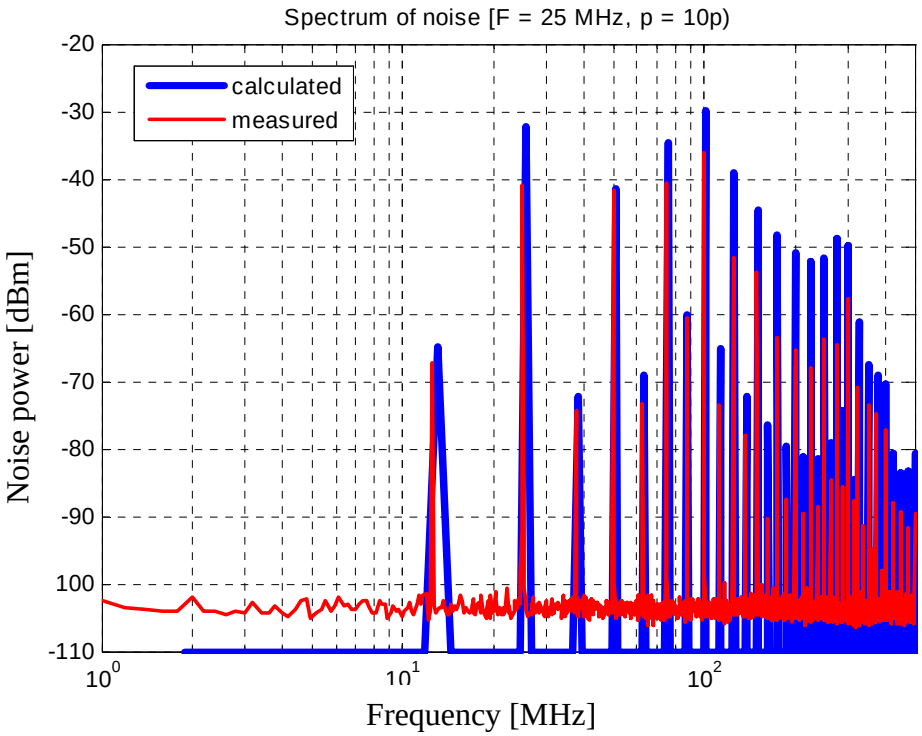


Figure 17. Calculated noise spectrum using TCO current distribution vs. measured noise spectrum at 25 MHz, 10% TFF

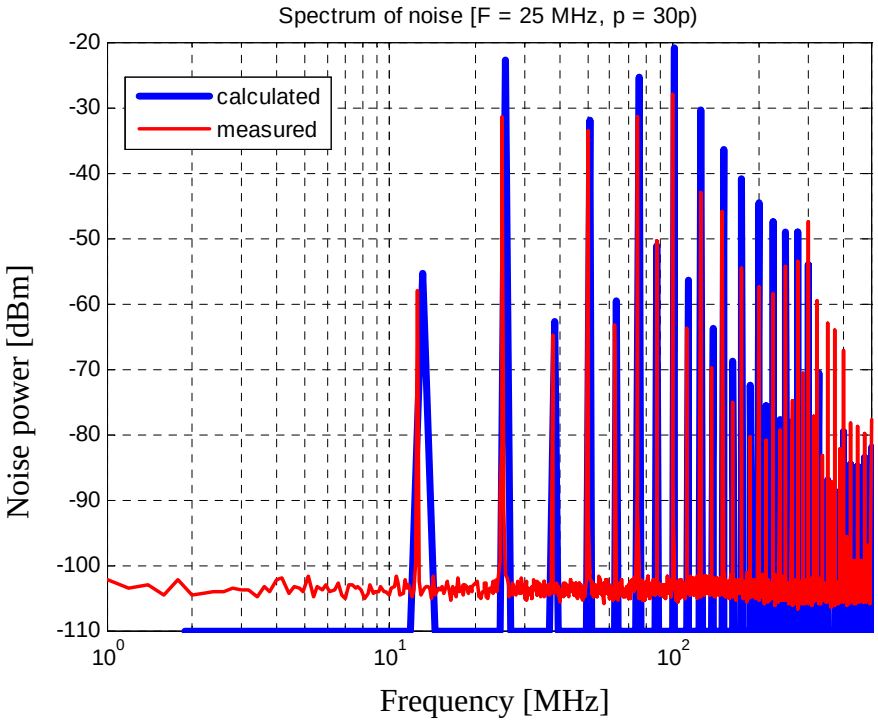


Figure 18. Calculated current spectrum using TCO current distribution vs. measured noise spectrum at 25 MHz, 30%

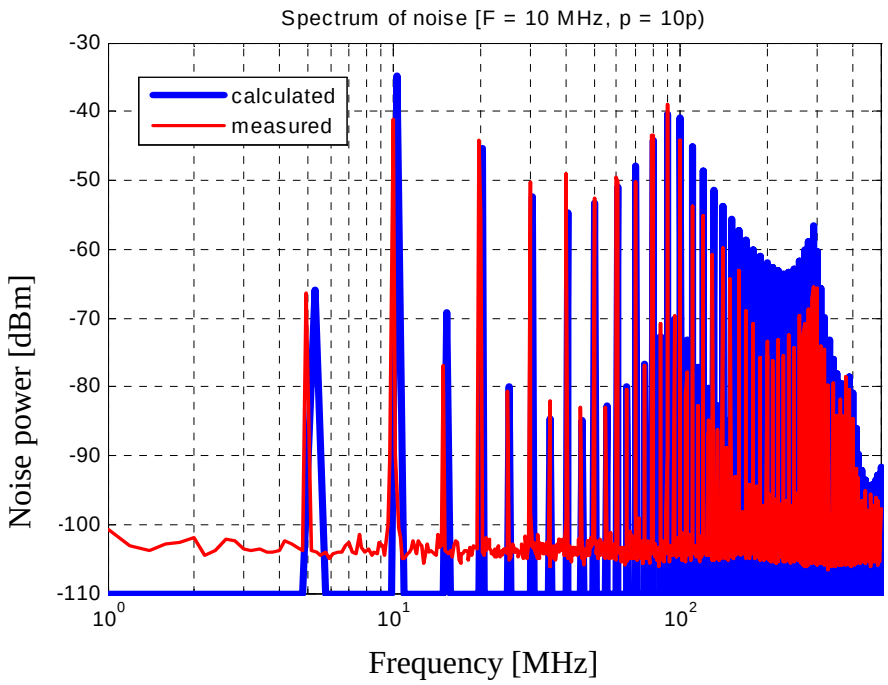


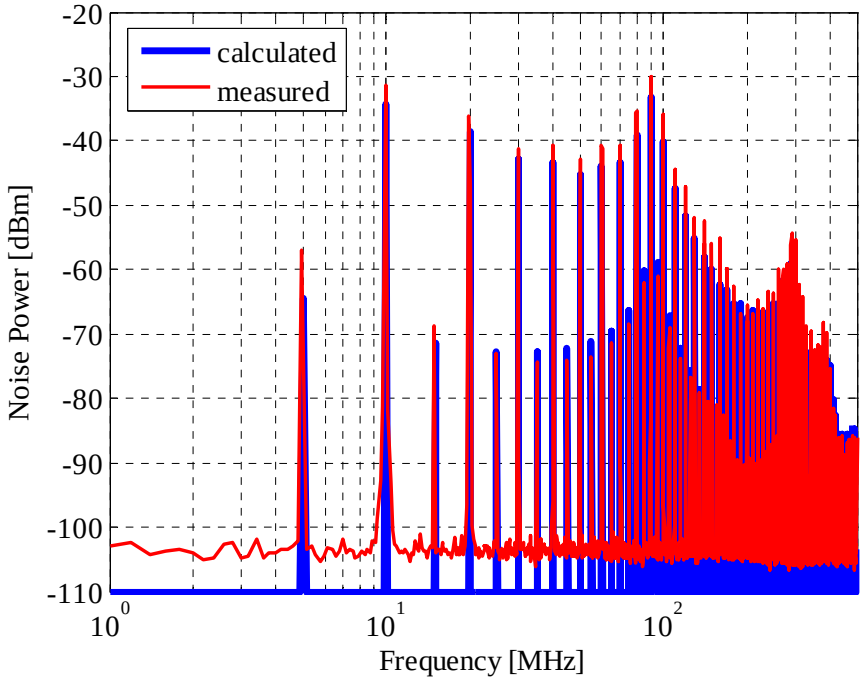
Figure 19. Calculated noise spectrum using TCO current distribution vs. measured noise spectrum at 10 MHz, 10% TFF

As seen in Figures 17, 18, and 19, this method provides relatively good correlation between the measured and simulated noise spectrums.

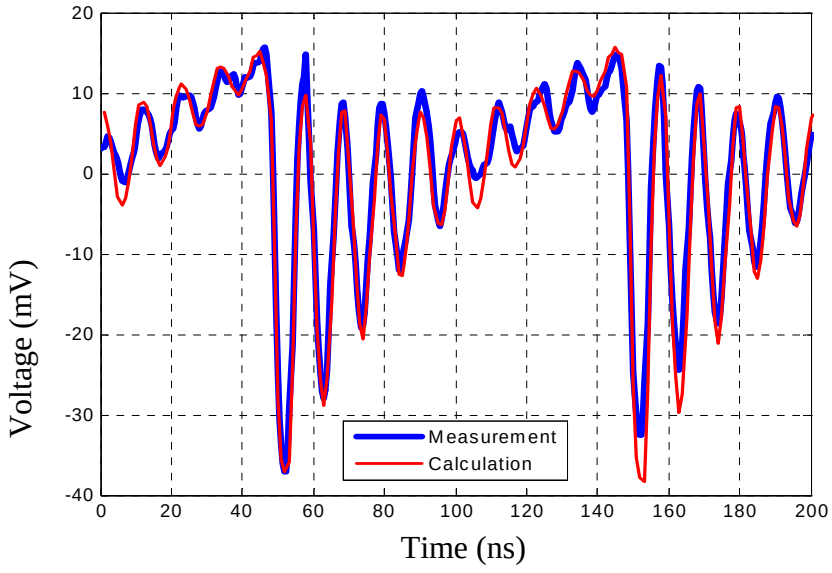
5.2. PowerPlay Power Analyzer Evaluation Methodology

Another, more accurate approach for estimating current uses the Quartus II PowerPlay power analyzer [16]. Calculating the noise spectrum from the PowerPlay power analyzer data does not require any curve fitting. Figure 20(a) compares measured noise spectrums of 30% TFF utilized at 10 MHz at the Port 1 with respect to the FPGA. (The board here does not contain any capacitors.)

The noise can also be calculated in a time domain by using the inverse Fourier transform of the current spectrum and the system transfer impedance. Measurements are made with an oscilloscope and the estimated current spectrum noise is converted back to the time domain. Figure 20(a) shows a spectrum comparison of the calculated and measured noise at 10-MHz clock and 30% TFF, and Figure 20(b) shows a comparison of the waveforms at Port 1 with the same data. Figure 21(a) and (b) compares the calculated and measured noise spectrum and noise voltage at the same Port and percentage of logic utilization for a clock frequency of 50 MHz. There is a strong correlation between measured and calculated noise waveforms and spectrums for both frequencies. The comparison is also made with respect to the FPGA die at a 10-MHz clock at the near point (Port 3) in Figure 22, and at a far point at a 100-MHz frequency in Figure 23.



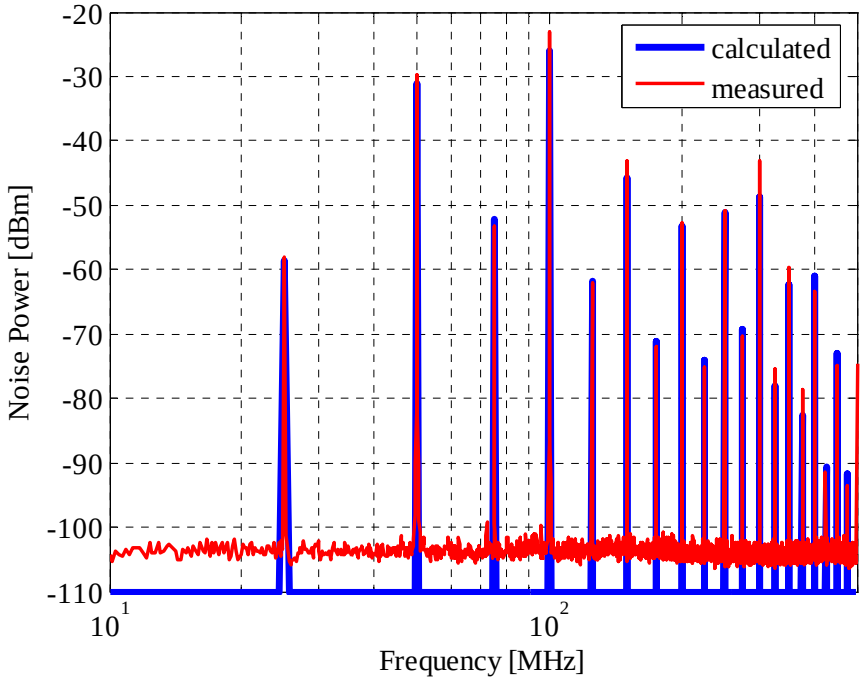
(a)



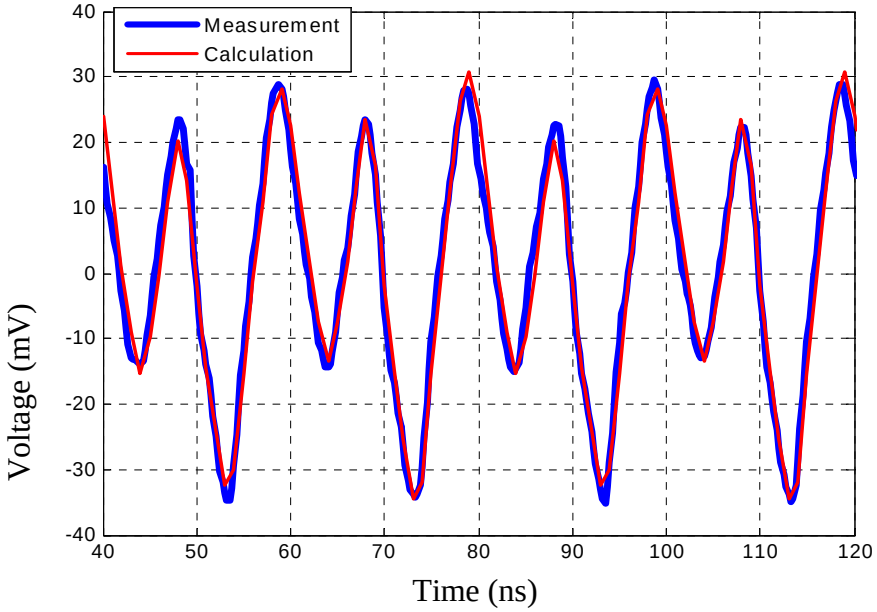
(b)

Figure 20. (a) Comparison of the calculated and measured noise spectrums (b) Comparison of the calculated and measure noise voltage 10 MHz clock, 30% TFF, far point, Port 1.

On all graphs, the calculated noise spectrum shape depends mainly on the transfer function between the core and the observation point, because the noise current spectrum at die (shown in Figure 6) is relatively flat over frequency.



(a)



(b)

Figure 21. (a) Comparison of the calculated and measured noise spectrum (b) Comparison of the calculated and measure noise voltage 50 MHz clock, 30% TFF, far point, Port 1.

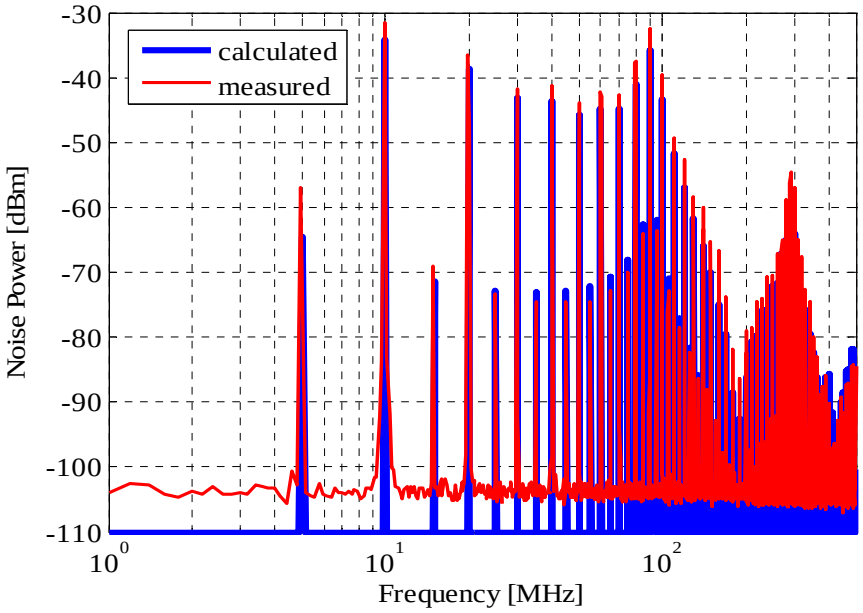


Figure 22.Calculated noise spectrum using PowerPlay power analyzer vs. measured noise spectrum at 10 MHz, 30% TFF, near point, Port 3

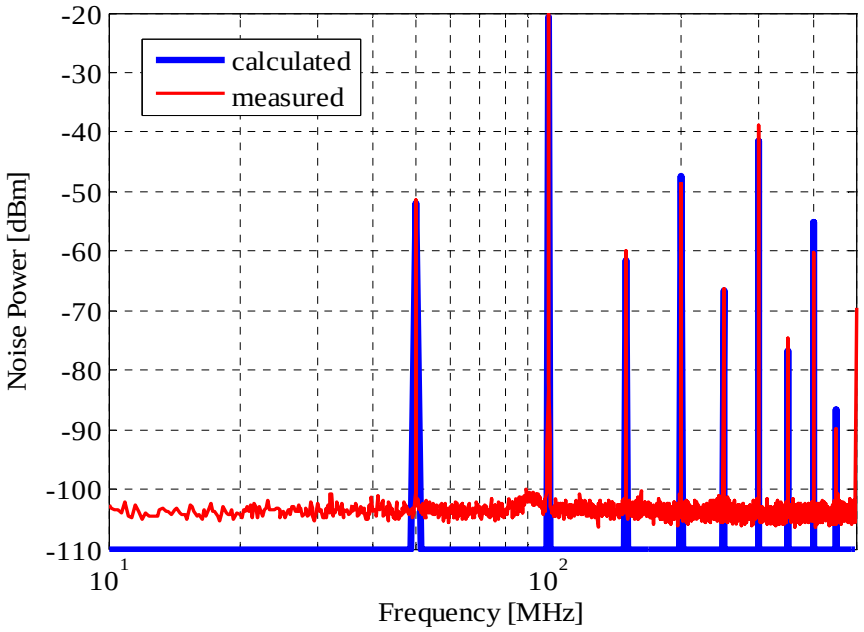


Figure 23. Calculated noise spectrum using PowerPlay power analyzer vs. measured noise spectrum at 100 MHz, 30% TFF, far point, Port 1

Note that the evaluation of the dynamic current modeling methodology has two principal uncertainties that cannot be or are difficult to measure directly. One of them is the accuracy of the current modeling with PowerPlay power analyzer, and the other is the accuracy of the modeling of those system parts that contain impedance with respect to the FPGA die. A strong correlation between the measured and calculated data confirms both of the two developed methodologies: dynamic current modeling and system impedance simulation with respect to FPGA die.

6. Effect of Decoupling Capacitances on the PCB

By placing decoupling capacitors around the FPGA, the noise spectrum can be reduced. The measured noise spectrum at the far point with and without 37 decoupling capacitors is shown in Figure 24 and Figure 25, at 10 MHz and 25 MHz, respectively. The calculated total system impedance transfer functions from die to far point on the PCB are also plotted for two cases, with and without 37 decoupling capacitors.

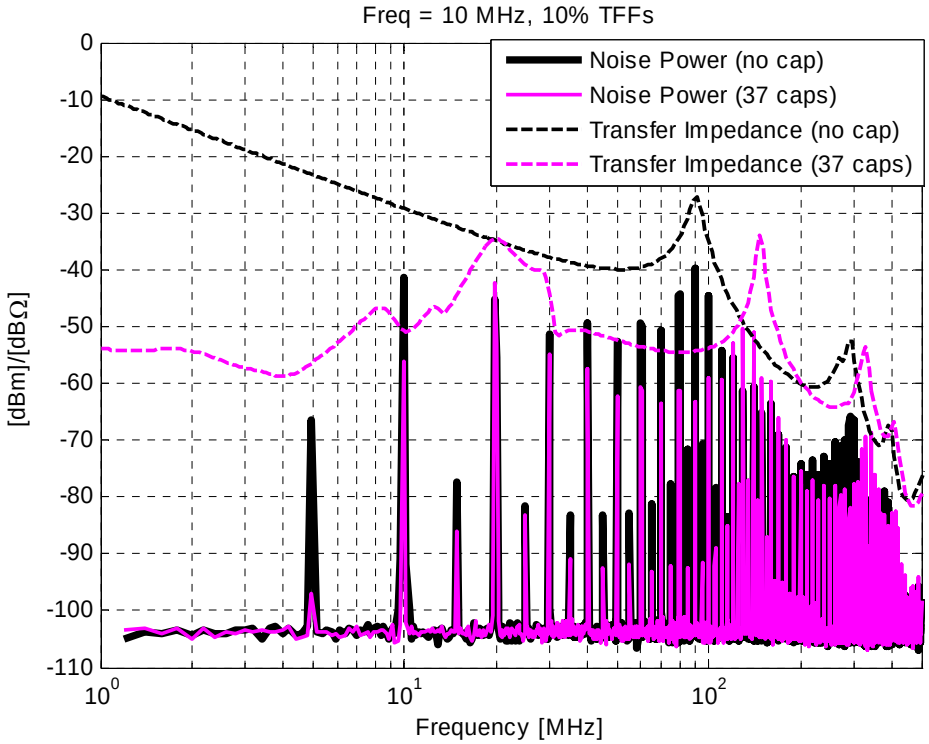


Figure 24. Measured in Port 1 noise spectrum with and without 37 de-caps along with calculated impedance transfer functions, 10-MHz clock

Figures 24 and 25 show two main maximums at frequencies around 90 MHz and 300 MHz in noise spectrums. The noise spectrum maximums almost perfectly match the maximums of the total transfer functions presented on the same figures. Some small difference between frequencies of noise maximums and frequencies of total transfer impedance maximums may be explained by inaccuracies in the estimation of connector inductance used in a simulation. These maximums in a system impedance transfer functions in Figures 26 and 27 are origin of the two main maximums of the PCB impedance transfer function shown in Figure 11. Adding decoupling capacitors to the PCB caused these maximums frequencies to shift to the higher frequency field.

From the last two graphs, it follows that adding decoupling capacitors reduces noise at frequencies below 100 MHz, with some additional peaks in the 15–35 MHz range. This peak is due to the resonance effect of an FPGA on-die capacitor, the parasitic inductances of die-package-PCB, and inductances of the decoupling capacitors.

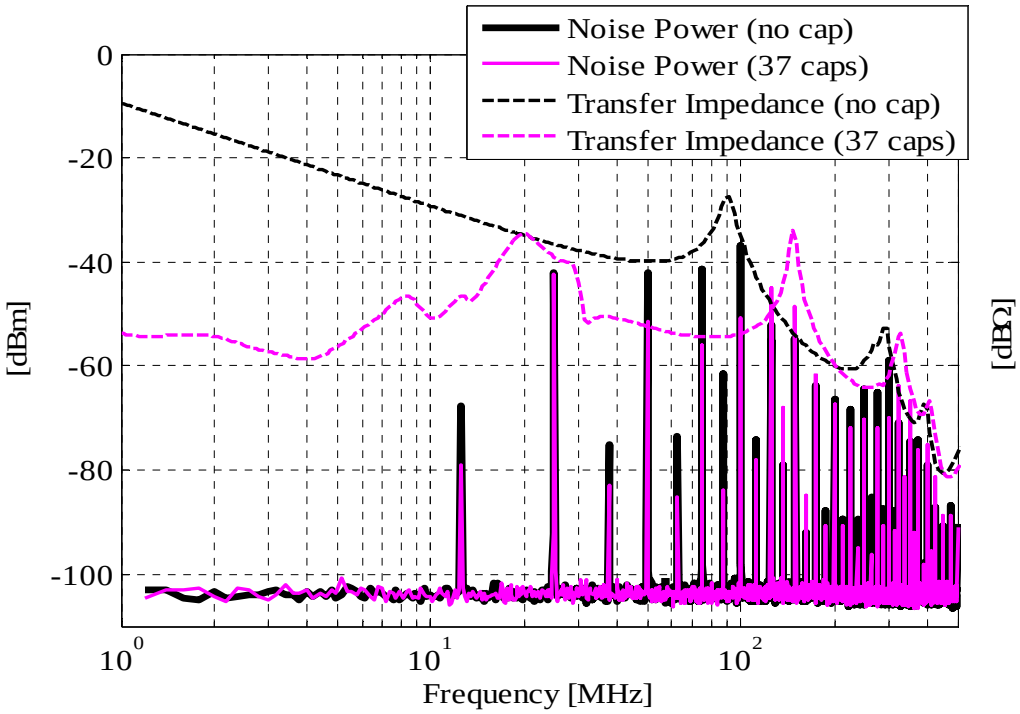


Figure 25. Measured in Port 1 noise spectrum with and without 37 de-caps along with calculated impedance transfer functions, 25-MHz clock

There is also some noise reduction at high frequencies above 200 MHz. This very important fact means that decoupling helps to reduce high frequency noise, in contrast with the common conclusion about uselessness decoupling for the frequency range above 150–200 MHz.

7. Future Work and Conclusions

The developed methodology [15, 16] of a dynamic current prediction base on the Power Analyzer implementation is a very effective way for predicting the following in a system Die-Package-PCB-decoupling:

- Dynamic current waveform and spectrum
- Noise waveform and spectrum on PCB
- Effect of the decoupling capacitors on PCB

The experiments show the surprisingly good accuracy of the prediction. The strong correlations between the calculations and the measurements prove the proposed methodology of the current modeling, as well as the developed approach for the PDN analysis and design of the system decoupling.

Future work will focus on experiments with more complex patterns, further development of modeling of dynamic current and decoupling, and on possible method applications.

8. Acknowledgements

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