Design for Low Power in Actel Antifuse FPGAs

As system power budgets grow tighter, the need for lower power components becomes more critical. For communications infrastructure applications, board cooling, cabinet space minimization, and system reliability all play a role in the system-level design. For e-appliances, battery life, thermal dissipation, and small form factors are the major design challenges. Intelligent device selection and design techniques can improve the chances of meeting a power budget. Many programmable logic devices (PLDs) claim to be high performance, but this performance often comes with a large power penalty. Actel's antifuse FPGAs offer an ideal solution for low-power yet high-performance applications.

This application note describes how Actel's antifuse FPGAs can be used in power-sensitive applications. The first section describes the antifuse technology and power-friendly architectural features of Actel's FPGAs. The second section provides some design techniques for minimizing power in the system.

This application note focuses mainly on Actel's eX family, but most of the discussion also applies to Actel's SX and SX-A families. Detailed discussions on these architectures can be found in the corresponding datasheets.

Power-Friendly Features of Actel's FPGAs

Extremely Small-sized Interconnect Elements

Actel's eX and SX-A/SX families are built on an advanced CMOS process, using a patented metal-to-metal antifuse element. The antifuse interconnect is like a pure metal interconnect, as opposed to an SRAM interconnect, which has a transistor-based switch. This passive element eliminates the totem-pole power consumed by SRAM interconnect switches. This antifuse structure is extremely small compared to SRAM-based switches, enabling the entire routing resource to be located on the top on the silicon. This results in a "sea-of-modules" architecture buried under metal layers, helping to reduce die size and switch resistance and capacitance, resulting in lower power consumption (Figure 1).

This also helps to reduce the switch resistance and capacitance, which results in less power consumption.

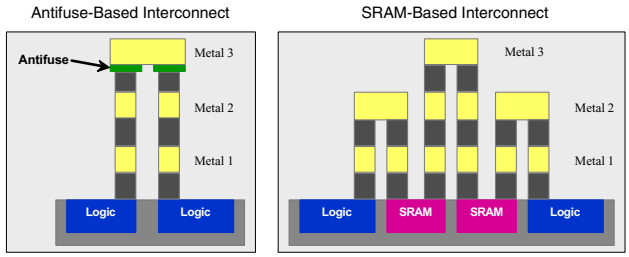

Figure 1 • *Antifuse and SRAM Interconnects*

Segmented Routing Resources

Routing-resource capacitance is a function of length, width, and the load of the routing track. Segmented routing resources are shorter than full-length, so they have less capacitance. Segmentation also allows the unused routing wires to be disconnected for capacitance reduction. However, if a signal needs to run longer distances, multiples of these segments must be connected together. This stitching has to go through routing switches. Since an antifuse switch is very fast and power friendly, this architecture can afford to have segmented routing without hurting power and timing when multiple segments are connected together. The eX, SX-A, and SX architectures use two innovative local routing resources called FastConnect and DirectConnect to connect logic modules together. FastConnects and DirectConnects have very short resources to connect adjacent cells; therefore, they have extremely low capacitance. In addition to FastConnect and DirectConnect, these architectures also have other routing resources consisting of various segment lengths. These are connected together to route signals that need to run longer distances.

Low-Power Mode Pin

A special low-power pin is available on the eX devices as an additional means to reduce power. It shuts off all internal charge pumps, reducing static current to almost 0. However, the user must take care to reset registers when exiting this mode, as discussed later in this application note.

Fine-Grained Architecture

Actel's eX, SX-A, and SX families are built on a fine-grained 4-input MUX-based architecture with some control inputs. One cell can implement logic functions of up to 5-inputs, making logic mapping more efficient. This fine-grained

architecture, coupled with abundant segmented routing resources, helps reduce power without penalizing performance.

Nonvolatile Fuse and Live at Power Up

Since Actel's FPGAs use an antifuse technology, they are nonvolatile and live at power up. This feature helps to reduce power because the device does not need to be reconfigured during the power up sequence. Since antifuses are permanently programmed, no current is required to store and retain configuration information, thereby reducing static current. SRAM based FPGAs need to be reprogrammed and consume more power.

Single-Chip Solution

Another advantage to being nonvolatile is that the programming configuration is maintained when the device is powered down. This means that no boot-up PROM is required to store the programming information and reconfigure the device at each power-up. Being a single-chip solution, these devices require less area on the board and use less power than other FPGAs.

Design Techniques to Reduce Power

CMOS-based designs consume three types of power: internal (short circuit), leakage (static), and switching (capacitive). Internal power dissipates during the short-circuit connection between V_{DD} and ground when a gate is transitioning. Leakage power is a parasitic effect common to the CMOS processes. Switching power dissipates whenever a load capacitance is charged or discharged. Switching power and short circuit together are known as dynamic power.

This application note introduces techniques to reduce static and dynamic power.

Static Power Reduction

Static current, though typically very small compared to dynamic current, becomes important for battery-operated handheld devices. This is especially true for the case where the device is not active but remains powered up. Factors that contribute to static current include I/Os and internal transistors that have not fully switched on or off, resistance on internal routing resources, pull-ups or pull-downs on inputs, and tristate drivers. In volatile technologies, some static power is required to retain programming information. Antifuses are a nonvolatile technology, so no static current is required for configuration storage.

The following practices can reduce the static current in an Actel FPGA:

1. Drive inputs to the full voltage level so that all transistors are turned on or off completely.
2. Avoid using pull-ups and pull-downs on I/Os because these resistors draw some current.
3. Avoid driving resistive loads or bipolar transistors, since these draw a continuous current, thereby adding to the static current.
4. Tie down unused clock pins as recommended in the datasheets. Floating clock inputs can add substantially to static currents.
5. When partitioning the design across multiple devices, minimize I/O usage among the devices.

Using the LP Mode Pin on eX Devices

Actel's eX family is designed with a special low-power “sleep” mode. The device enters into an extremely low-power standby mode 800 ns after the LP pin is driven high. The standby current drawn in this mode is less than 100 µA. While in low-power mode, all I/Os (except the clock inputs) are tristated and the core is turned off. Because the core is turned off, all the data stored in the flip-flops is lost and the user must initialize the device again after entering the operational mode (200 micro-seconds after the pin is driven low). Also, the user should shut off all clocks entering through CLKA, CLKB, and HCLK. These clock inputs are not tristated, so the clock signal may enter the device, adding to the power consumption. Clock inputs should be brought to logic 0 or 1 when the device enters low power mode.

Sometimes it may be difficult for the user to stop the clock from entering the device. In such a case, the user can use a normal input pin next to CLKA or CLKB and instantiate CLKINT into the design. So, the clock would enter the device through a normal input close to the clock pins and then go on routed clock resources through CLKINT (Figure 2).

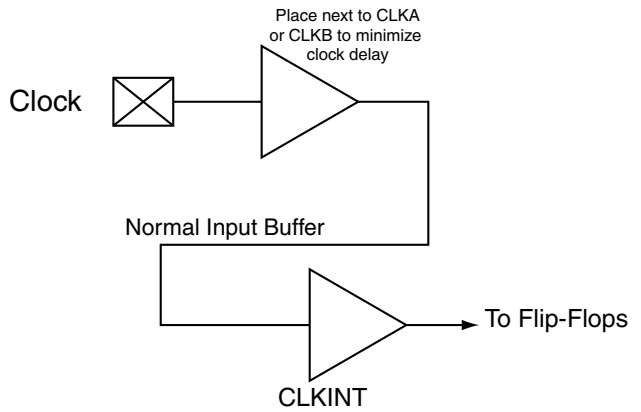

Figure 2 • *Alternative Clock Input for eX Devices*

By doing this, there is no need to worry about stopping the clock when the device is in low-power mode because the normal I/Os are tristated in this mode. However, there will be a larger clock delay of about 0.5 ns, which is acceptable in most low-power designs. Designers need to make sure to

ground the CLKA or CLKB pin associated with the CLKINT buffer.

Actel's Designer place-and-route software provides an easy way to assign pins through its ChipEdit and PinEdit utilities. Refer to the methodology guide of the relevant synthesis tool to find out how to synthesize the design containing technology cells.

Note that CLKINT macro can be used only for routed clocks. HCLK does not have the capability to route internal nets onto HCLK resources. So, HCLK resources cannot be driven from a normal input. HCLK should not be used if the LP pin is used or, alternatively, HCLK can be used and the clock signal should be stopped externally when the LP pin is active.

Reducing Dynamic Power Consumption

Dynamic power consumption is the power consumed while the clock is running and the inputs are switching. For CMOS circuits, dynamic power primarily defines overall power consumption. Dynamic power has several components, mainly capacitive-load charging and discharging (internal and I/Os) and short-circuit current. Most of the dynamic power is consumed by charging and discharging capacitance, internal and external, to the device. If the device is driving heavily with many I/O loads, the dynamic current due to the I/Os becomes a substantial part of the entire power consumption.

For a given driver in the design, dynamic power is calculated by the equation

$$P = CL \times V_{DD}^2 \times f$$

Where CL is the capacitive load, V_{DD} is the supply voltage, and f is the switching frequency. The total power is the sum of the power consumed by each driver.

Since V_{DD} is fixed, internal power reduction is achieved by decreasing the average logic-switching frequency, reducing the amount of logic switching at each clock edge, reducing the propagation of the switching activity, and lowering the capacitance of the routing network, especially for high-frequency signals. For low-power designs, take precautions at each abstraction level, from system level to technology level. The higher in the abstraction level a decision is taken to reduce power, the higher the impact will be.

Design Practices to Reduce Switching Activity

Switching-activity reduction can be controlled at various levels of the design flow. Architectural decisions in the early design phases have the greatest impact. The designer should consider clock gating, bus-timing multiplexing, glitch reduction, using power-friendly datapath elements, reducing the level of logic for high-switching signals, etc. Some of these techniques are discussed below.

Clock Gating

This is the most widely used practice for power reduction to stop the clock whenever the device is not in use. Clock gating can be applied to subsections of the design as well as the whole device. However, correctly stopping the clock is very important. The gating signal and logic should be generated properly to eliminate any glitch on the clock line. Also, the gating logic adds some delay to the clock, which affects setup and hold times. Since antifuse is an extremely fast technology, the clock delay introduced is very minimal and can be managed easily. While using clock gating, the user should take care of the placement of gating logic to minimize delay in the clock network. A typical gating logic is shown in Figure 3.

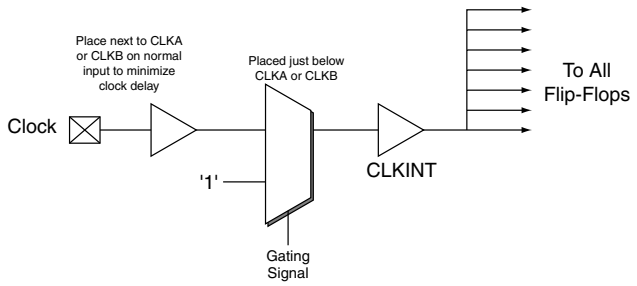

Figure 3 • *Typical Gating Logic*

The gating signal should be synchronized with a rising clock edge to avoid glitches. The gating signal should be clean and synchronous with the clock to avoid any glitch on the clock line. The extra delay due to the MUX and the routing delay will be 1.8 ns if the pad and the MUX are placed adjacent to the routed clock pins. Place-and-route software will place CLKINT into one of the routed clock pads. The routed clock pin in which CLKINT has been implemented should be grounded on the board. This placement helps with the power consumed by gating logic because it uses very short and local routing resources.

Clock gating is not possible on HCLK because it is directly connected to all of the sequential cells' clock inputs. However, if clock gating is not used, HCLK should be used because this clock consumes less power. HCLK consumes less power and is faster than routed clocks. In general, HCLK should be the clock of choice unless the user is planning to use gated clock.

Guarded Evaluation

This is a technique used to stop inputs from switching to the blocks whose outputs are not used. For example, consider a multiplier whose outputs are used only under certain conditions. In this case, the input to a multiplier can be

stopped from toggling whenever outputs are not used. It will stop unnecessary switching from entering into the multiplier. One latch only requires one combinatorial cell in the eX, SX-A, and SX families; thus they are not expensive in terms of area utilization (Figure 4).

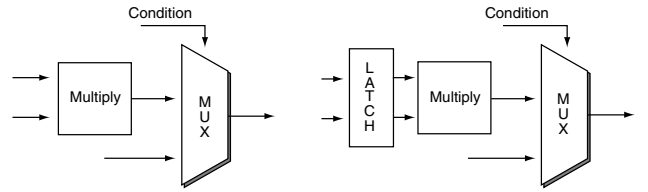

Figure 4 • Guarded Evaluation

Bus Multiplexing

Highly congested designs tend to consume more power due to longer wire lengths. Placement has to be porous and more spread out to route the design, resulting in longer wire lengths and more switches per wire. All of this contributes to bad timing results, as well as increased power consumption. The number of busses in a design can be reduced by time-multiplexing wide busses. Logic in a block tends to be clustered together, so busses running across different blocks have to travel relatively long distances. Reducing such busses helps both timing and power. Also, in DSP designs, data is correlated, which means most of the data bits do not change from one clock cycle to another. The busses carrying correlated data should be multiplexed together to further reduce switching into the MUX/DEMUX logic (Figure 5).

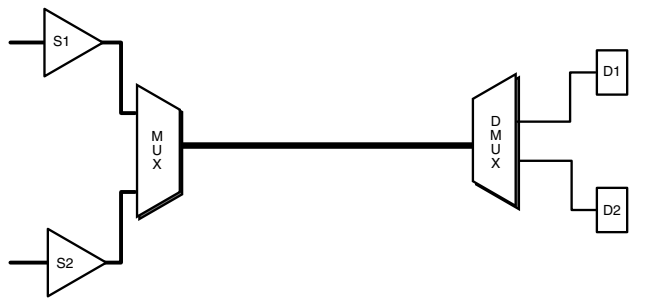

Figure 5 • Bus Multiplexing

Glitch Reduction and Pipelining

Glitches are unwanted switching activities that occur before a signal settles to its intended value. Each clock edge changes the inputs to the combinatorial logic between registers. Every node has a different delay from different inputs, which change their state several times before settling down. Glitches on a node are dependent on the logic depth to that node, i.e. the number of logic gates from the node to the primary inputs (or sequential elements). The deeper and wider the logic cone behind a node, the more it glitches. These glitches can be reduced by reducing the depth of logic levels and by reducing switching inputs to the logic cone.

Pipelining, timing-driven synthesis and good mapping to the logic cell can reduce the number of logic levels. Most of these factors have an impact on timing as well as power. A circuit synthesized for timing has more area but fewer levels of logic. This reduces the glitches on the nodes in the circuit, thereby helping with power. However, if the area penalty is too high, it may reduce the power advantages. In such cases, signals with a high switching rate should be mapped to reduce the levels of logic. Other paths with low switching rates can be optimized for area. The user needs to partition the design to separate high-switching and low-switching paths, while weighing the benefits against the disadvantages.

Pipelining is another technique that involves introducing the registers in the middle of long combinatorial paths. This adds latency but increases the speed and reduces the levels of logic. The introduction of extra registers consumes power but minimizes the glitches drastically. This glitch reduction has some power advantage. For example, a pipelined 16x16-bit unsigned multiplier generated from ACTGEN (Actel's macro-generation utility) consumes less power than its unpipelined counterpart (Figure 6).

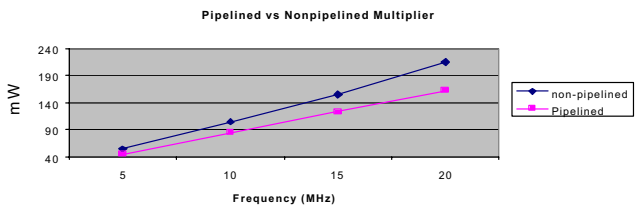

Figure 6 • Pipelining Timing Advantages

Timing-driven place-and-route (TDPR) clusters logic well and reduces the average wire length of a route. This helps to reduce power. FastConnect and DirectConnect routing resources have very low capacitance (TDPR uses them whenever possible). This helps with both timing and power.

Logic Depth Reduction for Frequently Switching Signals

By reordering “if - then...else” constructs, the user can move glitchy or fast-changing signals down the logic cone. This reduces switching activity propagation and power consumption (Figure 7).

During synthesis, high-switching probability input signals to the combinatorial logic can be modeled as late-arriving signals. The synthesis tool tries to reduce the levels of logic from these inputs, thus minimizing switching-activity propagation. If all inputs have the same switching

probability, it is better to synthesize the logic as a balanced tree (Figure 8).

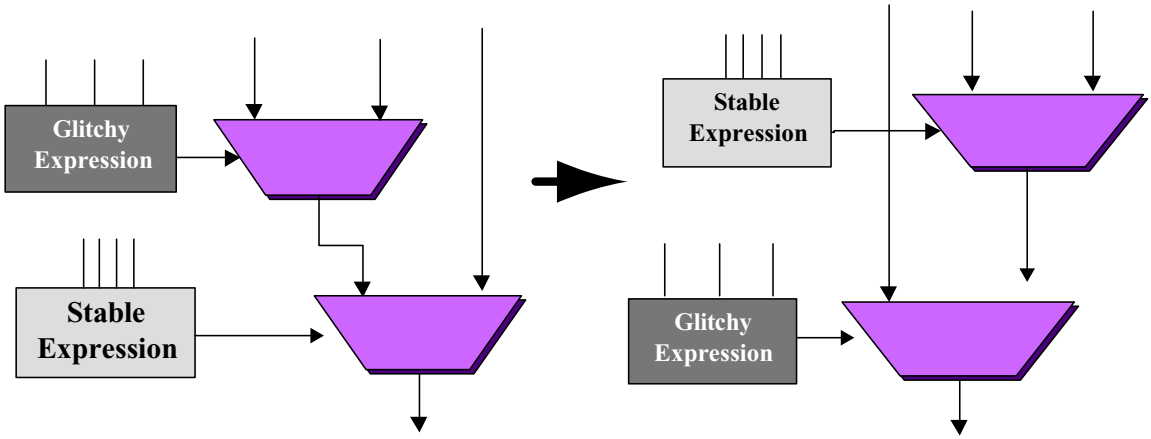

Figure 7 • Reduction of Switching Activity Propagation

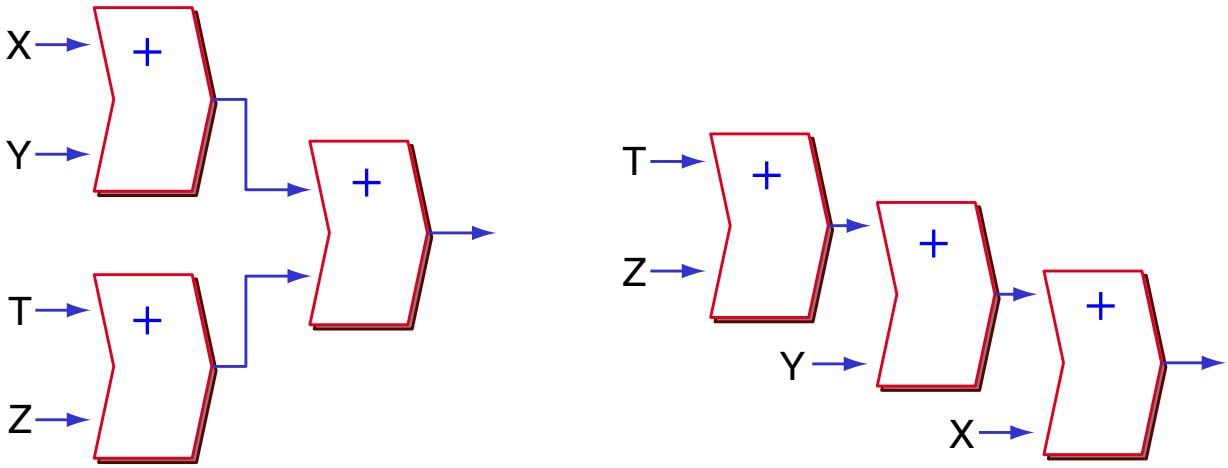

Figure 8 • Switching Probabilities

Power-Friendly Datapath Component Selection

Architectures of datapath elements have an impact on the power consumed. For example, a ripple carry has a low fanout and minimizes logic area use and helps for power reduction. However, it uses a deep switching propagation, so some trade-offs are required. In a ripple carry, the longest path is from the LSB of the inputs to the MSB of the output. If the LSBs of the inputs are switching more frequently, it may be more advantageous to use medium- or high-speed implementations. Assuming random input changes, three ACTGEN 32-bit adder implementations have the relative power consumption displayed in Figure 9.

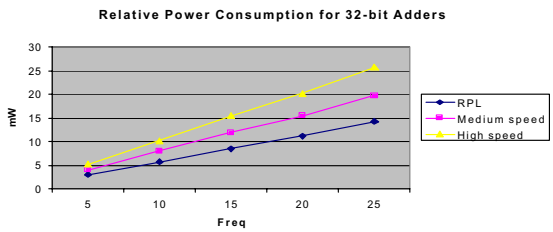

Figure 9 • Power Consumption for 32-Bit Adders

Decoder outputs are generally heavily loaded, so providing them as enable signals will stop unnecessary switching with outputs when the decoder is not in use (Figure 10). For counters, Gray counters have the minimum switching rate and generally should be used. For internal memory addressing, Gray addressing should be used.

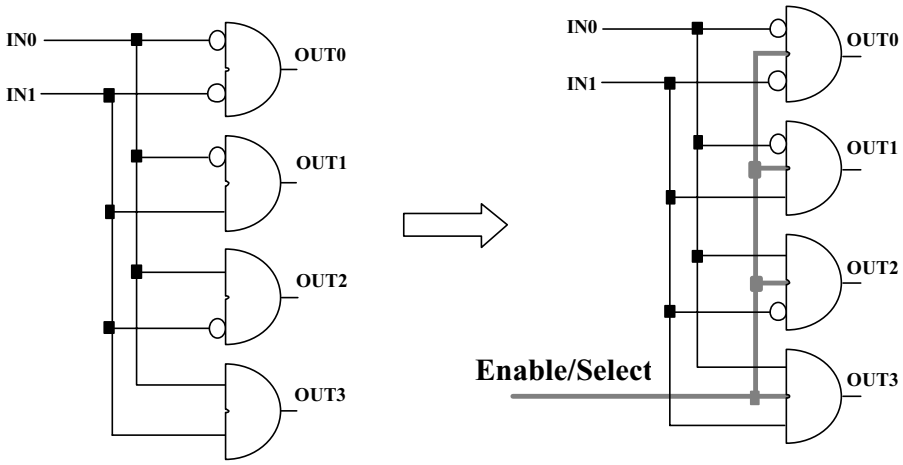

Figure 10 • *Outputs*

State Machine Encoding

Traditionally, state machines are encoded in binary. However, by Gray-coding adjacent states, the number of transitions can be reduced. Sometimes it may not be possible to Gray encode all the states. In this case, the user can increase the number of flip-flops in the state vector to minimize the number of flip-flops that are switching. Another alternative could be one-hot encoding. Though one-hot encoding uses many more flip-flops, it may reduce the use and the depth of combinatorial logic. This is especially the case for state machines with several outputs when each output is a function of several states. In one-hot encoding, every state is already decoded, so this would use less logic for the outputs. Depending on the type of state machine, the designer can choose among Gray, one-hot, or in-between styles. Most synthesis tools provide a way to select the encoding style during synthesis. However, the most effective way is to write the RTL directly into the intended encoding because the designer can select encoding to minimize the number of bit changes per transition.

Using asynchronous logic

Though it is not generally recommended to use asynchronous logic, it may sometimes save power. One example is clock gating, as described earlier. Typically, the clock consumes about 30% of the total dynamic power. In the eX, SX-A, and SX families, every sequential element has clock-selection logic of routed clocks, a hardwired clock (HCLK), or normal routing resources. For every flip-flop used, there is clock-selection logic switching at clock speed. Reducing the switching of clock inputs at the flip-flops helps to minimize power consumption. For example, an asynchronous binary counter consumes only 50% of the power of its synchronous counterpart. However, asynchronous logic may create timing problems such as race conditions, hold-time violations, etc. Whenever asynchronous logic is used, it is highly recommended to run timing simulation under min-max conditions. Also, the simulation vector should be complete to cover all possibilities. Generally, the designer should avoid using asynchronous logic until absolutely required.

Reducing Clock Speed

Though clock speed is fixed, sometimes it may be possible to do things in parallel at lower speeds rather than serially at higher speeds. As mentioned earlier, the clock consumes a large percentage of the total power because of the clock-selection logic associated with each flip-flop. Anything directed at reducing the switching activity of clock inputs to the flip-flops helps to reduce power. Using extra logic modules to compensate for lower clock speeds may in fact save power because of the low-power characteristics of Actel's module and routing architecture.

Conclusion

Actel's antifuse devices inherently have low resistance and capacitance characteristics, and the “sea of module” architecture uses virtually no silicon for routing. This makes them power friendly. In addition to being low power, the antifuse switch resistance provides very high speeds so the user can enjoy low-power advantages without suffering a

performance penalty. The user also can influence power consumption by applying different techniques, such as using the eX low power mode, reducing switching frequency (as described in this application note).

http://www.actel.com

Actel Europe Ltd.
Daneshill House, Lutyens Close
Basingstoke, Hampshire RG24 8AG
United Kingdom
Tel: +44-(0)125-630-5600
Fax: +44-(0)125-635-5420

Actel Corporation
955 East Arques Avenue
Sunnyvale, California 94086
USA
Tel: (408) 739-1010
Fax: (408) 739-1540

Actel Asia-Pacific
EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan
Tel: +81-(0)3-3445-7671
Fax: +81-(0)3-3445-7668

5192668-1/9.00