IBIS Models: Background and Usage

Introduction

For better understanding of the signal integrity on printed circuit boards (PCBs), hardware designers often need to simulate the design with I/O characteristic models. The designer must carefully consider signal integrity issues such as deformation of electronic signals as they travel on the PCB, cross talk, ground-bounce and simultaneously switching outputs (SSO). Input/Output Buffer Information Specification (IBIS) models have been developed to address the above issues by providing I/O parameters in analog terms. This Technical Brief explains how to use IBIS models. In addition, this document discusses information contained in an IBIS model, explains what can be extracted from the model and provides examples of Actel IBIS models.

Background

IBIS is the Input/Output Buffer Information Specification from the Electronics Industry Alliance. It is a modeling technique that provides a simple table-based buffer model for semiconductor devices. The IBIS models can be used to characterize I/V output curves, rising/falling transition waveforms, and package parasitic information of the device. However, it is important to note that an IBIS model is intended to provide nonproprietary information about I/O buffers; it is not a delay model for timing analysis purposes. At Actel, the generation of IBIS models is part of the documentation package of new FPGA devices. Designers will be able to save time by easily generating prototype circuit boards even before they receive the device. This enhances time-to-market for their products.

SPICE models can be used to model various components on PCBs. However, the SPICE netlist of the I/O transistors of various components contains proprietary information. Furthermore, there are many different SPICE formats in the industry today, and not all are compatible with one another. This method is also time consuming and therefore, a nonproprietary component model was needed for rapid simulations. IBIS is that model.

IBIS Characteristics

Operating Conditions: Typical/Minimum/Maximum

In each IBIS model, three device conditions are usually specified: typical, minimum, and maximum. The simulations obtained within the IBIS model have the minimum and maximum ranges being the boundaries and the typical being the nominal range/value. Table 1 summarizes the three conditions.

Table 1 • **Ranges and Operating Conditions**

Range	Operating Condition	Temperature	%V_{CC}
Minimum	Weakest	High, 70°C	90% V_{CC}
Typical	Nominal	25°C	V_{CC}
Maximum	Strongest	Low, 0°C	110% V_{CC}

Refer to the waveforms in Figure 2 on page 3, showing the simulated values in the 3 ranges.

Notice that the minimum range occurs at the I/O's maximum temperature, whereas maximum range occurs at minimum temperature. Designers must be careful while analyzing the data, bearing in mind that the temperature range would be different for military vs. industrial vs. commercial.

File Structure

A standard IBIS model file consists of three sections:

- Header Info – this section contains basic information about the IBIS file and what data it provides.
- Component, Package, and Pin Info – this section contains all information regarding the targeted device package, pin lists, pin operating conditions, and pin-to-buffer mapping.
- V-I Behavioral Model – this section contains all data to recreate I-V curves as well as V-t transition waveforms, which describe the switching properties of the particular buffer.

Usually, an Actel IBIS file contains the information for each section, as shown in Table 2.

Table 2 • **Typical Contents of an Actel IBIS File**

Header Information	Component, Package, Pin Information	Model
IBIS version	Component	Model Type
File name	Manufacturer	Temperature Range
File Revision	Package	Voltage Range
Date	Pin	Pull-down, Pull-up, GND Clamp, POWER Clamp reference
Source	Pin Mapping	Ramp Rate
Notes		Rising/Falling waveform
Disclaimer		
Copyright		

IBIS Overview

Buffer I/V Characteristics

Every signal pin on an Actel FPGA contains a CMOS buffer that can be configured as an input, output, or bidirectional buffer. A simplified output buffer schematic is illustrated in Figure 1. When the PMOS output transistor turns OFF and the NMOS transistor ON, the output is placed in logic low. When the PMOS transistor is turned ON, and the NMOS device is OFF, the output is placed in logic high (Table 3 on page 3). With both turned off, the output is in a high impedance state.

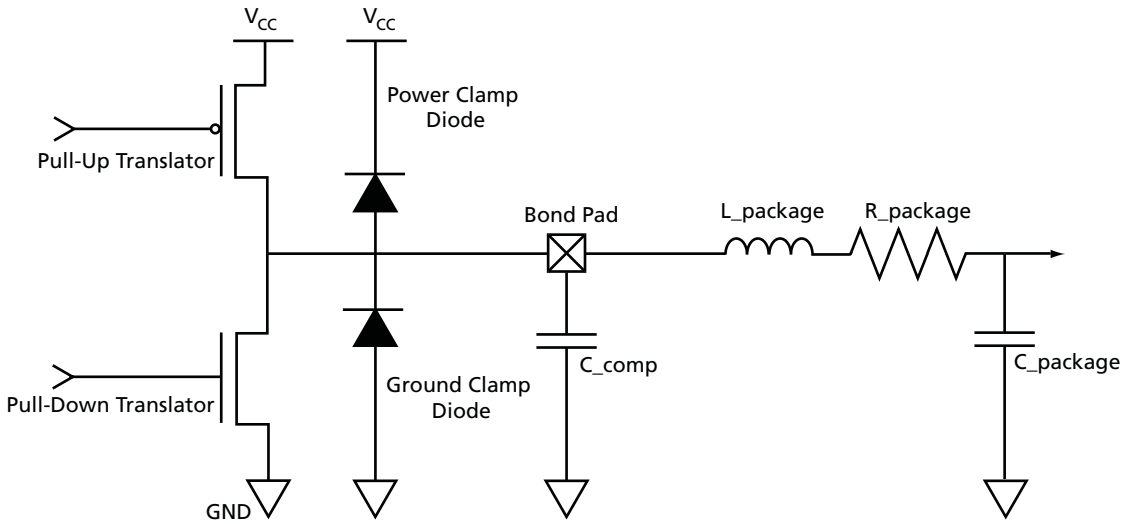


Figure 1 • **Simplified Output Buffer Schematic**

Table 3 • **Buffer Logic State Conditions**

PMOS	NMOS	Logic State
Off	On	Logic low
On	Off	Logic high
Off	Off	High impedance

Furthermore, the output buffer features GND and power clamp diodes. The main purpose of these diodes is to maintain the output buffer voltage between 0.7 V below ground (when logic low) and 0.7 V above V_{CC} (when logic high). These diodes start to conduct when the pin is driven outside these limits. It should be mentioned that for Actel device families with Hot Swapping I/Os there is additional circuitry that affects the operation of the diodes; specifically, the power clamp diode. The last portion of the buffer includes the capacitance of the silicon die (C_comp), the resistance (R_package), the inductance (L_package) and the capacitance (C_package) of the bond lead and package pin.

IBIS I/V Curves

By slowly increasing the voltage with an ammeter and voltmeter connected at the buffer, four different I/V curves can be derived. They are pull-up, pull-down, GND clamp and power clamp curves. Since a buffer measurement is carried out with three configurations (min, typ, and max), the result is a set of twelve IBIS I/V curves.

For MX and older FPGA families, the I/V curves are based on measured data and not the SPICE netlist. For SX and newer products (SX-S, SX-A, eX, and ProASIC) the curves are only based on SPICE models.

The pull-down curve is a result of subtracting the GND clamp I/V curve from the logic-low I/V curve, since this is where the pull-down transistor is active (Figure 2). The full range of the measurement is from $-V_{CC}$ to $2V_{CC}$ which is the possible range of voltages that the output could see in a transmission line environment.

Similarly the pull-up curve is generated by subtracting the power clamp I/V curve from the logic-high I/V curve, since this is where the pull-up transistor is active (Figure 3 on page 4). Again, the full range is from $-V_{CC}$ to $2V_{CC}$.

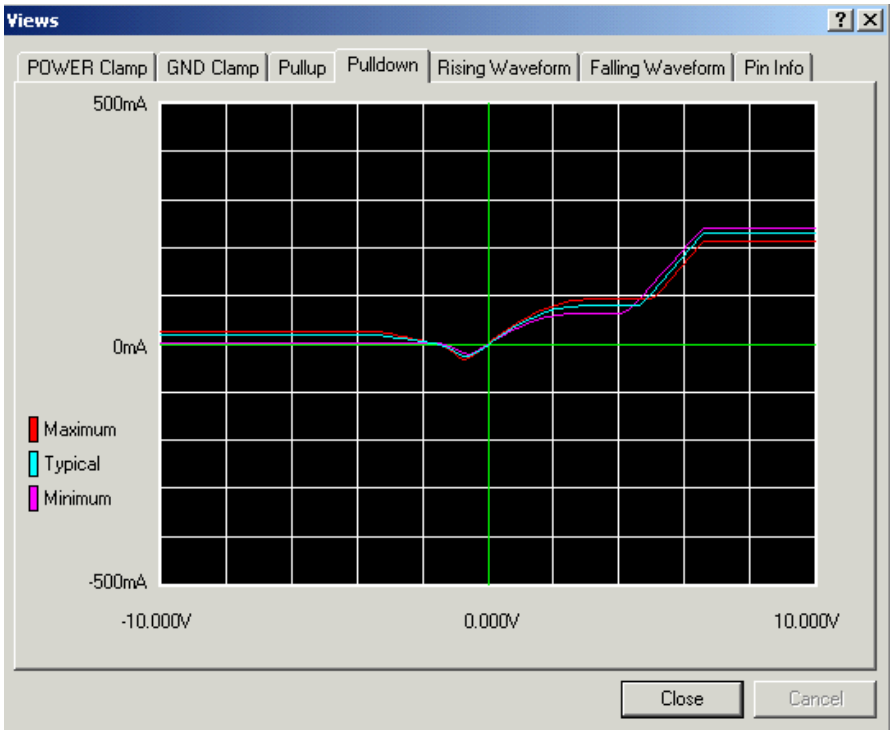


Figure 2 • **Sample Pull-Down Curve**

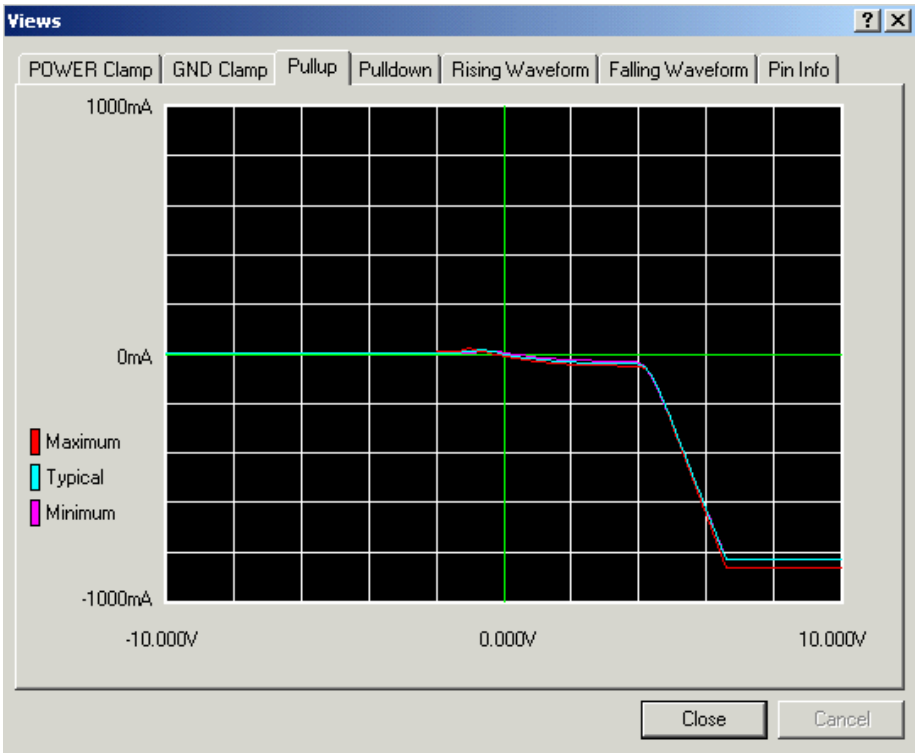


Figure 3 • **Sample Pull-Up Curve**

The GND clamp curve is derived from the ground relative data gathered while the buffer is in the high-impedance state and illustrates the region where the ground clamp diode is active (Figure 4). The range is from $-V_{CC}$ to V_{CC}.

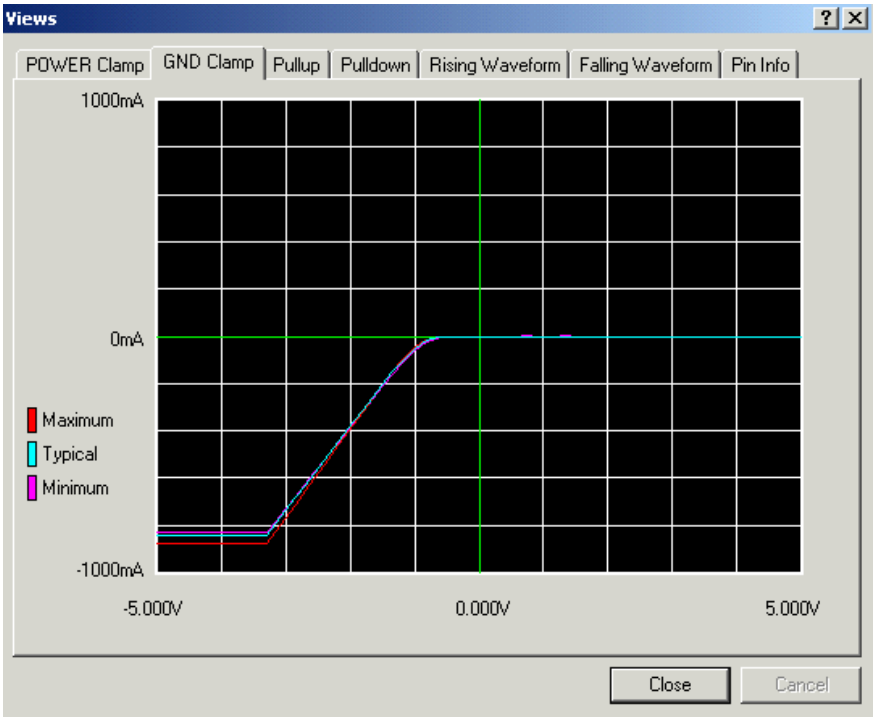


Figure 4 • **Sample GND Clamp Curve**

The power clamp curve is derived from the V_{CC} relative data gathered while the buffer is in a high impedance state and shows the region where the power clamp diode is active. This measurement ranges from V_{CC} to $2V_{CC}$. (Figure 5).

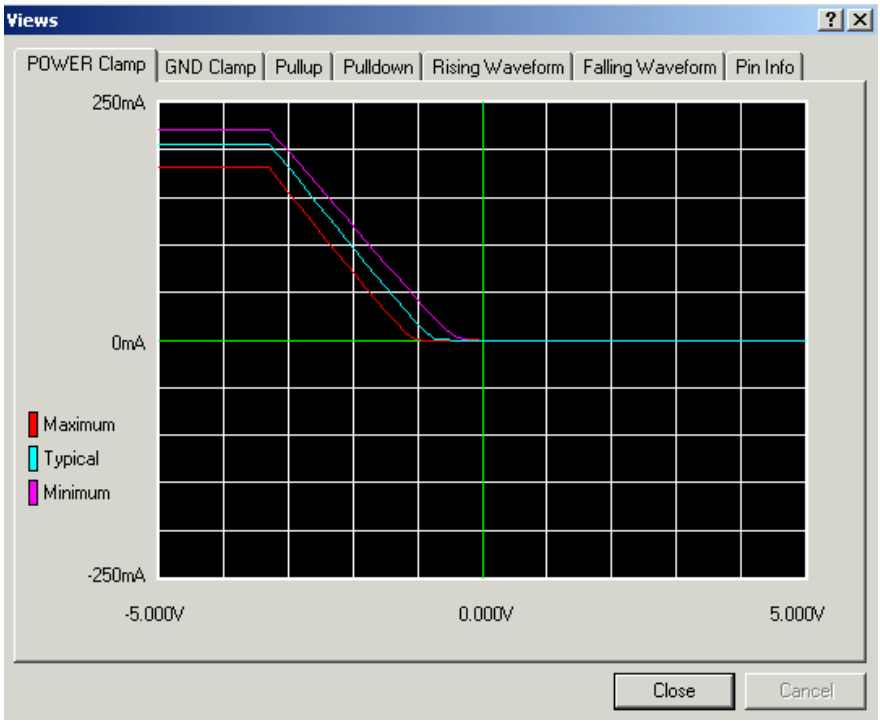


Figure 5 • **Sample Power Clamp Curve**

The pull-up and power clamp curves are V_{CC} relative, meaning that the voltage values are referenced to the V_{CC} pin. The output current of a pull-up (or power clamp) configuration depends on the voltage between the output and V_{CC} pin and not the voltage between the output and ground pins. The voltages in IBIS data tables are derived from the following equations:

$V_{table} = V_{CC} - V_{output}$ (for pull up and power clamp)

$V_{table} = V_{output}$ (for pull down and GND clamp)

Therefore, for a 3.3 V component, –3.3 V in the table means an actual +6.6 V on the output pin, and so on.

The preceding samples of each of four types of IBIS I/V curves were generated using Hyperlynx IBIS Viewer. The flat end portion of the curves is due to the current clamping during the measurement.

IBIS Transition Waveforms

The IBIS model can also provide rising and falling V-t waveforms, which illustrate the transitions from GND to V_{CC} and from V_{CC} to GND. These curves are always taken from Spice simulations. The ramp rates are taken when the output voltage varies from 20% to 80% V_{CC} (rising), and from 80% to 20% V_{CC} (falling). Figure 6 and Figure 7 on page 7 show the rising and falling waveforms, respectively (generated using Hyperlynx). Designers should notice that the ramp rates given by "[Ramp]" in the IBIS file are different from slew rates. In calculation of the ramp rates the package parasitics are ignored. These ramp rates are much faster than slew rates in which the package parasitics are taken into account.

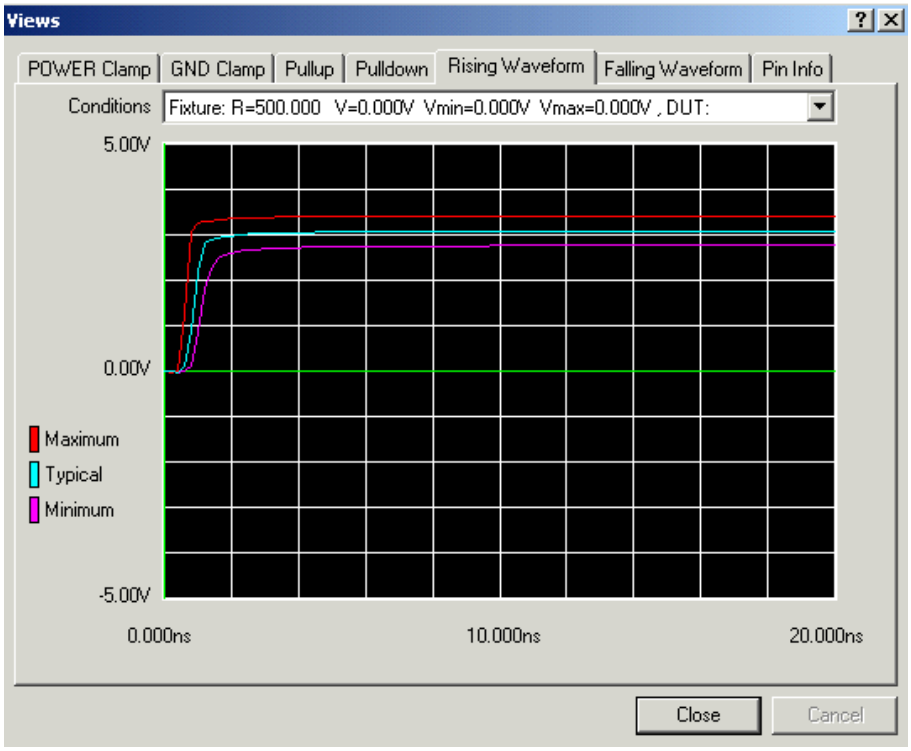


Figure 6 • **Sample Rising Waveform**

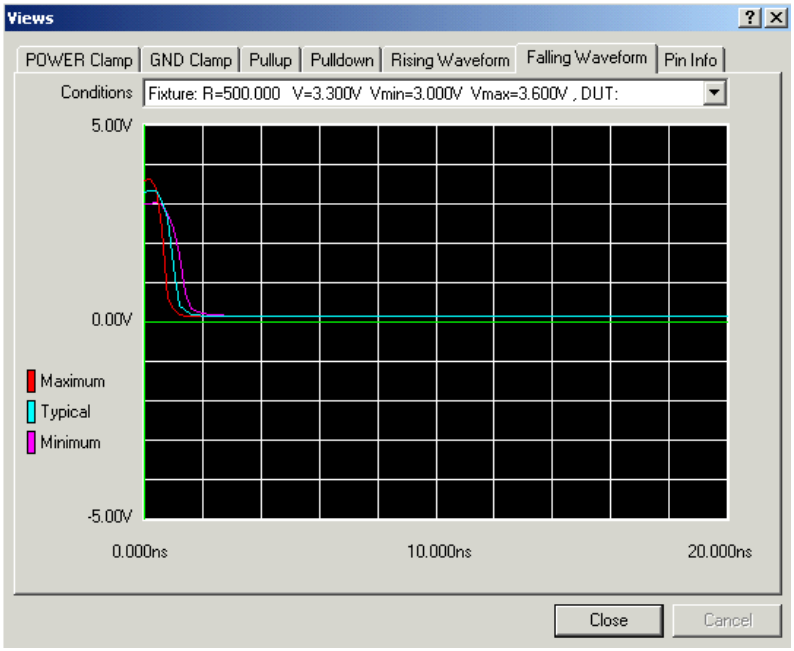


Figure 7 • **Sample Falling Waveform**

Sample Actel IBIS File for the MX Family

```
|*********************************************************************
| IBIS file mx09_33v.ibs aided by s2ibis2 version 1.1
| North Carolina State University Electronics Research Laboratory  1995
|*********************************************************************
|
[IBIS ver]        2.1
[File name]       mx09_33v.ibs
[File Rev]        2.x5
[Date]            March 31 1998
[Source]          V/I curve data extracted from silicon lab measurements. Ramp
data extracted from SPICE netlist. All performed at Actel.
[Notes]           V/I max min curve data was measured in the lab under max and
                  min Vcc and Temp conditions. The measurements were done on
                  pre-production parts. Please see User's Area" section of
                  Actel's Webpages for more information regarding product or
                  package data. Actel's Homepage URL is http://www.actel.com
                  Check for the availiability of a rev 2.1 mx09_33v.ibs in
                  September 1998.
[Disclaimer]      This information is for modeling purposes only, and is not
                  guaranteed.
```

```
[Copyright]      Copyright 1998, Actel Corporation, All Rights Reserved.
|
|*********************************************************************
|                  Component mx09_0.5um_33v
|*********************************************************************
|
[Component]      mx09_0.5um_33v
[Manufacturer]   Actel Corporation
[Package]
| variable       typ                min                max
| Un-comment the appropriate package
|
|R_pkg       104m     97m      111m      | PLCC 84
|L_pkg       10.3nH   8.29nH   12.31nH   | PLCC 84
|C_pkg       2.04pF   1.84pF   2.24pF    | PLCC 84
|…….cont'd
|
[Pin]  signal_name          model_name           R_pin     L_pin     C_pin
ALLIO  IO1_out              ALL_IO_PINS
| 1_in IO1_in               INPUT1
| 1_en IO1_en               ENABLE1
GNDP   GND                  GND
VCCI   VCCI                 POWER
|
[Pin Mapping]  pulldown_ref    pullup_ref      gnd_clamp_ref   power_clamp_ref
|
ALLIO          GND             VCCI            GND             VCCA
| 1_in         NC              NC              GND             VCCA
| 1_en         NC              NC              GND             VCCA
GNDP           GND             NC
VCCI           NC              VCCI
VCCA           NC              VCCA
|
|*********************************************************************
|                           Model ALL_IO_PINS
|*********************************************************************
|
[Model]          ALL_IO_PINS
Model_type       I/O
Polarity         Non-Inverting
```

```
Enable           Active-Low
Cref =  35.00pF
Vref =  0.000V
C_comp           2.40pF              2.48pF              2.33pF
Vinl = 0.8V
Vinh = 2.0V
|
|
[Temperature Range]       25.00               70.00               0.000
[Pullup Reference]        3.30V               3.00V               3.60V
[Pulldown Reference]      0.000V              0.000V              0.000V
[POWER Clamp Reference]   3.30V               3.00V               3.60V
[GND Clamp Reference]     0.000V              0.000V              0.000V
[Pulldown]
| voltage     I(typ)              I(min)              I(max)
|
-3.30E+00     1.83E-02     3.00E-03     2.59E-02
-3.15E+00     1.67E-02     2.82E-03     2.37E-02
-3.00E+00     1.51E-02     2.64E-03     2.14E-02
|......cont'd

[Pullup]
| voltage     I(typ)              I(min)              I(max)
|
-3.30E+00     3.46E-03     3.34E-03     5.58E-03
-3.15E+00     3.38E-03     3.52E-03     5.52E-03
-3.00E+00     3.72E-03     3.26E-03     5.80E-03
|......cont'd
[GND_clamp]
| voltage     I(typ)              I(min)              I(max)
|
-3.30E+00     -8.41E-01     -8.31E-01     -8.80E-01
-3.15E+00     -7.87E-01     -7.79E-01     -8.23E-01
-3.00E+00     -7.34E-01     -7.28E-01     -7.67E-01
|......cont'd
[POWER_clamp]
| voltage     I(typ)              I(min)              I(max)
|
-3.30E+00     2.06E-01     2.21E-01     1.81E-01
-3.15E+00     1.93E-01     2.09E-01     1.68E-01
```

```
-3.00E+00     1.81E-01     1.98E-01     1.55E-01
|......cont'd
|
[Ramp]
| variable       typ                 min                 max
dV/dt_r          1.98/0.23n          1.80/0.26n          2.16/0.14n
dV/dt_f          1.98/0.28n          1.80/0.35n          2.16/0.25n
R_load = 1.00M
|
[Rising Waveform]
R_fixture = 0.50k
V_fixture = 0.000
V_fixture_min = 0.000
V_fixture_max = 0.000
| time           V(typ)              V(min)              V(max)
|
  0.000S         0.000V              0.000V              0.000V
   0.20nS       -17.96mV            -12.51mV            -26.17mV
   0.40nS       -27.82mV            -27.72mV             12.14mV
|......cont'd
|
[Falling Waveform]
R_fixture = 0.50k
V_fixture = 3.30
V_fixture_min = 3.00
V_fixture_max = 3.60
| time           V(typ)              V(min)              V(max)
|
  0.000S          3.30V               3.00V               3.60V
   0.20nS         3.32V               3.01V               3.63V
   0.40nS         3.33V               3.04V               3.42V
|......cont'd
|
| End [Model] ALL_IO_PINS
|
| End [Component] mx09_0.5um_33v
|
[End]
```

How to Use Actel IBIS Models

Actel has developed many different families of antifuse and Flash-based FPGAs. They come in a variety of packages. However, IBIS models for Actel products are developed with a single model pin, called ALLIO. This pin can serve as a signal pin during board level simulations and can model all of the I/Os on the device. The designer simply replicates the pin as many times as needed to suit the design. For each Actel family, IBIS models are created for each I/O mode, then the package parasitics for all allowable packages are included in the IBIS model. The designer can simply uncomment the applicable package parasitics before performing simulation and analysis.

Different IBIS simulators are available in the industry today, some of the vendors include:

- Cadence
- Mentor
- Microsim
- VeriBest
- Innoveda (Hyperlynx)

Information Extracted from an IBIS Model

IBIS data can be exploited to extract useful information on I/O characteristics. One is determining the current drive capability of the I/O in terms of source and sink currents. Another is defining a simple I/O equivalent circuit for board-level calculations.

I/O Source and Sink Currents

Source and sink currents are two important characteristics of I/O buffers. IBIS pull-up and pull-down I/V data are reliable sources to determine the source and sink currents, respectively. However, note that the source and sink currents obtained from IBIS models are not suitable for reliability assessment. In other words, the IBIS models merely represent the I/V characteristic of the I/O buffers but do not take into account reliability factors such as electro-migration. Sink current at a particular voltage can be obtained from the pull-down minimum current (Imin) set of IBIS data. Similarly, the minimum current extracted from pull-up data is a reliable source for determining the source current of the I/O for each voltage level. For example, the IBIS file for the SX-A device family illustrates that the device is capable of sourcing and sinking 35 mA and 30 mA, respectively, at a 3.3 V LVTTL operating voltage based on the following equations:

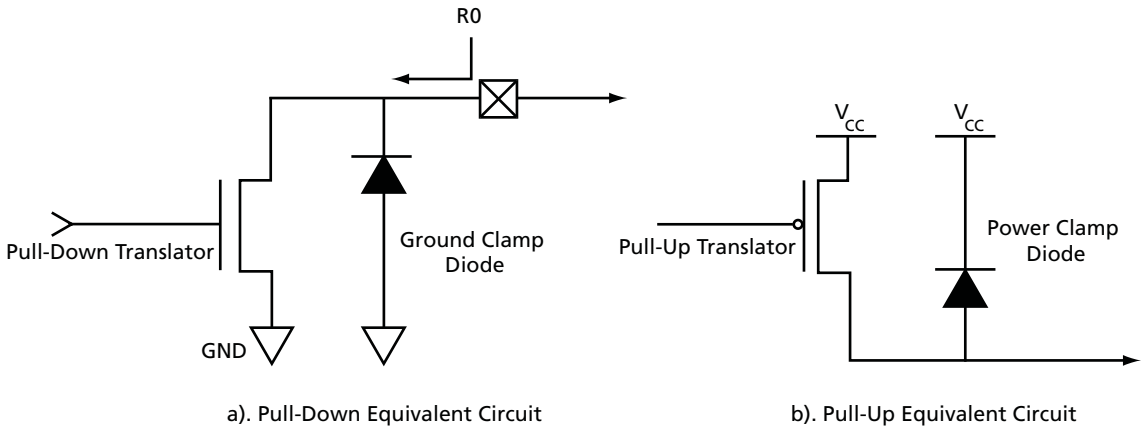
$V_{table} = 3.3\ V – V_{OH}$ (min) (for source current)

$V_{table} = V_{OL}$ (max) (for sink current)

To derive more accurate estimates for source and sink current, the effect of clamp curves should be taken into account. However, Power and GND clamp diodes have minor effects within the operational range of voltage.

Simple I/O Equivalent Model

Many designers find it very useful to replace the I/O buffer with a simple equivalent circuit for board-level calculations as shown in Figure 8. The most important parameter of this model is the output resistance, Ro, seen from outside of the pin. IBIS models themselves do not take package effects into consideration (during model generation). The package data is provided for the simulators only and therefore the IV data DOES NOT include effects of package parasitics.



a). Pull-Down Equivalent Circuit

b). Pull-Up Equivalent Circuit

Figure 8 • **Pull-Down and Pull-Up Equivalent Resistors**

To calculate Ro, the linear part of the pull-up and pull-down IBIS curves can be used. The first step is to locate the linear portion. For example in the pull-down curve of Figure 2 on page 3, it can be seen that the I/V relation is almost linear in the 0 V to 1.5 V range. For voltages more than 2 V the current enters in saturation mode. The amount of the current in the linear range can be obtained either by the curve or IBIS file values. For the typical pull-down I/V curve, the value of Ro can be calculated as 1.35V / 53.4 mA = 25.2 Ω Similarly, a typical Ro for pull-up IBIS curve can be obtained as 1.35 V / 26.3 mA = 51.3 Ω. These impedances are only “first order approximations.” Also, all the curves that are ON, need to be taken into account, i.e., pull-up + both clamps when driving a 'Hi' and pull-down + both clamps when driving a 'Lo.' However, the first order approximation provides enough accuracy for most of applications.

Conclusion

Designers often need to prototype their PCBs before they have any devices to test. IBIS models allow designers to conveniently simulate I/O behavior and characteristics and thus more accurately analyze various components on their board. This is achievable through the generation of various I/V output curves, rising and falling transition waveforms, and package parasitic information.

Actel IBIS models are internally developed, generated from SPICE simulations, and compared with the silicon data to model the real device as closely as possible. By providing Actel customers with the IBIS models, designers can analyze device I/O behavior before having the physical device available for test.

List of Changes

Previous Version	Changes in Current Version 5192686-3/12.06*	Page
5172686-2/5.02	Reliability information has been added to the "I/O Source and Sink Currents" section.	11

Note: ** The part number is located on the last page of the document.*

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